A Review on Graphene Based Field Effect Transistor (GFET)

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A Thesis Presented to

The Academic Faculty

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This is certify that the work presented in this thesis is an outcome of the study and research carried out by the authors under the supervision of **Dr. Syed Iftekhar Ali**, Associate Professor, Dept. of Electrical and Electronic Engineering, Islamic University of Technology (IUT).

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ABSTRACT

With the advancement of technology, the necessity of devices in nanometer range has gone up. A new addition in this nano device family is Graphene based Field Effect Transistor or GFET. Graphene is a single sheet of graphite and it has some amazing properties those made it possible to use it in the fabrication of GFET. The main difference of this device with the regular FETs is that the channel of GFET is of single layer Graphene flake. The fabrication process is a bit complex due to ensure the use of SINGLE layer Graphene flake as the channel of the GFET. There are a few fabrication processes depending on what kind of GFET is being tried to be fabricated. There have been so many experiments to find out the characteristics of GFET and they seem to very unique according to their types. Different GFET models are being tried to be developed by the specialists lately to operate them in newer levels and there are some revolutionary inventions happened on that matter. The potential uses of GFET are amazing which makes us think that may be it would be a great idea to work further on the application of GFET.

LIST OF FIGURES

LIST OF SYMBOLS

Symbol	*Meaning*
f_T	Transistor frequency
E_F	Fermi Level
E_G	Band Gap
V_d	Drift velocity
E	Applied electric field
μ	Mobility
q	Charge
V_G	Gate voltage
V_{ch}	Channel voltage
V_{FB}	Flat band voltage
V_{Dirac}	Dirac point voltage
k_B	Boltzman's Constant

CHAPTER 1

INTRODUCTION

In this review paper we will discuss about the graphene, graphene based FET, its classifications, fabrication, characterization, operation principle, modelling, application and advantages of GFET. In this chapter we will discuss background and motivation of this review paper. The chapter will end with outlines of the review paper.

1.1 Background and Review Motivation

The Moor's law **[1]** says that the number of transistors that can be crammed on an integrated circuit doubles approximately every two years. But the speed of Cramming is now noticeably decreasing this trend has Continued for more than half a century and is expected to Experience its most fundamental challenge in the next 10 to 20 years, according to the semiconductor industry Roadmap. The main problem is the poor stability of Materials if shaped in elements smaller than 10 nanometers in size. At this scale, all semiconductors – including Silicon – Oxidize, decompose an uncontrollably migrate along surfaces like water droplets on a hot plate. **[2]**

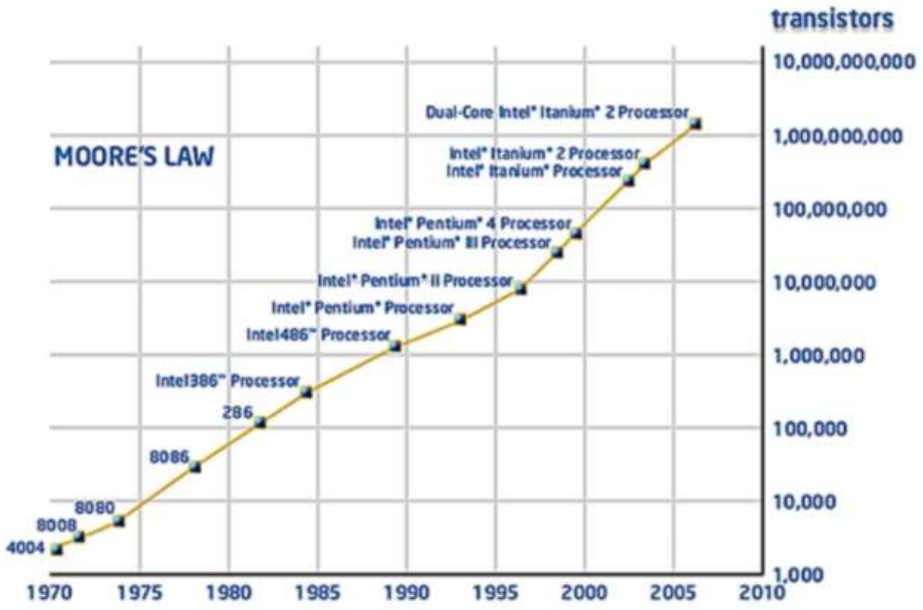


Figure 1.1 – Moore's Law

Graphene, a sheet of carbon one atom thick, has been studied for its potential use in electronics, and was initially identified as a material that would replace silicon and Make devices faster and easier to manufacture. Unlike all other known materials, graphene remains highly stable and Conductive even when it is cut into devices one nanometer Wide. The main issue with this nanotechnology is that Graphene has no "band gap". In semiconductors, electrons can be at two different energy levels known as conduction and valance bands. The energy space that exists between the regions is named the band gap. The energy gap between the two permits transistors to switch on and off which allows the storage of information in the ones and zeroes of binary code. This problem can be solved by Making graphene inverters, which is a necessary Component of a digital transistor.

Graphene devices have grown by leaps and bounds over the past few years and they are probably the best bet to eventually replace Silicon. Demonstrations like this are Important because they show that wafer -scale production is possible, and the properties, while not ideal, are truly Impressive, in that they're already beginning to push the Limits of Si technology.

From the isolation of real two-dimensional carbon sheet graphene in 2004, its outstanding electrical and mechanical properties have been experimentally shown. Among its characteristics, three specific ones make it very unique among other candidates for future faster and smaller electronics. The first and maybe the most important priority of graphene is its ultrahigh intrinsic mobility. It has been shown that graphene's upper mobility limit at room temperature is absolutely higher than silicon and any other material at this time **[3].** The next advantage is the fact that graphene is thermodynamically stable in 2-D which makes it an ideal material as the channel material in case of gate control in integrated circuits technology **[4]**. Finally the compatibility of graphene with standard silicon technology **[5]** makes it easy and cost-effective to integrate with existing CMOS fabrication plants.

1.2 Outline of the Review Paper

This report is organized into nine chapters. The first chapter already has covered the background, objectives and review motivation.

In chapter 2, we mainly are giving some brief introduction of graphene, its structure, history, properties, applications etc. And also the reason of choosing graphene.

Chapter 3 will summarize the graphene field effect transistor and their classifications.

In chapter 4 we will discuss about the fabrication process of GFET in various ways.

Chapter 5 is about the characterization of GFET mainly top gate and back gated depending on various theories.

Chapter 6 will summarize the operation principle of GFET on various condition.

In chapter 7 the modelling of GFET will be discussed.

Chapter 8 will cover the applications of GFET in both practical and potential cases. The advantages of GFET over FET will also be discussed in this chapter.

In the last chapter 9 will cover the conclusion and future work of this review paper.

CHAPTER 2

OVERVIEW OF GRAPHENE

This chapter mainly is giving some brief introduction on physic of Graphene, some history and about Graphene FET.

2.1 Introduction of Graphene

Graphene is made up entirely of carbon atoms bound together in a network of repeating hexagons within a single plane just one atom thick. It is excellent conductor of electricity and since carbon is common element, it makes it attractive option for synthesizing cheaper CPU's. The mobility of graphene is above 200,000 cm^2/vs. At room temperature. "Greater than 100 times that of Silicon, 30 times Gas, and larger even than carbon nanotubes, "Said professor Gem, physicist working at the University of Manchester." It is only the material where electrons at room temperature can move thousands of interatomic distances without scattering". Good quality graphene is literally flaked from sample of graphite – the black rock that used in pencils. The flakes are deposited on a substance and then manipulated**. [2]**

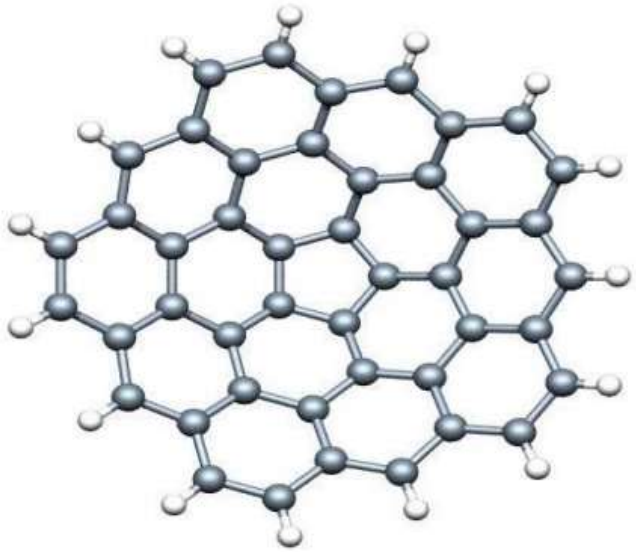


Figure 2.1: Graphene is an atomic-scale honeycomb lattice made of carbon atoms**[2]**

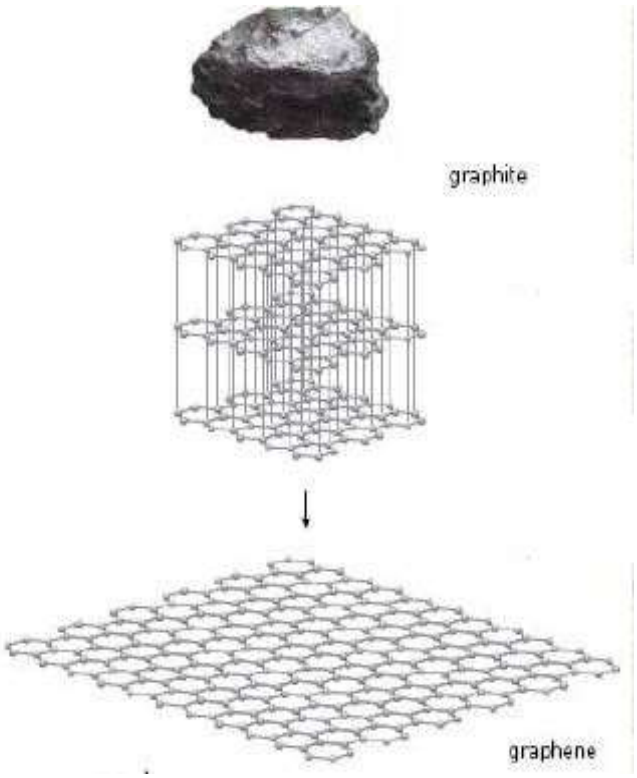


Figure 2.2- Graphene from Graphite

Recently, graphene, a 2-D carbon-based material, has attracted a lot of attention. In 2004, groups from Manchester University (Manchester, U.K.) and from Georgia Institute of Technology (Atlanta, GA, USA) published two pioneering papers on the preparation ofgraphene and the occurrence of the field effect in their samples **[6], [7].** Moreover, high carrier mobility's have been observed in graphene **[7].** These two papers not only ignited a revolution in solid-state physics but also fueled speculations that graphene could be used for transistors with scaling limits and operating speeds beyond those of conventional transistors. Already in 2007, graphene found its place in the Emerging Research Devices chapter of theirs, research programs to develop graphene transistors were established worldwide, and soon the first operating graphene transistors were demonstrated**[8].**

2.2 History of Graphene

Graphene began to attract much attention in the scientific community in late 2004 after the publication of the two seminal paper son graphene **[6],[7]**. Insofar, 2004 was the magic year for graphene, but the history of this material goes back much further, as shown in Fig. 2.3. As early as 1947, at a time when the name graphene did not yet exist, Wallace calculated the band structure of a single layer of carbon atoms arranged in a hexagonal 2-D lattice, i.e., graphene, and predicted its gapless nature **[9]**. In 1962, Boehmet al. produced single graphene layers by the reduction of graphite oxide **[10]**; in 1969, single-layer graphene on platinum has been observed **[11]**; and in1975, graphene has been produced by the thermal decomposition of SiC **[12]**.

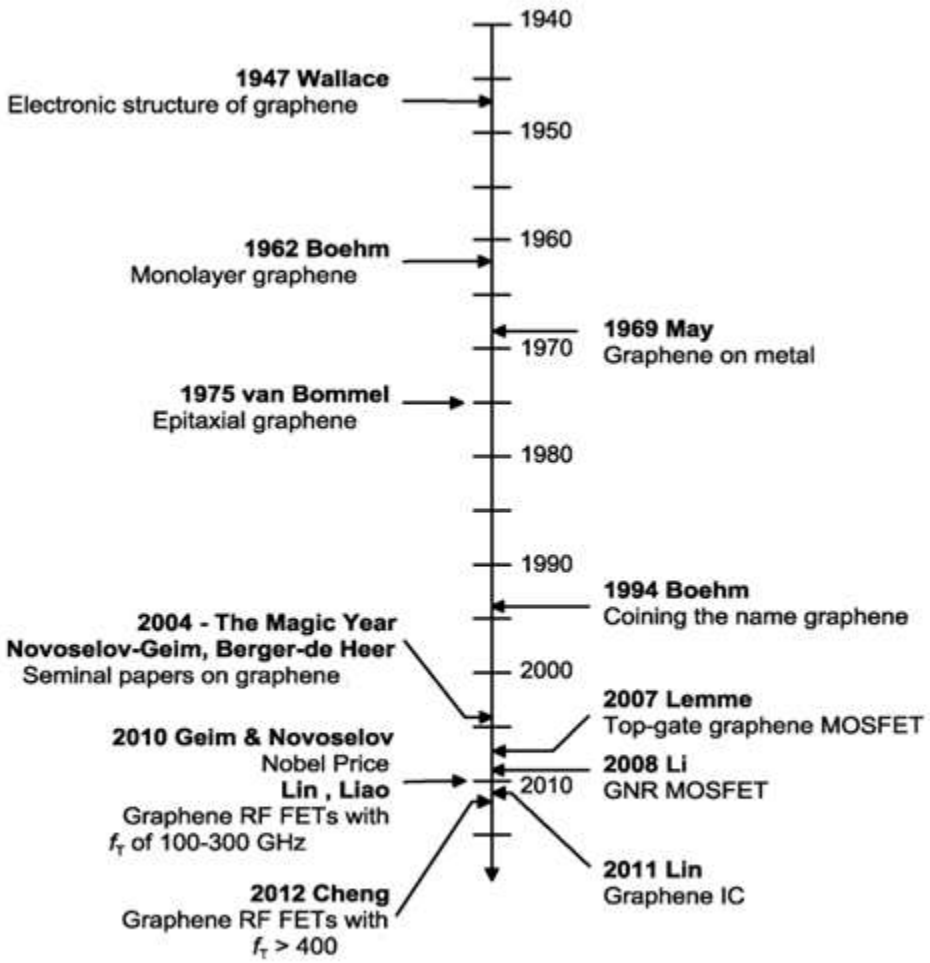


Figure 2.3 - Important milestones of the evolution of graphene electronics**[8]**

Initially, however, these results found only limited attention in the community. In 1994, the name graphene has been introduced for single carbon layers of the graphitic structure **[13]**. After another ten years, eventually, the interest in graphene exploded and the number of papers on graphene published per year grew at an enormous pace, as shown in Fig. 2.4

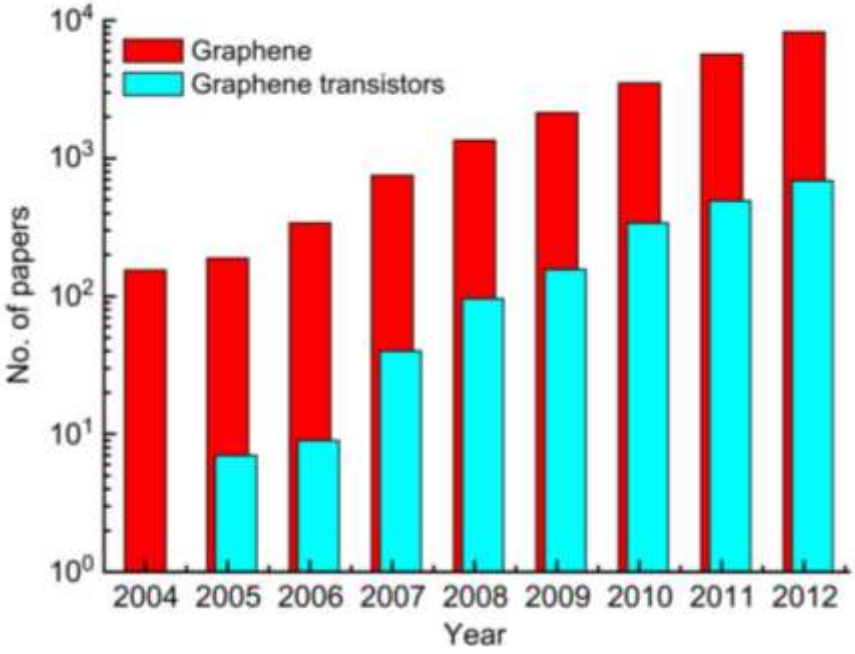


Figure 2.4 - Number of papers published per year and listed in Web of Science under the search terms ‘‘graphene’’ and ‘‘graphene transistor.’’

Physicists discovered remarkable effects in grapheme **[14], [15],** and soon device engineers became interested in the new fascinating material **[16], [17]**. The first grapheme MOSFET has been reported in 2007 **[18]**, and since then a continuously increasing number of groups successfully fabricated graphene transistors. In 2010, graphene MOSFETs with cutoff frequencies in the 100–300-GHz range have been reported **[19], [20]**; in 2011, the first graphene integrated circuit has been presented **[21]**; and in 2012, a grapheme MOSFET with a cutoff frequency Exceeding 400 GHz has been demonstrated **[22]**.

Meanwhile the tenor of the discussion on graphene has changed, and its future in electronics is assessed still cautiously optimistic but much less enthusiastic.

A series of recent competent commentaries has dealt with graphene's role in electronics **[23]–[28]**. The concurrent opinion is that graphene will not replace Si or the III–V compounds soon or in the midterm future. A key issue here is the bandgap. While all conventional semiconductors possess a sizeable bandgap (e.g., Si 1.1 eV, Ge 0.7 eV, GaAs 1.4 eV), natural graphene is a zero-gap material and the missing gap has consequences for the operation of graphene transistors. The most obvious effect discussed already in the early days of graphene transistors is that FETs with gapless channels do not switch off and, therefore, are not suited for complex logic circuits. Recently, the effect of the missing gap on the operation of grapheme RF transistors has also received increasing attention. **[8]**

A promising direction currently pursued in grapheme research is directed to complement the conventional semiconductors instead of trying to replace them and to use graphene in applications where other materials fail or perform poor. Indeed, intensive work is underway on graphene transparent electrodes **[29]** and on graphene devices for flexible and printable electronics **[30], [31]**.

2.3 Properties of Graphene

A wish list for the ideal semiconductor would include the following features:

- Sufficiently wide band gap, combined with excellent carrier transport properties and a high thermal conductivity;
- Producible on large-diameter substrates, process friendly, and compatible with Si CMOS technology;
- interfaces to dielectrics with good long term stability and low defect density not affecting carrier transport in the semiconductor close to the interface; and
- Low contact resistance. Unfortunately, such a material does not exist and device engineers must always live with tradeoffs.

How does graphene meet these requirements?

Natural large-area graphene is gapless and behaves like a semimetal; thus, already the first requirement is not fulfilled. Graphene's band structure features cone-shaped valence and conduction bands that touch each other at the K points of the Brillouin zone, as shown schematically in Fig. 2.5(a)

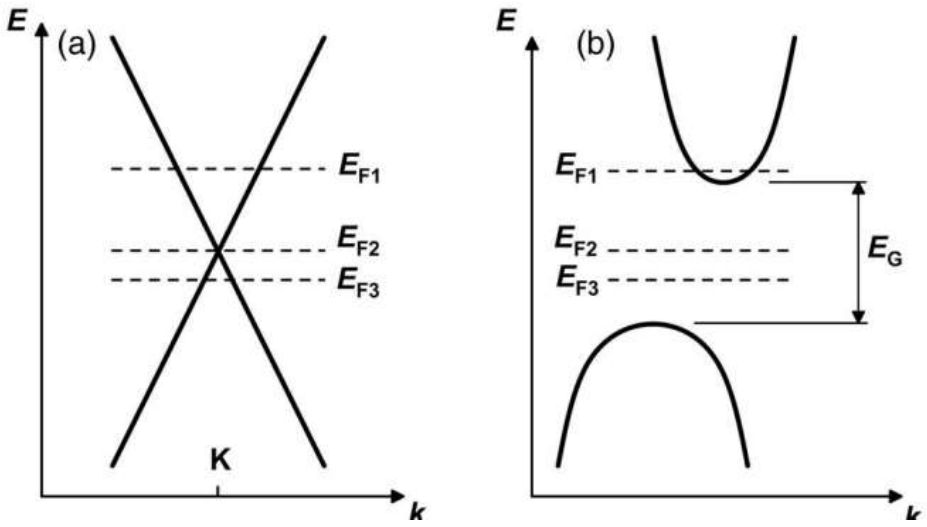


Figure 2.5 – (a) Schematic band diagram of gapless large-area graphene. **(b)** Band diagram of an indirect semiconductor, e.g., Si.

In contrast, the bands of conventional semiconductors are parabolic and separated from each other by a gap with size E_G; see Fig. 2.5(b) **[8]**

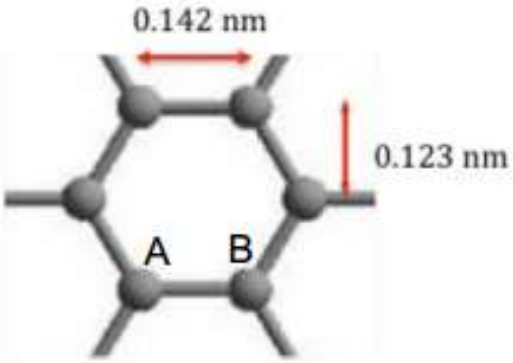
2.3.1 Physical Property

- **Thickness -**

With only one layer of carbon atoms, graphene is the thinnest material ever found.The thickness is about 0.335 nm.

- **Density-**

Each hexagon contains 2 carbon atoms.
⇒2 carbon atoms in 0.052 nm^2
⇒density = 0.77 mg/m^2



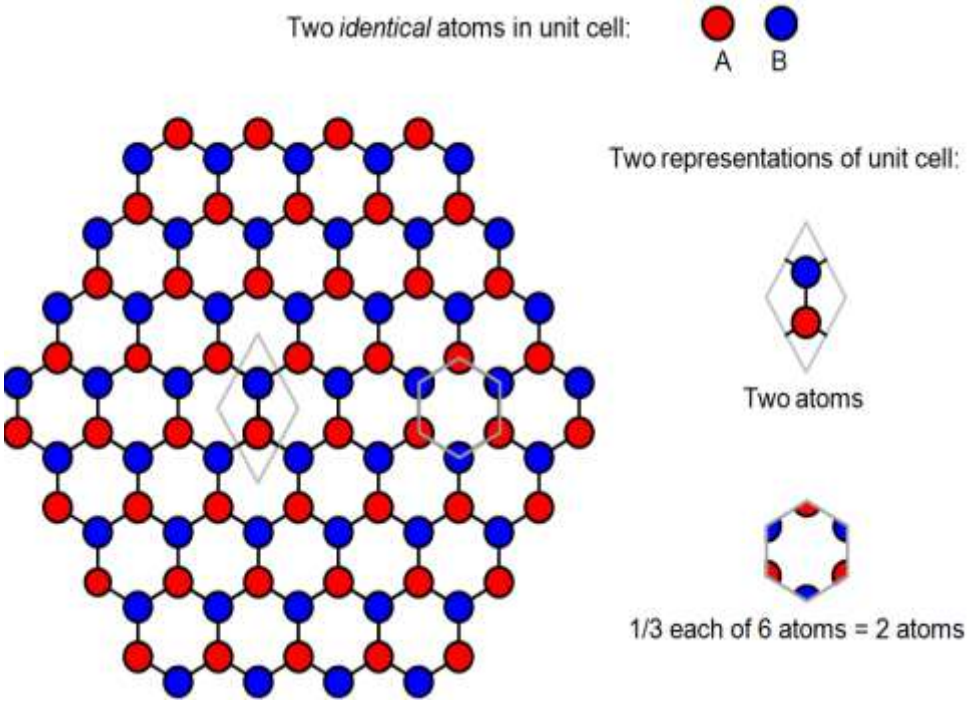


Figure 2.6 - Graphene Unit Cell

2.3.2 Optical Property [30]

- One atom thick membrane
- Nearly transparent
- Monolayer graphene absorbs $\pi\ \alpha \approx 2.3\%$ of white light (97.7 % transmittance), where α is the fine-structure constant.

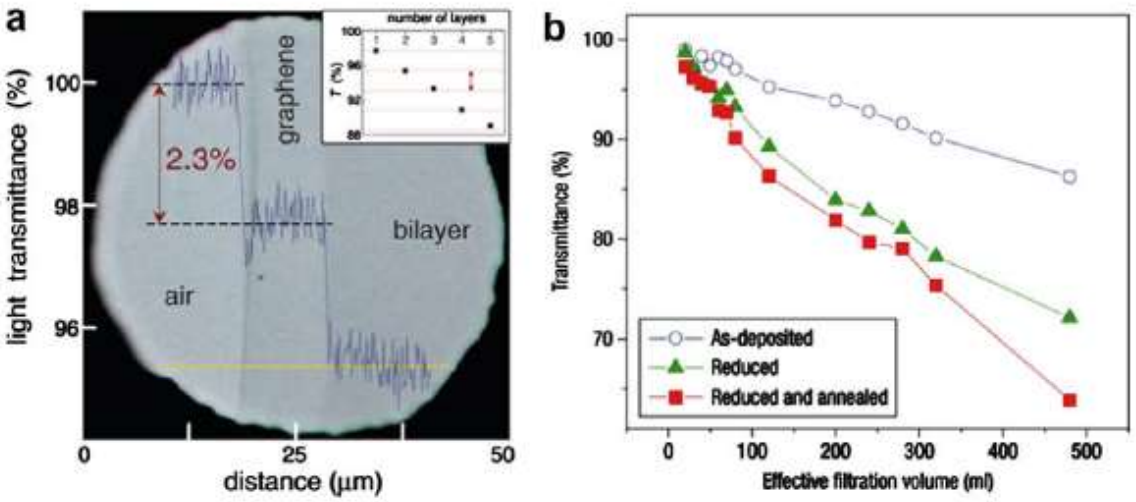


Figure 2.7 – (a) Distance vs. light Transmittance curve and **(b)** Effective filtration volume vs. Transmittance curve

2.3.3 Electronic properties:

- High electron mobility (at room temperature ~ 200.000 $cm^2/(V{\cdot}s)$,, ex. Si at RT~ 1400 $cm^2/(V{\cdot}s)$, carbon nanotube: ~ 100.000 $cm^2/(V{\cdot}s)$, organic semiconductors (polymer, oligomer): <10 $cm^2/(V{\cdot}s)$

$$v_d = \mu E$$

Where $\mathbf{v_d}$ is the drift velocity in m/s (SI units)
E is the applied electric field in V/m (SI)
μ is the mobility in $m^2/(V{\cdot}s)$, in SI units.

- Resistivity of the graphene sheet ~10^{-6} Ω·cm, less than the resistivity of silver (Ag), the lowest resistivity substance known at room temperature (electrical resistivity is also as the inverse of the conductivity *σ*, of the material, or

$$\rho = \frac{1}{\sigma}$$

2.3.4 Mechanical Properties [33]

- High Young's modulus (~1,100 Gpa)
- High fracture strength (125 Gpa)
- Graphene is as the strongest material ever measured, some 200 times stronger than structural steel.

Figure 2.8 – Graphene Sheet Strength

2.4 Potential Graphene Application

Graphene can be used in these following sectors-

- Single molecule gas detection
- Graphene transistors
- Integrated circuits
- Ultracapacitors
- Graphene biodevices
- Touch screen
- Photodetectors

What to expect from Graphene - (Major Applications)

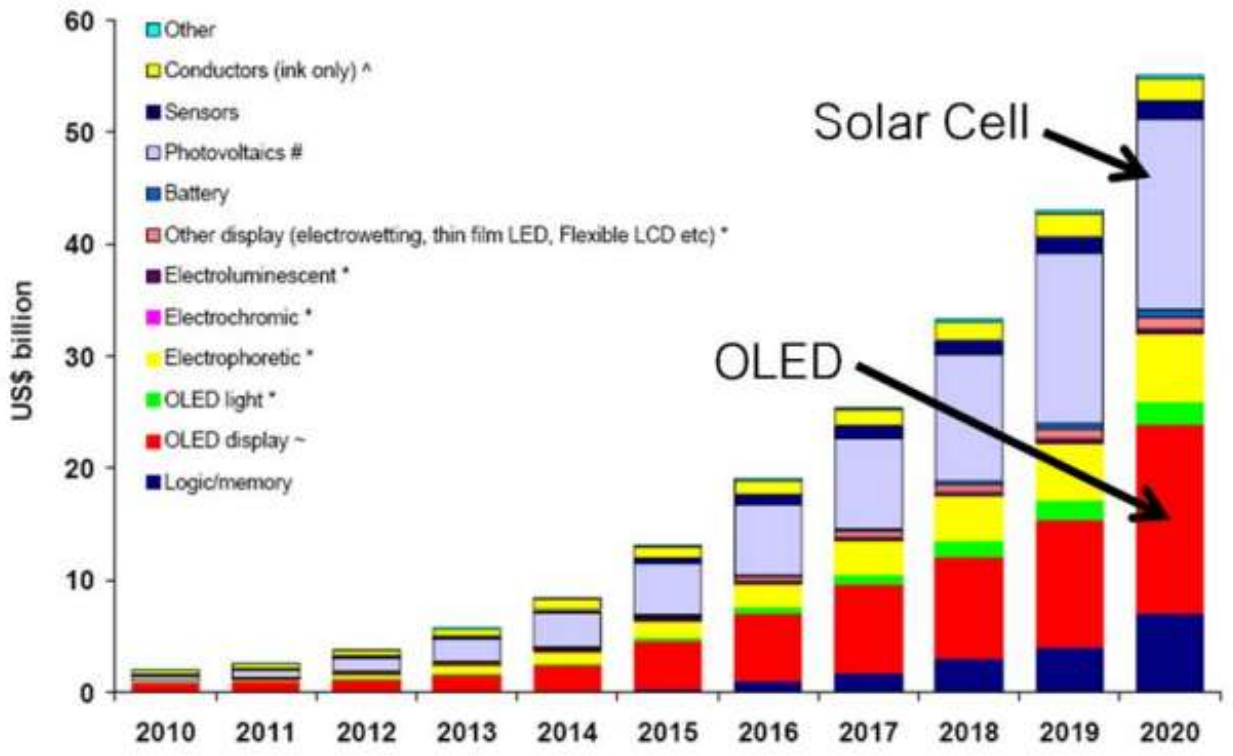


Figure 2.9 – Carbon Nanotubes and Graphene for Electronic

CHAPTER 3

GRAPHENE BASED FIELD EFFECT TRANSISTOR AND BACKGROUND

In this chapter we will summarize the current proposed Graphene based FET's structure and some future GFET concept being proposed by researchers. GFET introduction, classifications

3.1 GFET Introduction

Graphene based field effect transistors are known as GFET(s). Like a conventional FET, GFET has three major terminals- source, drain and Gate. The size of a GFET is 90nm – 100nm.

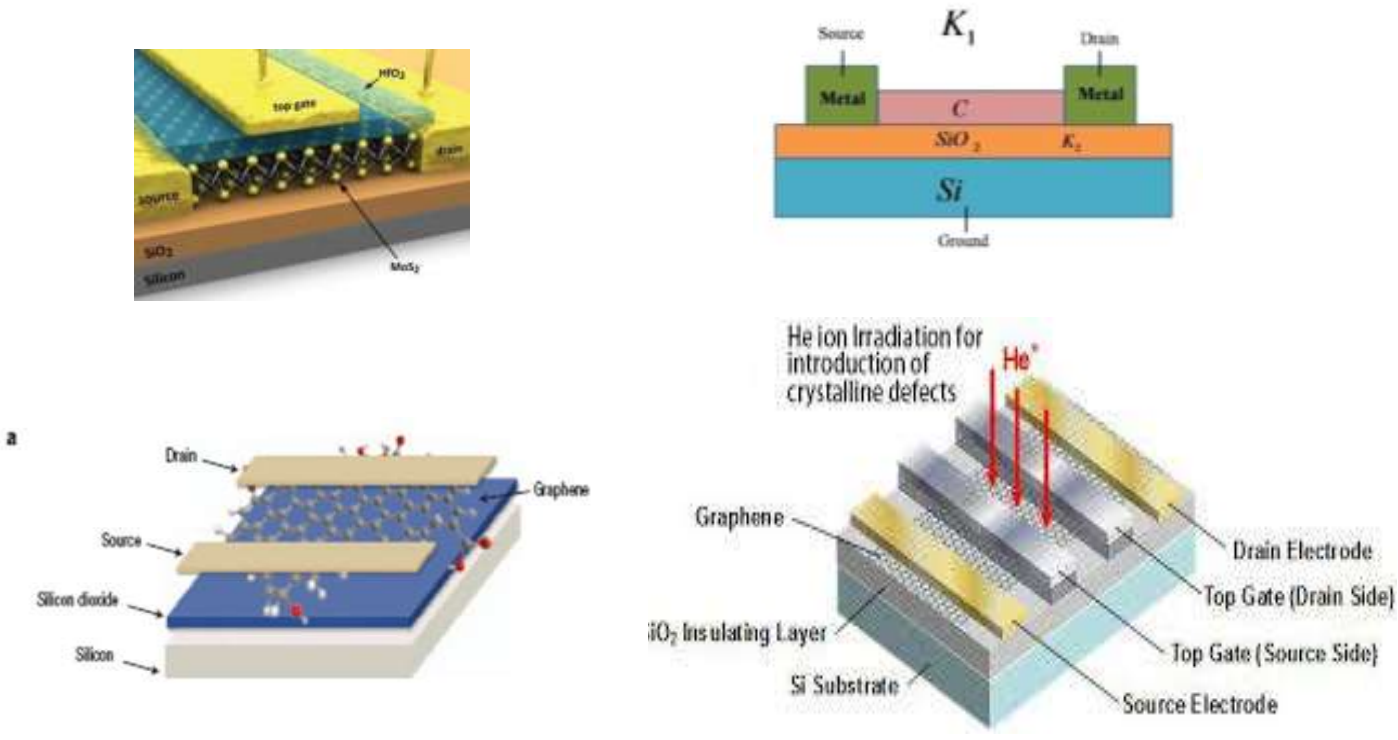


Figure 3.1 – Different types of GFET

3.2 Classifications and Basic Transistor Structures

A variety of different graphene transistor configurations has been presented during the past five years that can be categorized in different ways, as shown in Fig. 2.6. In the following, we review the current status of graphene transistors and start with MOSFETs having large-area gapless channels, examine their potential for analog/RF applications as well as for flexible and printable electronics, and introduce the side-gate architecture. Next, bilayer and GNR MOSFETs operating like conventional MOSFETs (i.e., no tunneling involved) are considered, followed by a short discourse on tunneling MOSFETs. Finally, vertical graphene transistor concepts exploiting tunneling mechanisms are briefly considered. **[8]**

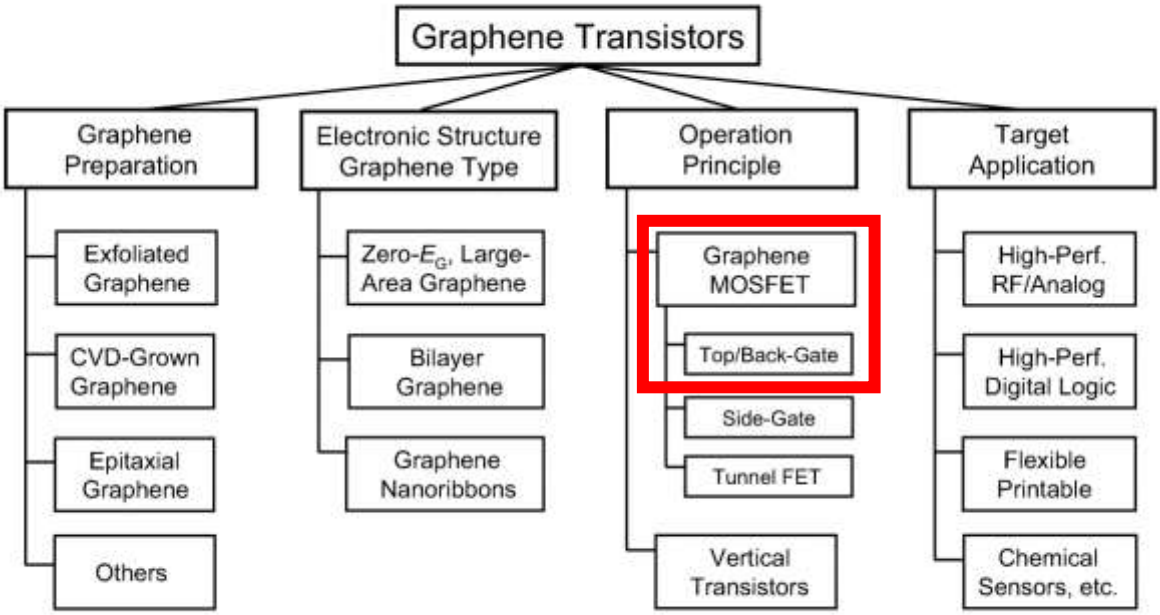


Figure 3.2 - Classification schemes for graphene transistors.

So, mainly two types-

- Top gate GFET
- Back gate GFET

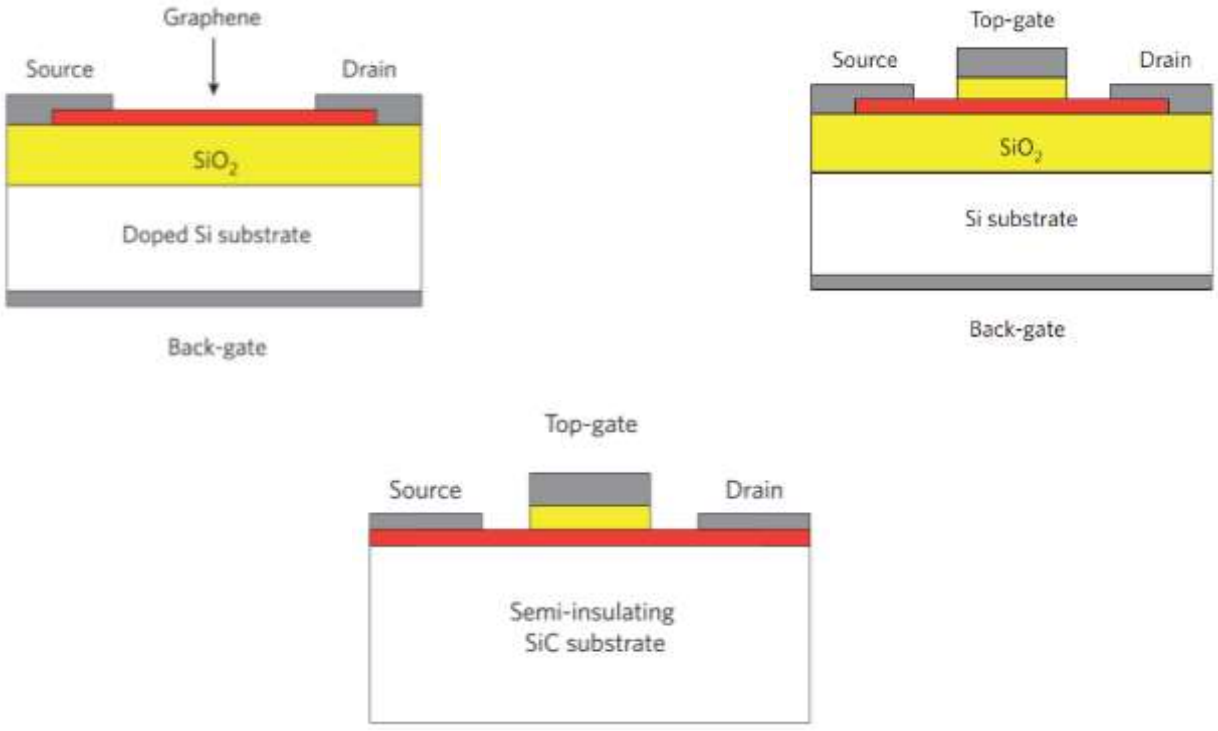


Figure 3.3 - Schematics of different graphene MOSFET types: back-gated MOSFET (upper left); top-gated MOSFET with a channel of exfoliated graphene or of graphene grown on metal and transferred to a SiO2-covered Si wafer (upper right); top-gated MOSFET with an epitaxial-graphene channel (lower mid).

CHAPTER 4
GRAPHENE BASED FIELD EFFECT TRANSISTOR FABRICATION

Graphene FET fabrication consists of couple of steps. There is a general process of GFET fabrication and some commercial process of fabrication.Graphene fabrication process can be described by the following flow chart:

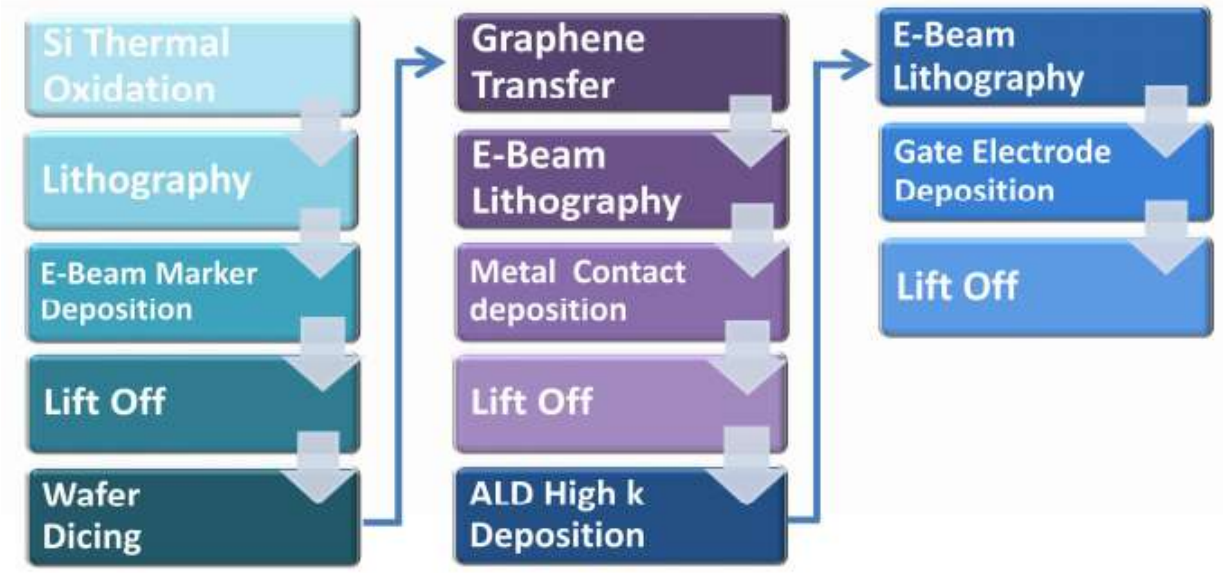


Figure 4.1- Graphene FET fabrication process flow chart

In this chapter, fabrication process will be discussed **[34]**.

4.1 Graphene production

4.1.1 Substrate preparation

An appropriate substrate requires an insulator film with specific thickness for identification of graphene on the substrate.Therefore, fabrication process started with thermal oxidation of n-type silicon wafer in oxidation furnace. In order to

have maximum contrast in visible light, 90nm oxide thickness was chosen and 99 nm practical thickness was measured by ellipsometry.These marks also help to spot graphene flakes for device designing purposes. The layout of e-beam alignment marks has a special design in order to enable mapping the final 0.5 cm x 0.5 cm chips.

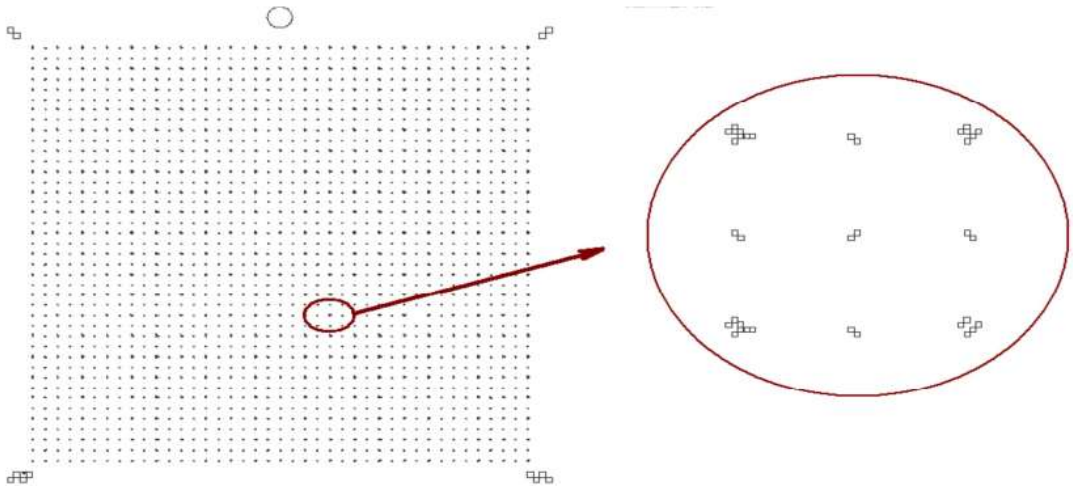


Figure 4.2- The lay out for EBL alignment marks.

In order to have large atomic contrast, 100 nm Tungsten deposited using electron beam evaporation tool (Provac PAK 600 Coating System) and patterned using lift off process. The result was inspected with an optical microscope.

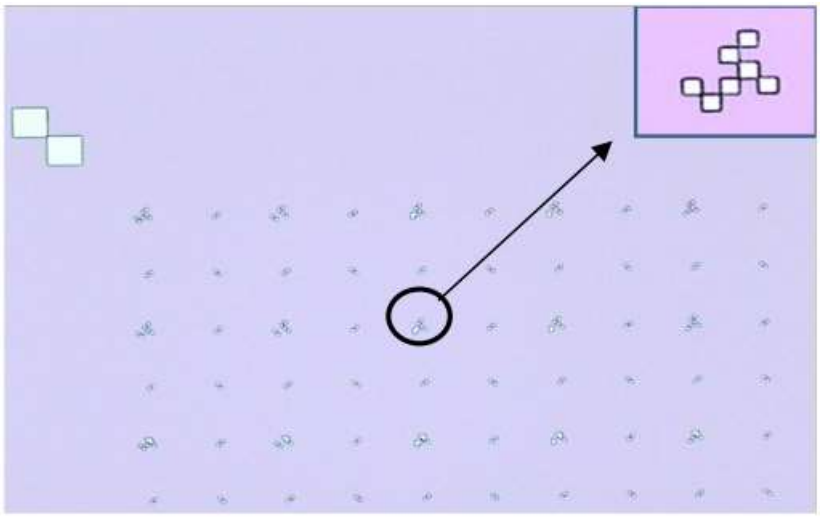


Figure 4.3- EBL alignment marks under microscope

Then, the wafer was diced (Disco DFD640 saw) into 0.5 cm X 0.5 cm pieces. But, before dicing, we coated the wafer with photoresist in order to prevent possible effect of the dicing process on SiO_2 surface.

4.1.2 Graphene production and transfer

Graphene was exfoliated from natural graphite with adhesive tape which helps to repeatedly peel away graphite layers until thin layers of graphite or thick layers of grapheme remain on the tape. Then, graphene was transferred onto the clean surface of the prepared substrate by sticking the tape on the chip and taking it off after a while. Afterward, the chips were inspected to find graphene flakes.

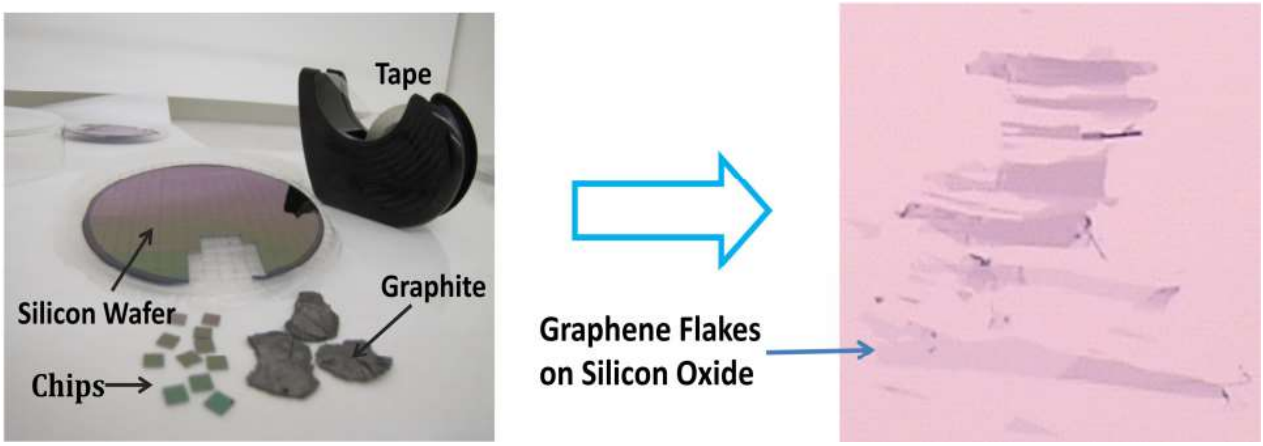


Figure 4.4 - Graphene was exfoliated by adhesive tape and transferred onto the substrate (pictute on the right hand side). The most transparent flakes in the picture are single layer graphene while dark purple shows thicker multilayer graphene.

4.2 Device Fabrication

Device fabrication initiated by device design followed by one or two steps of e-beam lithography, metal deposition, high-k atomic layer deposition, and lift-off which we will briefly explain each in this part. The process steps are shown schematically in figure 4.5

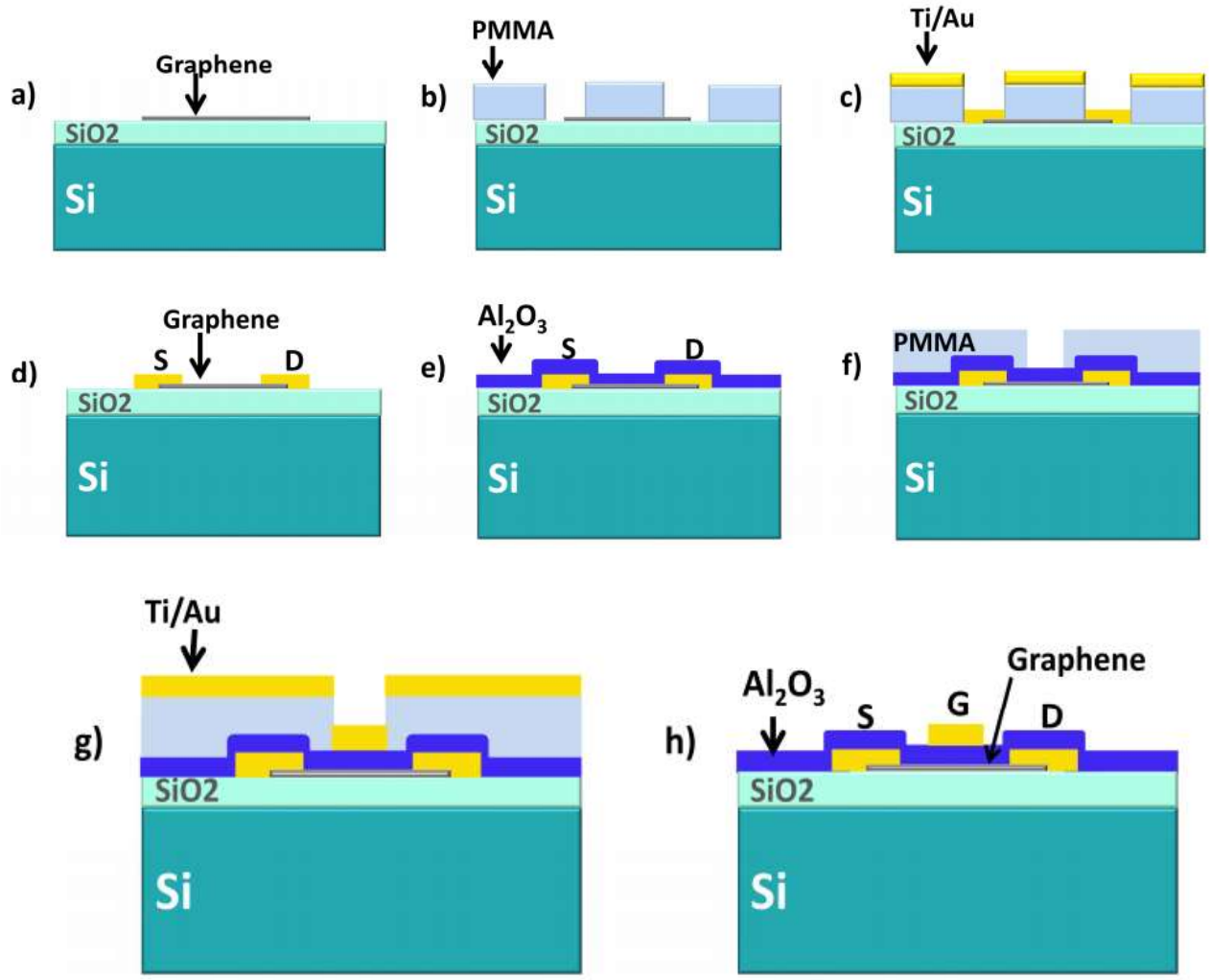


Figure 4.5 - GFET fabrication process steps, **a)** graphene is transferred onto the substrate, **b)** resist coating (PMMA), **c)** PVD of Ti/Au on the sample, **d)** Lift-off, **e)** Al_2O_3 deposition by ALD, **f)** resist coating (PMMA), **g)** PVD of Ti/Au on the sample, **h)** after Lift-off.

4.2.1 Design

Because of random shape and position of exfoliated graphene flakes, different devices corresponding to different flakes were designed with AutoCAD software. In our chips, one or three devices were designed for a graphene flake depending on the size and shape of that flake.

Figure 4.6 shows an example of device design.

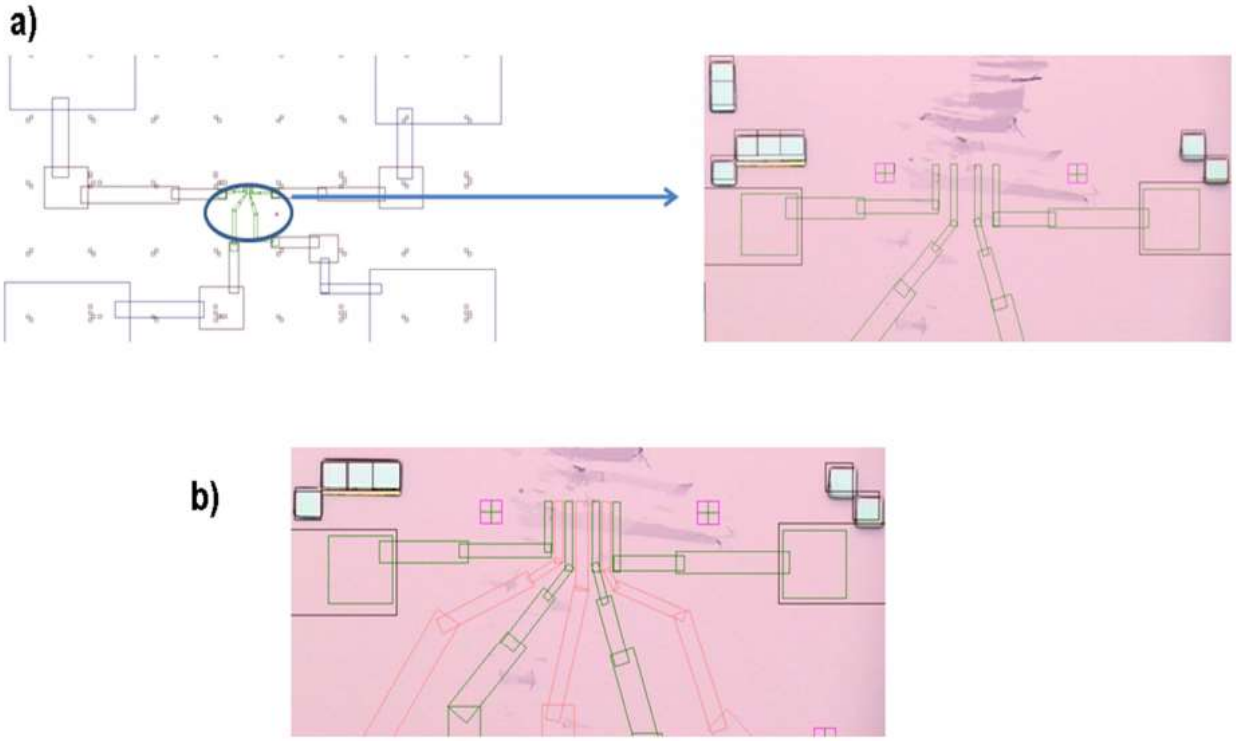


Figure 4.6 - The design on a graphene flake, **a)** three back-gated devices on a graphene flake, **b)** designing of the top gate electrode for the same flake.

Designing of our GFETs can be divided into two parts, subsequent e-beam lithography steps. First part was involved designing of source/drain contacts, measurement pads, and also alignment marks for the second step of e-beam lithography (fig. 4.6.a). Second, the top gate electrode and measurement pads were patterned (fig. 4.6.b).

4.2.2 E-beam Lithography (EBL)

Random nature of exfoliated graphene made using of EBL inevitable in GFET fabrication process. One-step and two-steps e-beam lithography applied for back-gated and top-gated devices respectively. Approximately 200 nm PMMA (A2) was spinned as EBL resist, and was exposed by Raith Turnkey 150 SEM & E-beam lithography system. The resist was developed by Methyl isobutyl ketone (MIBK)

Followed by Isopropanol (IPA). Figure 4.7 shows the pattern of back-gated devices after the resist was developed.

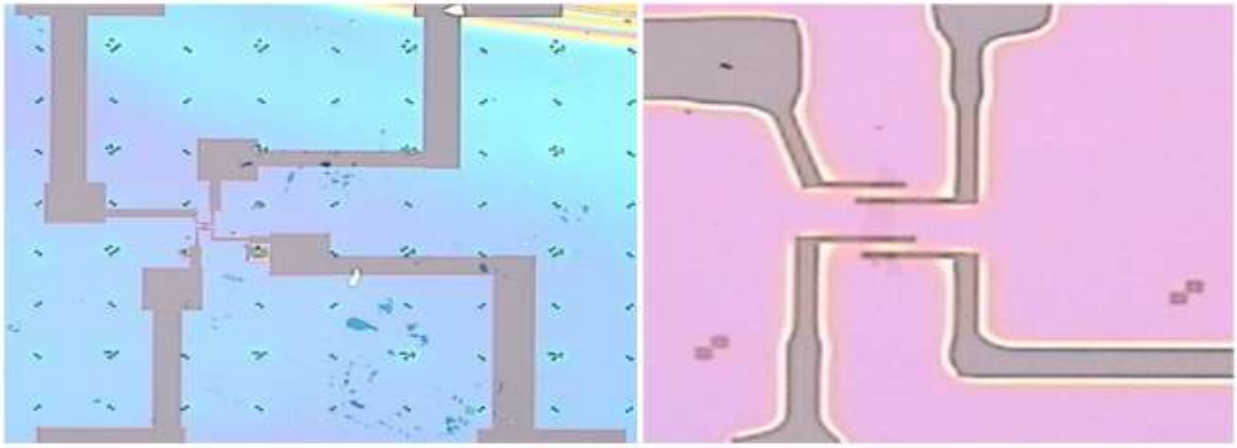


Figure 4.7 - Pattern of metal contacts under microscope, connections and pads after resist developing 30 seconds in MIBK.

4.2.3 Source and Drain Metal Contacts

We deposited 5/40 nm Ti/Au using electron beam physical vapor deposition (PVD). Ti is used to solve the adhesion problem of gold on SiO_2. Figure 4.8 shows an example of resulting source and drain contacts after the lift-off in acetone with a short period of sonication.

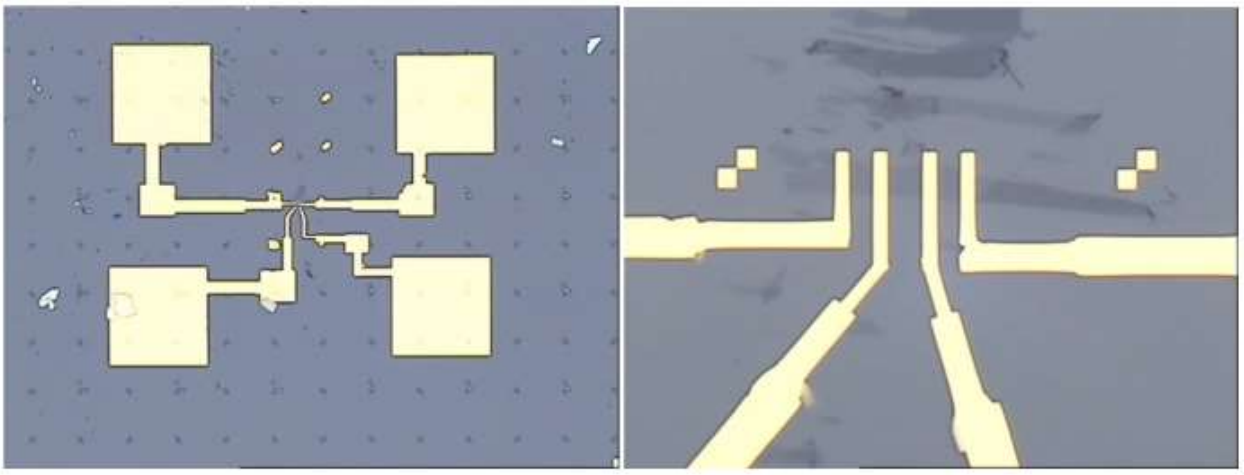


Figure 4.8 - The top-view of the back-gated device under microscope after lift-off process.

Now the back-gated GFET is ready for electrical characterization. At this step, we continue the process description to fabricate top-gate devices.

4.2.4 High k material deposition using ALD

As it was discussed in chapter one, applying a high k material as gate insulator can increase both charge control and screening effect. However the deposition method is critical in order to have fewer defects to the graphene sheet, and high quality high-k material. Atomic Layer Deposition (ALD) is known as an appropriate choice for high-k deposition on graphene **[35]**. So we used ALD (BENEQ TFS 200, fig 2.8) in order to deposit Al_2O_3 on the sample.

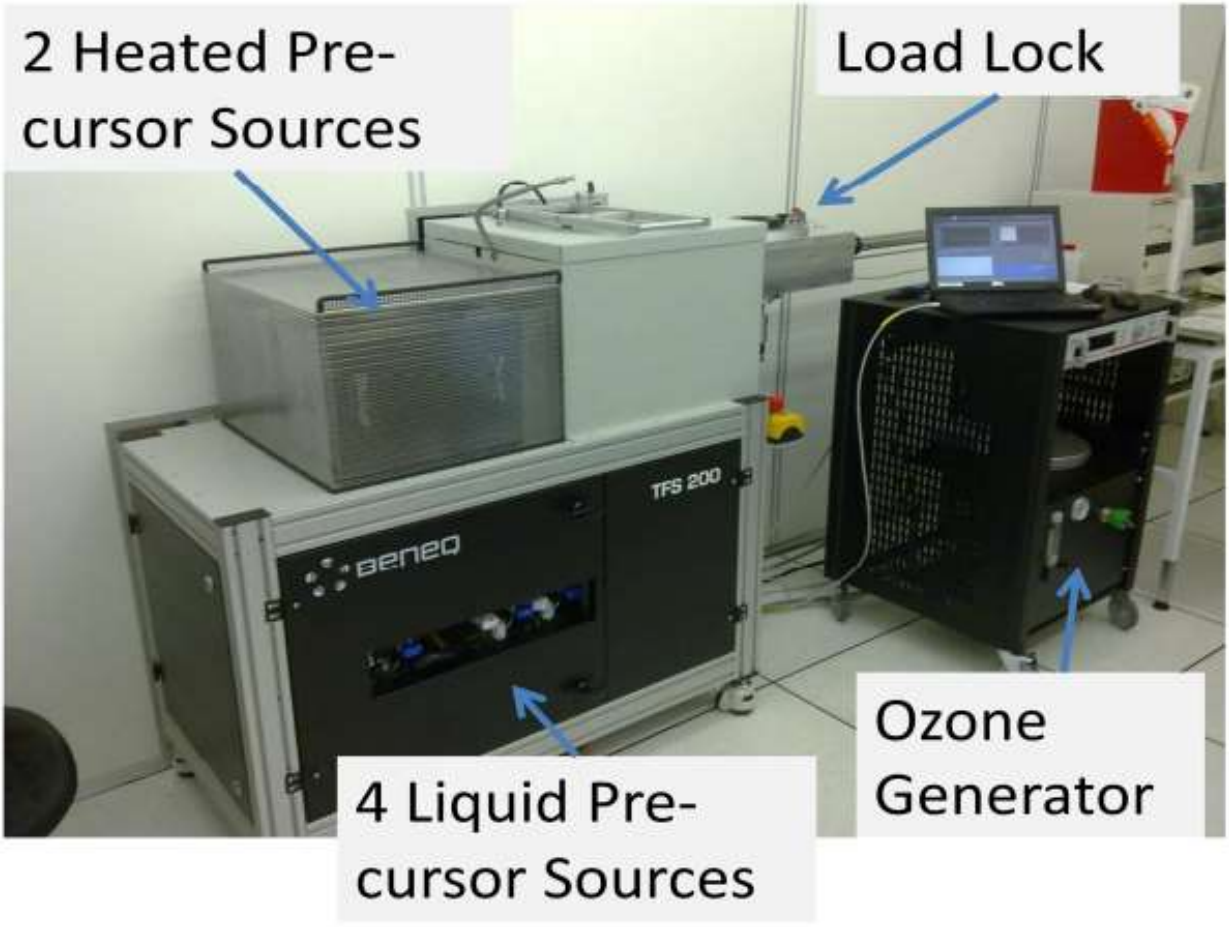


Figure 4.9 - The ALD tool and its different parts.

Atomic layer deposition (ALD) is considered as a chemical vapor deposition method with sequential self-terminating gas-solid reactions **[36]**. As it is shown in figure 4.10.a, four steps happen in the chamber/reactor of ALD tool to make a cycle.

- Reaction of the first reactant gas (trimethylaluminum, in case of Al_2O_3 deposition) with functional hydroxyl group of the surface. This reaction terminates when the hydroxyl group on the surface saturates.

- Remained gas (trimethylaluminum) and the by-product (Methane) are removed from the reactor in this step.

- Pulsing the second reactant (water vapor) reactivates the surface. The reaction stops after saturation of the surface.

- The reactor is evacuated. Repetition of this cycle provides desirable amount of deposited material on the surface. The cross-flow reactor is shown schematically in figure 4.10.b.

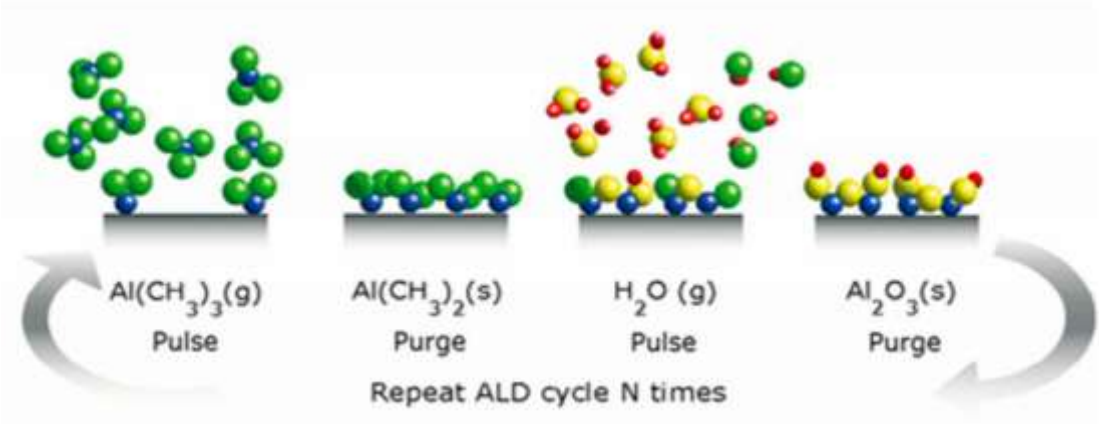


Figure 4.10 - Shows four steps of a cycle in atomic layer deposition of Al_2O_3. It starts with flowing of Trimethylaluminum into the reactor, reaction with functional group on the surface, puging of remained TMA and by-products, flowing of H_2O into the reactor and reactivation of the surface, and finally purging the gases from reactor.

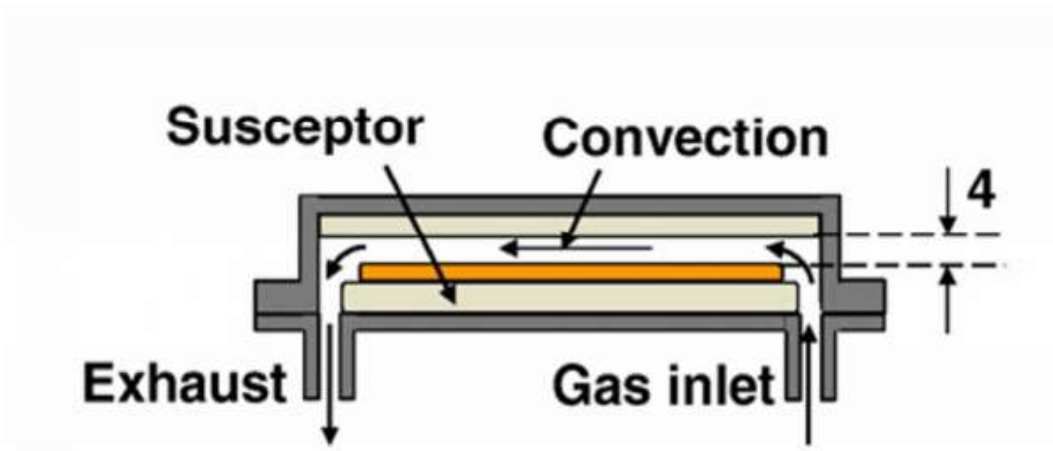


Figure 4.11 - Cross-flow reactor system which is used in our ALD tool

However, because of the absence of a functional group, direct ALD is not possible on the surface of graphene. Using a thin film of oxidized metal could function as a nucleation layer for ALD process **[37]**.

So, 3-4 nm Aluminum was deposited on the sample using e-beam vapor deposition, and it was exposed to the air for natural oxidation. Then, the sample was transferred to the ALD reactor for annealing and in-situ Al_2O_3 deposition using trimethylaluminum and water vapor as reactant gases.. As it can be inferred from figure 3.10, 300 complete cycles should be run in 200˚C in order to have 30 nm thick Al_2O_3.

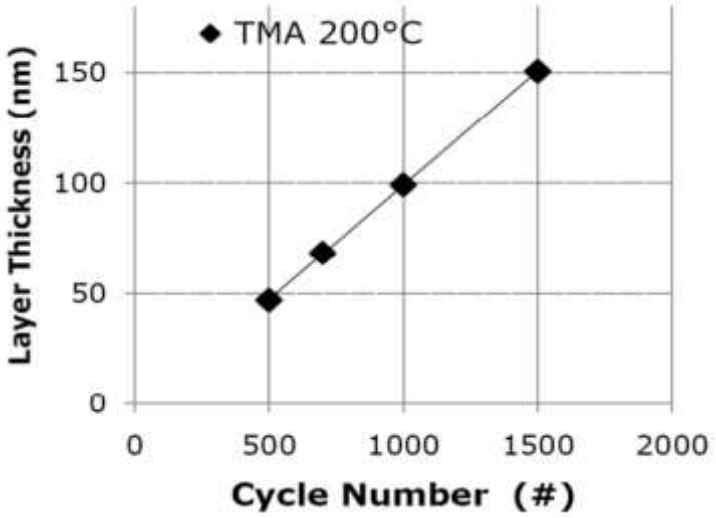
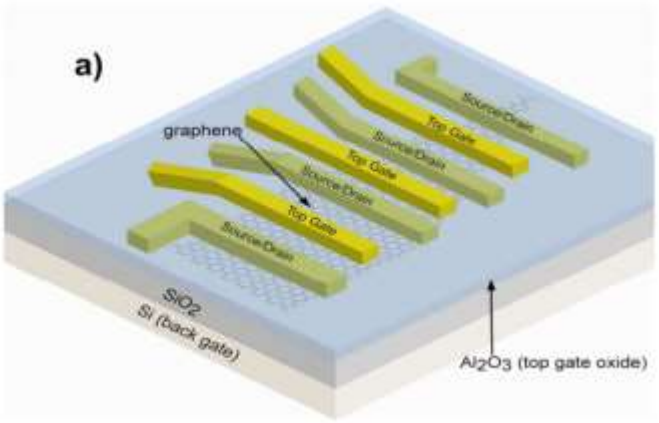


Figure 4.12 - Layer thickness versus cycle number for deposition of Al2O3 using TMA at 200˚C **[38]**.

4.2.5 Gate Electrode

Fabrication of gate electrode requires another EBL step, metal deposition and lift-off. Roughly 200 nm PMMA deposited on the sample using OPTIspin SST20 coating tool. For e-beam lithography we used the alignment marks fabricated in previous steps (pink squares in figure 4.6).The same as what was done for source and drain contacts, 5/40 nm of Ti/Au was deposited by Provac PAK 600 Coating System, and followed by lift-off in Acetone. Finally, the schematic and top view picture of resulted top-gate GFET are illustrated in figure 4.12.a and 4.12.b respectively.



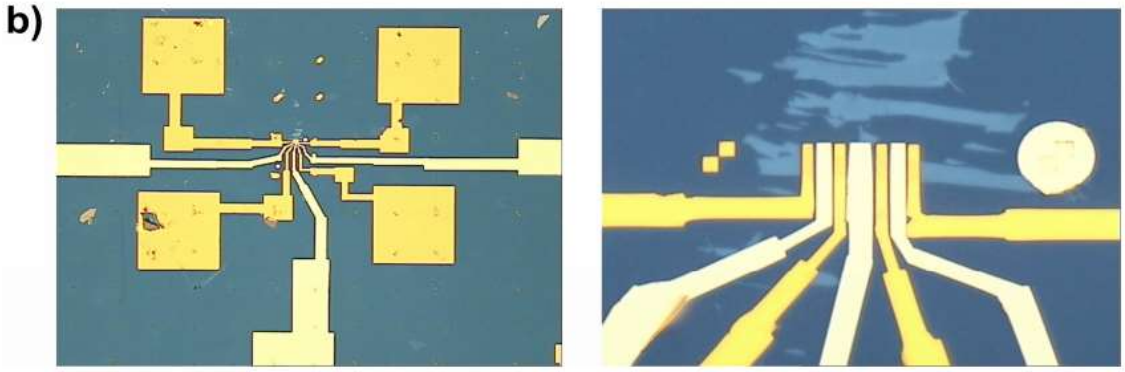


Figure 4.13 - Top-view under microscope of GFET with top gate.

There are a few more processes of fabrication of Graphene FET. They are briefed below**[39]**:

A. IBM Process

Graphene devices have been made previously by placing the graphene sheet on top of an insulating substrate, such as silicon dioxide. However, this substrate can degrade the electronic properties of graphene. However, the team of researchers has found a solution to minimize that. A diamond- like carbon is placed as the top layer of substrate on a silicon wafer. The carbon is nonpolar dielectric and does not trap or scatter charges as much as the silicon dioxide alone. This new grapheme transistor, due to the diamond-like carbon, shows excellent stability in temperature changes, including extremely cold temperature like that in space. IBM has announced the development of a new graphene transistor which has a cutoff frequency, a measure of device speed under operating conditions and is typically a fraction of intrinsic speeds often reported, of 155GHz (155 billion cycles per second). These new high-frequency transistors are being targeted to applications primarily in communications such as phones, internet, and radar.

B. Fujitsu Method

Fujitsu has made transistors on graphene grown directly on insulating substrates with a novel structure this process involves starting with an iron film catalyst over an oxide film on a silicon substrate. To make transistors, the iron is formed into strips using a conventional photolithography before graphene growth. Once the graphene has been grown, source and drain electrodes of titanium-gold film are formed at the ends of each graphene strip. This leaves the center, which will eventually become the channel, exposed. The source and drain metal also bonds the ends of each graphene strip to he substrate, allowing the iron under it to be etched away with acid to leave a graphene channel suspended as a bridge.

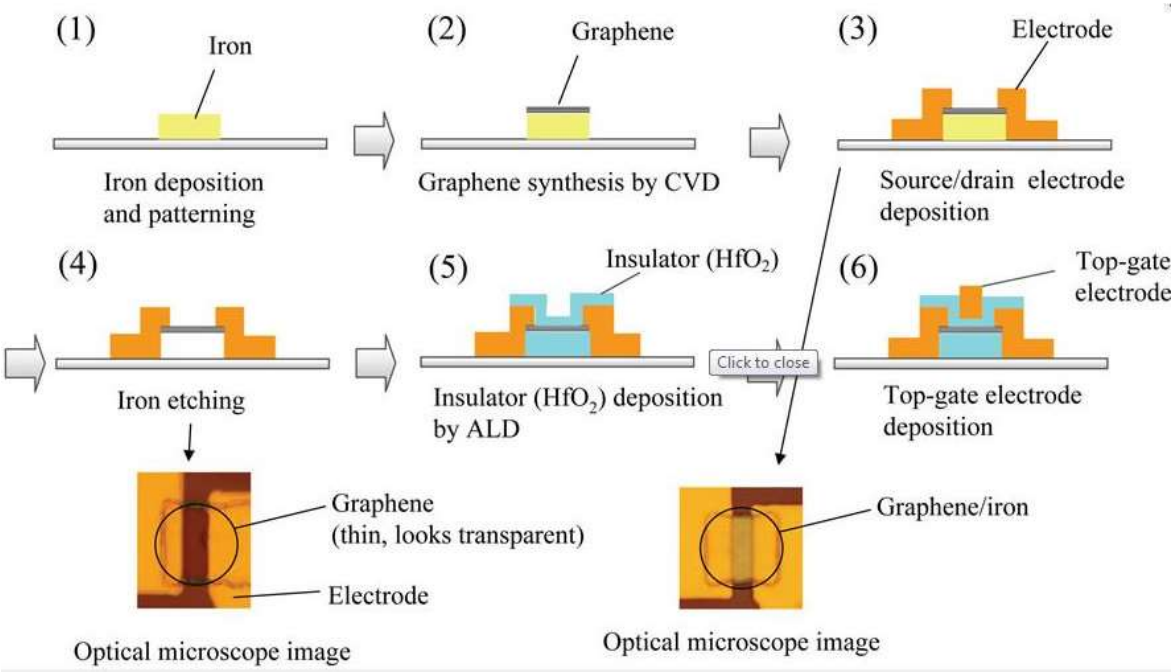


Figure 4.14 - Fujitsu process of making graphene transistor.

To stop this breaking, atomic layer deposition is used to replace the missing iron support with insulating hafnium dioxide. At the same time, HfO_2 also grown on top of the channel to form an insulator for the gate which is finally laid down on top. It enables formation of graphene transistors across the entire surface of a large substrate. The relationship between drain current and gate voltage clearly shows am bipolar characteristics that are particular to graphene. As graphene at the thickness of a few nanometers is transparent, it is a candidate for use as the channel and electrode material in thin-film transistors used in video displays. The manufacturing of these new graphene transistors can be accomplished utilizing technologies already in place for standard silicon devices.

CHAPTER 5

CHARACTERIZATION OF GRAPHENE FET

In this chapter, characterization of graphene FET will be briefly discussed based on the fabrication process stated in the previous chapter.

5.1 Raman spectroscopy

Raman Spectroscopy is a process that confirms if the graphene flake that is being used as the channel of the GFET is of single layer or not. It is a non-destructive and efficient process of detecting a single layer graphene flake. The Raman Spectroscopy that is being discussed here is applied with Horiba LabRAM.

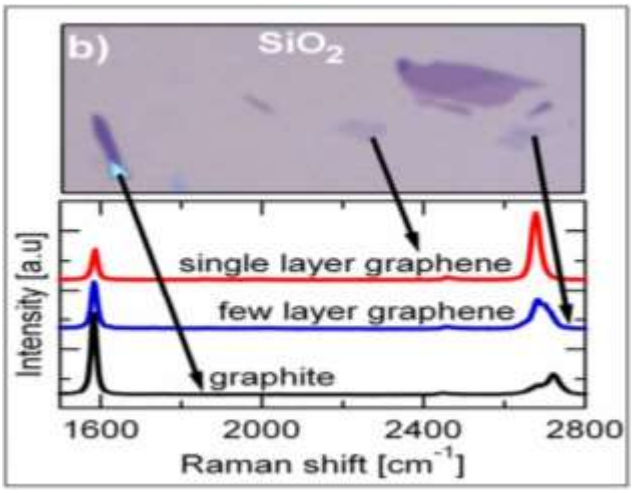


Figure 5.1 - Microscope image of single layer and few layer graphene flakes, graphite; and their corresponding Raman shift**[40]**.

Figure 5.1 shows Raman Spectrum for single layer and multilayer graphene, and also graphite **[40]**. The Raman spectrum of single layer graphene has two intense features; a peak around 1580 cm^{-1} due to sp^2 vibrations (G band), and more intense single sharp peak (2D band) around 2700 cm^{-1}**[41]**. This 2D band is broader in bilayer graphene and graphite, since it consists of four and two

components respectively **[42]** because of changes in band structure and electron-coupling **[41]**.

5.1.1 The experimental procedure raman spectroscopy

Microraman spectroscopy at room temperature with Horiba LabRAM and Ar^+ laser source (λ=514.5 nm) is performed here. The laser beam was aimed on the centre of graphene flake (the inset of fig. 5.2) using a microscope. The resulted Raman spectrum in figure 5.2 shows a sharp G-peak at 1580 cm^{-1}, and a strong single 2D-peak at 2700 cm^{-1}. Comparing these results with the Raman finger print of monolayer graphene in figure 5.1, confirms the single-layer graphene in the channel area**[43]**.

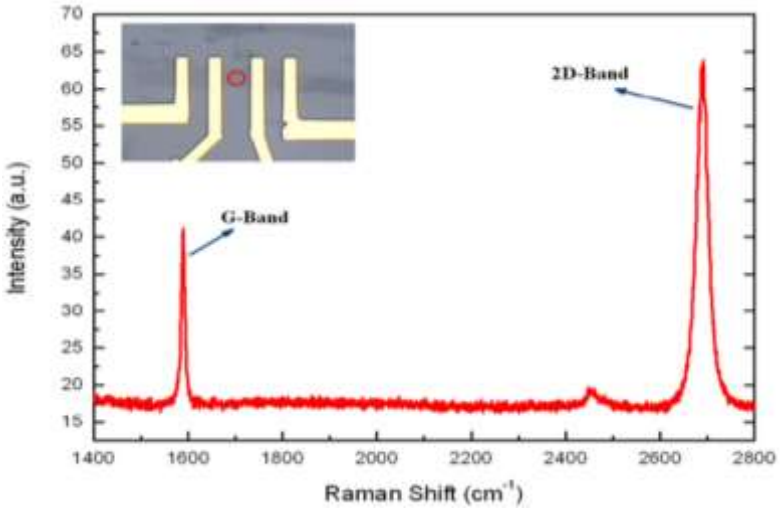


Figure 5.2 - Raman shift with sharp 2D-band peak. The Raman spectroscopy confirms the single layer graphene we used in the channel. The inset shows the location of the laser beam on the graphene flake**[43]**.

5.1.2 Investigating the effect of Al_2O_3 deposition on the graphene flake

In order to investigate the effect of Al_2O_3 deposition on the graphene flakes, Raman spectroscopy was also performed for a sample after the deposition process. Its Raman spectrum is shown in figure 5.3. The G-peak and strong single peak of 2D-band in this Raman spectrum shows that still the single layer graphene is there. It means that the graphene's electronic structure is not mainly affected by the deposition process. In addition, having no observable peak at 1350 cm^{-1} (D-

band) which is a measure of defects in graphene crystal implies that no damage is introduced to the graphene flake**[44]**.

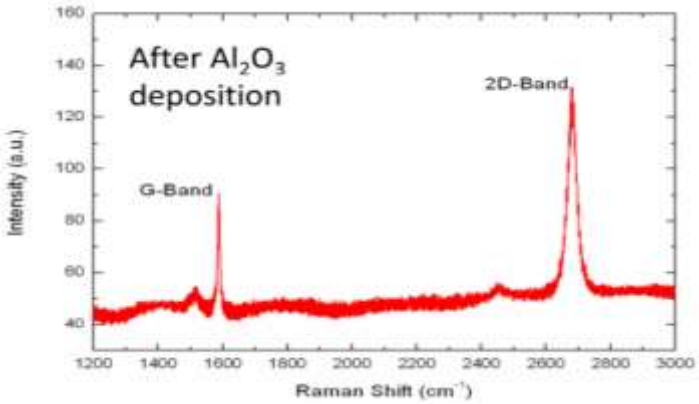


Figure 5.3 - Raman spectrum for a graphene flake with Al_2O_3 deposited on top**[44]**.

5.2 Characterization of back-gate devices

After first step of EBL and lift-off process, the back gate devices were ready for electrical measurement. Now, there are several cases need to be studied here like when a high-k deposited layer is on top and when the GFET is uncovered. Also there is the case when the back-gate devices have back contacts.

5.2.1 GFET with a high-k deposited layer on top

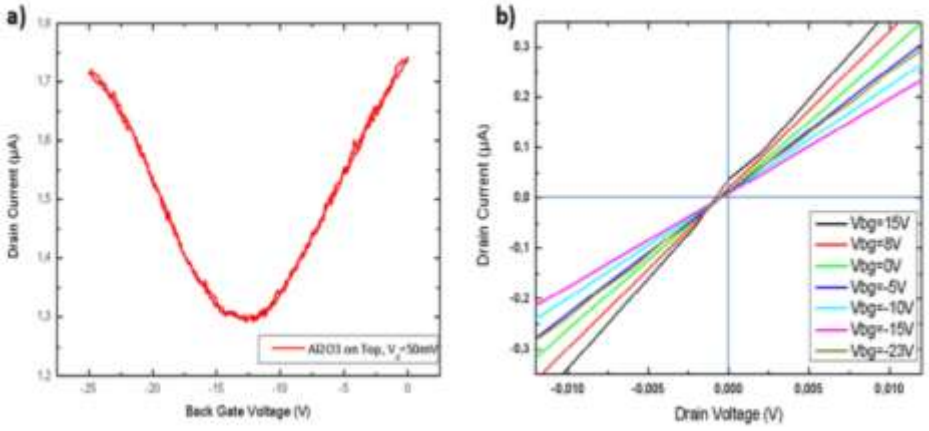


Figure 5.4 - **a)** Back gate transfer characteristics of GFET with a high-k deposited layer on top. **b)** Output characteristics shows linear behavior in the low-field regime**[45]**.

Figure 5.4 shows the transfer and output characteristics for a back-gated device with 20 nm Al_2O_3 layer on top, and gate length of 5.2 µm. As it was expected, the drain current is modulated almost symmetrically with back gate voltage. Also, transfer characteristics have a minimum conductivity point (Dirac Point) at roughly -14 V.

Figure 5.4(b) illustrates the drain current as a function of source-drain voltage from -15 mV to +15 mV for various gate voltages. The drain current linearly increases with source-drain voltage which is a typical behavior for GFETs at low bias**[45]**.

5.2.2 Uncovered back-gate GFET

GFET is measured immediately after source/drain metal contacts were fabricated. So, the top side of the device was exposed to the air (uncovered device). Back gate bias was applied via the chuck stage; source pad was grounded and drain pad biased 50 mV. While the drain current was measuring, the chuck voltage swept from -15 V to 30 V and backward. The transfer characteristic of a device is depicted in figure 5.6. In this figure, dual back gate voltage sweep (fig. 5.6) reveals a minimum conductivity point of around +5 V, and existence of hysteresis about 3.5 V in this device**[46]**.

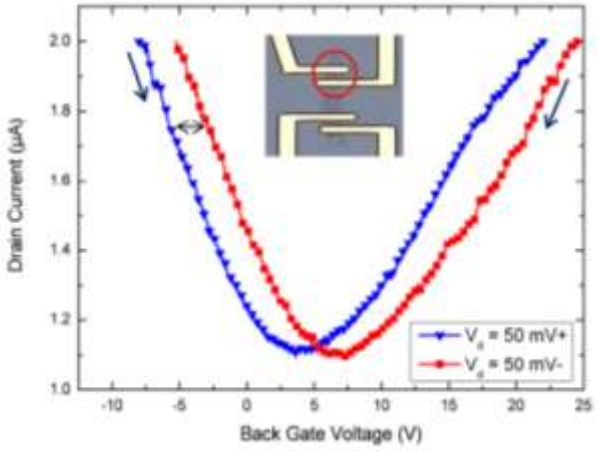


Figure 5.5 - Dual gate sweep I-V characteristics at V_{ds}=50 mV. The inset shows the microscope image of three devices on a graphene flake. The measured device is pointed out with red circle. Arrows show the direction of the voltage sweeping and hysteresis**[46]**.

5.2.3 Comparison in characteristics between uncovered devices and devices with Al_2O_3 on the top

Deposition of Al_2O_3 by the method applied here had four distinctive effects on back gate transfer characteristics.

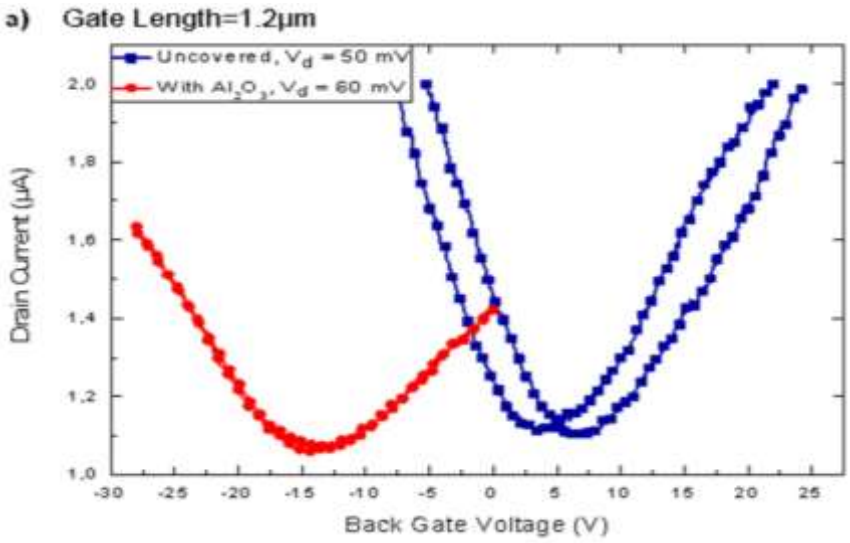


Figure 5.6 - Back gate transfer characteristics for uncovered (blue) device and with Al2O3 (red) for Gate length = 1.2 µm**[47]**

1. Effectively suppressed hysteresis for high-k dielectric.
2. A shift of the charge neutrality point (minimum conductivity) towards negative gate voltages.
3. Less spikes and more smoothness in the transfer characteristic of devices with top high-k film.
4. Degradation in mobility roughly by a factor of two by the deposition process**[47]**.

5.2.4 Back gate devices with back contact

As it was discussed, the substrate preparation involved thermal oxidation of the silicon wafer resulting in a 90nm thick layer of SiO_2 also on the back side of the wafer. It may affect transfer characteristics and mobility calculation of back gated devices. In order to understand how far it can affect the mobility, the back oxide is removed and back contact for the chips are made.

The chip is coated with photo resist and put it into the buffered HF for one minute to remove the back oxide. Then 100 nm Aluminum deposited on the back of the chip, using electron beam evaporation. The drain current versus gate voltage measurements in two different source drain voltages is shown in Figure 5.7.

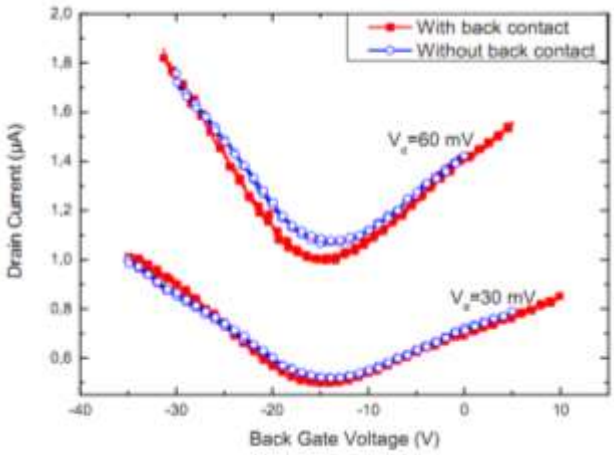


Figure 5.7 - Back gate transfer characteristics with using and without using back contact in two different source drain voltages (V_d =30 mV and V_d=60 mV)**[48]**.

Figure 5.7 indicates that there is no significant variation in electron transport. However, up to sixty percent mobility improvement is extracted for different devices. Thus, removing of back oxide and making the back contact resulted in more accurate mobility calculation and improved device performance**[48]**.

5.3 Characterization of top-gate devices

After Al_2O_3 deposition, electron beam lithography and lift-off, top-gate GFETs are ready for electrical characterization. Thus the top gate bias is applied using top

gate pad while the substrate is grounded. Current-voltage measurements confirm the top gate modulation with very low gate leakage current (Figure 5.8).

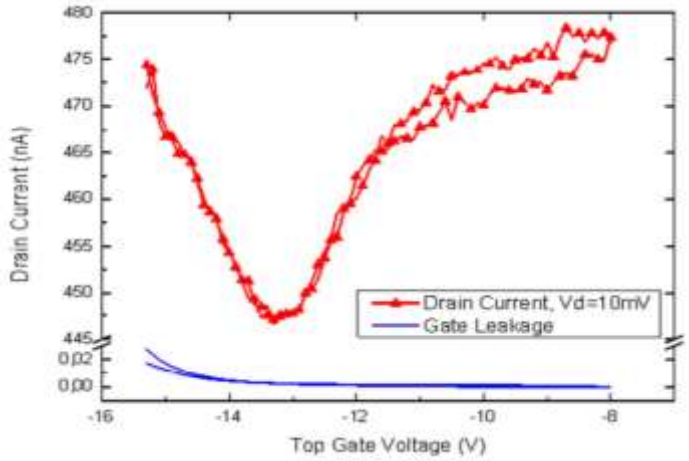


Figure 5.8 - Dual gate voltage sweep and gate leakage of top gate GFET at V_{ds}=10 mV**[49]**.

In Fig. 5.8, dual gate voltage sweep measurement shows almost no hysteresis in this device with gate length of 1.5 micron. Yet, the electron dominated transport at gate voltages greater than 2 volts away from Dirac point has a non-ideal behavior with some hysteresis. This behavior is not fully understood yet.

Figure 5.9 shows the transfer characteristics for a top-gate device in two different source-drain voltages, 10 mV and 30 mV. It can be seen that the drain current roughly scales with the source-drain voltage these top gate devices**[49]**.

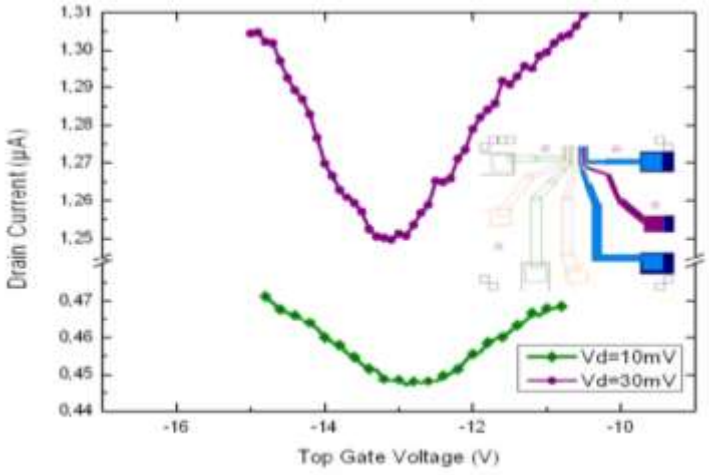


Figure 5.9 - Top gate transfer characteristics in low field, V_{ds} = 10 mV and 30 mV. The inset figure shows the tope view schematic of the device**[49]**.

CHAPTER 6
OPERATION OF GRAPHENE BASED FIELD EFFECT TRANSITOR

In this chapter we will summarize the operation principle of GFET, I-V characteristic, band energy diagram, charge density etc.

6.1 Operation of GFET

For both top and back gate GFET the operation principle can be divided into two sections. **[50]** The are-

1. Qualitative capacitance voltage characteristics
2. Qualitative current–voltage characteristics

6.1.1 Qualitative capacitance voltage characteristics

As a simple model that can explain the gate control of the channel charge, consider a series of two capacitors, one for the geometric capacitance of the gate and other for the quantum (DOS) capacitance of the graphene. The quantum capacitance **[32]** defined as,

$$C_q = \partial Q / q \partial E_F$$

represents the extra voltage required to modulate the charge density for a fixed electrostatic potential, which becomes significant—that is not infinite—when the DOS is limited as it is in semiconductor quantum wells and, even more so, graphene. Because of the linear band structure of the graphene, the quantum capacitance is dependent on the Fermi level, unlike a two-dimensional electron system (2DES) where the quantum capacitance is constant and dependent only on the effective mass of the carriers in the parabolic limit. Using this capacitance

model one can obtain the dependence of the channel charge on the gate voltage as shown in figure 6.1(a) in the zero temperature limit. Figure 6.2(b) shows the

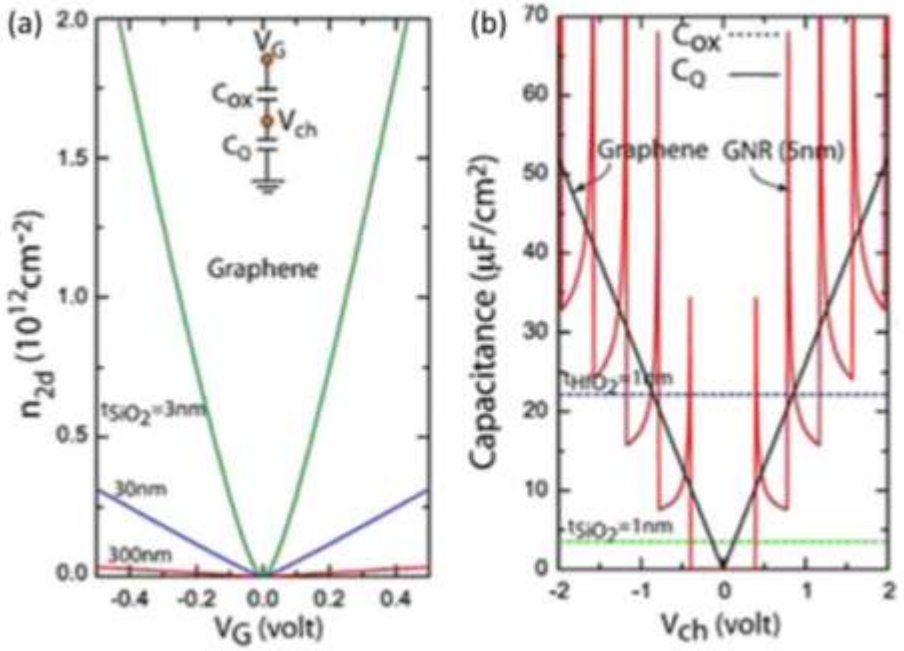


Figure 6.1 - (a) 2D carrier density in graphene as a function of gate voltage for different oxide thicknesses. **(b)** Quantum capacitance of 2D graphene and a 5 nm GNR compared with the parallel-plate capacitance of a 1 nm SiO_2 and HfO_2

quantum capacitance voltage characteristics for a 5 nm GNR (solid red) and bulk graphene (solid black). As you can see from figure 6.1 (b) effective oxide thickness (EOT) approaching 1 nm and reasonable channel voltages ($-E_F/q$ referenced to the Dirac point potential) the quantum capacitance of the graphene becomes comparable or less than than the oxide capacitance, and the benefits of reducing the gate EOT decrease. Thus, the small quantum capacitance of graphenes can negatively impact device FOMs. For example, as we have seen before, for large f_T having a small C_g helps. Also, the gate voltage-dependent capacitance adds nonlinearity which can negatively impact linearity metrics of the amplifiers and mixers. For more detailed analysis of carrier statistics and quantum capacitance of graphene sheets and nano ribbons refer to **[35]**.

6.1.2 Qualitative current–voltage characteristics

Although bulk graphene-based FETs have mobilities much larger than similar conventional FETs, because of the zero band gap of bulk graphene, the ON/OFF ratios are typically less than 10. Also because of the zero band gap, GFETs have ambipolar characteristics. Figure 6.2 (a) shows the typical transfer characteristics of GFETs, which can be understand as follows. As we have discussed earlier, at the heart of FET operation is the ability to modulate the charge density in the channel. In the absence of chemical doping, the gate voltage at the minimum current is the flat-band voltage, V_{FB}, usually referred to as the Dirac voltage, V_{Dirac}. This voltage corresponds to having the Fermi level at the Dirac point, as shown in figure 6.2(b). For $V_G > V_{FB}$ the Fermi level is in the conduction band and the right side of $I–V_{in}$ figure 6.2(a) is due to conduction of electrons, whereas for $V_G < V_{FB}$ the Fermi level is in the valence band and left side of I–Vin figure 6.2(a) is due to conduction of holes, and in the either case the conductivity is high because of the availability of carriers.

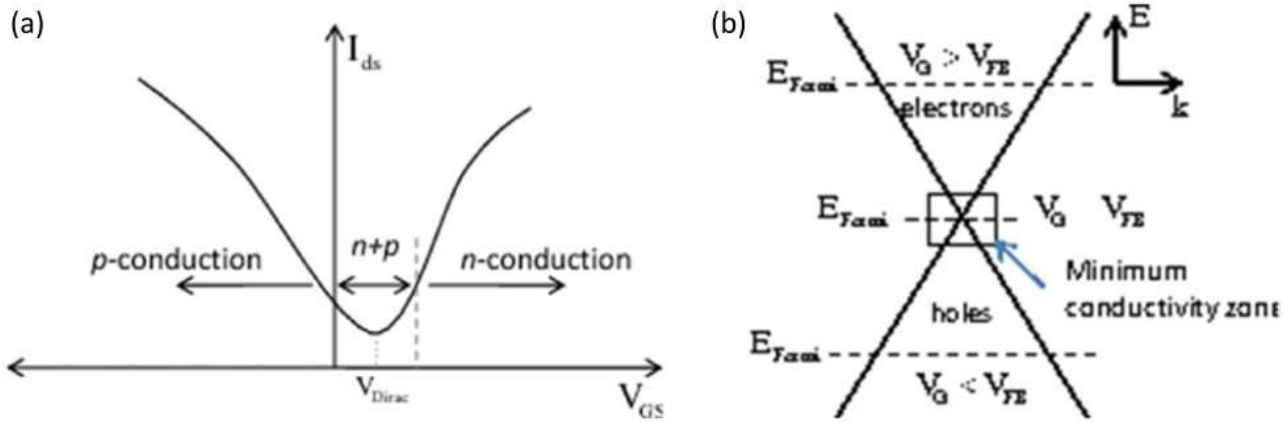


Figure 6.2 - (a) Schematic of typical transfer characteristics of a graphene-based FET and **(b**) schematic of band energy diagram showing the Fermi level for electron, hole and minimum conductivity zones.

With V_G near V_{FB}, there are a few of either carrier type and the conductivity of graphene is minimized. However, there remains a thermal distribution of carriers and spatial fluctuations in energy of the Dirac point, so that the minimum current remains significant at $V_G=V_{FB}$ even when the FETs are cooled to very low temperatures. Another typical property of the transfer characteristics of graphene FETs is the asymmetry between electron and hole conduction. Given the symmetry between the conduction and valence bands of graphene, this asymmetry is attributed to a geometry-dependent combination of gate-voltage-dependent contact resistances and formation of p–n junctions between the channel and the source and drain regions for only $V_G<V_{FB}$ or only $V_G>V_{FB}$ for p-type or n-type source drain regions, respectively. As can be seen from the above description, the further V_G is from the flat-band voltage, the more metallic the graphene becomes and the easier it is to modulate the absolute if not relative charged density and, thus, differential conductivity with the increased quantum capacitance. This situation contrasts to that for a three-dimensional metal, of course, where the electric fields from gates can only penetrate the metals to less than a nanometer, resulting in negligible modulation of the total carrier density available for conduction. This behavior once again illustrates why graphene is such an interesting material both from basic sciences and applications perspective.

Before considering the I–V characteristics of GFETs we must take note of what governs the saturation current with respect to the drain voltage V_D. Although intrinsic elastic mean free path in graphene may be large, near a few hundred nanometers, most of the experimentally studied devices still operate in the diffusive transport regime. The possible mechanisms for current saturation in conventional MOSFETs in this regime are pinch-off and velocity saturation. However, as we have seen in the above discussion, pinch-off cannot take place in bulk graphene-based FETs. Therefore, in order to drive the device into saturation regime, the drain to-source electric field must be large enough to cause velocity saturation. However, in devices with poor contacts, significant voltage is dropped across the contacts, making it difficult to drive the devices into saturation. Consequently, we see that even though most experimental results report higher mobilities for graphene, they do not see true saturation characteristics. As the quality of graphene is increased to achieve higher mobility, it becomes even more necessary to improve the contact quality to observe true saturation characteristics.

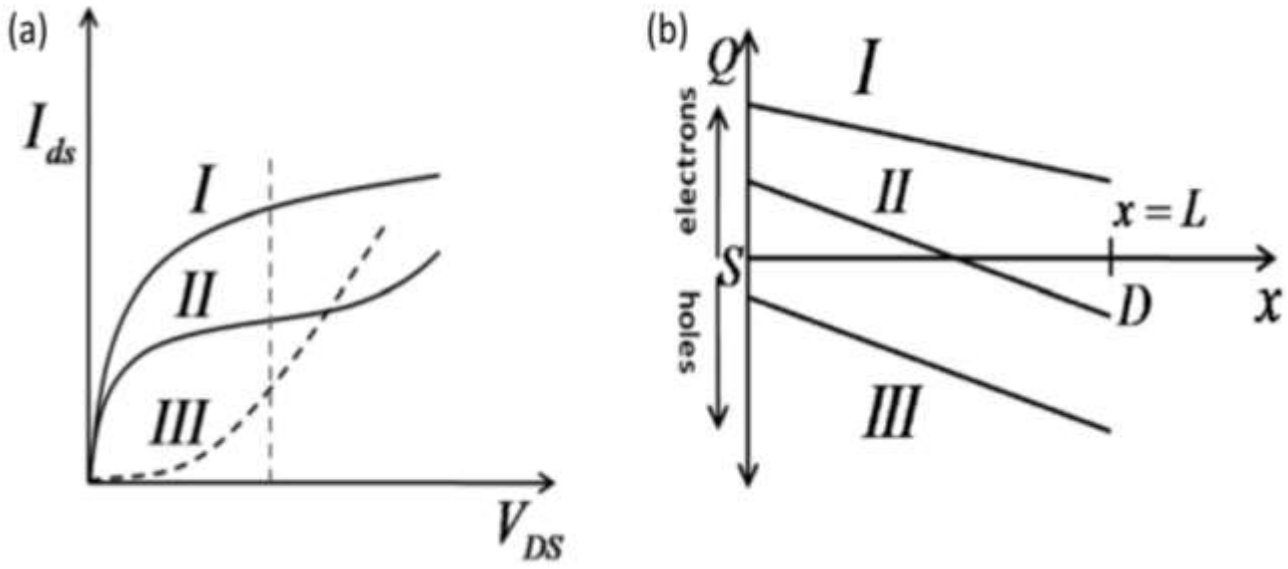


Figure 6.3 - (a) Schematic of qualitative IV characteristics for a graphene FET and **(b)** corresponding schematic plot of the total charge density in the channel as a function of distance from source (S) at approximately the indicated (vertical dashed line)V_{DS} in **(a)**. Curve I corresponds to V-$_{GS}$>V_{FB} and V D_{GS}>V_{DS}−V_{FB}, curve III corresponds to V_{GS}<V_{FB}, and curve II corresponds to V_{GS}>V_{FB} and V_{DS} ≈V_{GS} –V_{FB}

However, under certain gate voltages it is possible to see quasi-saturation behavior in the GFET even without velocity saturation. Typical characteristics are illustrated in figure 6.2 (a) for positive drain voltages, with cases I to III representing decreasing gate voltage. As illustrated in figure 6.2(b), in case I the channel is n-type everywhere and the current increases with increasing gate voltage as to be expected. However, the carrier concentration and, thus, conductivity decrease down the channel and the current increases sub-linearly with V_D. In case III, the channel is p-type everywhere and again the current increases with increasing gate voltage as to be expected. However, this time the carrier concentration and, thus, conductivity increase down the channel and the current increases super linearly with V_D. In case II, however, with sufficient V_D, the channel carrier type along the channel changes where the Fermi level crosses the Dirac point. The conductivity is large on to either side of this crossing, but the current is limited by the conductivity near this crossing point. Thus, under the

onset of this condition, the differential channel conductivity is substantially decreased. This condition is as close as the GFET gets to pinch-off. However, unlike for a pinch-off region in a conventional MOSFET, the length of the low conductivity region, e.g. where roughly speaking the Fermi level is within k_{BT} of the Dirac point in this case, actually decreases with increasing field and the down-channel conductivity continues to rise, so that the overall conductivity again begins to increase with increasing V_D and the current again increases super linearly V_D. Furthermore, of particular importance for shorter channel devices, band-to-band tunneling, which again has unity transmission probability for normal incidence, increases for off-normal incidence as well.

CHAPTER 7

MODELING OF GRAPHENE FET

In this chapter, we will be discussing the modeling of graphene based Field Effect Transistors (GFETs). The variation in the modeling comes with the variation of operation of GFETs. Only large-signal and small-signal models are mentioned in this chapter.

7.1 Large signal model

An exhaustive study of the drain–source current using the drift equation for GFET transistors can be found in **[51]**. The result of this paper shows that the drain–source current can be expressed as,

$$I_D = \mu W \frac{\int_0^{V_{DSi}} \left(|Q_{net}| + en_{puddle} \right) dV}{L + \mu \left| \int_0^{V_{DSi}} \frac{1}{v_{SAT}} dV \right|} \quad \text{…….. (1)}$$

where μ is the mobility, W is the transistor width, L is the transistor length, Q_{net} is the net mobile charge density per unit area, e is the elementary charge (1.6×10^{-19} As), $n_{puddle} = \Delta^2/\pi h^2 v_f^2$, and V_{DSi} is the internal drain–source voltage. The parameter Δ represents the special inhomogeneity of the electrostatic potential, h is the reduced Planck constant, and v_f is the Fermi velocity.

The whole model is very compact and perfectly suitable for building SPICE and Verilog-A models; and consequently, it is also suitable for circuit simulation purposes. While the model shows outstanding accuracy, it can be appreciated that it is still complicated to be used by analog circuit designers. The main problem is that it lacks a simple closed mathematical expression for the drain current like the one that is available for CMOS FET transistors (Shichman–Hodges model) **[52]** or like the collector current in bipolar transistors (Ebers–Moll model) **[53]**. A simple expression for the drain current is fundamental since the parameters for small-signal hybrid-π model and figures of merit are directly derived from this equation**[54]**.

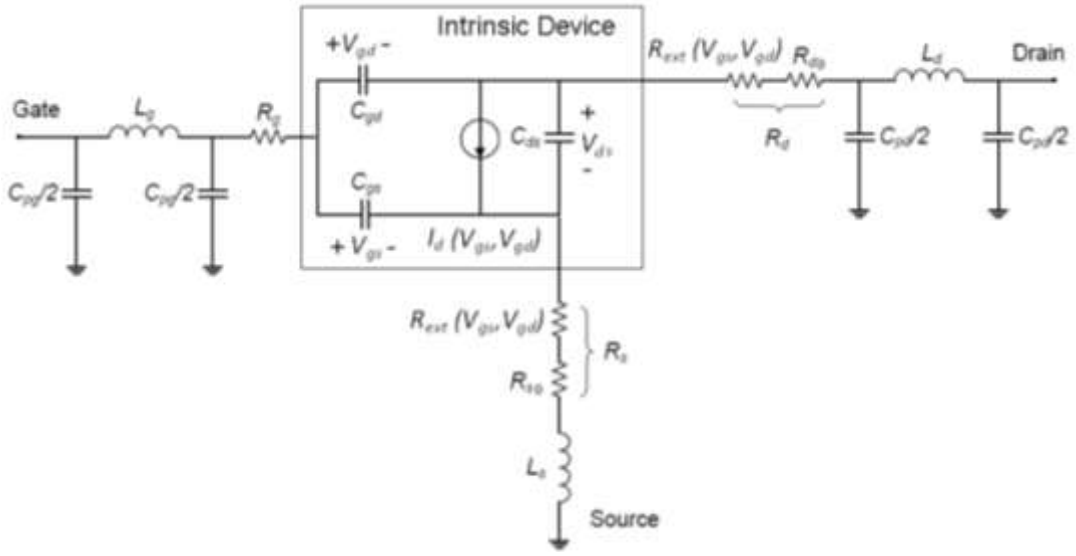


Figure 7.1 - Large signal model of a G-FET. C_{pg}, C_{pd}, L_g, L_d and L_s are pad parasitic capacitances and inductances. R_g is the gate resistances and, R_s and Rd are the source and drain resistances including contact and access resistances**[55]**.

7.2 Simplified large-signal model

The difficulty in finding a simple expression for the GFET drain current lies in the complexity of (1). Fortunately, the replacement of technology dependent parameters taken from the measured GFETs and physical constants unveils that there is a term that dominates and therefore (1) can be reduced to,

$$I_D \simeq \frac{\mu \mathrm{W} C_{\mathrm{TOP}} \left(V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2\right)}{\frac{L}{V_{\mathrm{DSi}}} + \frac{\mu}{\omega}\sqrt{\frac{\pi C_{\mathrm{TOP}}}{e}}\sqrt{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2}}$$

which is a closed analytical expression that relates the main technology parameters and biasing conditions.

One important observation that can be made from the simplified expressions is the impact of short-channel lengths on the GFET drain current. It has been experimentally shown that there is strong dependence of short lengths in the GFET transport characteristics **[56]**, **[57]**. For very short lengths and high electric fields, the current becomes independent of the channel length, something that has also been confirmed experimentally in [26]. Under these conditions, the drain current saturates, stops depending on μ, and takes a value of approximately

$$I_D \simeq \omega W \sqrt{\frac{C_{\mathrm{TOP}} \times e}{\pi}} \sqrt{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2} \qquad \textbf{[58]}$$

7.3 Small-signal model

7.3.1 Small-signal circuit of a typical FET device

The parameters that have an influence on the high-frequency performance of the transistor, in particular the Figure of Merit (FOM) cut-off frequency f_T and maximum oscillation frequency f_{max}, are easily recognizable in the small signal model of the FET transistor, which for graphene-based devices maintains the same topology and components than the original one for semiconductors.

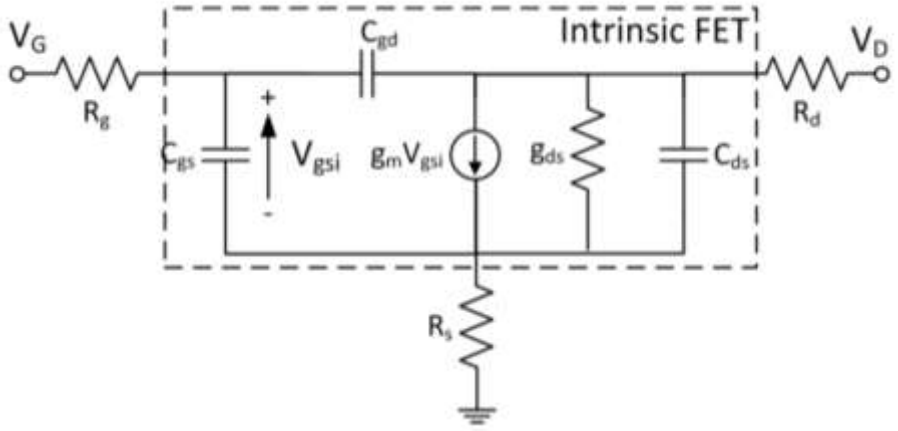


Figure 7.2 - The small signal circuit of a typical FET device, showing the intrinsic device and its access and gate resistance parasitics, along with capacitive coupling between electrodes**[59]**.

In Fig. 7.2 the encircled part of the circuit represents the intrinsic transistor, i.e. the ideal device without access parasitic impedances. Intrinsic values of FOM refer to the maximum theoretical performance that is obtained after de-embedding. The extrinsic values of the parameters may give the reader a more accurate idea of the actual performance and usefulness of a device.

The access resistance is composed by the transition between metal and graphene (the contact resistance RC and the contact capacitance CC) and the resistance of the ungated graphene between the source/drain electrode and the gate oxide/gate metal stack. The value of the contact resistance depends on many factors, including the quality and type of graphene, the metal stack, and the presence of lithographic residues. It can also depend on the length of the graphene strip that lies below the metal, if this is less than a few hundreds of nanometers**[59]**.

7.3.2 GFET small-signal model

While the large-signal model in (1) encloses the physics of the device in a single expression, it is still too complex to be used in quantitative circuit analyses of the behavior of amplifier configurations. These analyses are normally performed by taking advantage of linear system theory in which a simplified small-signal representation of the transistor biased in the operating point is used. The small-signal representation, also called hybrid-π model, is shown in Fig. 7.3. The parameters g_m, r_o, C_{gs},and C_{gd} can be obtained by linearization of the large-signal model. Naturally, the small-signal representation provides only limited information, which is valid for small excursions from the operating point.

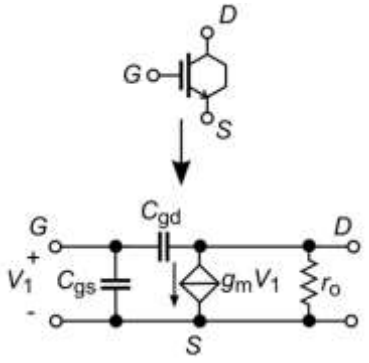


Figure 7.3 - GFET symbol and equivalent hybrid-π model for small-signal Analysis**[60]**.

A. Transconductance, g_m

The expression for the transconductance gain can be directly derived from (1).

$$g_m = \left.\frac{\delta I_D}{\delta V_{\mathrm{GSi}}}\right|_{V_{\mathrm{DSi}},\mathrm{const}}$$

$$g_m = \left(\frac{I_D}{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2}\right) \times \left(1 - \frac{1}{2}\frac{I_D}{W\omega}\sqrt{\frac{\pi}{e \times C_{\mathrm{TOP}}}}\frac{1}{\sqrt{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2}}\right) \quad \text{.... (2)}$$

Fig. 7.4 shows g_m values calculated using (2) and the complete model. It can be observed that (1) follows closely the complete model in particular for Veff > $V_{DSi}/2$. It is interesting to notice that gm drops substantially at large V_{GSi} biasing voltages, mainly due to the effect of V_{SAT}. Therefore, the best g_m performance is actually achieved at low V_{eff} voltages.

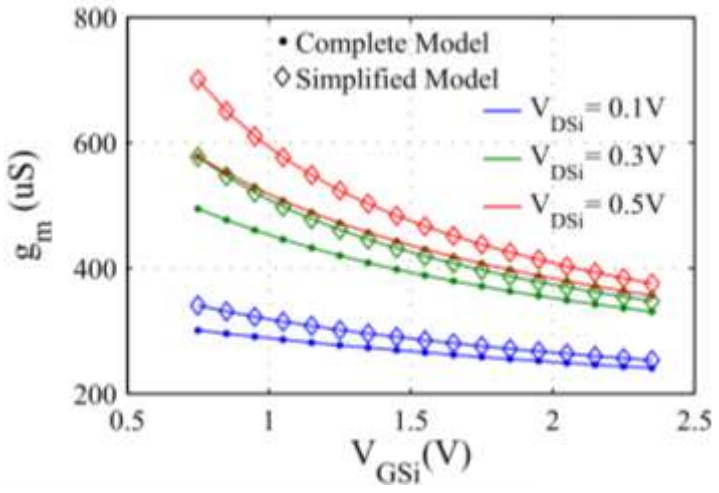


Figure 7.4 - Transconductance gm calculated using the complete and simplified model for the 440-nm length and 1-µm width GFET from **[61]**. $N_f \approx 0$, $V_{TH,0} \approx 0V$, $C_{TOP} = 3.6 \times 10^{-3}$ F/m^2, $\mu = 7000$ cm^2 V^{-1} s^{-1},and $h\omega = 56$ meV**[60]**.

B. Output Resistance, r_o

The output resistance can be calculated as $r_0 = 1/g_0$, where g_0 is the output conductance. An expression for g_o can also be directly derived from (1)

$$g_o = \left.\frac{\delta I_D}{\delta V_{\mathrm{DSi}}}\right|_{V_{\mathrm{GSi,const.}}}$$

$$g_o = \frac{I_D}{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2} \times \left[-\frac{1}{2} + \frac{I_D}{\mu \mathrm{W} C_{\mathrm{TOP}}} \left(\frac{L}{{V_{\mathrm{DSi}}}^2} + \frac{\frac{\mu}{\omega}\sqrt{\frac{\pi C_{\mathrm{TOP}}}{e}}}{4\sqrt{V_{\mathrm{eff}} - V_{\mathrm{DSi}}/2}} \right) \right] \quad \text{..... (3)}$$

One important characteristic of the GFET device is that under some biasing conditions, g_0 becomes negative **[62]**, **[63]**. A negative g_0 makes the device unstable, and in general, this region needs to be avoided in amplifier design. On the other hand, a negative g_0 is a very welcome asset when designing oscillators. The biasing conditions in which g_0 changes from positive to negative values can be found by making g_0=0 in (3) and solving for V_{DS}. The expression for this boundary condition is,

$$V_{\mathrm{DS,lim}} = \frac{-2L + \sqrt{4L\left(L + \frac{\mu}{\omega}\sqrt{\frac{\pi C_{\mathrm{TOP}}}{e}}{V_{\mathrm{eff}}}^{3/2}\right)}}{\frac{\mu}{\omega}\sqrt{\frac{\pi C_{\mathrm{TOP}}}{e}}\sqrt{V_{\mathrm{eff}}}} \quad \text{..... (4)}$$

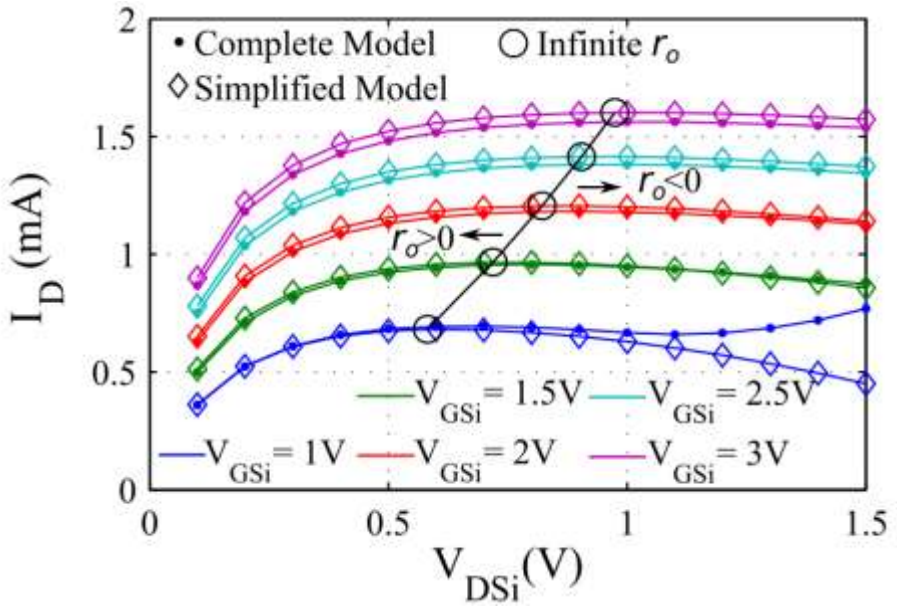


Figure 7.5 - Calculation of negative r_o biasing requirements for the 440-nm length and 1-µm width GFET from **[10]**. $N_f \approx 0$, $V_{TH,0} \approx 0V$, $C_{TOP} = 3.6 \times 10^{-3}$ F/m^2, µ=7000 cm^2 V^{-1} s^{-1}, and hω = 56 meV**[60]**.

Fig. 7.5 shows I_D versus V_{DS} plots for different V_{gs} voltages. In addition, the plot shows the points in which $g_o = 0$ ($r_o = \infty$), which were found using (4). It can be observed that (4) predicts very well the transition from positive to negative output resistance**[60]**.

CHAPTER 8

GRAPHENE BASED FIELD EFFECT TRANSISTOR APPLICATIONS

Graphene is a new but popular star in material research field, and especially of large potential for high frequency device and circuit applications, due to its ultra high mobility under low electric field and high saturation velocity under high electric field. By utilizing the ideal gate dielectric Y_2O_3 to the surface of graphene, high-performance GFET can be fabricated. GFET with frequency response up to hundreds of GHz was realized based on both mechanically exfoliated and epitaxial grown graphene, and the compatibility with traditional wafer-scale Si fabrication process flow was experimentally proved. Besides amplifiers with gain, GFET can be also used to build ambipolar devices and circuits such as frequency doublers, RF mixer, digital modulators and phase detectors. Furthermore, the wafer-scale integrated circuits based on graphene are realized, operating RF mixing up to 10 GHz frequency. In general, graphene is a very promising kind of material for future RF analog ambipolar electronics. With the basic unit of high frequency applications, i.e. mixer and amplifier, and process circuits based on graphene, an integrated RF system can be fabricated solely on a large-area single layer graphene, which is compatible with Si CMOS fabrication process and of higher performance. However, large efforts still needs to be made for the problem that have not been solved, such as decreasing the contact resistance between graphene and metal, developing a suitable gate selfalign profile for high frequency graphene devices, realizing controllable saturation property in GFET, and so on.**[64]**

There are many potential applications of Graphene Field Effect Transistors but as scientists have started to work on it recently so we found its application only in some circuits.In this chapter those circuits are discussed.

8.1 Ambipolar electronics based on graphene

Comparing to sacrificing mobility for band gap opening, directly taking advantage of the ambipolar property of grapheme for RF applications seems a better choice. Ambipolar electronics based on graphene has attracted lots of attention in the field of graphene application, such as frequency doublers, mixers, digital modulators, phase detectors, etc.The symmetric I_{DS}-V_{GS} relation around Dirac point plays an importance role in the applications.

$$I_{ds}=a_0+a_2(V_{gs}-V_{Dirac})^2+a_4(V_{GS}-V_{Dirac})^4+\cdots \quad (1)$$

For ambipolar applications, the test is always configured as shown in Figure 8.1, with the gate electrode as the input port, the output port (drain electrode) biased with V_{DD} via a load resistor RL, and source electrode grounded. Hence, the output voltage can be described as

$$V_{DS} = V_{DD} - I_{DS}R_L, \quad (2)$$

Where V_{DS}-V_{GS} relation shows similar shape with I_{DS}-V_{GS} relation but a negative sign.

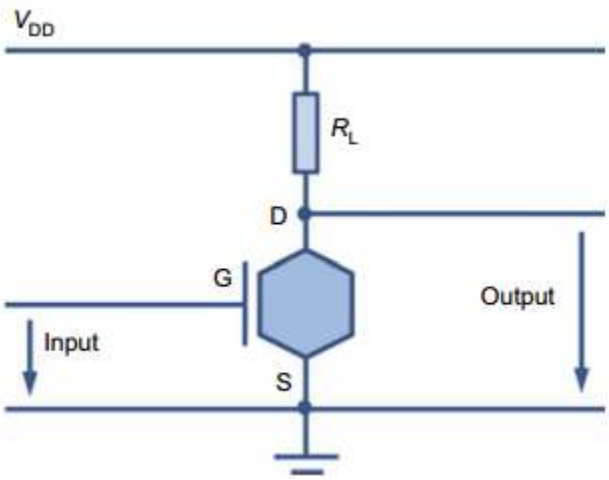


Figure 8.1 - Typical circuit configuration for ambipolar electronics based on GFET.

8.1.1

Frequency doublers

If I_{DS}-V_{GS} relation of GFET performs perfect parabolic property about Dirac point

$$I_{DS} = a_0 + a_2 (V_{GS} - V_{Dirac})^2, \quad (3)$$

And the input gate sinusoidal signal is biased at Dirac point with an amplitude of A and radian frequency of ω

$$V_{GS} = V_{Dirac} + A\sin \omega t. \quad (4)$$

From eqs. (2)–(4), we can deduce the output drain voltage as

$$V_{DS} = V_{DS,0} + 1/2\, a_2 R_L A^2 \cos 2\omega t, \quad (5)$$

Where $V_{DS,0} = V_{DD} - a_0 R_L - a^2 R_L A_2/2$.

Clearly, the output frequency is doubled purely via the simple GFET, and the deviation from the ideal parabolic relation will lead to more even-order harmonics, Such as quadruple and sextuple frequencies. Odd-order harmonics will also be introduced to the system once the *I*DS-*V*GS relation deviates to an asymmetric shape. Similarly, from the principle illustration in Figure 12(a), we can also easily Tell that an input single period ofsinusoidal wave will lead to double period at the output port. Wang et al. **[65]** reported ambipolar frequency doubler based on exfoliated graphene for the first time in 2009, which showed a frequency response up to 10 kHz and output second-order harmonic wave purity of more than 90%. A single transistor is enough for frequency doubling while filters or rectification units are not necessary. However, the signal gain of the back-gate setup is very low (less than 1/200) due to its small transconductance for typical back-gate GFETs. Afterwards, Y_2O_3 top-gate was introduced and utilized to graphene based frequency doubler as shown in Figure 8.2(b)–(d) **[66]**. Benefited by the high-efficiency gate oxide, the signal gain is increased by 10 times (as high as 1/20) compared to that of the back-gate geometry and the working frequency

was pushed to 200 kHz. The top-gate geometry also clearly improved the symmetric property of the transfer curve, which is needed in the frequency doubling operation. The operation frequency is limited by the testing system, including the substrate, pads, probes and cables, but the intrinsic frequency response of graphene can be very high. Besides, ambipolar frequency doublers based on wafer-scale CVD grown graphene are also realized, with frequency response up to 1.4 GHz, which demonstrated the great potential of graphene for RF applications **[67]**.

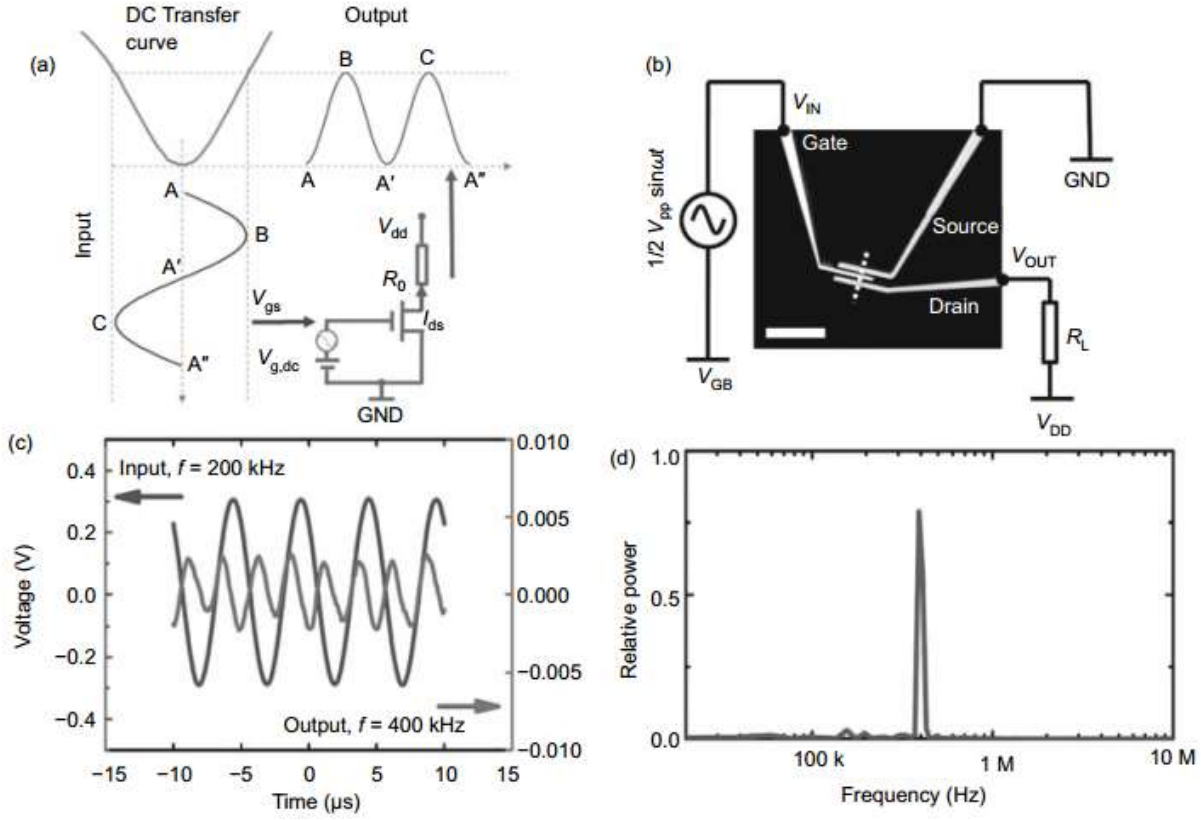


Figure 8.2 GFET based frequency doubler. **(a)** Schematic diagram showing the working principle of GFET based frequency doubler. **(b)** Optical microscope image depicts experimental configuration of the device. **(c)** Measured input and output waveform of the GFET based frequency doubler, with an input frequency of 200 kHz. **(d)** Power spectrum obtained via Fourier transforming the output signal in **(c)**

Besides, frequency doubler can be also realized based on small band-gap (SBG) CNT, which behaves the similar ambipolar transport property as graphene, as

shown in Figure 8.3(a) **[68]**. Comparing to graphene, SBG CNT exhibit extremely higher carrier mobility on SiO_2 substrate due to the suppressed substrate scattering, which is shown in Figure 8.3(b) **[69]**. Moreover, the easy-obtained saturation behavior of CNT FETs, which is usually hard to be realized in GFETs,is also one of the advantages for achieving a higher operation frequency and gain (more than 0.15), as shown in Figure 8.3(d),8.3(c). Also, the output of the frequency doubler is of high second-order harmonic purity, as shown in Figure 8.3(d).

8.1.2 RF mixers

In telecommunications, a mixer is a nonlinear device that receives two different frequencies at the input port and appears a mixture of several frequencies at the output, including both original input frequencies, the sum of the input frequen cies, the difference between the input frequencies, and other intermodulations **[70]**. If we apply two sinusoidal waves $A_1 \sin \omega_{1t}$ and $A_2 \sin \omega_{2t}$ to the input port, where A_1, A_2 are the amplitudes and ω_1, ω_2 are the radian frequencies of the two input signal, based on eq. (1) the output will appears no odd-order intermodulations, which can be usually detected in conventional unipolar mixers and affect the dynamic range for circuit operations. Deviation from the ideal symmetric property will introduce some odd-order intermodulations. While a RF signal and local oscillator (LO) signal with frequencies of f_{RF} and f_{LO} are applied to the input of an ambipolar mixer based on graphene, in the frequency spectrum of the output, the power at even-order frequencies is higher than the power at the odd-order frequencies, which is consistent with the prediction that the odd-order intermodulations are suppressed. The performance of the mixer can be enhanced by improving the symmetry of the transfer property **[71]**. Afterwards, an integrated circuit including ambipolar mixer and on-wafer inductors for DC coupling, is realized based on graphene epitaxial grown on SiC, and the mixer can work at frequency as high as 10 GHz, also with temperature stability (performance reduction less than 1 dB) between 300 and 400 K, which also revealed the wafer-scale application for graphene based mixer **[72]**.

8.1.3 Digital modulators

Since graphene can work as both frequency doublers and amplifiers (in-phase or anti-phase), and the working mode can be transformed between each other simply by changing the bias voltage of the input signal of the GFET, signal modulators such as phase shift keying (PSK) and frequency shift keying (FSK) can be realized based on ambipolar GFET.As shown in Figure 8.4(a), we define p-region with negative transconductance as Region I, the region around Dirac point as Region II, and n-region with positive transconductance as Region III, and along with eq. (2) the gain shows different sign with transconductance

$$A_{\mathrm{v}} \equiv \frac{\partial V_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} = -g_{\mathrm{m}} \frac{R_{\mathrm{out}} R_{\mathrm{L}}}{R_{\mathrm{out}} + R_{\mathrm{L}}},$$

Where R_{out} the output resistance of the FET. The gain in Region I is positive due to the negative transconductance and the device acts as an in-phase amplifier, while the gain in Region III is negative due to the positive transconductance and the device acts as an inverted amplifier. In Region II, the device transfers between n-region and p-region alternately, resulting in frequency doubling.

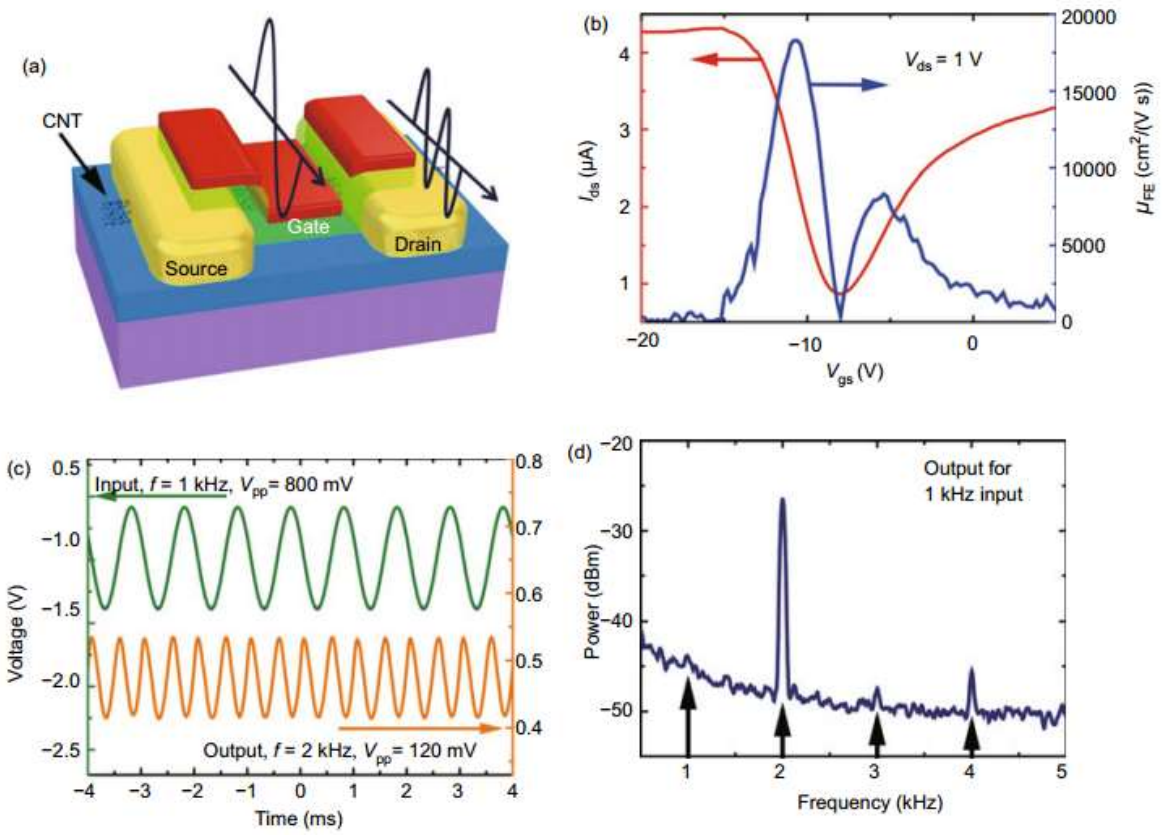


Figure 8.3: Frequency doubler based on SBG CNTs. (a) Schematic diagram illustrating the geometry of a CNT based ambipolar FET and its working principle as a frequency doubler. (b) Transfer characteristic for a long channel back-gate CNT FET (left scale) and corresponding field-effect mobility curve (right scale). (c) AC performance of a CNT based frequency doubler, with input and output waveform for an input 1 kHz sinusoidal wave. (d) Measured output signal spectrum for 1 kHz input. The four arrows indicate the frequencies of 1, 2, 3 and 4 kHz, respectively from left to right.

Based on the configuration shown in Figure 8.4(b), if the bias voltage alters between Region I and III and we denote Region I and III as binary “0” and “1” respectively, each alternation will introduce an inverting to the signal at the output and a transfer between “0” and “1” will be recognized.Hence, a binary phase shift keying (BPSK) is realized and this ambipolar GFET is proved to be used as a digital modulator before signal transmitted (Figure 8.4(c)). Similarly,the transfer between Region I/III and II will introduce a frequency alternation to the output signal. If we denote the fundamental and doubled frequency as binary “0” and “1” respectively, a binary frequency shift keying (BFSK) is realized based on the single transistor (Figure 8.4(d)).Yang et al. **[73]** successfully performed BFSK modulation based on the Kansas City standard (KCS) for audio cassette drives

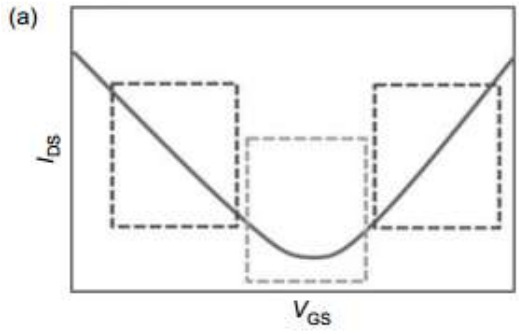
where fundamental frequency f = 1200 Hz and doubled frequency 2 f = 2400 Hz. The proposed single transistor digital modulator can greatly simplify the circuit design in telecommunication applications.

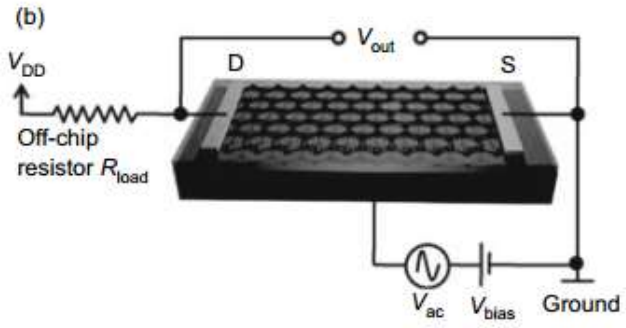
8.1.4 Multiplier phase detectors

If we applied a sinusoidal wave $A_1\sin(\omega t+\theta 1)$ and a square wave A_2 rect(ωt + θ2) to the input of the phase detector, the DC component of the output can be written as the product of the two input signal **[74].**

$$A_d = A_1 A_2 \frac{2}{\pi} \sin(\theta_1 - \theta_2) \simeq K_d \theta_e,$$

where K_d is the gain of the detector and θe is the phase difference in radians between the input signals. Hence, the relation between DC component and the phase difference can be utlized for phase detection. A multiplier is generally needed f this process, which complicates the circuit. While for GFET, a single transistor can fulfill the phase detection and a gain 0−7 mV/radian was reached, which can be further largely improved by reducing the series resistance, increasing the gate efficiency, and pushing the transistor to saturation region.





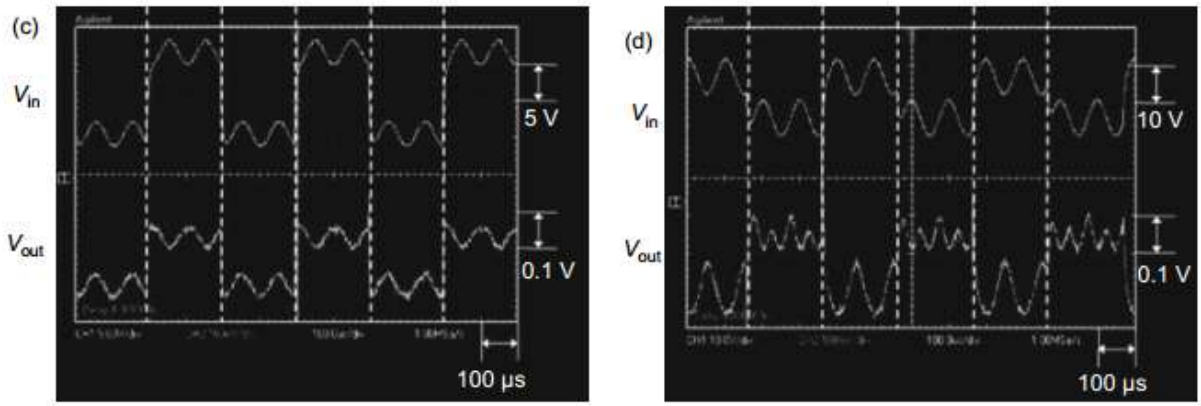


Figure 8.4: Digital modulators based on GFET. (a) Transfer curve of a typical GFET. (b) The schematic test configuration of the single transistor digital modulators. (c) The waveform for BPSK modulation. (d) The waveform for BFSK modulation. Reprinted of (b)–(d) with permission from Ref. **[73]**.

CHAPTER 9

CONCLUSION AND FUTURE WORK

This chapter is concluding the entire review thesis and propose/recommend some future enhancement work to bring this research work more interesting.

9.1 Conclusion

Graphene devices have grown by leaps and bounds over the past few years, and they are probably the best bet to eventually replace Silicon. Demonstrations like this are important because they show that wafer- scale production is possible, and the properties, while not ideal, are truly impressive, in that they're already beginning to push the limits of Si technology. Such Advantages of graphene transistors are, their high motilities for both electrons and holes; having ideal electrostatics that enable aggressive scaling; and straightforward integration with CMOS. But graphene has a low energy band gap, so grapheme continues to conduct a lot of electrons even in it's off state. If there be a billion of graphene transistors on a chip, a large amount of energy would be wasted. This can be improved if graphene ribbons can be made thinner, and by using techniques like doping and making grapheme inverters. It has become clear that graphene devices based on the conventional MOSFET principle suffer from some fundamental problems.

The purpose of this review paper is to gather the knowledge of graphene FET. It will not only help us to know its fabrication process, characterization, operation, circuit modelling but also its implementation in general circuits to improve its performance. All the basic principles are discussed in different chapters of this paper which can helpful for the scientists or engineers who want to start or work more on this topic.

As it is a very recent topic so we did not find its too many applications. But its use in a few circuits are shown in chapter 8.The main analysis is to study on the characteristics and potential application of GFET compared to the convention equivalent technology MOSFET. We found the performance of this new generation graphene FET is much better compared to the MOSFET.

9.2 Future work

Introducing more efficient and easier ways of fabricating a GFET is on progress. These fabrication processes can have an impact on the characteristics of GFETs. And also several GFET model can be presented in the meantime, so their operating procedure is also a concern to the curious students who are trying to work on GFETs. And there are all these potential applications which have not yet been initiated in commercial level. So, our future plan is to emphasis all these things together that will help to acquire a comprehensive idea of GFETs.

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