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Design and Simulation of a controller compensated Buck Converter

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By

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Declaration

This is to certify the project titled "Design and Simulation of a controller compensated Buck Converter" is supervised by Prof. Dr. Kazi Khairul Islam. This project work has not been submitted anywhere for a degree.

Approved by

Prof. Dr. Kazi Khairul Islam, Professor, Dept**. of Electrical and Electronic Engineering (EEE)**

And Project supervisor

Signature……

Date…….

Head of the Department,

Prof. Dr. Md. Shahid Ullah

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Date …….

Acknowledgement

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Abstract

DC-DC converters are used in every day electronic devices. Like transformers are to ac power, they can change the state of a dc power from high to low and vice versa. In this thesis, the buck converter is designed for specifications of our volition. A Matlab Simulink model of this converter is modeled in open loop, from which is seen the vulnerability of this converter to noise and perturbations in the input power source.

The demand for robust and ultimate controllers has attracted a multitude of researchers in the field of control systems engineering over the years. Ultimate controllers compensate system transfer functions in closed loop and maintain constant and stable output responses, immune to attenuations. The search for this ultimate controller has led to the introduction of controller concepts such as PID, Fuzzy, Sliding mode, Neural and many other control techniques. Here in this thesis we discuss the design and simulation of a PID controller for control of buck converter and the basic concepts of fuzzy control techniques.

Contents

Tools Used in this thesis.

Microsoft word 2010

Microsoft Visio 2007 and 2013

Snipping tool

Matlab/ Simulink 2013

CHAPTER 1

DC-DC CONVERTER TOPOLOGIES

1.0 Introduction

DC-DC converters are those devices that are employed to efficiently convert DC electrical power from one voltage level to another. These devices are indispensable because DC power unlike AC power cannot be stepped either up or down with a transformer. In this regard we can say that DC-DC converters are the transformers for DC power. DC-DC converters general use switching techniques in order to convert DC power from a voltage level to another. Applications for these devices can be seen where 5V DC on a personal computer motherboard has to be stepped down to 3V, 2V or less for CPU chips; where 1.5V from a single cell must be stepped up to 5V or more, to operate electronic circuitry; where 24V DC from a truck battery must be stepped down to 12V DC to operate a car radio, CB transceiver or mobile phone etc.

1.1 DC-DC Converter Classification

Many different types of DC-DC converters exit with each convenient for a particular application due to some peculiar behavior. For convenience, they are classified into different groups such as linear and non-linear, isolated and non-isolated, multiple switched converters etc. Another important distinction is between converters which offer full dielectric isolation between their input and output circuits, and those which don't. Needless to say this can be very important for some applications, although it may not be important in many others [i]. In this thesis we are only going to consider classification into isolated and non-isolated DC-DC converters.

1.1.1 Non-Isolated DC-DC Converters

Non-isolated DC-DC converters usually make use of inductors and there is no dielectric separation between the input and the output. They are mostly used when the voltages need to be stepped with lower ratios (e.g. 24/12, 12/5 etc.) just as is typical in most computer devices.

Five types of converters are typical in this category of converter classification. They are the buck, boost, buck-boost, Cuk and the charged-pump converters. We are going to make a subtle description of these converters in the following sections.

1.1.1.1 Buck Converter

In this thesis we have considered only Buck converter as our converter of focus, therefore we shall only detail discussions of this converter alone. A brief discussion of the other converters will be made in the next section.

Buck converter is a step down type of DC-DC converter that employs two switches, a capacitor, an inductor, in order to affect step down of DC voltage from a higher level to a lower. Buck converter is the most widely used DC-DC converter topology in power management and microprocessor voltage regulator applications. A control circuit (often a single IC) monitors the output voltage, and maintains it at the desired level by switching Q1 on and off at a fixed rate (the converter's operating frequency), but with a varying duty cycle (the proportion of each switching period that the switch is turned ON) [i].

In light of the switches used, we can classify Buck converter into synchronous and asynchronous buck converters. Both converters operate in the same manner only that the synchronous Buck converter is more efficient than the asynchronous Buck. These two are shown in Figure 1and Figure 2 below.

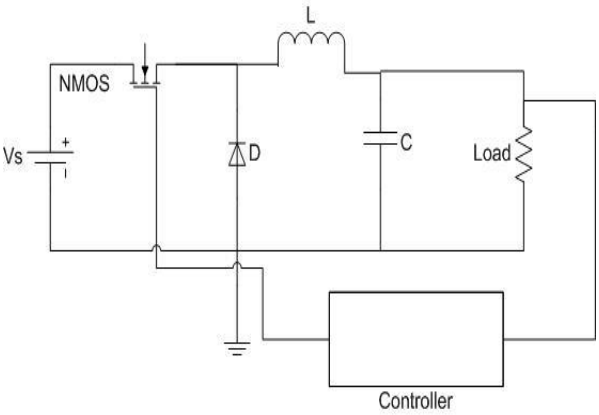

Figure 11: Asynchronous Buck Converter

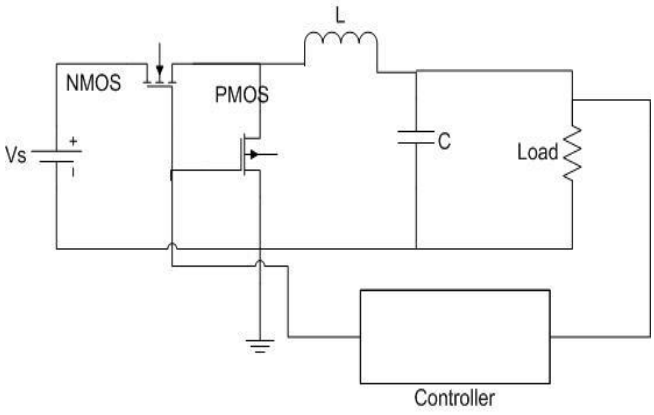

Figure 12: Synchronous Buck Converter

Synchronous and asynchronous buck converters both have similar structures differing by the PMOS that replaces the diode of asynchronous buck in the synchronous buck. The same control pulse width modulator (PWM) is applied to the gates of the enhancement mode (normally OFF) NMOS and the depletion mode (normally ON) PMOS, therefore when one MOSFET is on, the other one is automatically off and vice versa. The better efficiency of the synchronous buck is a consequence of the forward-biased voltage drop of the diode being greater than that of the PMOS. The efficiency of the asynchronous buck

converter can be alleviated by using the Schottky diode whose forward-biased voltage drop is in the range of 0.5V, lower compared to a normal PN junction diode.

The transfer function of a buck, equation 11 is directly proportional to the duty cycle, σ

$$\frac{V_o}{V_s} = \sigma . \tag{11}$$

This means that with the input voltage fixed, any change in duty cycle will directly result in a relative change in the output.

1.1.1.2 Another Buck Converter; the Switched- inductor Buck Converter

In order to combat the need for the extreme duty cycles, higher order topologies have been utilized. Multistage buck converter circuits are capable of having more median duty cycles. The quadratic buck circuit, for example, has the transfer function

$$\frac{V_s}{V_s} = \frac{\sigma}{\sigma^2} . \tag{12}$$

However, the losses caused by the increase in parasitic resistances due to the increase in components, counteracts the increase in efficiency gained by having a more median duty cycle. In order to compensate for the need of a more median duty cycle and the parasitic losses, the switched inductor topology; figure 3 is examined. The switched inductor topology has the transfer function

$$\frac{V_o}{V_s} = \frac{\sigma}{2-\sigma} . \tag{13}$$

The switched-inductor topology utilizes the same number of components as the traditional quadratic circuit but has less current flow through the inductor inductors and switches within the circuit. The decrease in the current flow through these components leads to less losses due to parasitic resistances. In addition, the size of the inductor is reduced because less energy storage is required [ii].

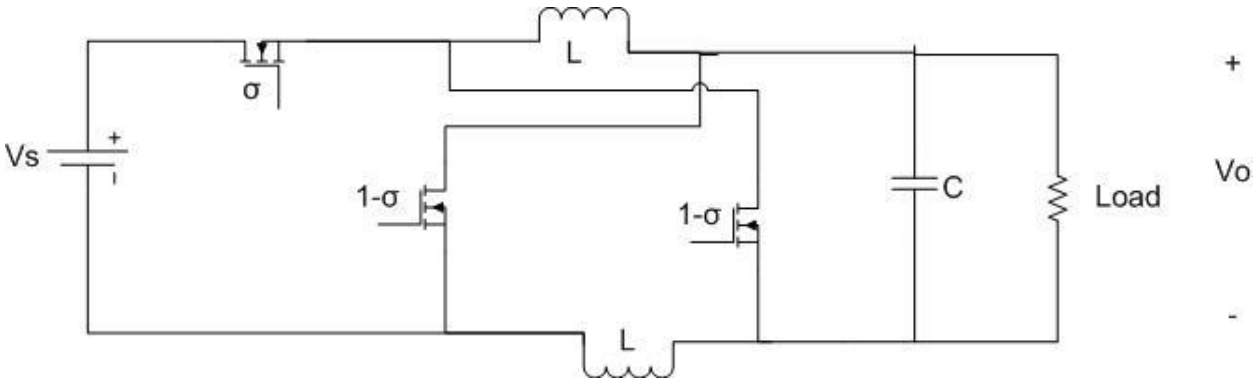

Figure 13: Switched-Inductor Buck Converter

The normal (classical) buck converter is capable of reliable operation between duty cycles of 0.1 and 0.9. Outside these extremes, the operation becomes unreliable since heavy losses due to switching decrease the efficiency of the converter. Switched-inductor buck converters can operate efficiently within these duty-cycle extremes (i.e. below 0.1 and above 0.9). Therefore it would be wise to employ the use of switched-inductor buck converters when applications demand high or very low duty cycles and to use the classical buck converter otherwise.

1.1.1.3 Boost, Buck-Boost, Cuk and Charged pump Converters

The basic boost converter is no more complicated than the buck converter, but has the components arranged differently (Figure 1.4) in order to step up the voltage. When Q is switched on, current flows from the input source through L and Q, and energy is stored in the inductor's magnetic field. There is no current through D, and the load current is supplied by the charge in C. Then when Q is turned off, L opposes any drop in current by immediately reversing its EMF so that the inductor voltage adds to (i.e., boosts) the source voltage, and current due to this boosted voltage now flows from the source through L, D and the load, recharging C as well. The output voltage is therefore higher than the input voltage, and it turns out that the voltage step-up ratio is equal to:

$$\frac{V_o}{V_s} = \frac{1}{1-\sigma}, \tag{14}$$

where 1-σ is actually the proportion of the switching cycle that Q is off, rather than on. [i] So the step-up ratio is also equal to:

$$\frac{V_o}{V_s} = \frac{\mathrm{T}}{T_{OFF}}. \tag{15}$$

The buck-boost converter (figure 1.5) unlike buck or boost can step voltage either up or down depending on the value of the duty cycle.

Here when MOSFET Q is turned on, inductor L is again connected directly across the source voltage and current flows through it, storing energy in the magnetic field. No current can flow through D to the load, because this time the diode is connected so that its reverse biased. Capacitor C must supply the load current in this T_{ON} phase. But when Q is turned off, L is disconnected from the source. Needless to say L again opposes any tendency for the current to drop, and instantly reverses it's EMF. This generates a voltage which forward biases D, and current flows into the load and to recharge C. With this configuration the ratio between the output and input voltages turns out to be:

$$\frac{V_o}{V_s} = -\frac{\sigma}{1-\sigma} \tag{16}$$

which again equates to:

$$\frac{V_o}{V_s} = -\frac{T_{ON}}{T_{OFF}}. \quad (17)$$

So the buck-boost converter steps the voltage down when the duty cycle is less than 50% (i.e., $T_{ON} < T_{OFF}$), and steps it up when the duty cycle is greater than 50% ($T_{ON} > T_{OFF}$). But note that the output voltage is always reversed in polarity with respect to the input so the buck-boost converter is also a voltage inverter. When the duty cycle is exactly 50%, for example, V_{out} is essentially the same as V_{in} except with the opposite polarity [i].

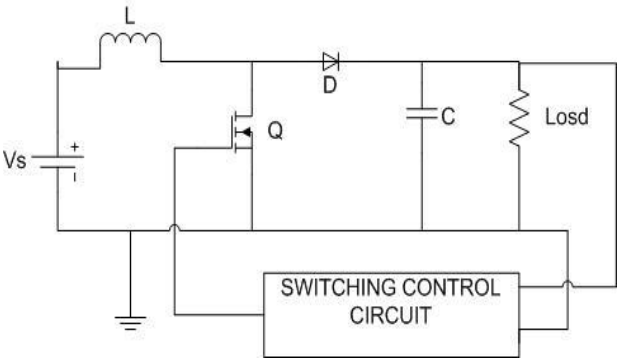

Figure 14: Basic Boost converter structure

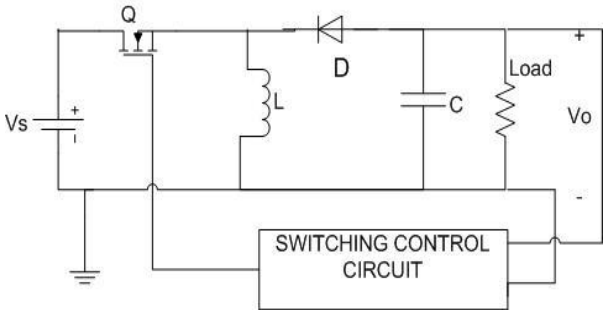

Figure 15: Buck-Boost Converter

The Cuk (Figure 16) converter, named after its inventor [iii], also known as the ultimate converter operates in a similar manner as the buck-boost converter. The circuit configuration is in some ways like a combination of the buck and boost converters, although like the buck-boost circuit it delivers an inverted output. It provides an output that is greater than or less than the input depending on σ, but the output is of opposite polarity to the input. Its transfer function is same as that of the buck-boost converter.

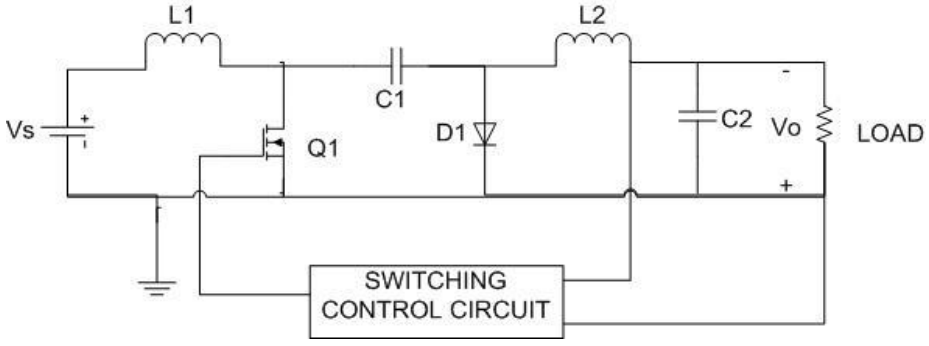

Figure 16: Cuk Converter

The basic circuit for a voltage doubling charge-pump converter is shown in Figure 17, and as you can see, it mainly uses four MOSFET switches and a capacitor C1 usually called the

charge bucket capacitor. Operation is fairly simple. First Q1 and Q4 are turned on, connecting C1 across the input source and allowing it to charge to V_{in}. Then these switches are turned off, and Q2 and Q3 are turned on instead. C1 is now connected in series with the input voltage source, across output reservoir capacitor C2. As a result some of the charge in C1 is transferred to C2, which charges to twice the input voltage. This cycle is repeated at a fairly high frequency, with C2 providing the load current during the part of the cycle when Q2 and Q3 are turned off. As you can see all of the energy supplied to the load in this type of converter flows through C1, and as ripple current. So again this capacitor needs to have a relatively high value, have low ESR (to minimize losses) and be able to cope with a heavy ripple current. A slightly different circuit configuration from that shown in Figure 17 can be used to deliver an inverted voltage of the same value as V_{in}, instead of a doubled voltage. This type of converter finds use in generating a negative supply rail for electronic circuits running from a single battery.

On the whole, though, the fact that charge-pump converters rely for their operation on charge stored in a capacitor tends to limit them to relatively low current applications. However for this type of operation they are often cheaper and more compact than inductor-type converters [i].

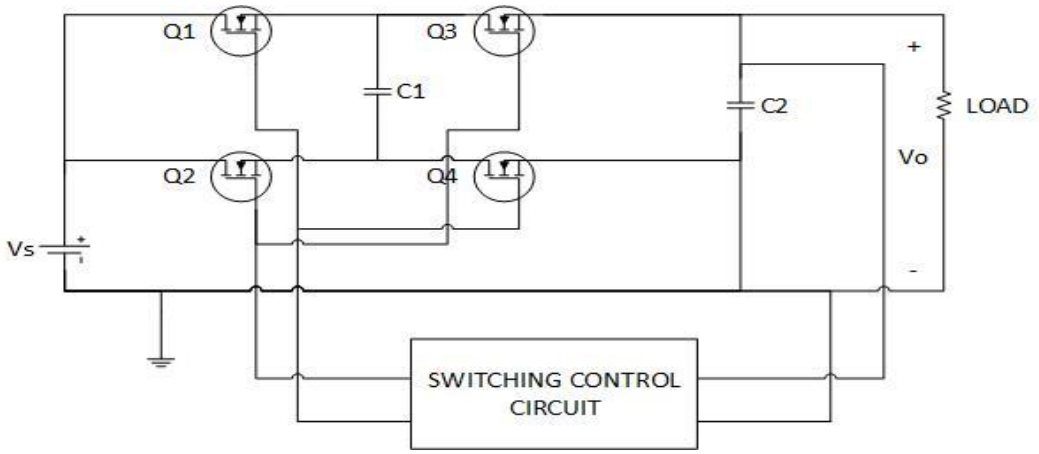

Figure 17: Charged pump converter

112 Isolated DC-DC Converters

Some electronic devices, especially medical electronic devices call for extra safety requirements. These safety requirements are provided by the use of isolated DC-DC converters. Four basic types of isolated converters are typical, and they are; flyback converter (Figure 18), the forward converter (Figure 19), isolated boost (Figure 110) and isolated Cuk converter (Figure 111).

1.1.2.1 Flyback Converter

The basic circuit for a flyback type converter is shown in Figure 1.8. In many ways it operates like the buck-boost converter of Figure 1.8, but using a transformer to store the energy instead of a single inductor.

When MOSFET Q1 is switched on, current flows from the source through primary winding L1 and energy is stored in the transformer's magnetic field. Then when Q1 is turned off, the transformer tries to maintain the current flow through L1 by suddenly reversing the voltage across it generating a flyback pulse of back-EMF.

Q1 is chosen to have a very high breakdown voltage, though, so current simply can't be maintained in the primary circuit. But because of transformer action an even higher flyback pulse is induced in the secondary winding L2. And here diode D1 is able to conduct during the pulse, delivering current to the load and recharging filter capacitor C1 (which provides load current between pulses). So as you can see, the flyback converter again has two distinct phases in its switching cycle. During the first phase Q1 conducts and energy is stored in the transformer core via the primary winding L1. Then in the second phase when Q1 is turned off, the stored energy is transferred into the load and C1 via secondary winding L2.

The ratio between output and input voltage of a flyback converter is not simply a matter of the turn ratio between L2 and L1, because the back-EMF voltage in both windings is determined by the amount of energy stored in the magnetic field, and hence depends on the winding inductance, the length of time that Q1 is turned on, etc. However the ratio between L2 and L1 certainly plays an important role, and most flyback converters have a fairly high turn ratio to allow a high voltage step-up ratio.

Because of the way the flyback converter works, the magnetic flux in its transformer core never reverses in polarity. As a result the core needs to be fairly large for a given power level, to avoid magnetic saturation. Because of this flyback converters tend to be used for relatively low power applications like generating high voltages for insulation testers, Geiger counter tubes, cathode ray tubes and similar devices drawing relatively low current.

Although it's not shown in Fig.6, a third small winding can be added to the flyback transformer to allow sensing of the flyback pulse amplitude (which is reasonably close to the output voltage V_{out}). This voltage can be then fed back to the MOSFET switching control circuit, to allow it to automatically adjust the switching to regulate the output voltage [i].

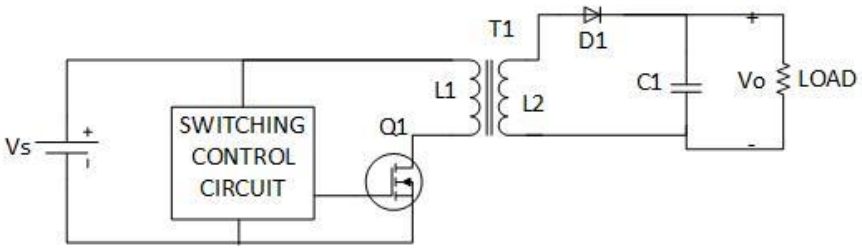

Figure 18: Flyback Converter with high voltage step up factor

1.1.2.2 *Forward Converter*

The most common type of forward converter is the push-pull type (Figure 19). The forward converter uses the transformer in a more traditional manner, to transfer the energy directly between input and output in the one step.

As is shown in Figure 19 there are two switching MOSFETs, Q1 and Q2, connected to either end of a centre-tapped primary winding on the transformer. The positive side of the input voltage source is connected to the centre tap [i].

In operation, the switching control circuit never turns Q1 and Q2 on at the same time; they're turned on alternately. And since their sources are connected back to the negative side of the input voltage, this means that the input voltage is first connected across one half of the primary winding, and then across the other. So current flows first in L1, and then in L2 [i]

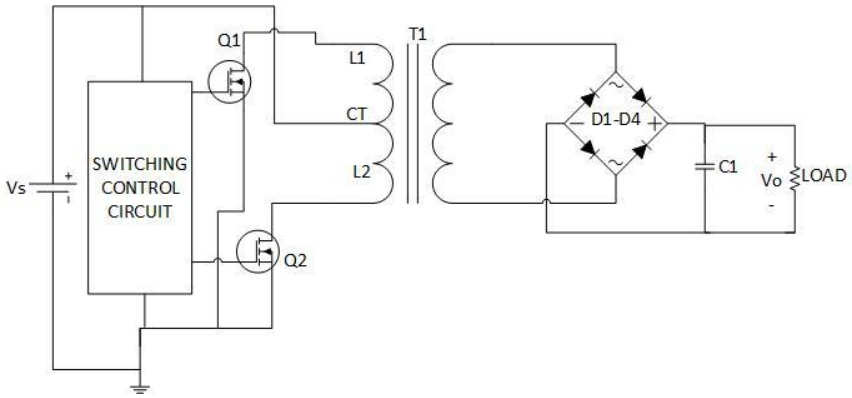

Figure 19: Forward Converter

The forward converter is basically just away of being able to use a transformer for DC, by converting the DC energy into AC so the transformer can handle it. After being transformed the AC is then rectified back into DC [i].

One important application for forward converters is in car hifi amplifiers, where they're used to step up the relatively low battery voltage to higher voltage supply rails, to allow

the amplifiers to develop higher power output. Another common use for the forward DC-DC converter is as the heart of many modern multi-voltage 'switch mode power supplies, as found in computers, TV sets and many other types of electronic equipment. In these cases the incoming AC mains voltage is generally rectified straight away to produce 340V DC (in the case of 240V mains voltage), which is then used to drive the forward converter [i].

1.1.2.3 Isolated Boost Converter

The isolated boost converter (Figure 1.10) is very much similar to the non-isolated type. In this converter, the inductor of the boost converter is replaced by the core of a transformer. Thus energy is stored in the transformer core. If we consider the transformer to be like an inductor, then we can be safe to say that the isolated boost converter operates in the same manner as the non-isolated boost converter.

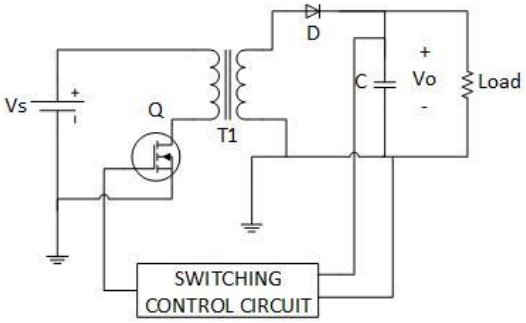

Figure 1.10: Isolated Boost converter

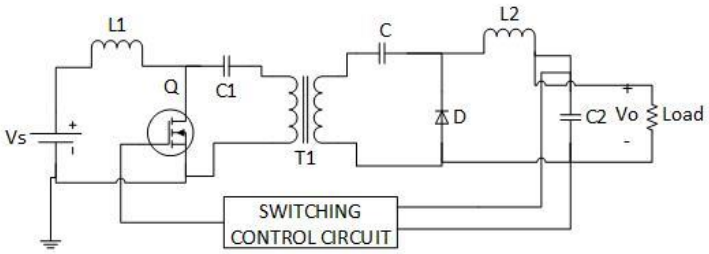

Figure 1.11: Isolated Cuk Converter

1.1.2.4 Isolated Cuk Converter

Figure 1.11, shows a basic structure of an isolated Cuk converter which has a rather more complicated structure compared to the non-isolated Cuk converter. It has two inductors and three capacitors. It performs the same task of both step up and step down of DC voltage, as the non-isolated Cuk, but with more safety and higher ratios.

1.2 DC-DC Converter Applications

DC-DC converters have seen a wide range of applications over the years in many electronic devices. Some examples of these applications are delineated in the following subsections.

1.2.1 Long Distance Supply Lines

When the supply is transmitted via a cable, there are several reasons why using an isolated DC-DC converter is a good design practice. The noise pick-up and EMC susceptibility of a cable is high compared to a pcb track. By isolating the cable via a DC-DC converter at either end, any cable pick-up will appear as common mode noise and should be self-cancelling at the converters.

Another reason is to reduce the cable loss by using a high voltage, low current power transfer through the cable and reconverting at the terminating circuit. This will also reduce noise and EMC susceptibility, since the noise voltage required to affect the rail is also raised.

For example, compare a system having a 5V supply and requiring a 5V, 500mW output ata remote circuit. Assume the connecting cable has a 100 Ohm resistance. Using an RN-0505 to convert the power at either end of the cable, with a 100mA current, the cable will lose 1W (I^2R) of power.

The RO/RN would not be suitable, since this is its total power delivery; hence there is no power available for the terminating circuit. Using an RB-0512D to generate 24V and a RA-2405D to regenerate 5V, only a 21mA supply is required through the cable, a cable loss of 44mW.

12.2 LCD Display Bias

An LCD display typically requires a positive or negative 24V supply to bias the crystal. The RO-0524S converter was designed specifically for this application. Having an isolated OV output, this device can be configured as a +24V supply by connecting this to the GND input, or a –24V supply by connecting the +Vo output to GND.

12.3 EIA-232 Interface

In a mains powered PC often several supply rails are available to power an RS232 interface. However, battery operated PC's or remote equipment having an RS232 interface added later, or as an option, may not have the supply rails to power an RS232 inter face. Using an RB-0512S is a simple single chip solution, allowing a fully EIA-232 compatible interface to be implemented from a single 5V supply rail, and only 2 additional components.

12.4 3V/5V Logic Mixed Supply Rails

There has been a lot of attention given to new l.C.'s and logic functions operating at what is rapidly emerging as the standard supply level for notebook and palmtop computers. The 3.3V supply is also gaining rapid acceptance as the defacto standard for personal telecommunications, however, not all circuit functions required are currently available in a 3.3V powered IC. The system designer therefore has previously had only two options available; use standard 5V logic or wait until the required parts are available in a 3V form, neither being entirely satisfactory and the latter possibly resulting in lost market share.

There is now another option, mixed logic functions running from separate supply rails. A single 3.3V line can be combined with a range of DC-DC converters, to generate voltage levels to run virtually any standard logic or interface IC. A typical example might be an

RS232 interface circuit in a laptop PC using a 3.3V interface chip, which accepts 3.3V logic signals but requires a 5V supply. Recom has another variation on this theme and has developed two 5V to 3.3V step down DC-DC converters (RL-053.3 and R0-053.3). These have been designed to allow existing systems to start incorporating available 3.3V l.C.'s without having to redesign their power supply.

This is particularly important when trying to reduce the overall power demand of a system, but not having available all of the functions at the 3.3V supply.

The main application for this range of devices are system designers, who want to provide some functionality that requires a higher voltage than is available from the supply rail, or for a single localized function. Using a fully isolated supply is particularly useful in interface functions and systems maintaining separate analogue and digital ground lines.

12.5 Isolated Data Acquisition System

Any active system requiring isolation will need a DC-DC converter to provide the power transfer for the isolated circuit. In a data acquisition circuit there is also the need for low noise on the supply line; hence good filtering is required. By using DC-DC converters, a very high isolation barrier can be provided. Converters are employed to provide the power isolation and data isolation [iv].

CHAPTER 2

DESIGN OF BUCK CONVERTER

2.0 Introduction

One of the most popular converters for the consumer electronics industry is the DC-DC step−down converter, also known as the buck converter. The synchronous buck converter is used to step a voltage down from a higher level to a lower level. With industry moving to higher performance platforms, efficiency of the power converter is critical. The design of the power converter must be optimized to maximize performance and to meet customer requirements. Because of this, it is important to understand the fundamentals of the synchronous buck converter and how to appropriately select the circuit components.

Despite their widespread use, buck-converter designs can pose challenges to both novice and intermediate power supply designers, because almost all of the rules of thumb and some of the calculations governing their design are hard to find. And though some of the calculations are readily available in IC data sheets, even these calculations are occasionally reprinted with errors. In this article, all of the design information required to design a buck converter is conveniently collected in one place.

Buck-converter manufacturers often specify a typical application circuit to help engineers quickly design a working prototype, which in turn often specifies component values and part numbers. What they rarely provide is a detailed description of how the components are selected. Suppose a customer uses the exact circuit provided. When a critical component becomes obsolete or a cheaper substitute is needed, the customer is usually without a method for selecting an equivalent component [v].

In this thesis we shall discuss a step-down regulator topology; one with a fixed switching frequency, pulse width modulation (PWM) and operation in the continuous current mode (CCM). The principles discussed can be applied to other topologies, but the equations do not apply directly to other topologies. To highlight the intricacies of step-down converter design, we present an example that includes a detailed analysis for calculating the various component values.

Four design parameters are required: input-voltage range, regulated output voltage, maximum output current and the converter's switching frequency. In Figure 2.1; which is a

similitude of Figure 1.2, these parameters are listed, along with the circuit illustration and basic components required for a synchronous buck converter.

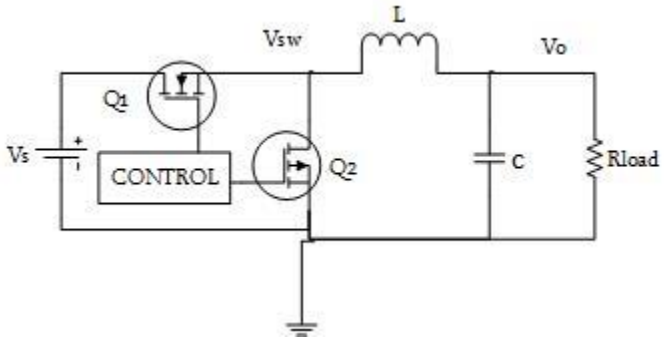

Figure 2.1: Synchronous Buck Converter

2.1 Synchronous Buck Converter Basics

The synchronous buck converter is straightforward in concept, and is used heavily in consumer electronics. A synchronous buck converter produces a regulated voltage that is lower than its input voltage, and can deliver high currents while minimizing power loss. As shown in Figure 2.1, the synchronous buck converter is comprised of two power MOSFETs, an output inductor and an output capacitor. This specific buck topology derives its name from the control method of the two power MOSFETs; the on/off control is synchronized in order to provide a regulated output voltage and to prevent the MOSFETs from turning on at the same time.

Q1, the high side MOSFET, is connected directly to the input voltage of the circuit. When Q1 turns on, current is supplied to the load through the high side MOSFET. During this time, Q2 is off and the current through the inductor increases, charging the LC filter. When Q1 turns off, Q2 turns on and current is supplied to the load through the low side MOSFET. During this time, the current through the inductor decreases, discharging the LC filter. The low side MOSFET provides an additional function when both MOSFETs are off. It clamps the switch node voltage via the body diode to prevent V_{SW} from going too far negative when the high side transistor first turns off.

Figure 2.2 shows the basic waveforms for the synchronous buck converter in continuous conduction mode. The total change in inductor current is known as the peak−to−peak inductor current, ΔI_L. The switch node voltage is smoothed out by the LC output stage in order to produce a regulated DC voltage at the output. The MOSFETs are controlled synchronously to prevent shoot−through. Shoot−through occurs when the high side and low side MOSFET are both on at the same time, providing a direct short to ground.

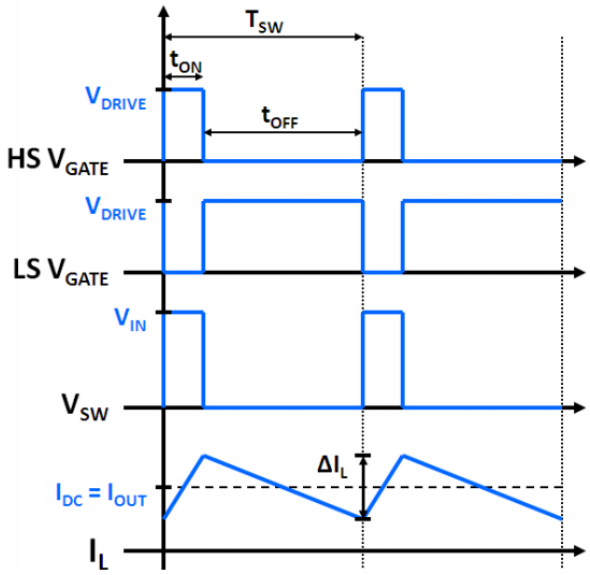

Figure 2.2: Waveforms of a Synchronous Buck Converter

The high side MOSFET on−time determines the duty cycle of the circuit, and is defined in Eq. (2.1).

$$\sigma = \frac{T_{ON}}{T_{ON}+T_{OFF}} \approx \frac{V_{OUT}}{V_{IN}} \qquad (2.1)$$

If the duty cycle, σ, is equal to 1 then the high side MOSFET is on 100% of the time and the output voltage equals the input voltage. A duty cycle of 0.1 means that the high side MOSFET is ON 10% of the time, producing an output voltage that is approximately 10% of the input voltage [vi].

2.2 Buck Converter Power Losses

The buck converter power losses are influenced by multiple factors, including the power MOSFETs, output stage, controller / driver, feedback loop, and layout of the converter itself. The duty cycle is less than 0.5 for most buck converter designs, with a standard duty cycle of 0.1 to 0.2 in the computing and server market. Design platforms are moving to higher switching frequencies, providing the ability to reduce converter size and form factors. At the same time, converters must deliver greater performance and have higher efficiency. The output stage performance greatly impacts the overall performance of the buck converter. For this reason, it is important to optimize the inductor and capacitor selection for the specific application. The rest of this application note focuses on the output stage design [vi].

2.3 Choosing the Components of a Synchronous Buck Converter

It is imperative in the design of a buck converter to choose the right components. Wrong components will result in undesired responses. These components are selected in relation to some predefined parameters such as the duty cycle, switching frequency, inductor ripple current etc. Volition techniques for various components are discussed in the subsequent subsections. In this thesis we design for the following specifications.

Parameter	Value
Input Voltage, V_s	12V
Output Voltage, V_o	5V
Duty Cycle, σ	0.417
Switching Frequency, f	400KHz
Load Current, I_{Load}	2A
Ripple Current, I_{Ripple}	$0.3I_{Load}$
Ouput ripple Voltage, V_{Ripple}	50mV

Table 2.1: Buck Converter Design Specification Table.

2.3.1 Inductor Selection

Calculating the inductor value is most critical in designing a step-down switching converter. First, assume the converter is in CCM, which is usually the case. CCM implies that the inductor does not fully discharge during the switch-off time.

The voltage across the inductor ***L*** is, in general given by [vii],

$$e_L = L\frac{di}{dt}. \quad (2.2)$$

If we assume the inductor current rises linearly from I_1 to I_2 during a time period t_1, then,

$$Vs - Vo = L\frac{I_2 - I_1}{t1} = L\frac{\Delta I}{t_1}. \quad (2.3)$$

This in terms of t_1 is written as

$$t_1 = \frac{\Delta IL}{V_s - V_o} \quad (2.4)$$

Assuming also that the inductor current falls linearly from I_2 to I_1 within time t_2, we get

$$-Vo = L\frac{\Delta I}{t_2} \quad (2.5)$$

Or

$$t_2 = \frac{\Delta IL}{V_o} \quad (2.6)$$

Where $\Delta I = I_2 - I_1$ is the peak-to-peak ripple current of the inductor L. Now, equating the values of ΔI in Eqs. (2.3) and (2.5), we get

$$\Delta I = \frac{(V_s - V_o)t_1}{L} = \frac{V_o t_2}{L} \quad (2.7)$$

Substituting $t_1 = \sigma T$ and $t_2 = (1 - \sigma)T$ gives the output voltage, Vo as

$$Vo = V_s \frac{t_1}{T} = \sigma V_s \quad (2.8)$$

Where $T = t_1 + t_2$, the switching period, can be expressed as

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s - V_o} + \frac{\Delta IL}{V_o} = \frac{\Delta ILV_s}{V_o(V_s - V_o)} \quad (2.9)$$

From which the inductance, L, can be given by

$$L = \frac{V_o(V_s - V_o)}{\Delta I f V_s} = \frac{V_s \sigma(1-\sigma)}{f \Delta I} \quad (2.10)$$

As can be seen from Eq. (2.9), there is a tradeoff between inductance and ripple current. Lower target ripple current equates to higher minimum inductance. To optimize the output filter performance it is recommended to target 20% −40% inductor ripple current.

2.3.2 Selecting the Capacitor

The output capacitor functions to maintain a regulated output voltage for the time period during which the power source is switched off and is required to limit the amount of ripple in the output voltage to as small an amount as possible.

Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high equivalent-series resistance (ESR) in the output capacitor. The maximum allowed output-voltage overshoot and ripple are usually specified at the time of design. Thus, to meet the ripple specification for a step-down converter circuit, you must include an output capacitor with ample capacitance and low ESR [iv].

The current through a capacitor in general is given by,

$$i_c = c \frac{dv_c}{dt} \quad (2.11)$$

Implying that

$$v_c = \frac{1}{C} \int i_c \, dt \quad (2.12)$$

Or

$$v_c = \frac{\Delta I}{C}\Delta T \tag{2.13}$$

If we consider the section of the circuit represented in Figure 2.3, considering only ac signals, and that $v_o = \Delta V$, we notice that,

$$\Delta V = v_c + i_c ESR \tag{2.14}$$

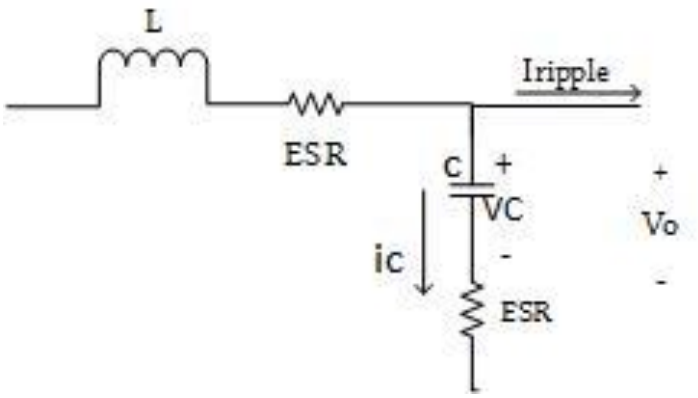

Figure 2.3: Section of Buck converter showing capacitors ESR.

By substituting for v_c from Eq. (2.13) into Eq. (2.14), and solving for C, the capacitance, we get

$$C = \frac{\Delta T}{\frac{\Delta V}{\Delta I} - ESR} = \frac{\Delta I \Delta T}{\Delta V - \Delta I . ESR} \tag{2.15}$$

Where $\Delta T = \sigma / f$.

Eq. (2.15), takes into consideration the role played by the capacitor's ESR in determining the capacitance value.

2.3.3 MOSFETs Selection.

Selecting a MOSFET can be daunting, so engineers often avoid that task by choosing a regulator IC with an internal MOSFET. Unfortunately, most manufacturers find its cost prohibitive to integrate a large MOSFET with a dc-dc controller in the same package, so power converters with integrated MOSFETs typically specify maximum output currents no greater than 3 A to 6 A. For larger output currents, the only alternative is usually an external MOSFET [v].

To simplify the gate drive circuitry for the MOSFET, a P-channel device is preferable to an N-channel device. An N-channel device would require a gate drive circuit that incorporates a method to drive the gate voltage about the source. The cost of a level translator and charge pump will outweigh the savings of using an N-channel device versus a P-channel

device. Most small surface mount packages have thermal resistances of about 50 degrees Celsius per watt. With a calculated power dissipation of 0.3 watt, the MOSFET should experience a temperature rise of only 15 degrees C.

The idea of a synchronous buck converter is to use a MOSFET as a rectifier that has very low forward voltage drop as compared to a standard rectifier. By lowering the diode's voltage drop, the overall efficiency for the buck converter can be improved. The synchronous rectifier (MOSFET Q2, Figure 2.1) requires a second PWM signal that is the complement of the primary PWM signal. Q2 is on when Q1 is off and vice a versa. This PWM format is called Complementary PWM.

The values of the buck converter components chosen according to the design techniques delineated in this chapter are shown in Table 2.2.

Parameter	Value
Inductance, L	12µH
ESR of inductor, r_L	0.037Ω
Capacitance, C	19.5µF
ESR of Capacitor, r_C	0.03Ω
ON resistance of MOSFET #1, R_{ON}	0.02Ω
ON resistance of MOSFET # 2, R_{OFF}	0.0044Ω
Load Resistance, R_{load}	1Ω

Table 2.2: Table of values of Buck Converter parameters

CHAPTER 3

STATE SPACE AVERAGE MODEL OF BUCK CONVERTER

3.0 Introduction

It is common knowledge that the circuit model of converters is very essential to simulation and controller design. The significance of this premise has recently become evident, especially for the development of digital-controlled DC/ DC converters. There are several methods for deriving accurate and less calculation converter model. In circuit averaging method, the switched inductor with the left side commutating from V_s to ground is replaced by a time invariant two port containing: a DC transformer, a dependent current source in the primary and a dependent voltage source in the secondary. Furthermore, state-space averaging technique [viii] based upon the modern control theory is used to describe the dynamics of converters. The circuit is represented by simultaneous state space equations and the related solutions are derived by the theory of linear algebra. The average switching model using Switch network is discussed in [ix] where the converter is replaced by a two port network. Other methods such as modeling via the use of graph theoretic concepts are also discussed [x].

In this thesis we shall employ the method of state space averaging to represent our buck converter for simulation conveniences.

3.1 State Space Description for each Switching Interval

Figure 3.1 illustrate the structure of a synchronous buck that we shall model through state space averaging method. It is evident that devices such as resistors, capacitors, switches and inductors are not ideal in practical situations. In Figure 3.1, the switches are replaced by ideal switches and equivalent series resistances; the inductor and capacitor by an ideal inductor and capacitor respectively, along with an equivalent series resistances.

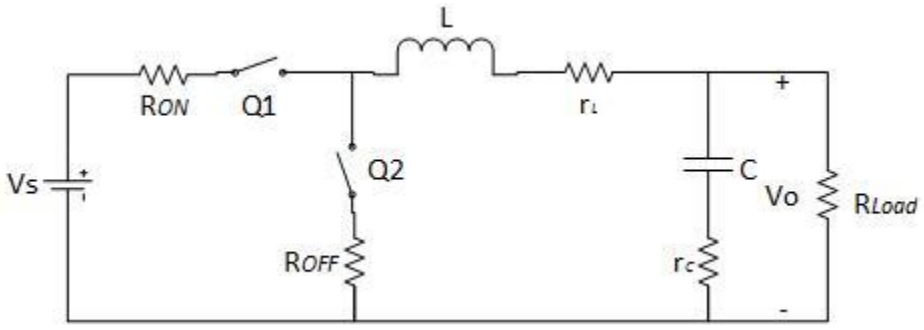

Figure 3.1: Structure of a practical Buck Converter

The converter can be described as switching between different time-invariant systems and the state-space description of each one of these systems is first derived.

3.11 The ON State.

The ON state is the period during which the switch is closed and current flows from the source, charging the inductor and the capacitor as illustrated in Figure 3.2. In the state space model described in [xi], a current source is injected in the output for purposes of control. In this thesis the converter is to be controlled by variation of the duty cycle.

From Figure 3.2, the following equations can be obtained.

$$V_L = L\frac{di_L}{dt} = V_s - V_o - i_L(r_L + R_{ON}) \quad (3.\ 1)$$

$$i_C = C\frac{dv_c}{dt} = -I_o + i_L \quad (3.\ 2)$$

Also,

$$I_o = \frac{V_o}{R_{Load}} = \frac{1}{R_{Load}}(v_c + r_c C\frac{dv_c}{dt}) \quad (3.\ 3)$$

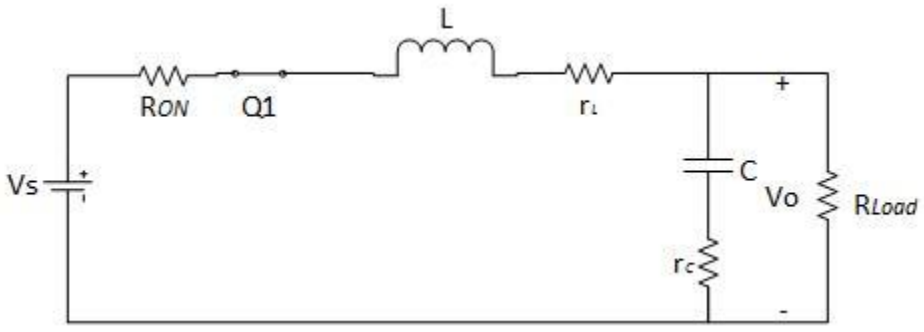

Figure 3.2: Circuit of Buck Converter During T_{ON}

By substituting Eq. (3. 3) onto (3. 2) and solving for $\frac{dv_c}{dt}$ we get the following equation.

$$\frac{dv_c}{dt} = -\frac{1}{C}\left(\frac{1}{r_c+R_{Load}}\right)v_c + \frac{1}{C}\left(\frac{R_{Load}}{r_c+R_{Load}}\right)i_L \quad (3.\ 4)$$

We can also note that;

$$V_o = v_c + r_c i_c = v_c + r_c C\frac{dv_c}{dt} \quad (3.\ 5)$$

If we substitute, $\frac{dv_c}{dt}$ of Eq. (3. 4) in (3. 5), we get;

$$V_o = \frac{R_{Load}}{r_c+R_{Load}} v_c + \frac{R_{Load} r_c}{r_c+R_{Load}} i_L \quad (3.6)$$

Now; substituting for V_o of Eq. (3. 6) in (3.1), we get the equation below.

$$\frac{di_L}{dt} = -\frac{1}{L}\left(\frac{R_{Load}}{r_c+R_{Load}}\right) v_c - \frac{1}{L}\left(r_L + R_{ON} + \frac{r_c R_{Load}}{r_c+R_{Load}}\right) i_L + \frac{1}{L} V_s \quad (3.7)$$

Eqs. (3. 4) and (3. 7) can be written in the form, $\dot{\boldsymbol{x}} = \boldsymbol{Ax} + \boldsymbol{Bu}$ and Eq. (3. 5) in the form y= **Cx** + **Du,** as in the following equation.

$$\begin{cases} \begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C(r_c+R_{Load})} & \frac{R_{Load}}{C(r_c+R_{Load})} \\ -\frac{R_{Load}}{L(r_c+R_{Load})} & \frac{1}{L}\left(r_L + R_{ON} + \frac{r_c R_{Load}}{r_c+R_{Load}}\right) \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} V_s \\ V_o = \begin{bmatrix} \frac{R_{Load}}{r_c+R_{Load}} & r_c // R_{Load} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \end{cases} \quad (3.8)$$

Eqs. (3. 8) and (3. 9), represent the state space of buck converter during the time period when the switch, Q1is closed.

3.12 The OFF State.

The OFF state of a buck converter refers to the switch Q1 is opened and Q2 closed. The circuit representation of this state is shown in Figure 3.3.

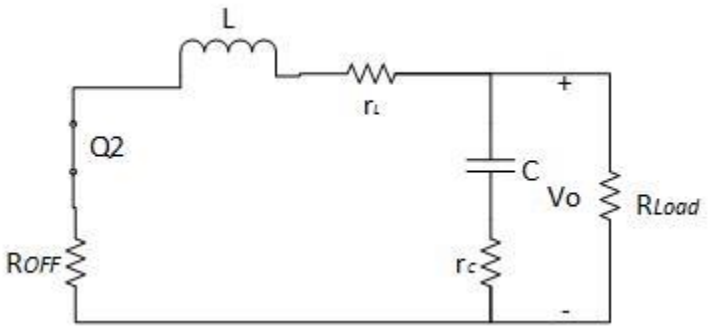

Figure 3.3: Circuit of Buck converter during T_{OFF}

As is shown, the only difference in Figure 3.2 and 3.3 is the absence of the power source in Figure 3.3 and the replacement of R_{ON} by R_{OFF}. It is easy to get the state space equation of this Off state, haven gotten that of the ON state, by simply replacing all the terms with V_s by zero and R_{ON} by R_{OFF}. Haven done this we get the state space representation of this state in the form $\dot{\boldsymbol{x}} = \boldsymbol{A1x} + \boldsymbol{B1u}$ and $y = \boldsymbol{C1x} + \boldsymbol{D1u}$.

$$\begin{cases} \begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C(r_c+R_{Load})} & \frac{R_{Load}}{C(r_c+R_{Load})} \\ -\frac{R_{Load}}{L(r_c+R_{Load})} & \frac{1}{L}\left(r_L + R_{OFF} + \frac{r_c R_{Load}}{r_c+R_{Load}}\right) \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \\ V_o = \begin{bmatrix} \frac{R_{Load}}{r_c+R_{Load}} & r_c // R_{Load} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \end{cases} \quad (3.9)$$

3.13 State Space Average of Buck Converter

The converter behaves like switching between the two different linear time-invariant systems during the switching period, so it looks like a time-variant system. State-space averaging will be used in the next subsection to approximate this time-variant system with a linear continuous time time-invariant system. In this subsection, the method of state-space averaging is presented. State space averaging is done by calculating a nonlinear time-invariant system by means of averaging [xi].

The two linear systems are averaged with respect to their duration in the switching period:

$$\begin{cases} \dot{x} = (\sigma A + (1-\sigma)A1)x + (\sigma B + (1-\sigma)B1)u \\ y = (\sigma C + (1-\sigma)C1)x \end{cases} \quad (3.10)$$

Upon comparing the values of A, B and C from Eq. (3. 8) and A1, B1 and C1 from Eq. (3. 9) we discover that A = A1, B = B1 and C ≈ C1. Substituting these parameters, we get the state space averaged model of the buck converter.

$$\begin{cases} \begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C(r_c+R_{Load})} & \frac{R_{Load}}{C(r_c+R_{Load})} \\ -\frac{R_{Load}}{L(r_c+R_{Load})} & \frac{1}{L}\left(r_L + R + \frac{r_c R_{Load}}{r_c+R_{Load}}\right) \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} \sigma V_s \\ V_o = \begin{bmatrix} \frac{R_{Load}}{r_c+R_{Load}} & r_c // R_{Load} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} \end{cases} \quad (3.11)$$

Where;

$R = \sigma R_{ON} + (1-\sigma) R_{OFF}$.

Since the only controllable parameter is the duty cycle, σ, whereas any changes in the source voltage, V_S, are regarded as noise, the controller output, u, equals σ.

3.2 Open Loop Simulation of Buck Converter

Open loop simulation is done by means control using a pulse width modulator (PWM). This is done with no feedback mechanism and output response is dependent upon the duty cycle chosen.

When we substitute the parameters listed in Table 2.2 into Eq. (3. 11), we obtained a state space equation as shown in Eq. (3. 12).

$$\begin{cases} \begin{bmatrix} \frac{dv_c}{dt} \\ \frac{di_L}{dt} \end{bmatrix} = \begin{bmatrix} -49788.4 & 49788.4 \\ -80906.15 & -3335.52 \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ 83333.3 \end{bmatrix} \sigma V_s \\ V_o = [0.971 \quad 0.0291] \begin{bmatrix} v_c \\ i_L \end{bmatrix} \end{cases} \quad (3.12)$$

The Simulink model of this converter is shown in Figure 3.4.

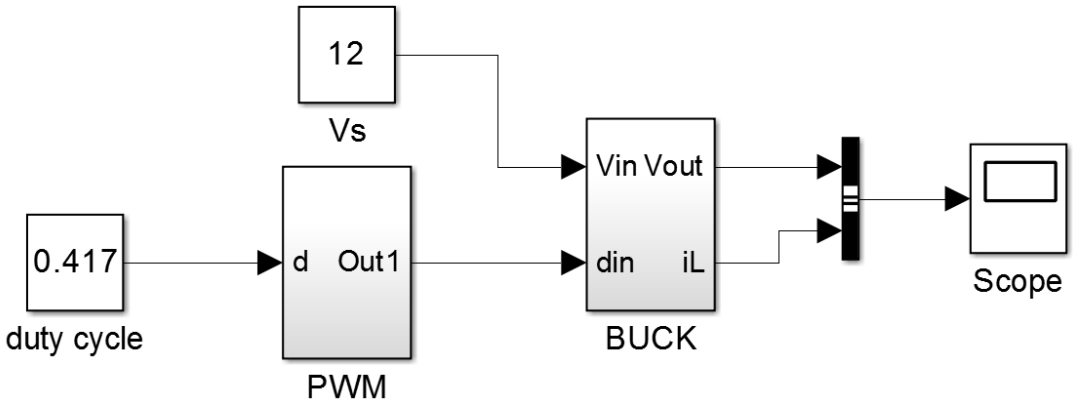

Figure 3.4: Open Loop model of Buck converter.

In Figure 3.4 above the Buck subsystem has a structure as shown in Figure 3.5. Note that this block is manually design so that we can easily view the response in other sections of the converter apart from the output (i.e. the state variables; which can be used for designing of controller by state space method [xii]).

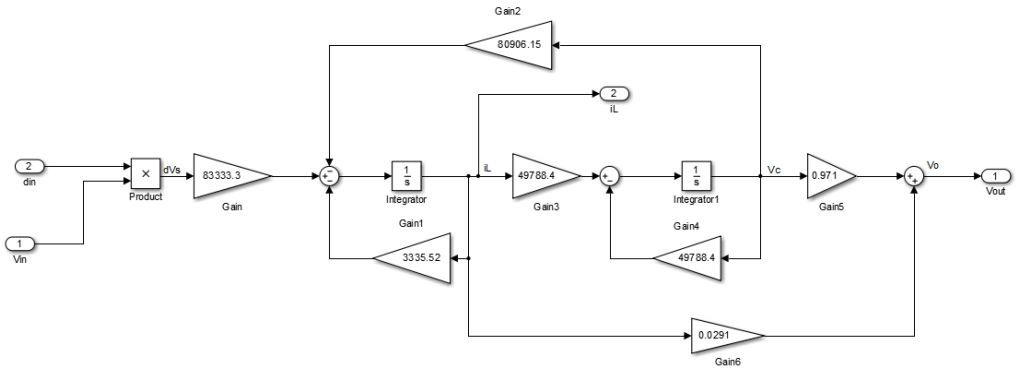

Figure 3.5: Buck converter structure designed from state space equation

The structure of the PWM shown in Figure 3.6 is modified so that a duty cycle of say 0.4 gives exactly a pulse of width 40% of the switching period. This modification has to be done became Matlab-Simulink only provide sawtooth generator width amplitudes varying from 1to -1, unlike 0 to 1as we require.

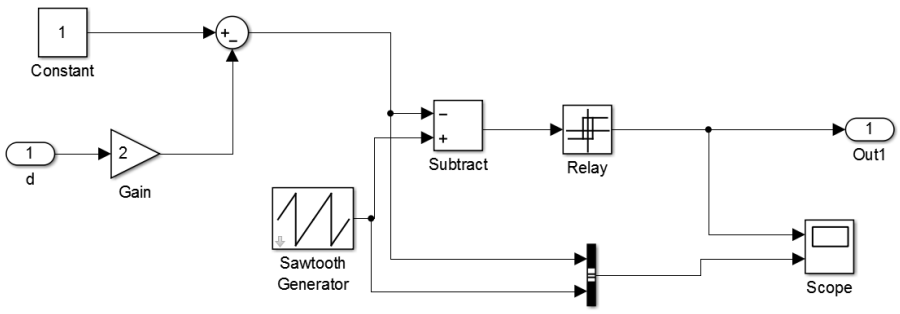

Figure 3.6: PWM for Switching of the Converter.

3.2.1 Open Loop Output Response.

The simulation results obtained from open loop simulation of buck converter are displayed in Figure 3.7.

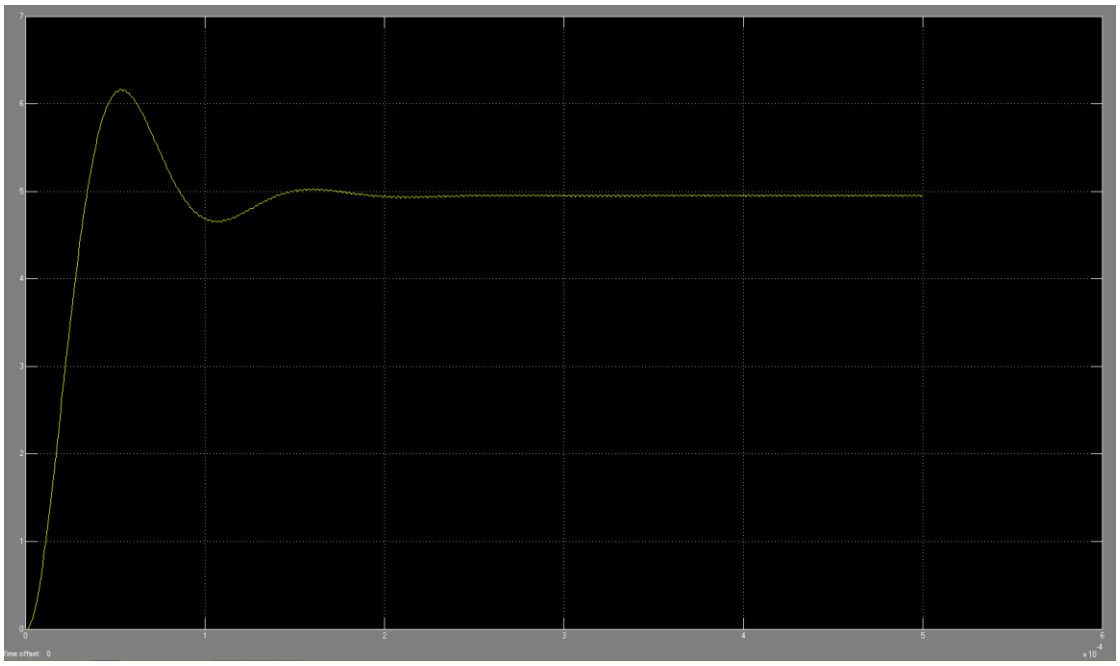

Figure 3.7: Open Loop output Response of a Buck Converter

The performance of this converter can be determined by examining the performance parameters of Table 3.1. Examination of these response parameters gives us an insight of how design compensator according to our desired response.

Parameter	Value
Peak Time	52µs
Peak Voltage	6.16V
Settling Time	129µs
Rise Time	22.8µs
Steady State Voltage	4.95V
Overshoot	24.3%
Steady State Error	0.05V

Table 3.1: Output Performance Parameters

Looking at Table 3.1, one would think 'the performance is not that bad', but since this is open loop, any changes in source voltage due to noise and other perturbations will also lead to changes in the converter's performance. An ideal converter is immune to noise and gives a constant response no matter what happens. This is our controller design goal.

CHAPTER 4

PID CONTROLLER DESIGN VIA ROOT LOCUS TECHNIQUES

4.0 Introduction

Root locus, a graphical presentation of the closed-loop poles as a system parameter is varied, is a powerful method of analysis and design for stability and transient response. Feedback control systems are difficult to comprehend from a qualitative point of view, and hence they rely heavily upon mathematics. The root locus is a graphical technique that gives us the qualitative description of a control system's performance that we are looking for and also serves as a powerful quantitative tool that yields more information than the other methods.

The root locus can be used to describe qualitatively the performance of a system as various parameters are changed. For example, the effect of varying gain upon percent overshoot, settling time and peak time can be vividly displayed. The qualitative description can then be verified with quantitative analysis.

Besides transient response, the root locus also gives a graphical representation of a system's stability. We can clearly see changes of stability, ranges of instability, and the conditions that cause a system to break into oscillation. In a root locus, the imaginary component of a pole corresponds to damped natural frequency, while the radius from the origin to the pole corresponds to natural frequency. The settling time for a system is determined by the slowest response among all responses. The least settling time can be achieved if the roots fall to the far left on the left-hand plane; overshoot can be prevented by placing the poles on the real axis [xi].

4.1 Basic Rules for sketching Root Locus

Number of branches: the number of branches of root locus equals the number of closed-loop poles.

Symmetry: the root locus is symmetrical about the real axis.

Real-axis segments: on the real axis, for $k>0$, the root locus exists to the left of an odd number of real-axis, finite open-loop poles and/ or finite open loop zeros.

Starting and ending points: the root locus at the finite and infinite poles of G(s)H(s) and ends at the finite and infinite zeros of G(s)H(s), where G(s) is forward transfer function of a system and H(s) is the feedback transfer function.

Behavior at infinity: the root locus approaches straight lines as asymptotes as the locus approaches infinity. Further, the equations of the asymptotes are given by the real axis intercept and angle in radians as follows:

$$\sigma = \sum \text{finites poles} - \sum \text{finite poles} / \#\text{finite poles} - \#\text{finite zeros}.$$

$$\alpha = 2(K+1)*pi / \#\text{finite poles} - \#\text{finite zeros}.$$

4.2 PID controller design using root locus

Transfer function of a pid controller is shown Eq. (4. 1) below.

$$G_{PID}(s) = Kp + Ki/s + sKd \quad (4.1)$$

It has two zeros plus a pole at the origin. One zero and the pole at the origin can be designed as the ideal integral compensator; the other zero can be designed as the ideal derivative compensator.

The design technique, consist of the following steps:

1. Evaluate the performance of the uncompensated system to determine how much improvement in transient response is required.
2. Design the PD controller to meet the transient response specifications. The design includes the zero location and loop gain.
3. Simulate the system to be sure all the requirements have been met.
4. Redesign if the simulation shows that requirements have not been met.
5. Design the PI controller to yield the required steady-state error.
6. Determine the gains, Ki, KP, KD.
7. Simulate the system to be sure all the requirements have been met.
8. Redesign if the simulation shows that requirements have not been met.

The matlab code for controller design can be found in appendix A.

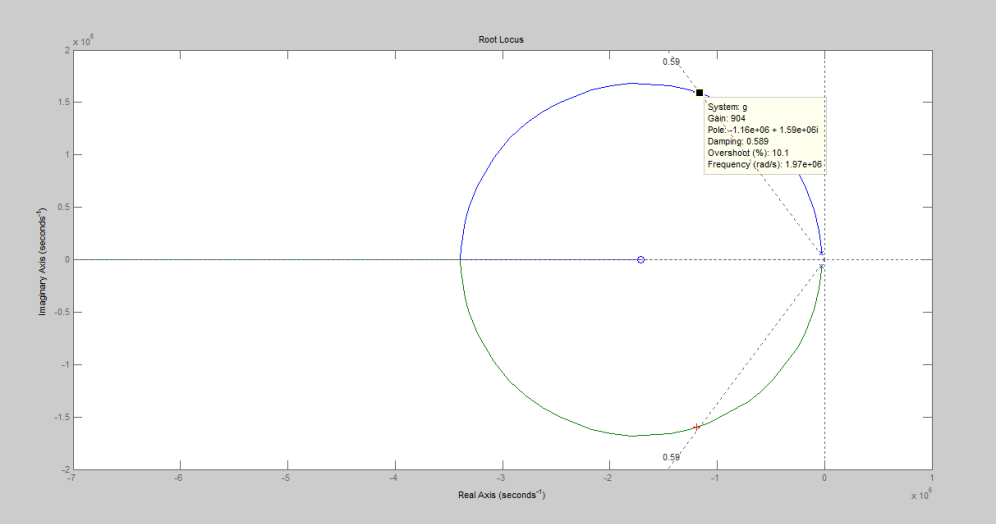

Figure 4.1: Root Locus plot of uncompensated system

At zeta = 0.59 (10% overshoot) from root locus we have the natural frequency 1.97e06. as we know peak time and natural frequency are related as

Tp = pi/ Wn*sqrt (1-zeta*zeta), from this relation we get the peak time. Now from this relation we can also calculate the natural frequency for the required peak time.

To compensate the system to reduce the peak time to two-thirds of that of uncompensated system, we must find the compensated system's dominant pole location. The imaginary part of the compensated dominant pole is, Wd = pi/ Tp and real part is σ = Wd/ tan117. By using root locus program, we can find the sum of angles from the uncompensated system's poles and zeros to the desired compensated dominant pole. Assume that the compensator zero is located at –Zc. Since Wd/ (Zc- σ) = tanα, where 'α' is the contribution required from the compensator zero.

We can find compensator (PD controller) zero location. After PD controller, we have designed the ideal integral compensator to reduce steady-state error to zero. Any ideal integral compensator will work, as long as the zero is placed close to the origin.

From root locus we get the system gain from which we can calculate KP, KD, ki terms. So compensated system root locus is shown below in Figure 4.2.

PID transfer function

G(s) PID = 394+199/ s+0.000056s

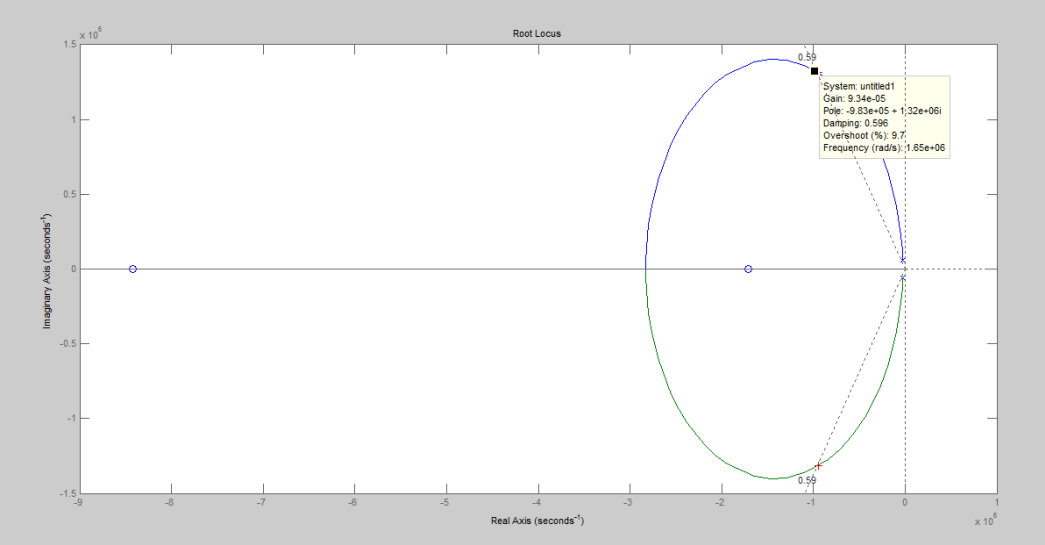

Figure 4.2: Root Locus Plot of compensated system

4.3 DIGITAL PID DESIGN VIA DIRECT ROOT LOCUS METHOD:

Root locus design for a digital PID is similar to an analog PID. Basically, the rules for drawing the root locus for both are the same except that stability, frequency and damping ratio are changed. In terms of stability, it is suggested that the poles be placed in the right-hand plane, and inside the unit circle. The closer the poles are to the origin, the faster the settling time will be.

The procedure to design a digital PID is exactly the same as an analog PID, where the poles and zeros work together to shape the root loci to the desired location. Even though there is no need to physically build a controller algorithm as the analog PID, one needs to consider whether the digital PID is realizable (*i.e.* the controller does not requires future variables). If the controller is not programmable, the digital PID needs to be redesigned. Modification such as adding another pole inside the unit circle can possibly make the controller realizable.

4.4 DIGITAL PID DESIGN VIA DIRECT FREQUENCY METHOD:

Direct frequency design is useful especially in deadbeat control, a method to make the system meet commands one sample time later than the desired time. Using direct frequency design, system requirements are first considered, and written in the form of a transfer function. The controller and system transfer function is set equal to the desired transfer function. Then, the proportional, integral and derivative terms can be solved. This is illustrated in Eq. (4. 2).

$$T(z) = \frac{C(z)}{R(z)} = \frac{D(z)G(z)}{1+D(z)G(z)} \qquad (4.\ 2)$$

In Eq. (4.2), *T(z)* represents the desired transfer function, *C(z)* represents sampled system output, *R(z)* represents sampled system desired input, *D(z)* represents a controller transfer function, and *G(z)* represents a discrete system transfer function. Again, the digital PID must be programmable, so that it does not require the knowledge of future variables.

4.5 Simulation Results of PID controlled buck Converter

Figure 4.3 shows a Simulink block diagram of a PD compensated buck converter. Here subsystem 1represents the PWM and subsystem is the state space modeled buck converter. The response obtained from this Simulink block was plotted in Figure 4.4.

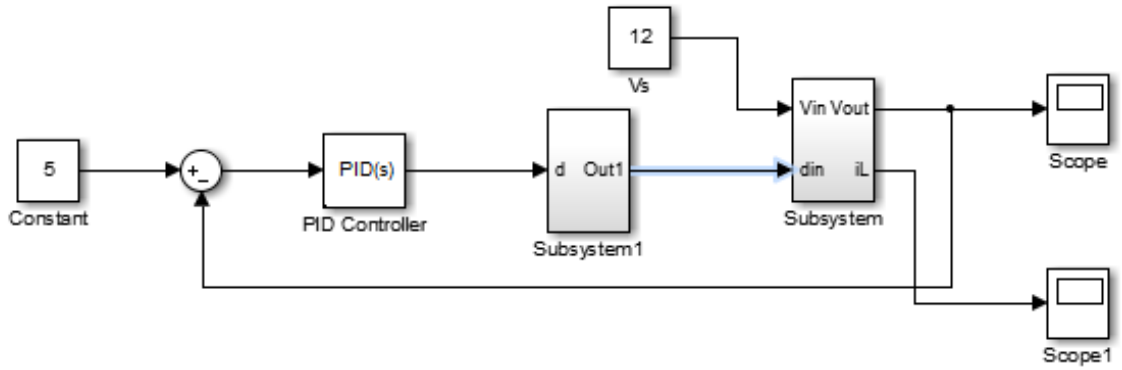

Figure 4.3: Simulink Model of closed loop buck converter

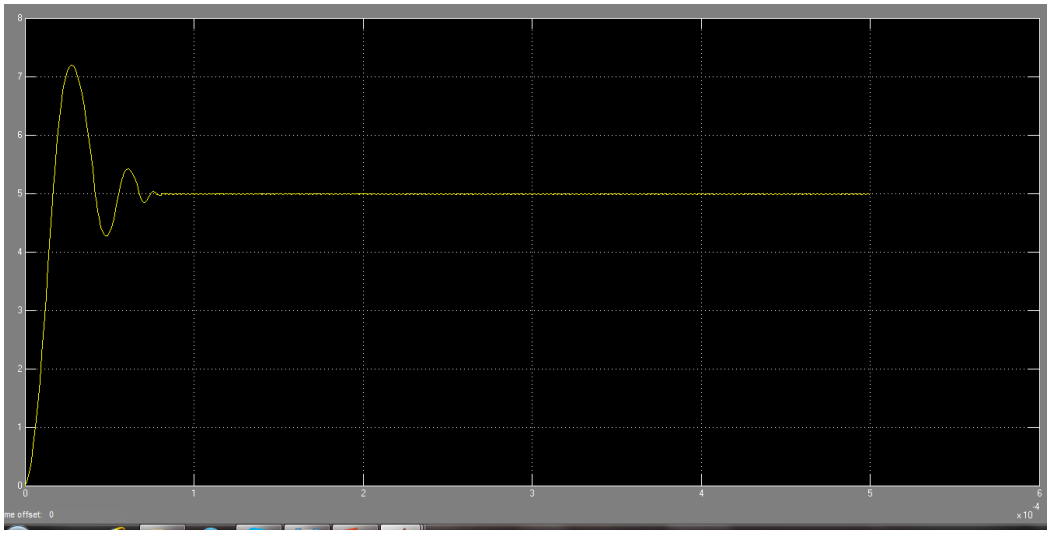

Figure 4.4: Output response of PID compensated Buck converter

Figure 4.4 shows the response obtained from a manually tuned PD controller. After several investigations we noted that the integral term of the controller had no effect on the

converter performance. Also a low pass filter of transfer function, 1/(0.01s+1), was inserted into the derivative term of the controller. The response obtained was from a proportional gain, P, of 5 and a derivative gain, Pd, of 0.155. The step response of this compensated converter is plotted as shown in Figure 4.5.

Step response of compensated buck converter

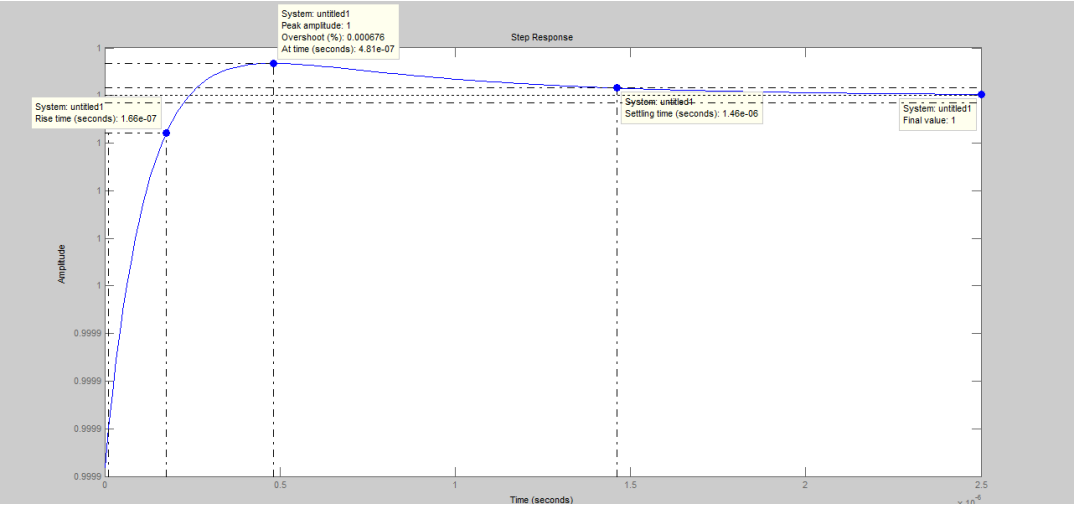

Figure 4.5: Step response.

Simulation results of compensated system

- Rise time = 166e-07,
- Peak time = 4.81e-07,
- Settling time = 146e-06,
- Steady state error = 0
- % overshoot = 0.00067

Improvements

- Rise time = from 4.66e-07 to 166e-07,
- Peak time = from 1.19e-06, to 4.81e-07,
- Settling time = from 3.53e-06 to 146e-06,
- Steady state error = from 0.001to 0
- % overshoot = from 24 to 0.00067

4.6 Remarks

From above results we see that various parameters like rise time, peak time, settling time, overshoot, and steady-state error have improved with PID compensation. Apart for the afore mentioned improvements, unlike the open loop response where slight changes will dramatically affect the performance of the converter, slight changes in the source voltage will not affect the converter response.

It was noticed the larger fluctuations in value of the source voltage of the simulated compensated converter led to complete failure of the system. With this problem we seek for a more robust controller, like a fuzzy logic controller or a neural converter.

CHAPTER 5

FUZZY CONTROLLER DESIGN FOR DC-DC CONVERTERS

5.0 Introduction

Linear controllers for DC-DC converters are usually designed based on mathematical models. To obtain a certain performance objective, an accurate model is essential. Linear controllers were designed based on converter's small signal model using frequency response and root locus design methods. The small signal model changes due to variations in operating point. To achieve a stable and fast response, two solutions are possible. One is to develop a more accurate model for the converter. However, the model may become too complex to use in controller development. A second solution is to use a nonlinear controller [xiii]. Since fuzzy controllers don't require a precise mathematical model, they are well suited to nonlinear, time-variant systems.

5.1 Overview of Fuzzy Control

Fuzzy control is an artificial intelligence technique that is widely used in control systems. It provides a convenient method for constructing nonlinear controllers from heuristic information.

Conventional controllers are designed based on a mathematical model. Closed loop control specifications include disturbance rejection properties, insensitivity to plant parameter variations, stability, rise time, overshoot and settling time and steady-state error. Based on these specifications, conventional controllers are designed. Major conventional control methods include classical control methods (frequency response and root locus techniques), state-space methods, optimal control, robust control, adaptive control, sliding mode control and other nonlinear control methods such as feedback linearization and back-stepping. These conventional control methods provide a variety of ways to utilize information from mathematical models on how to obtain good control.

Different from conventional control, fuzzy control is based on the expert knowledge of the system. Fuzzy control provides a formal methodology to represent and implement a human's heuristic knowledge about how to control the system.

5.2 Fuzzy Controller

It is appropriate to use a method from Artificial Intelligence to handle complexity of non-linearities in the system in order to achieve intelligent control action. Intelligent control using Fuzzy logic is the ability of a controller to comprehend, reason and learn about a process and is largely rule-based because the dependency involved in its deployment are much too complex to permit an analytical representation. To deal with such dependency, the mathematics of Fuzzy system integrates both the experience and knowledge or intuition

gained in the operation of a similar plant into the control algorithm. The general structure of a Fuzzy controller [xiv]-[xv] is represented in Figure 6.1 and the algorithm consists of a set of fuzzy rules which are related by the concepts of fuzzy implication and the compositional rule of inference [xvi]. The nine steps involved in the design of off-line implementation are:

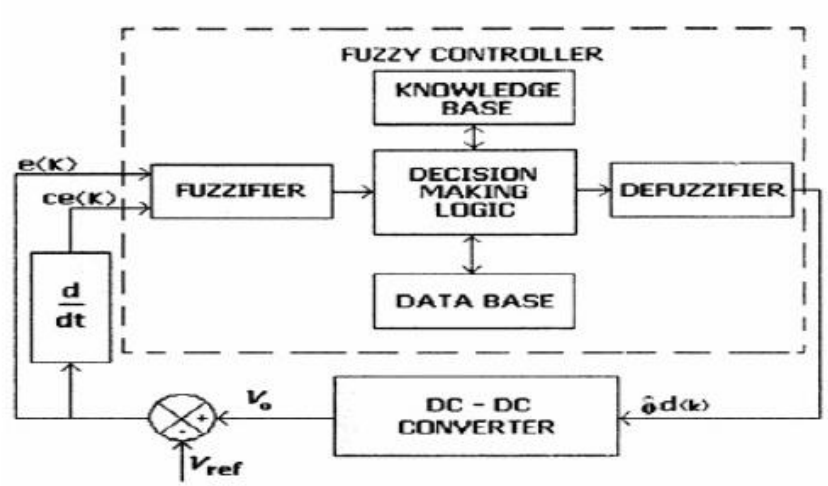

Figure 6.1: Basic configuration of closed loop Fuzzy controller

6.3 Identification of Input and Output Variables

The inputs to Fuzzy controller are the error signal e(k) and the time rate of change of error signal ce(k) which are defined in Eqs (6.1) and (6.2) respectively as

$$e(k) = V_o - V_{ref} \tag{6. 1}$$

$$ce(k) = e(k) - e(k-1) \tag{6. 2}$$

Where V_o, is the sampled output voltage of the DC–DC converter, V_{ref} is the reference output voltage and the symbol k denotes value at the beginning of *kth* switching cycle. The output of Fuzzy controller is the change in duty cycle, $\delta d(k)$ and duty cycle $d(k)$ at kth sampling time is in Eq. (6. 3)

$$\mathrm{d(k)} = \mathrm{d(k-1)} + \eta.\,\delta \mathrm{d(k)} \tag{6. 3}$$

where $\delta d(k)$ is the inferred change in duty cycle at *kth* sampling time and η is the gain factor.

6.3.1 Frame for Fuzzy Variables

The Universe of discourse of the interval spanned by each input and output variable is partitioned into a number of fuzzy subsets, assigning each subset a linguistic value. For ease of computation, seven fuzzy subsets are defined by the library of fuzzy set values for the error and time rate of change in error signal and they are represented as NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big).

6.3.2 Assignation of Membership Value to Fuzzy Variables

It is a graphical representation of the magnitude of participation of each input and is defined taking into account the conditions of normality and convexity of fuzzy sets; it embodies the mathematical representation of membership in a set and is required to have uniform shape, parameters and functions for the sake of computational efficiency, efficient use of the computer memory and henceforth performance analysis. Among the four membership functions available at present, three Gaussian functions are chosen to model, analyze and simulate the Fuzzy controller. The membership functions for the input and output variables are shown in Figures 6.2, 6.3, and 6.4.

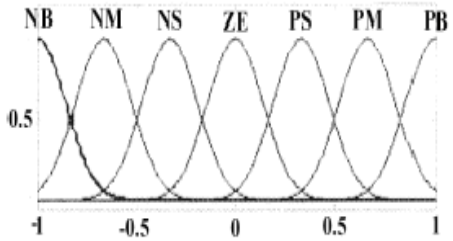

Figure 6. 2: Membership function for error signal

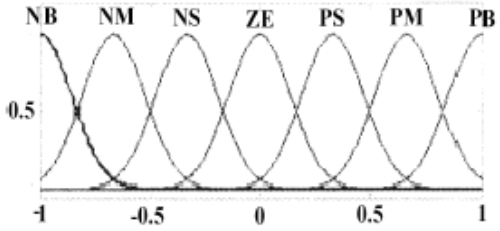

Figure 6.3: Membership function for change in error signal

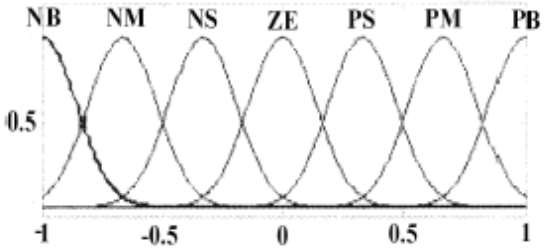

Figure 6.4: Membership function for control signal

6.3.3 Creation of rule-base

The collection of rules is called a rule-base and it expresses input-output relationship in linguistic terms; the rules are heuristic in nature and are typically written as antecedent – consequent pairs of IFTHEN structure; the inputs are combined by AND operator. The generic linguistic control rule [20] has the form as IF x is A AND y is B THEN z is C where x, y are the input linguistic variables and z is the output linguistic variable; A, B and C are the fuzzy subsets in the Universe of discourses X, Y and Z respectively. 49 rules based on Mamdani architecture are formed depending on the number of membership functions in order to play a key role in the improvement of system performance and is mentioned in Table 6.1and the rule- base in terms of surface view is shown in Figure 6.5.

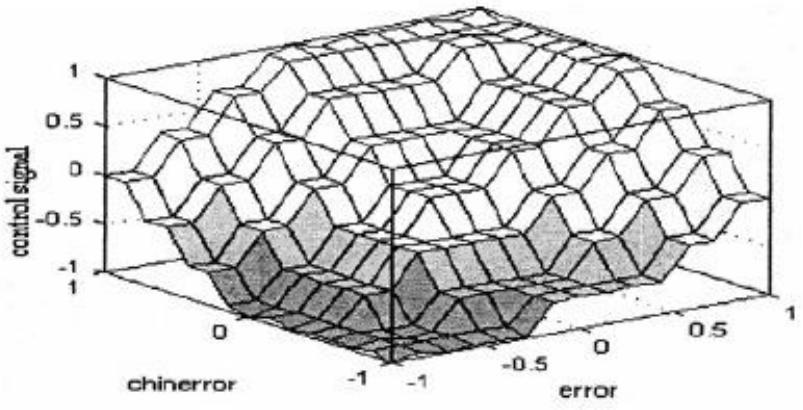

Figure 6.5: Rule base surface view

e\ce	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NM	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Table 6.1: Control signal rules

6.4 Fuzzification Process

Fuzzification matches input data with the conditions of the rules to determine how well the condition of each rule matches that particular input instance [xvii].

6.4.1 Firing

Determining applicability of each rule is firing. A rule fires at time, t if its premise membership value at time, t is greater than zero. The inference mechanism or decision making logic determines which rules fire to find out which rules are relevant to the current situation and combines recommendation of all the rules to arrive at a single conclusion [xviii].

6.4.2 Aggregation of Fuzzy outputs

The input to inference process is the set of all rules that fire and its output is the set of fuzzy sets that represents the inference reached by all the rules that fire. It is necessary to combine all the recommendation of all the rules to determine the control action and it is done by aggregating the inferred fuzzy sets.

6.5 Defuzzification Process

Conservation of the fuzzy to crisp or output is defined as Defuzzification. Mean of Maxima (MOM) method is implemented, wherein the highest membership function component in the output is considered [xix]. It disregards the shape of the fuzzy set but the computational complexity is relatively good.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

Open loop buck converter simulation is fraught with problems such as instability in practical power sources leading to non-constant output responses. These were alleviated when the converter was compensated by the PID transfer function. Improvements in performance such as dwindling of the steady state error value were also achieved by the help of PID controller.

6.2 Future Work

Fuzzy optimization has faced many challenging problems where experience or knowledge a priori often counts as a major determining factor of the controller performance. Methods of optimizing fuzzy membership functions, fuzzy rules and gain optimization, have drawn the attention of researchers in this field. One of these methods sought, is to use the robustness of Genetic Algorithm for optimization of fuzzy parameters. Genetic Algorithm techniques can be employed in the design of a fuzzy controller that helps to solve the problems that fraught Buck converter design.

The efficiency and effectiveness of a controller often always comes at a price. Hardware implementation of these so called ultimate controllers always demand high sums of money, leading in turn to higher prices of those electronic devices that make use of them. Researchers have sought and are still searching for ways to maintain the efficiency and robustness of controllers, while still maintaining lower and affordable prices.

Other alternative controller techniques such as neural network method can be exploited for the design and control of DC-DC converter. These methods using concepts of artificial intelligence can prove to be rewarding if their many advantages are harnessed for controller design purposes.

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Appendix A

Matlab code for Pid controller design.

MATLAB CODE

```
    s=tf('s');
>> n=[0,2.499999000000000e+03,4.273494040601700e+09];

   d=[1,5.529880000000002e+04,-3.753820743012000e+09];
>> g=tf(n,d)

g =

      2500 s + 4.273e09
  ----------------------
  s^2 + 5.53e04 s - 3.754e09

Continuous-time transfer function.

>> pos=input('10%');
10%
>> zeta=0.59;
>> rlocus(g)
sgrid(zeta,0)
[k,p]=rlocfind(g);
Select a point in the graphics window

selected_point =

  -6.6348e+05 + 1.3072e+06i

>> k

k =

  505.5544

>> p

p =

   1.0e+06 *

  -0.6596 + 1.3121i
  -0.6596 - 1.3121i
```

```
>> m=feedback(k*g,1)
step(m)

m =

      1.264e06 s + 2.16e12
  ----------------------
  s^2 + 1.319e06 s + 2.157e12

Continuous-time transfer function.

>> sd=-1.33333+5.1411i

sd =

  -1.3333e+06 + 5.1411e+05i

>> angle_at_desired_pole=(180/ pi)*angle(polyval(n,sd)/ polyval(d,sd))

angle_at_desired_pole =

   96.8882

>> d1=s+1390205;
>> rlocus(d1*g);
sgrid(zeta,0);
[k,p]=rlocfind(d1*g)
Select a point in the graphics window

selected_point =

  -2.9044e+05 + 5.6360e+05i


k =

   8.2602e-05


p =

   1.0e+05 *
```

```
  -2.8818 + 5.6620i
  -2.8818 - 5.6620i

>> m=feedback(k*d1*g,1);
step(m)
>>
>> d2=(s+0.5)/s

d2 =

  s + 0.5
  -------
     s

Continuous-time transfer function.

>> d=d1*d2;
rlocus(d*g)
>> sgrid(z,0)
[k,p]=rlocfind(d*g)
Undefined function or variable 'z'.

>> sgrid(zeta,0)
>> [k,p]=rlocfind(d*g)
Select a point in the graphics window

selected_point =

  -2.8662e+05 + 5.5421e+05i


k =

   8.0000e-05


p =

   1.0e+05 *

  -2.8134 + 5.6017i
  -2.8134 - 5.6017i
```

-0.0000 + 0.0000i

>> step(feedback(k*d*g,1)).