A HIGH STEP-UP DC-DC BOOST CONVERTER BASED ON COUPLED INDUCTOR AND SWITCHED CAPACITOR

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Declaration of Authorship

We, Md. Rafin Mahabub (160021098), Md. Asif Bin Zaman (160021143) and Zaheen Afroz Simin (160021167), declare that this thesis titled 'A high step up dc-dc boost converter based coupled inductor and switched capacitor' and the works presented in it are our own. We confirm that:

- This work has been done for the partial fulfillment of the Bachelor of Science in Electrical and Electronic Engineering degree at this university.

- Any part of this thesis has not been submitted anywhere else for obtaining any degree.

- Where we have consulted the published work of others, we have always clearly attributed the sources.

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Abstract

High step-up dc-dc converter is widely utilized in the sustainable energy system because of the front-end stage of the dc–ac converter. A unique high step-up DC-DC converter is projected which consists of a coupled inductor and switched capacitor. In this boost converter, capacitors are charged in parallel and discharged in series and a coupled inductor is used to get high step-up voltage gain. Due to the utilization of the energy kept in the leakage of the coupled inductor, each of the switches will notice zero-voltage switching. Which leads to low switching loss as well as improved efficiency. In addition, reduced voltage stress of the diodes and switches. As a result, low voltage components can be used. Here input continuous input current is used. The input voltage of the proposed converter is 45V, the output is 250V, and the highest efficiency is 95.3%.

Acknowledgements

Primarily, we offer gratitude to the Almighty Allah (SWT) for giving us the capability to do this work with good health. We are grateful to our research supervisor, Md. Thesun Al Amin sir, for the support and guidance throughout our research at Islamic University of Technology (IUT) since July 2020. He created a research environment for which we were able to explore many ideas without constraint. We have gained a wealth of knowledge and experience in science and engineering through his direction that is beyond value to our future endeavor. For these things, we give many thanks to him. We would like to thank all the faculty members of the department of EEE, IUT for their inspiration and help. Last but not the least we are thankful to our family, friends and well-wishers for their support and inspiration. Without them it would never have been possible for us to make it this far.

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List of Abbreviations

ZVS- Zero Voltage Switching

ZCS- Zero Current Switching

EMI- Electromagnetic Interference

PWM- Pulse Width Modulation

IGBT- Insulated-Gate Bipolar Transistor

SCR- Silicon Controlled Rectifier

MOSFET=Metal oxide semiconductor field effect transistor

BJT=Bipolar junction transistor

GTO=Gate turn-off thyristor

EV=Electric vehicle

PV=Photovoltaics

I. Introduction

1.1 Background & Motivation:

Conventional fossil energy supplies such as coal and oil are no longer able to satisfy rising demand because of its non-renewability. In comparison, the heavy use of fossil fuels has caused substantial environmental pollution [1], [2]. As a result, high quality, especially renewable energy systems are increasingly being used to supply electrical energy [3]-[5].

However, to increase low voltage to high bus voltage, both low-voltage sources, solar photovoltaics (PV) and fuel cells need a high step-up DCDC converter as the front stage. By adjusting the transformer ratio, isolated converters can achieve a high voltage gain. The high turning ratio, however, leads to a complex transformer system and large length. In the meanwhile, the converter's performance is substantially influenced by the voltage spikes induced by leakage induction and high voltage stress [6]-[8]. Non- isolated step-up converters are still commonly used.

Among the non-isolated DC-DC converters, the traditional boost converters will increase the voltage of the by raising the duty ratio. However, the ability to step-up is significantly limited by the parasitic resistance of the switch and the inductor. The high duty ratio, meanwhile, leads to a strong inductor current ripple, a large turn-off current and the switch's high voltage stress, resulting in a large lack of conduction and switching loss. In the meantime, the issue of

reverse recovery of the output diode is still severe because of the broad output diode current [9], [10]. For high voltage gain converters, the coupling-based inductor converter is also a very common option. A high voltage gain can be obtained by isolated converters, by changing the ratio of transformers. During switching transition, however, the leakage inductor of the coupled inductor induces extreme power loss and voltage spike. A passive clamp coupled inductor converter in[11] is proposed to solve the problems. Since the simple diode-capacitor clamp circuit is used to recycle the energy contained in the leakage inducer, the output diode voltage stress is quite large. A coupled inductor converter with an active clamp circuit is suggested in [12]. The number of modules, however, is significantly growing. The high voltage gain for switched capacitor converters can be accomplished by charging the switched capacitors in parallel and discharging them in sequence. The voltage gain of the switched capacitor converter, however, is closely related to the configuration of the circuit. A large number of cascaded switched capacitor units are needed when the required voltage gain is high, which inevitably increases the complexity of the circuit [13]-[15]. Switched capacitor converters integrated with a coupled inductor are seen in [16], [17] to achieve high voltage gain with less parts. High voltage gain can be realized by these converters and the transition voltage stress is minimal. These converters cannot however accomplish soft switching. In [18], the ZVS and ZCS are supplied to the switches through a passive snubber circuit. Additional coupling inductor, capacitor and diode are required on the snubber circuit, which increases the number of components considerably.

1.2 Basic Functionalities of The Proposed Converter:

A new high voltage gain, zero voltage switching, and highly efficient, low voltage stress converter is worked on in this article. Low on-state resistance MOSFETs can therefore be chosen, resulting in a reduced conduction loss and dramatically improved performance. The

leakage inductor energy of the coupled inductor is not used in this converter to increase voltage gain, as in[19], but used to supply switches with ZVS energy. As a result, all switches are capable of achieving ZVS. This tends to decrease the lack of switching and operate at high performance at greater switching frequency. In order to increase power density, high operating frequency is conductive by reducing the scale of magnetic components. The C_2 capacitor and Q_2 switch can also serve as an active clamp mechanism in order to suppress Q_1's voltage surge. The proposed converter's input current would be constant, which for the PV applications is very important.

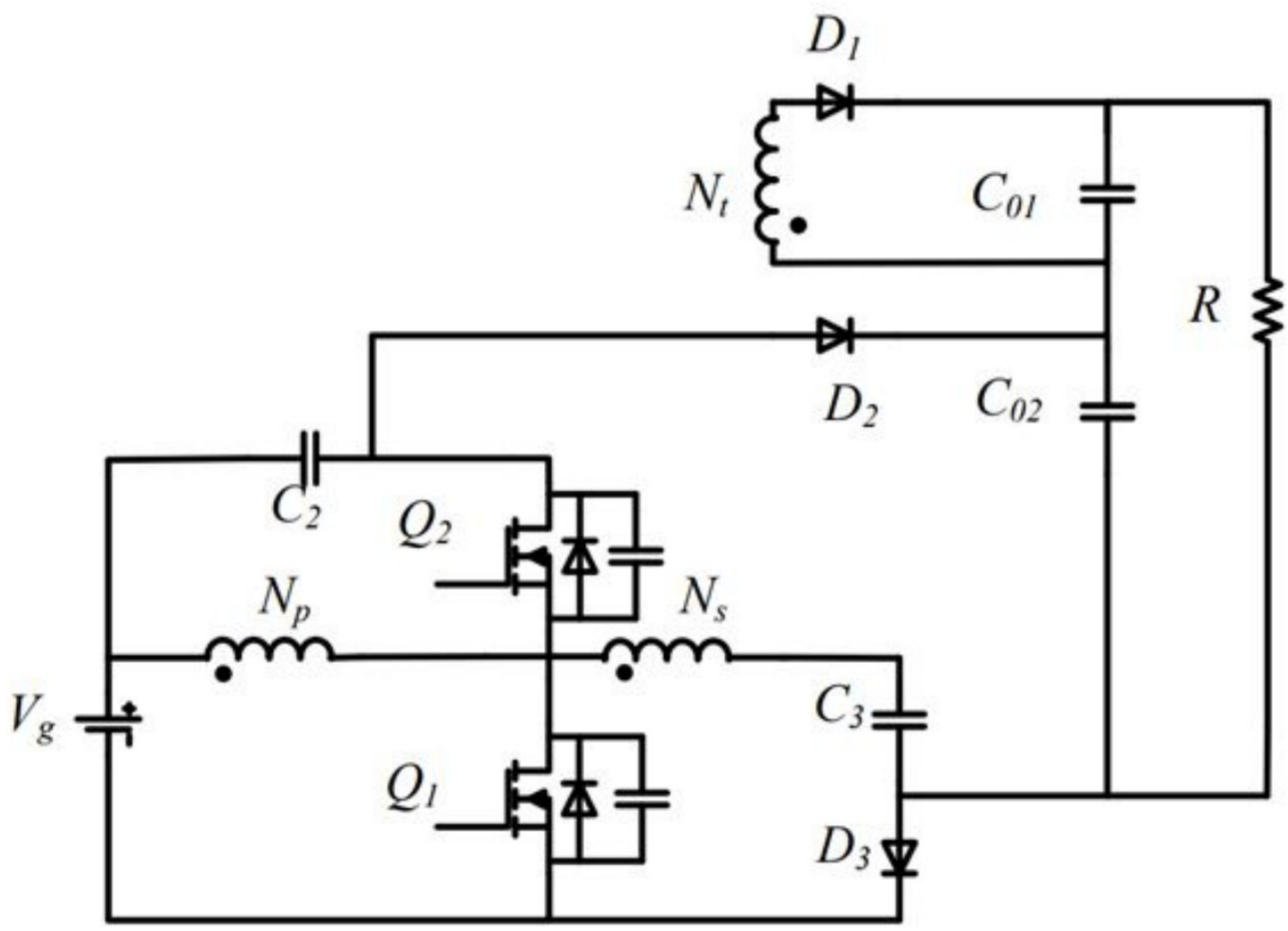


Figure 1.1: Circuit diagram of dc-dc converter. [29]

II. Basic concepts of DC-DC boost converter

2.1 Performance Parameters of DC-DC Boost Converter:

As an input, a dc-dc converter takes dc voltage and delivers dc output. From a fixed or variable dc input voltage, it may generate a fixed or variable dc output voltage. Ideally, a dc-dc converter's output voltage and input current are pure dc but contain harmonics or ripples in a realistic situation. There are two instances where the converter may draw current from the dc source. First of all, when the load is connected to the supply source and secondly when the input current is discontinuous. The dc output power can be written as

$$P_{dc} = I_a V_a \tag{2.1}$$

Here, I_a =Average load current

V_a =Average load voltage

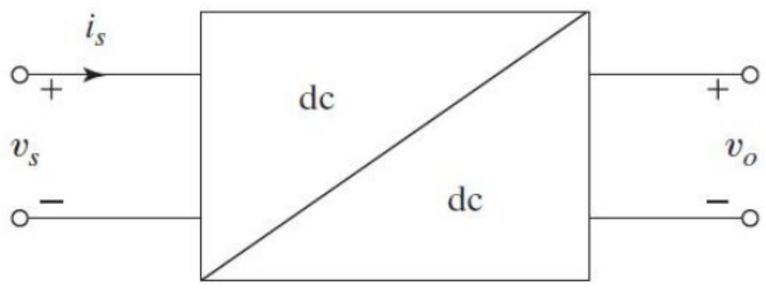


Fig 2.1:Block diagram of dc-dc converter[30]

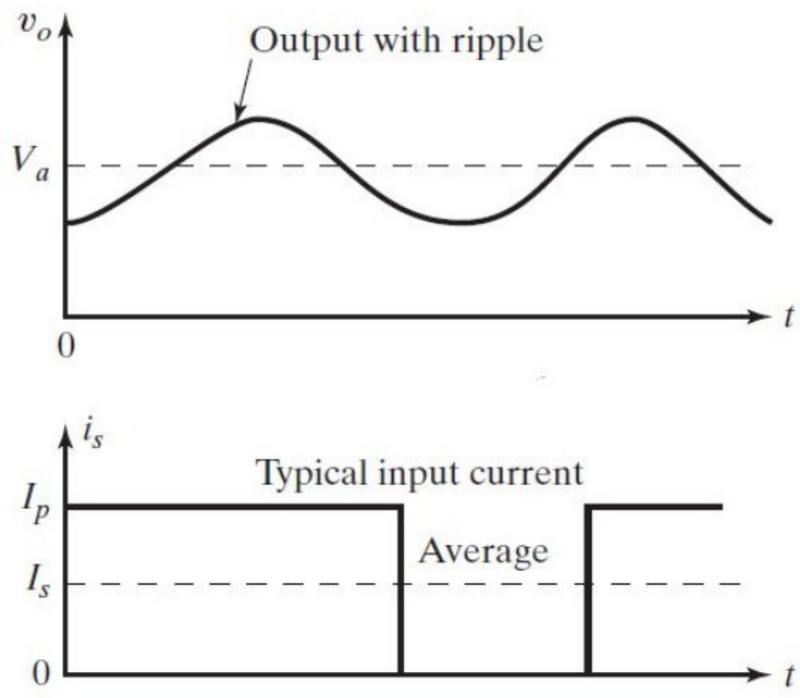


Fig 2.2:Input and output relationship of dc-dc Converter[30]

In figure 2.1,we can see the block diagram of dc-dc boost converter.Here,it is the input current and v_s is the source voltage. Fig 2.2 indicates that in practical cases, the dc-dc converter contains harmonics or ripples.

The ac output power of dc-dc converter can be written as

$$P_{ac} = I_o V_o \qquad (2.2)$$

Here,

I_o =rms load current

V_o =rms load voltage

The converter efficiency is

$$\eta_c = \frac{P dc}{P ac} \qquad (2.3)$$

The root mean square ripple content of the output voltage of converter is

$$V_r = \sqrt{V_o^2 - V_a^2} \qquad (2.4)$$

The root mean square ripple content of the input current of converter is

$$I_r = \sqrt{I_i^2 - I_s^2} \qquad (2.5)$$

Here,

Ii =rms value of dc supply current

Is =average value of dc supply current

The ripple factor of the output voltage is

$$RF_o = \frac{V_r}{V_a} \qquad (2.6)$$

The ripple factor of the input current is

$$RF_s = \frac{I_r}{I_s} \qquad (2.7)$$

Power efficiency, which is the ratio of output power to input power, will depend on the switching losses, which, in turn, will depend on the switching frequency of the converter.In order to reduce values and sizes, the switching frequency f should be high of capacitance and inductances.

2.2 Principle Of Step Down Operation:

Principle of step down operation of dc-dc converter is given in Figure 2.3. The switch SW(chopper) is closed for time t_1 . As a result the input voltage V_s appears across the load. After t_1 the switch turns off for a time t_2 . Fig:4 shows the waveshapes of output voltage and input current. The SW can be any semiconductor device which works as switch like (1)Metal oxide semiconductor field effect transistor(MOSFET),(2)Bipolar junction transistor(BJT),(3)Gate turn-off thyristor(GTO) or (4)Insulated-gate bipolar transistor(IGBT). In practical cases, these switches have a finite voltage drop ranging from 0.5V to 2V. For avoiding complexity, we will neglect the voltage drop of these switches.

The average output voltage is

$$V_a = \frac{1}{T}\int_0^{t_1} v_o dt = \frac{t_1}{T} V_s = f t_1 V_s = k V_s \qquad (2.8)$$

The average load current is, $I_a = V_a/R = kV_s/R$,

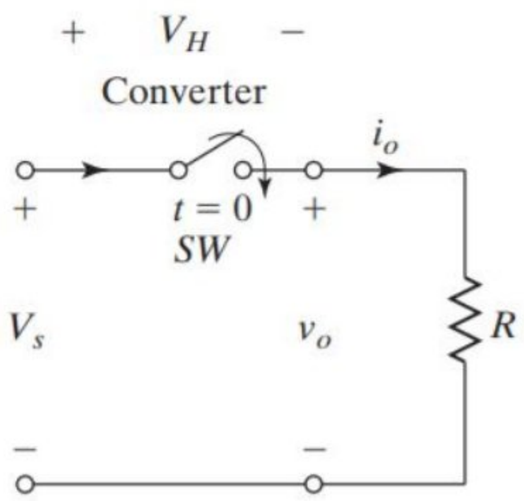


Fig 2.3:Circuit diagram of step-down operation[30]

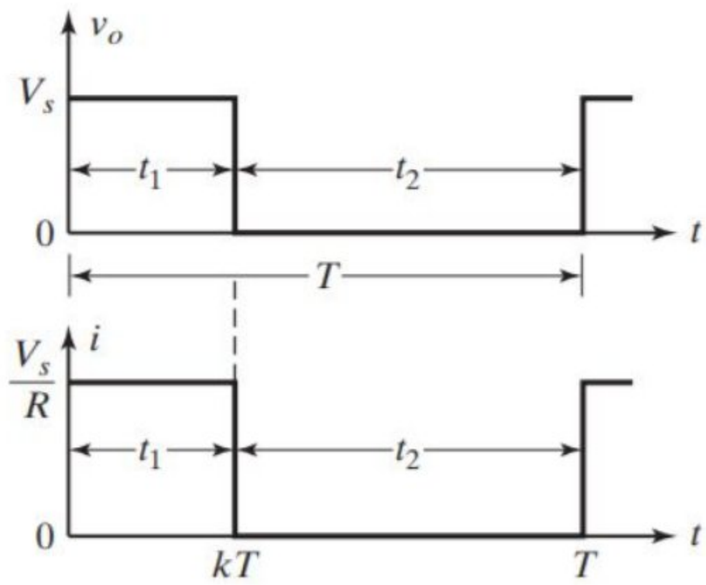


Fig 2.4:Waveform of step-down operation[30]

The above figures show a step-up converter with resistive load.

Where,

T = Chopping period;

$k = \frac{t_1}{T}$ is the duty cycle of the chopper;

f =chopping frequency.

The rms value of output voltage is

$$V_o = \left(\frac{1}{T} \int_0^{kT} v_o^2 dt \right)^{1/2} = \sqrt{k} V_s \tag{2.9}$$

Assuming that the converter is lossless, the input power to the converter is like the output power and therefore is given by

$$P_i = \frac{1}{T} \int_0^{kT} \frac{v_o^2}{R} dt = k \frac{V_s^2}{R} \tag{2.10}$$

The effective input resistance seen on the source is

$$R_i = \frac{V_s}{kV_s/R} = \frac{R}{k} \tag{2.11}$$

The above equation implies that the input resistance R_i is made a variable resistance $\frac{R}{k}$ by the converter. The divergence of the averaged input resistance to the duty cycle is shown in Figure 2.5. This should be mentioned that the switch in Fig: 2.3 may also be constructed by a BJT, a MOSFET, an IGBT or a GTO.

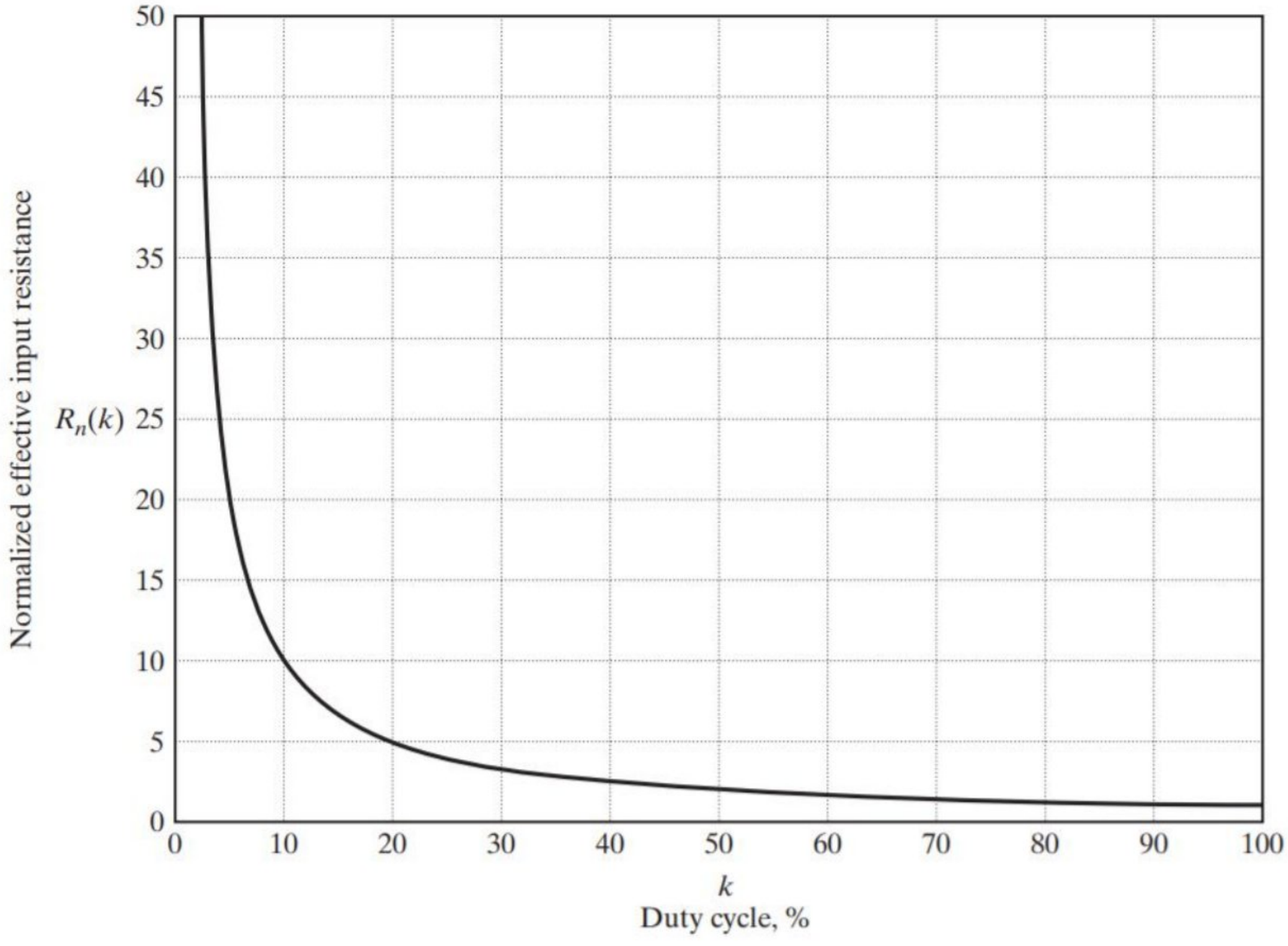


Fig 2.5:Effective input resistance against duty cycle[30]

The duty cycle k may range from zero to 1 by t1, t, or f. The output voltage Vo can thus be shifted from 0 to Vs by manipulating k, and the active power can be monitored.

1.Constant-frequency operation: Here, the switching or chopping frequency, f is kept constant. The on-time t_1 is varied. Therefore, the width of the pulse is also varied. This is known as pulse-width-modulation(PWM) control and it is used more frequently compared to other types of modulation[30].

2.Variable-frequency operation: In this operation, switching or chopping frequency is varied unlike keeping it constant like in the previous case. On time t_o or off time t_1 is kept constant. This is called variable frequency operation. To achieve high output voltage we need to vary the frequency at a wider range.But the frequency needs to be predictable. Otherwise,the design of the filter will be difficult.[30]

2.3 Generation Of Duty Cycle:

Assuming the duty cycle be k ,we can generate it by comparing with the dc reference signal v_r with a sawtooth carrier signal v_{cr} . We can define the reference signal v_r as

$$v_r = \frac{V_r}{T} t \qquad (2.12)$$

Where v_r =dc reference signal;

V_r =peak value of v_r ;

v_{cr} =sawtooth carrier signal;

V_{cr} =peek value of v_{cr} ;

T =chopping period

Carrier signal is defined as

$$V_{cr} = \frac{V_r}{T} kT = v_{cr}$$

Finally we the the duty cycle equation as

$$k = \frac{V_{cr}}{V_r} = M \qquad (2.13)$$

Here,

M =Modulation Index;

k =0 to 1 if v_{cr} is varied from 0 to V_{cr} .

The process of generating duty cycle is followed by the following steps

1. A triangular waveform with period T is generated as reference signal v_r and a dc carrier signal v_{cr} is generated for comparison purposes.
2. Then the signals are compared via a comparator. The difference $v_r - v_{cr}$ is passed through a hard limiter which helps obtaining a square-wave gate pulse of width kT. This waveform is passed through an isolating circuit. The final waveform is applied to a switching device.
3. Duty cycle k and variation in v_{cr} varies linearly with time.

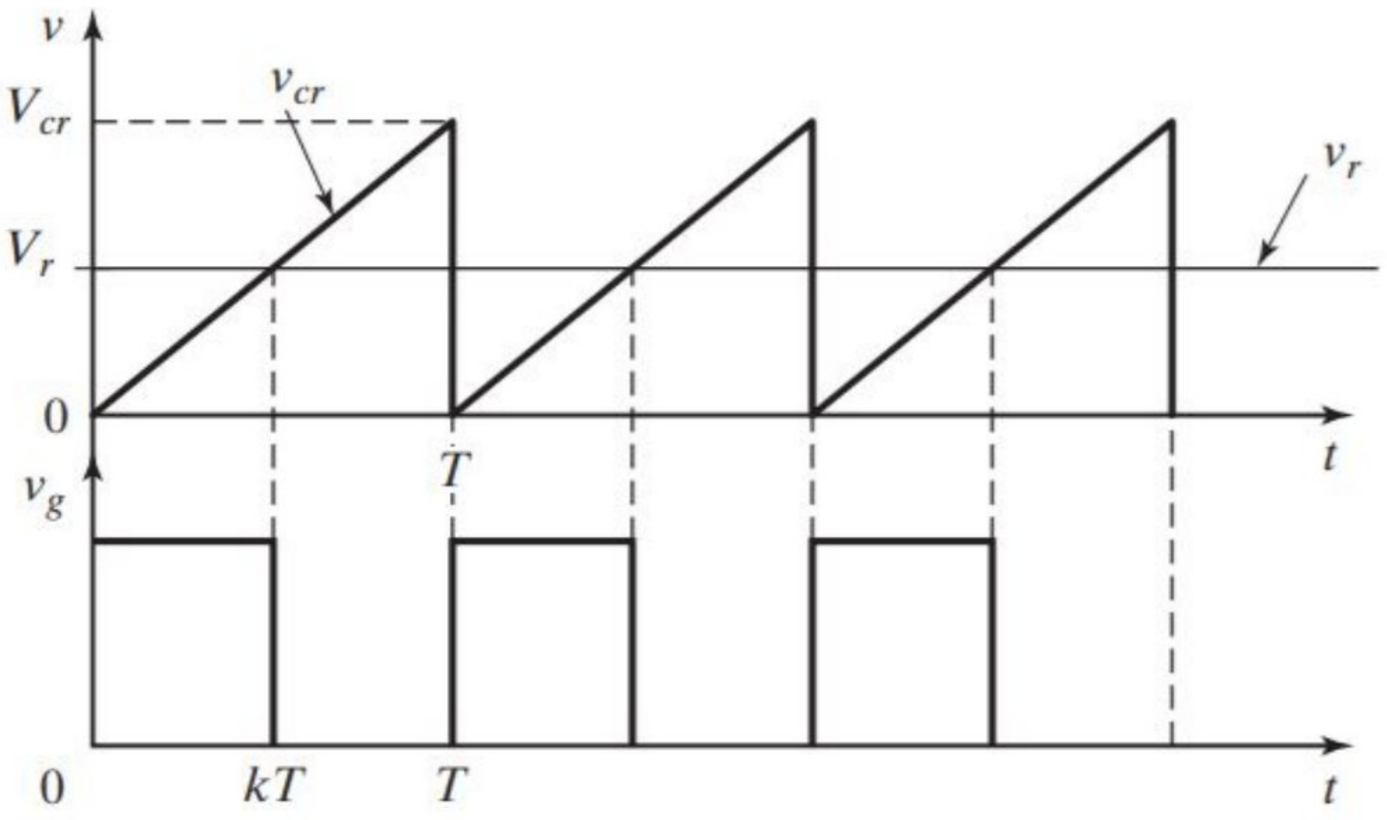
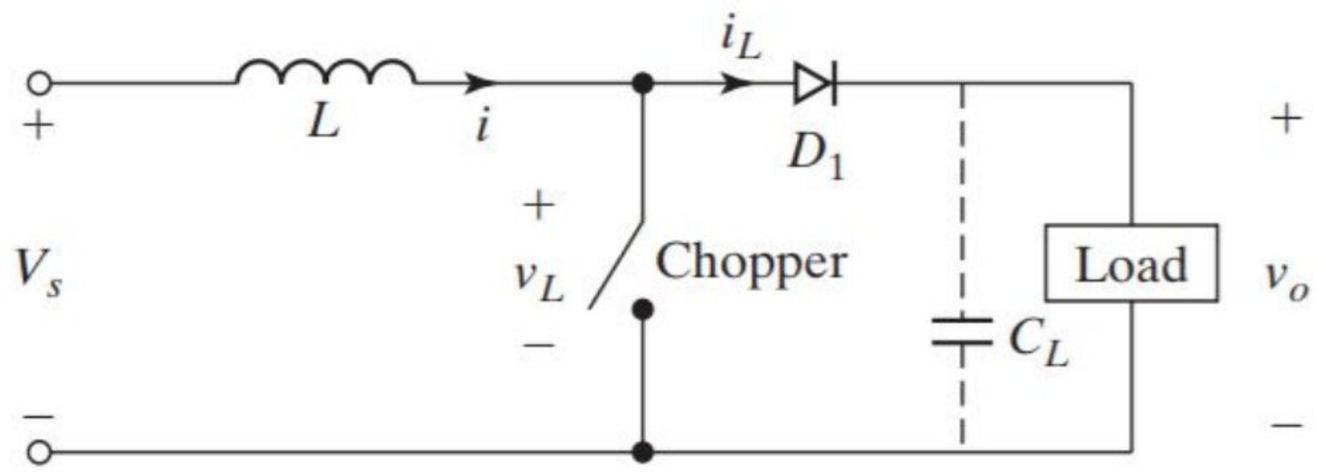


Fig 2.6: Comparison of reference signal with carrier signal[30]

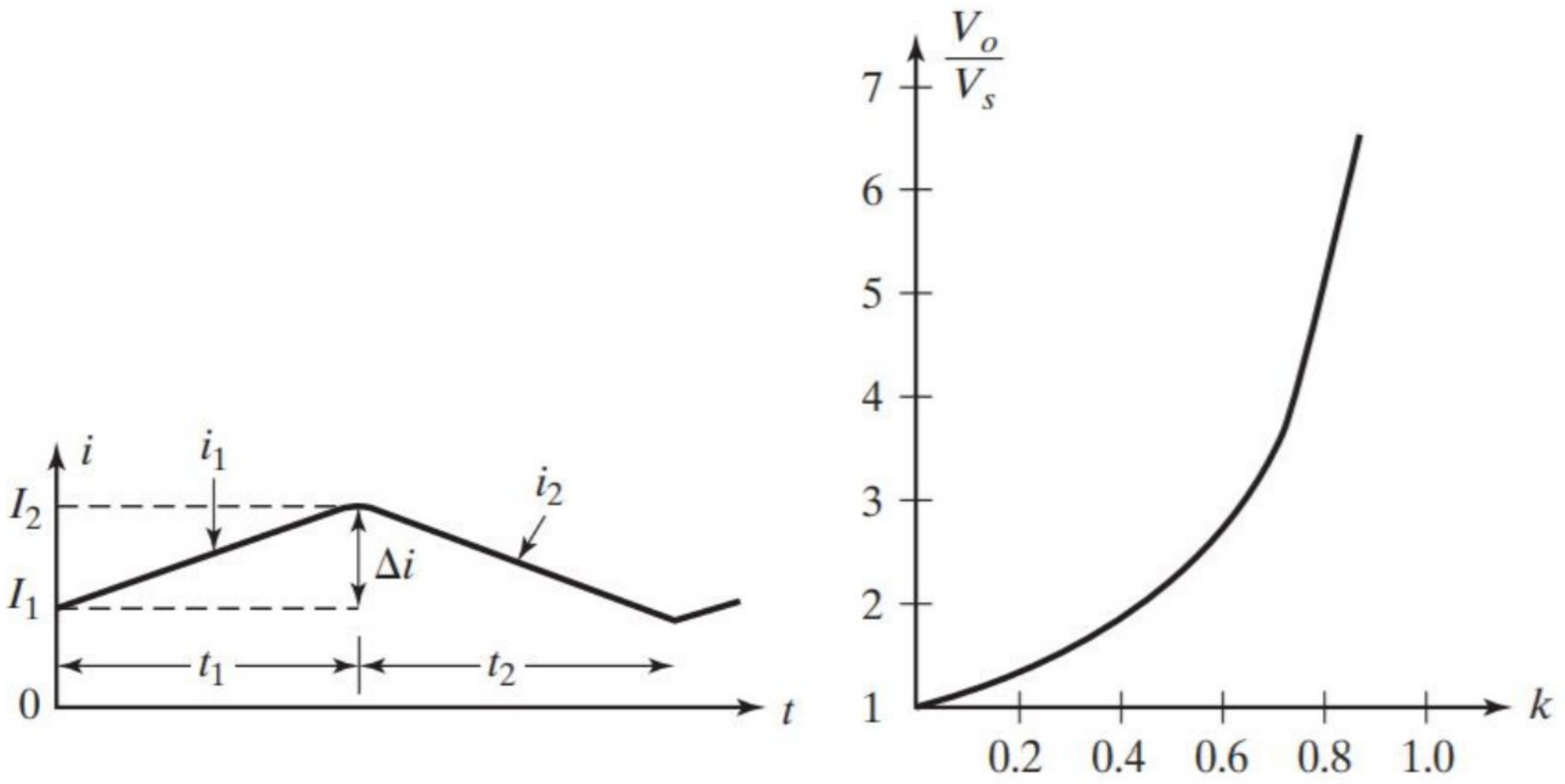
2.4 Principle Of Step-Up Operation:

A step up arrangement is shown in the following figure which can be used to step up dc voltage in a converter thereby can be used in several electronic devices applications where we need low input voltage but high output voltage.

Here,switch is closed for time t_1. Within this time inductor current rises and energy is produced which is stored in inductor L. In t_2 the switch is turned off. Then the stored energy in inductor flows through the circuit through diode D_1. The lost energy of the inductor is recovered when the switch is again turned on. If we assume that the current is flowing continuously without any interruption the figure looks like this (Fig:2.7).



(a) Step up arrangement[30]



(b)Current waveform (c)Output voltage

Figure 2.7: Arrangement of step up operation[30]

At time t_1 voltage across the inductor is

$$v_L = L\frac{di}{dt} \tag{2.14}$$

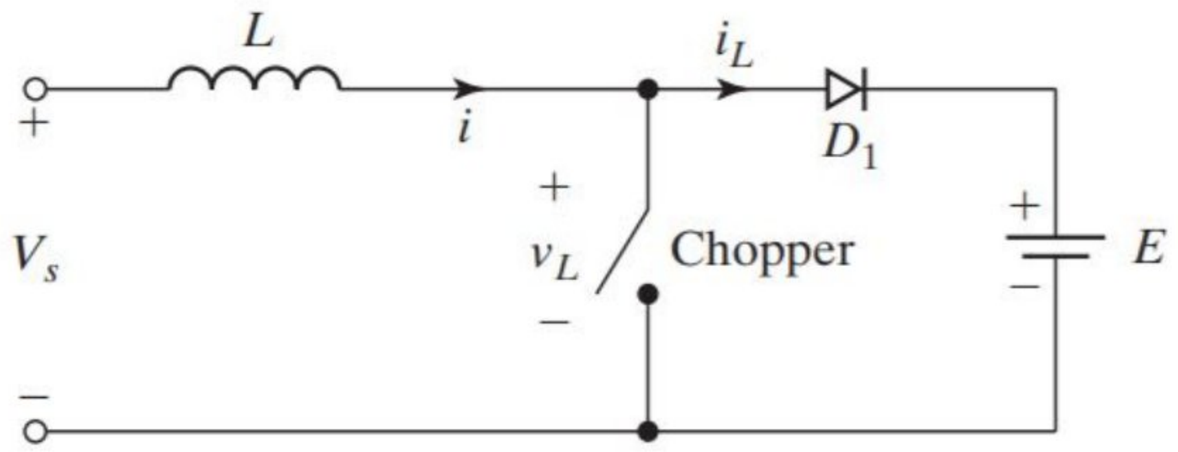
Peak to peak ripple current of the inductor

$$\Delta I = \frac{V_S}{L}t_1 \tag{2.15}$$

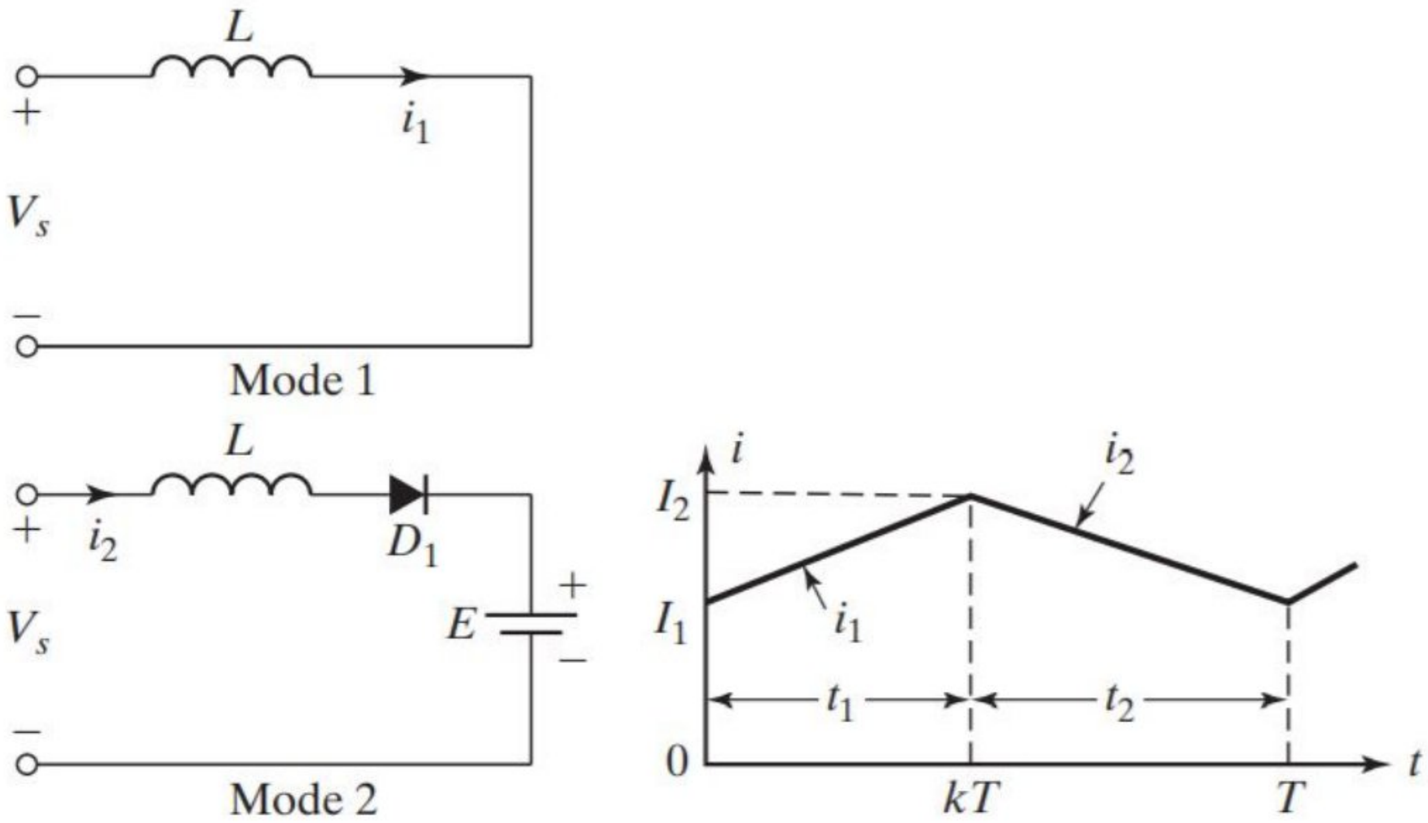
Average output voltage

$$v_o = V_s + L\frac{\Delta I}{t_2} = V_s\left(1 + \frac{t_1}{t_2}\right) = V_s\frac{1}{1-k} \tag{2.16}$$

The alternative circuit for the above operation can also be shown like the figure as follow:



(a)Circuit diagram[30]



(b) Equivalent circuits (c) Current waveforms

Figure 2.8:Arrangement of transfer of energy[30]

The above arrangement shows energy transfer from one voltage source to another. (a) shows the circuit diagram of the operation. (b) shows the equivalent circuit of mode 1 and mode 2. (c) shows the waveform of the operation.

In mode 1 ,the inductor current is defined by

$$i_1(t) = \frac{V_s}{L}t + I_1 \tag{2.17}$$

Here,

I_1 =Initial current of mode 1;

V_s =Supply voltage

The necessary condition of rising current in mode 1

$$\frac{di_1}{dt} > 0 \; or \; V_s > 0$$

The current in mode 2 is defined by

$$V_s = L\frac{di_2}{dt} + E$$

Then we get the inductor current for mode 2 as

$$i_2(t) = \frac{V_s - E}{L}t + I_2 \qquad (2.18)$$

Here, I_2 =Initial current of mode 2

The system must be stable and the current falls for a stable condition which can be given by

$$\frac{di_2}{dt} < 0 \; or \; V_s < E$$

The above condition must be met to prevent unstable conditions and rising current abruptly.

Therefore the final condition to be met is

$$0 < V_s < E \qquad (2.19)$$

2.5 Switching Mode Regulators:

Switching mode regulator is a kind of circuit which is used for transferring energy from input to output. The main components of switching mode regulator are power switch, inductor and diode. They can be rearranged to generate different kinds of outputs like step-up,step-down or inverter.

Dc converters can be used as switching mode regulators where it converts unregulated dc voltage to regulated dc output voltage. This is achieved by keeping the frequency fixed at turn off and turn on period which is also known as PWM. The switching devices used in this

operation are generally BJT,MOSFET or IGBTs. The elements of switching mode regulators are shown in Fig 2.9.

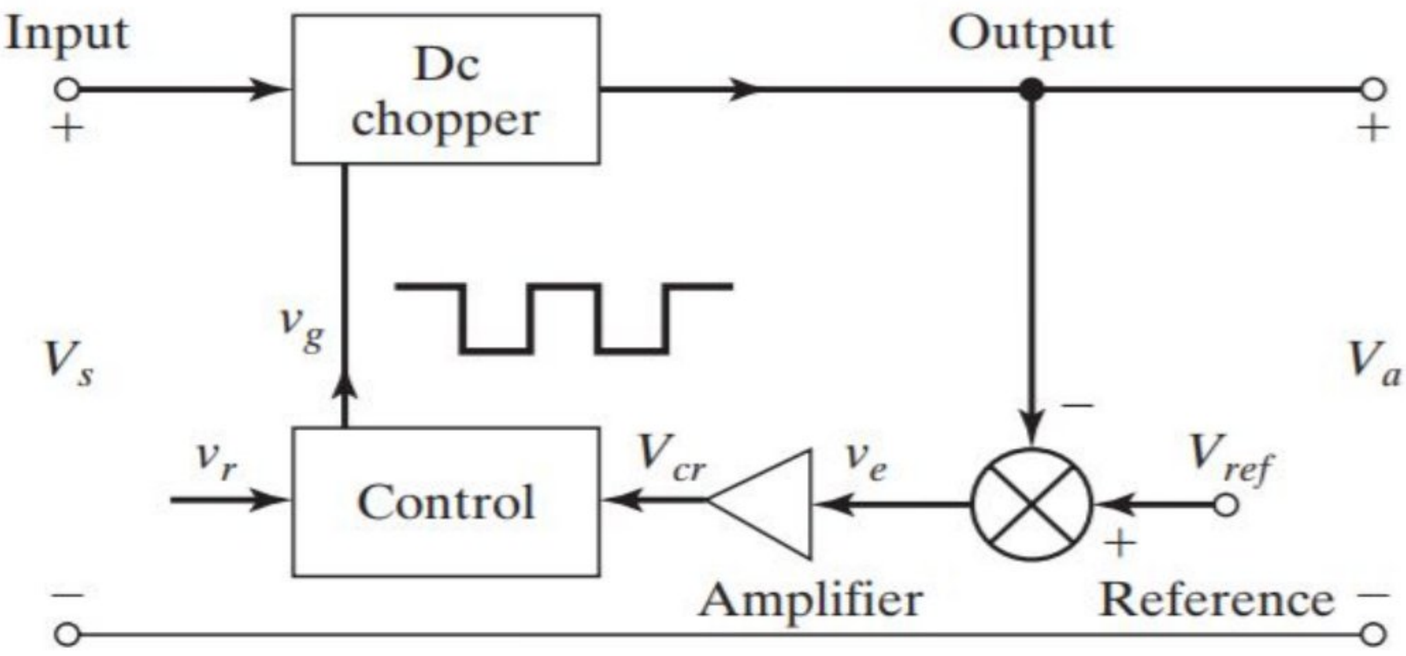


Fig 2.9:Elements of switching-mode regulators[30]

We can see from the figure that the output of the circuit contains harmonics. LC filter is used to reduce the ripple. We can get switching regulators as integrated circuits which are available in the market by different model names. The switching frequency can be determined by modifying the values of R and C. To maximize the efficiency of the converter the minimum oscillator period should be 100 times longer than transistor switching time(Example:If switching time of a transistor is 0.4μs,then the oscillator period would be minimum 40μs. This gives a maximum oscillator frequency of 25kHZ. The transistor switching loss causes

this limitation and thereby reduces efficiency. The core loss of inductors also plays a huge role in this regard.

There are four basic topologies of switching regulators:

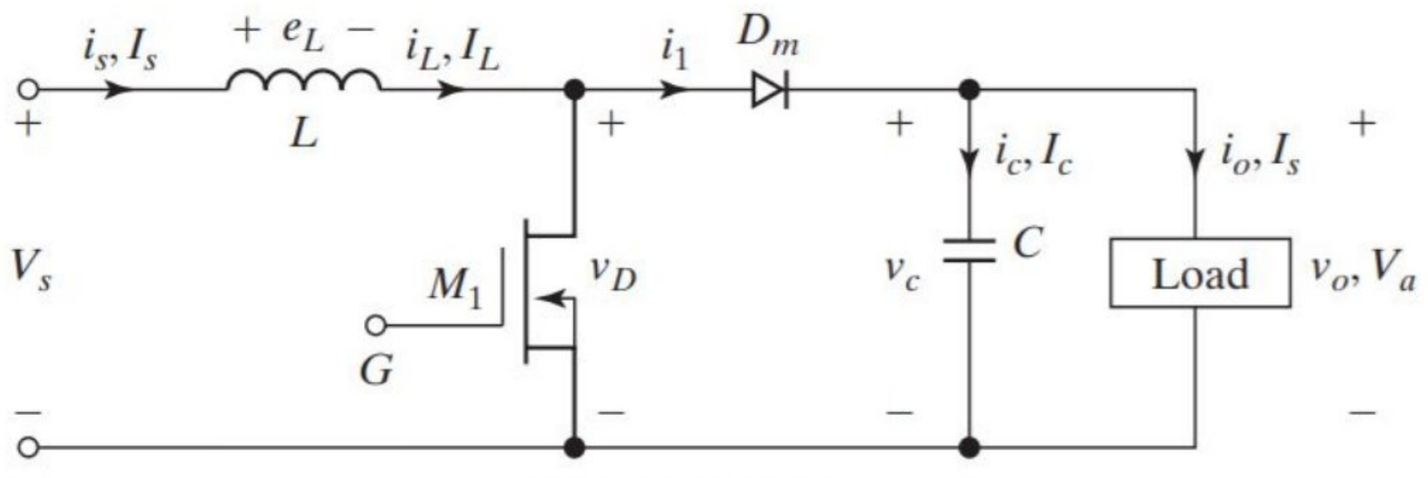
1.Buck regulators **3.**Buck-boost regulators

2.Boost regulators **4.**Cúk regulators

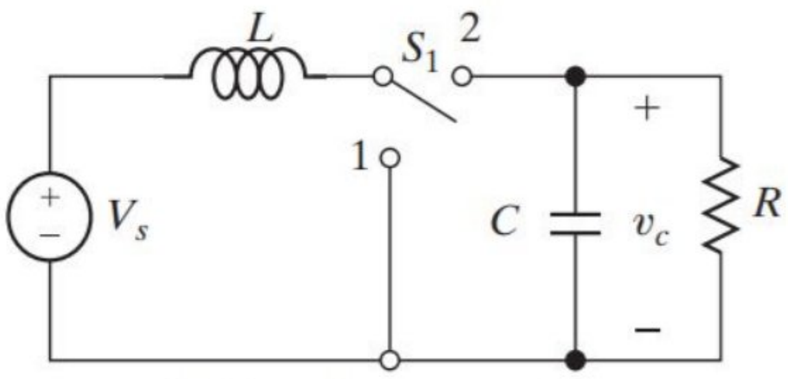
But we will solely focus on Boost converter as we are working on step-up boost converter.[30]

Boost Regulators

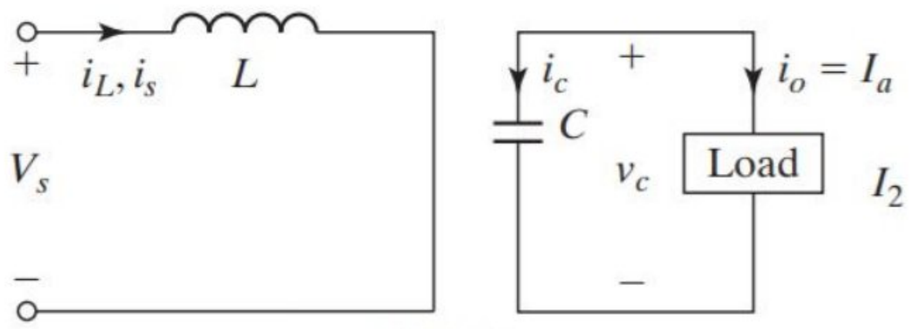
In boost regulator output voltage is greater then input voltage. That's why it is called a boost regulator. It is suitable for electronics devices which requires low voltage as input but for functioning it requires high output voltage. (a) shows the circuit diagram of the boost regulator. Here, M1 is the transistor which works as a controlled switch and diode D_m works as an uncontrolled switch. (a) shows boost converter representation with power MOSFET.In (b) we see an alternative circuit diagram where switch is used. The circuit operation is divided into two modes. Mode 1 begins at t=0 when switch M1 is turned on. The input current rises with time. It passes through inductor L and transistor Q_1.At t=t1,M1 is switched off and thus mode 2 starts. Previously, the current was flowing through the transistor. Now in mode 2, it will flow through L, C, load, and diode Dm. Until the next cycle starts the inductor current keeps falling. To compensate for the current loss,stored energy of the inductor L is transferred to the load. The equivalent circuit is shown in (b). The waveforms are shown in (c).



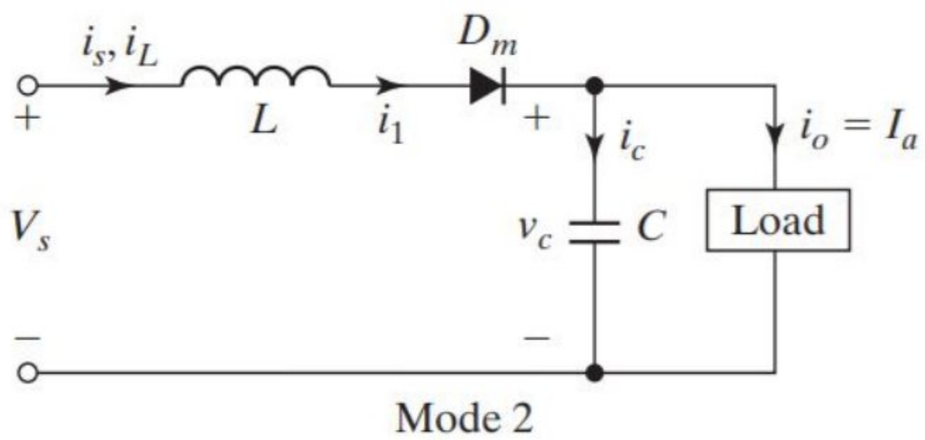
(a) Circuit diagram



(b) Switch representation



Mode 1



Mode 2

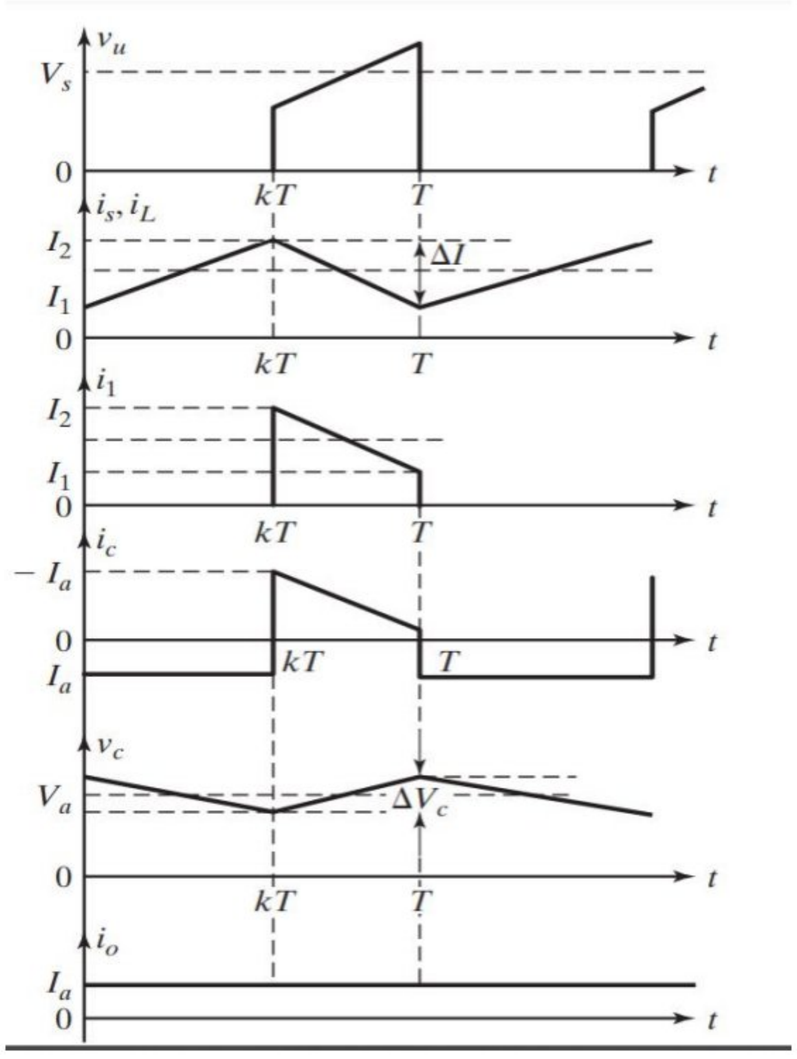


Fig2.10:Boost converter circuit diagram and waveforms[30]

Assuming inductor current I_2 is greater than I_1 in time t_1 we get

$$V_s = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \tag{2.20}$$

or

$$t_1 = \frac{\Delta I L}{V_s} \tag{2.21}$$

When in inductor current falls in time t_2 ,

$$V_s - V_a = -L\frac{\Delta I}{t_2} \tag{2.22}$$

or

$$t_2 = \frac{\Delta I L}{V_a - V_s} \tag{2.23}$$

From (2.20) and (2.22) we get,

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L} \tag{2.24}$$

Now,we substitute $t_1 = kT$ and $t_2 = (1-k)T$ .This yields to average output voltage

$$V_a = V_s\frac{T}{t_2} = \frac{V_s}{1-k} \tag{2.25}$$

From (2.25) we get

$$(1-k) = \frac{V_s}{V_a} \tag{2.26}$$

Substituting $k = t_1/T = t_1 f$ into (2 .26) we get

$$t_1 = \frac{V_a - V_s}{V_a f} \tag{2.27}$$

Considering $V_s I_s = V_a I_a = V_s I_a(1-k)$ we get average input current as

$$I_s = \frac{I_a}{1-k} \tag{2.28}$$

Peak-to-peak ripple current

$$\Delta I = \frac{V_s k}{fL} \tag{2.29}$$

Peak-to-peak capacitor ripple voltage.

$$\Delta V_c = \frac{I_a k}{fC} \tag{2.30}$$

Condition for continuous inductor current and capacitor voltage.

If I_L is the average inductor current,for continuous conduction in critical condition the inductor ripple current is $\Delta I = 2I_L$.

From equation (2 .25) and (2.29) we get

$$\frac{kV_s}{fL} = 2I_L = 2I_s = \frac{2V_s}{(1-k)^2}$$

By this the critical value of inductor L_c can be found

$$L_c = L = \frac{k(1-k)R}{2f} \tag{2.31}$$

Considering V_c as the average capacitor voltage,for continuous condition at critical condition capacitor voltage will be $\Delta V_c = 2V_a$. Using (2.30),we get

$$\frac{I_a k}{Cf} = 2V_a = 2I_a R$$

The final equation of critical value of capacitor C_c as

$$C_c = C = \frac{k}{2fR} \tag{2.32}$$

III. Switching of Converter

A DC/DC converter is a power supply class that transforms a direct current (DC) source from one voltage level to another. There are two types of DC/DC converters available: linear and switched. A linear DC/DC converter requires a resistive voltage drop to produce and change the output voltage, a switched DC/DC transforms the input energy continuously and then releases it to the output at a separate voltage. Storage may be either in a magnetic field component such as an inductor or a transformer, or in an electrical field component such as a capacitor. Transformer-based converters create insulation between input and output.

Switch mode converters have three major advantages:

• The efficiency of the power transfer is much greater.

• Since the switching frequency is higher, passive parts are smaller and lower losses make thermal control simpler.

• The energy stored by the inductor in the switching regulator can be converted into output voltages that can be lower than the input (step-down or buck), larger than the input (boost) or buck-boost with reverse polarity (inverter).

A linear converter will only produce a voltage lower than the input voltage, unlike a switching converter. Although there are many benefits, DC/DC converter conversion still has some drawbacks.

3.1 Hard Switching:

Transistors are usually three terminal devices. The terminals can be labeled as base, collector and emitter or gate, source and drain depending on the type of transistor. Any amount of current at the base terminal can regulate a much bigger value of current between the collector and emitter. Also the current between drain and source can be controlled by a little amount of voltage at the gate terminal.

The transition time required to reach the next stage is very short when the transistor is switched on or off, but it is not instantaneous. Both voltage and current are applied to the device at on-off transformations. Collector current and collector-emitter voltage shift dramatically with hard switching, creating noise and loss of switching. At the convergence of the voltage and current waveforms, switching losses arise. Basically when the gate voltage is applied, the voltage across the transistor starts to rise and the current starts to fall or vice versa. During these transitions of the voltage and current an overlap occurs between the current and voltage waveforms. This overlap of voltage and current is basically power loss which can also be called switching loss. A significant proportion of power converter losses are blamed for switching losses.

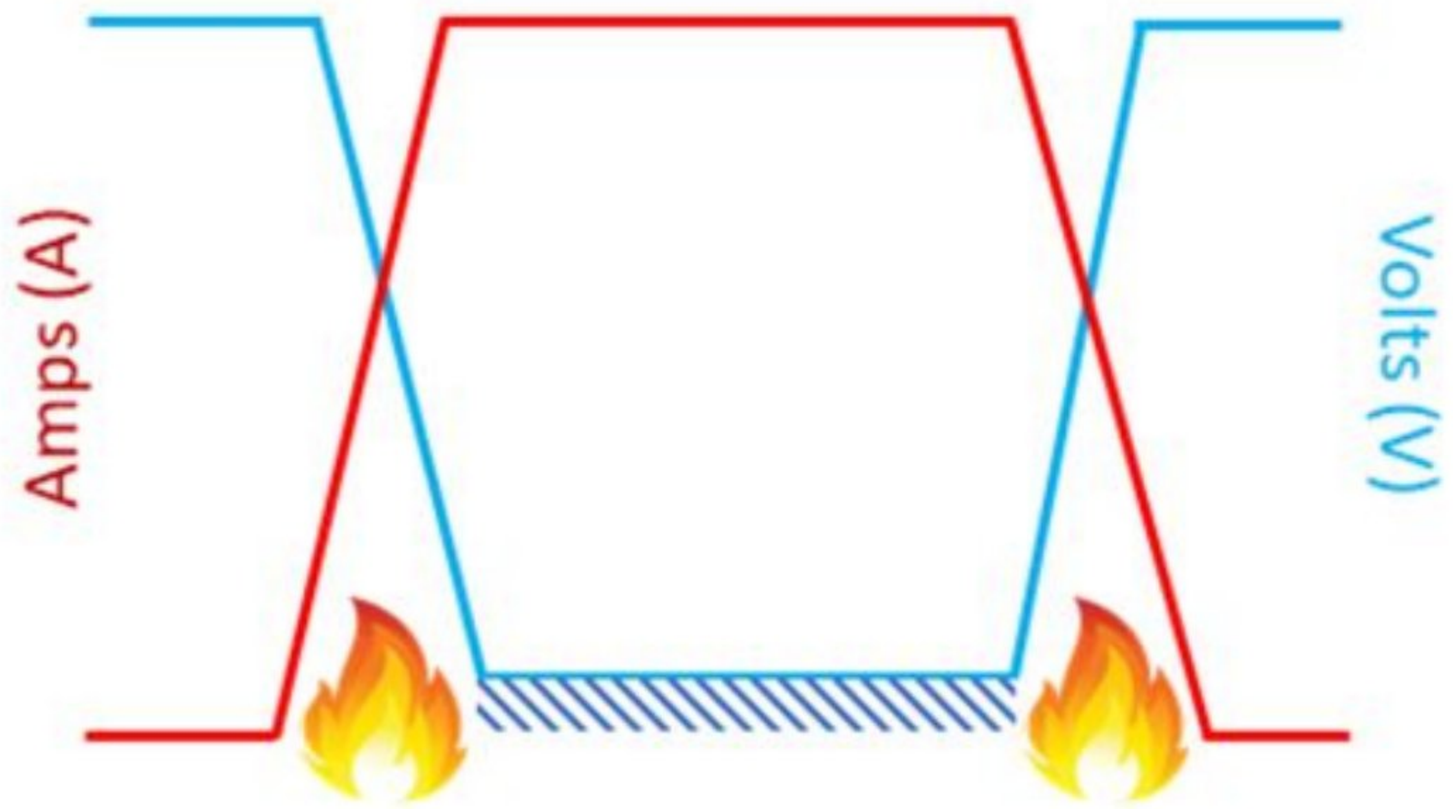


Figure 3.1: Traditional Hard Switching. [31]

It is understood that hard switching is difficult on transistors and shortens their useful life. For basic switches, inverters for motor drives, and switched-mode power supply applications, hard switching is used.

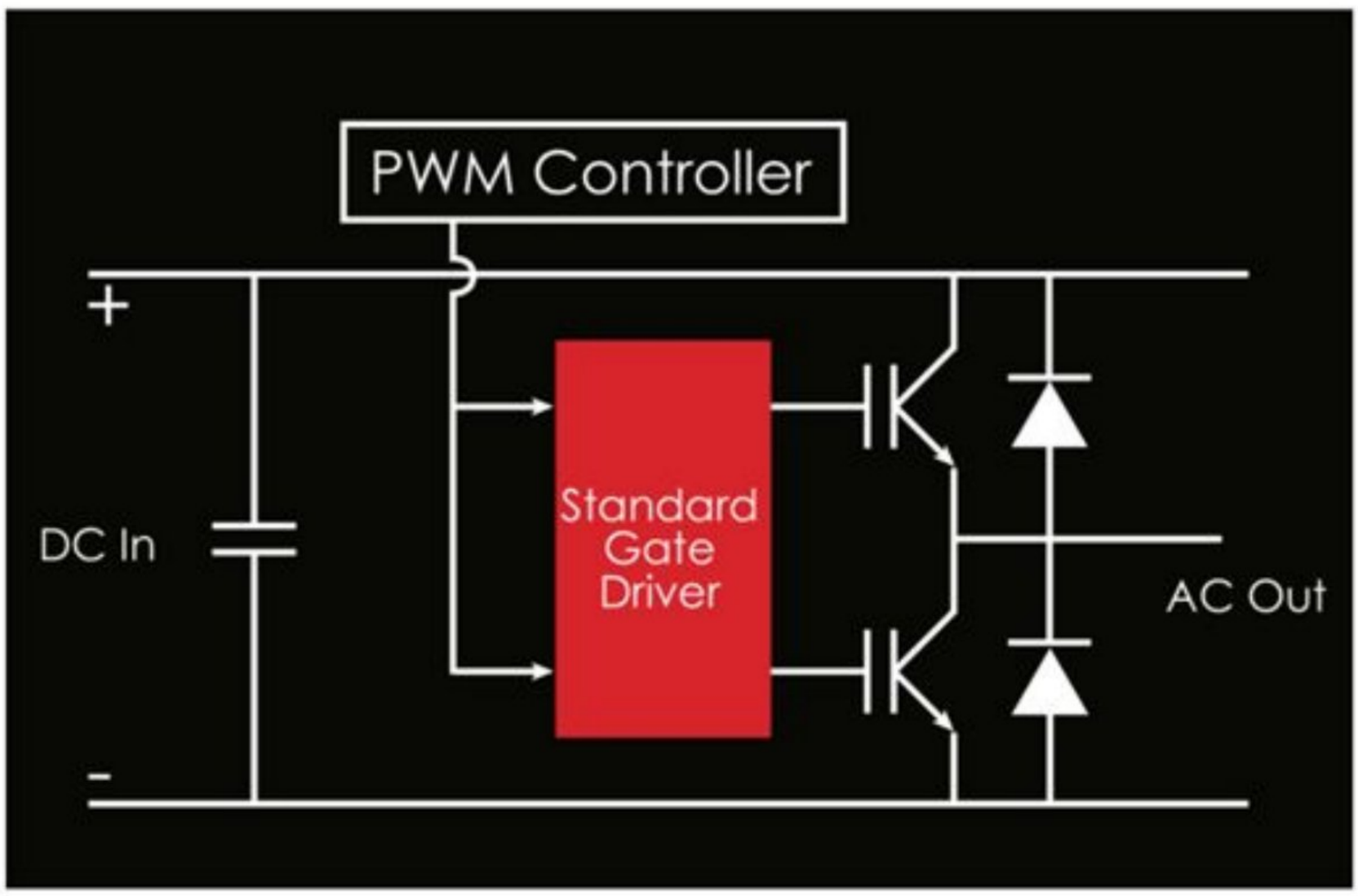


Figure 3.2: Hard Switched Architecture. [31]

Hard switching is easy to grasp and is thus nearly universally used outside of the low power DC to DC space of power converters. Hard switching was considered low-cost since to drive the transistors between states, only a small number of other components are needed. In fact, hard-switching is costly and inefficient at the system level. Hard-Switching has many well-known pitfalls, the greatest of which is that of shifting losses. Hard-switching power converters must reconcile the need for higher switching frequencies to meet the required system efficiencies with an appropriate system loss. This implies in reality that processes of high performance are built to steadily shift towards efficiency. The performance benefits are obtained from decreased cumulative switching cycles in each transistor (and hence cumulative switching losses) in the conversion phase. The downside to this strategy is that designers need to expand the size of other elements needed in the system to maintain the power between the longer switching intervals of the transistor for a prolonged period of time. [31]

3.2 Soft Switching:

Soft switching is intended to remedy some of the problems that occur during hard switching. The idea is basically to shift the rate of changes of the current and the voltage across the transistor such that they will not overlap each other or at least there will be a minimum overlapping. Here the transition gets operated in such a way that the voltage across the transistor will drop before the current across it starts to rise so that no convergence occurs. It is an ideal case as known as true soft switching. Usually when the overlapping is minimum it is called pseudo soft switching.

Usually three types of resonance circuit are used for soft switching to transform a system on and off at zero current or voltage to minimize the intersection of their waveforms:

- Lossy Snubber
- Passive Lossless Snubber
- Active Lossless Snubber

3.3 Zero Voltage Switching (ZVS):

A useful approach for enhancing voltage-converter performance is quasi-resonant switching, but conditions can be further improved by introducing full soft switching. Until the MOSFET is turned on or off, the voltage falls to zero (rather than a minimum) throughout soft switching, eradicating any convergence between voltage and current and minimizing losses. An added benefit is that electromagnetic interference is reduced by the steady switching waveforms.

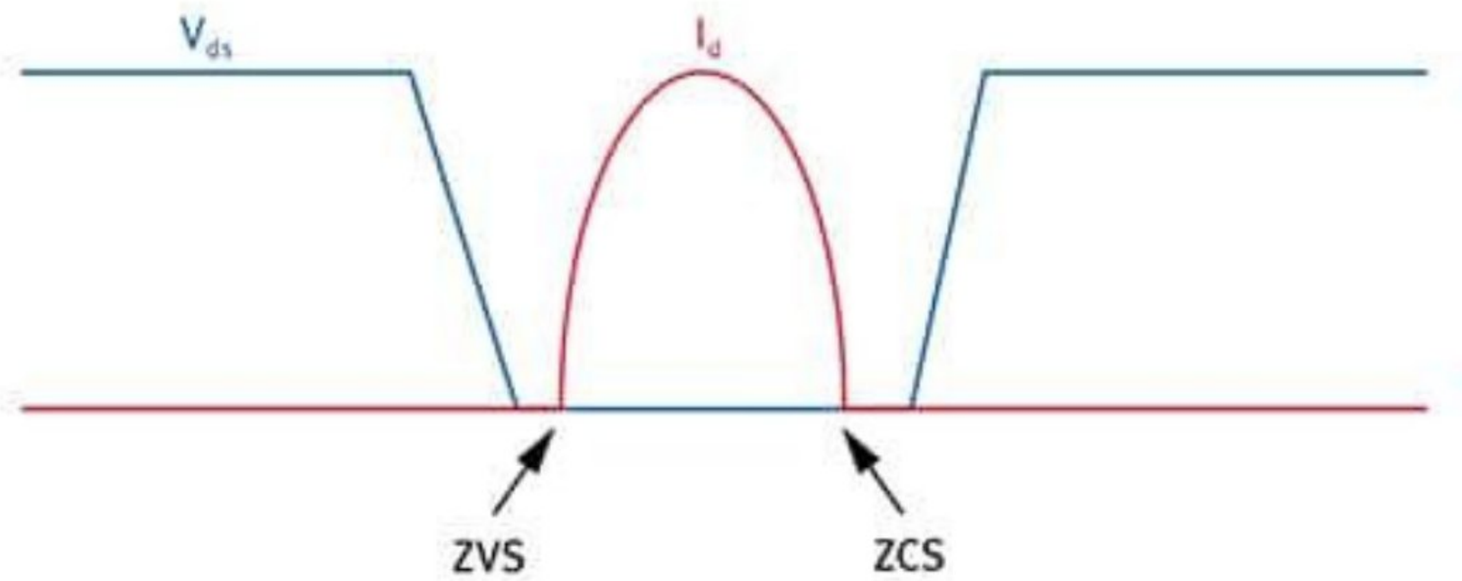


Figure 3.3: Soft-switching MOSFET current and voltage waveform (Courtesy of Infineon Technologies). [32]

The easiest way to describe Soft Switching (ZVS), during the MOSFET on-time PWM migration, is to use the "resonant" switching transitions. The approach may be considered to be PWM power using a constant off-time control which varies the converting frequency, or on-time to preserve the regulation of the output voltage. This is equivalent to a constant frequency conversion using a dynamic duty cycle over a single unit of time.

By modifying the efficient duty cycle, changing the converter frequency, the control of the output voltage is obtained. The L-C circuit of the converter reverberates during the ZVS switch off-time, navigating the voltage through the switch from zero to its maximum and back down again to zero when the switch can be restarted, and enabling lossless zero voltage switching. MOSFET transformation losses are zero, irrespective of frequency and voltage, which represents huge power savings and considerable efficiency improvement. These features made ZVS a good high-frequency, high-voltage converter technology. [32]

3.4 Zero Current Switching (ZCS):

Soft switching will reduce some of the switching loss mechanisms and likely decrease the electromagnetic interference generation. At zero current, the transistor turn-off transition happens. The transformation loss incurred by IGBT current tailing and by stray inductances is reduced by zero current switching. It can also be used for switching SCRs. [33]

IV. Operation of The Converter

The analogous circuit of the proposed converter is depicted in Fig.4.1, where an ideal transformer with a turn ratio of N_p:N_s:N_t represents the coupling inductor and a magnetizing inductor L_m as well as the main leakage inductor L_{lk}.

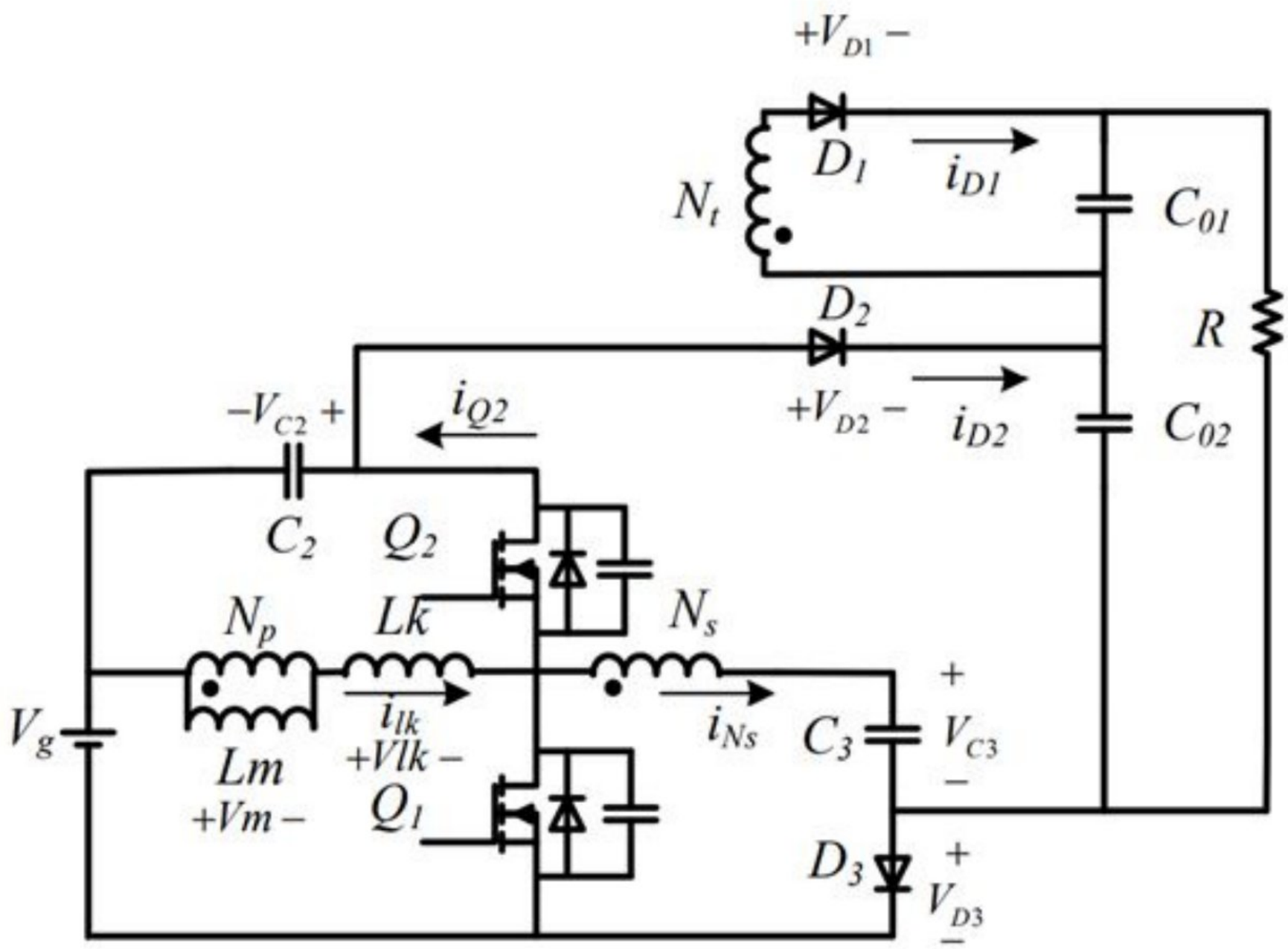


Figure 4.1: The equivalent diagram of the described converter circuit.[29]

Two switches, three diodes, and four capacitors are the main components of the converter circuit. Switch Q_2's body diode conducts before the switch is turned on, which leads switch Q_2 to realize ZVS automatically. ZVS is made for the switch Q_1 with the energy contained in the leakage inductor. Both switches will incorporate ZVS in a broad variety, helping to

minimize the loss of switching and ensuring high performance operation at higher switching frequency. Moreover, the C_2 capacitor and the Q_2 switch may both serve as an active clamp that suppresses the Q_1 turn-off voltage surge.

Such observations are made in order to simplify the study of the circuit:

- All capacitors are large enough, thus, during one switching cycle their voltages can be seen as constant.
- All the power devices of the circuit are considered ideal.
- The turn ratio of the coupling inductor $1:N_s:N_t$ shall be defined as $N_p:N_s:N_t$. The coupling coefficient k is identical with $L_m/(L_m+L_k)$.

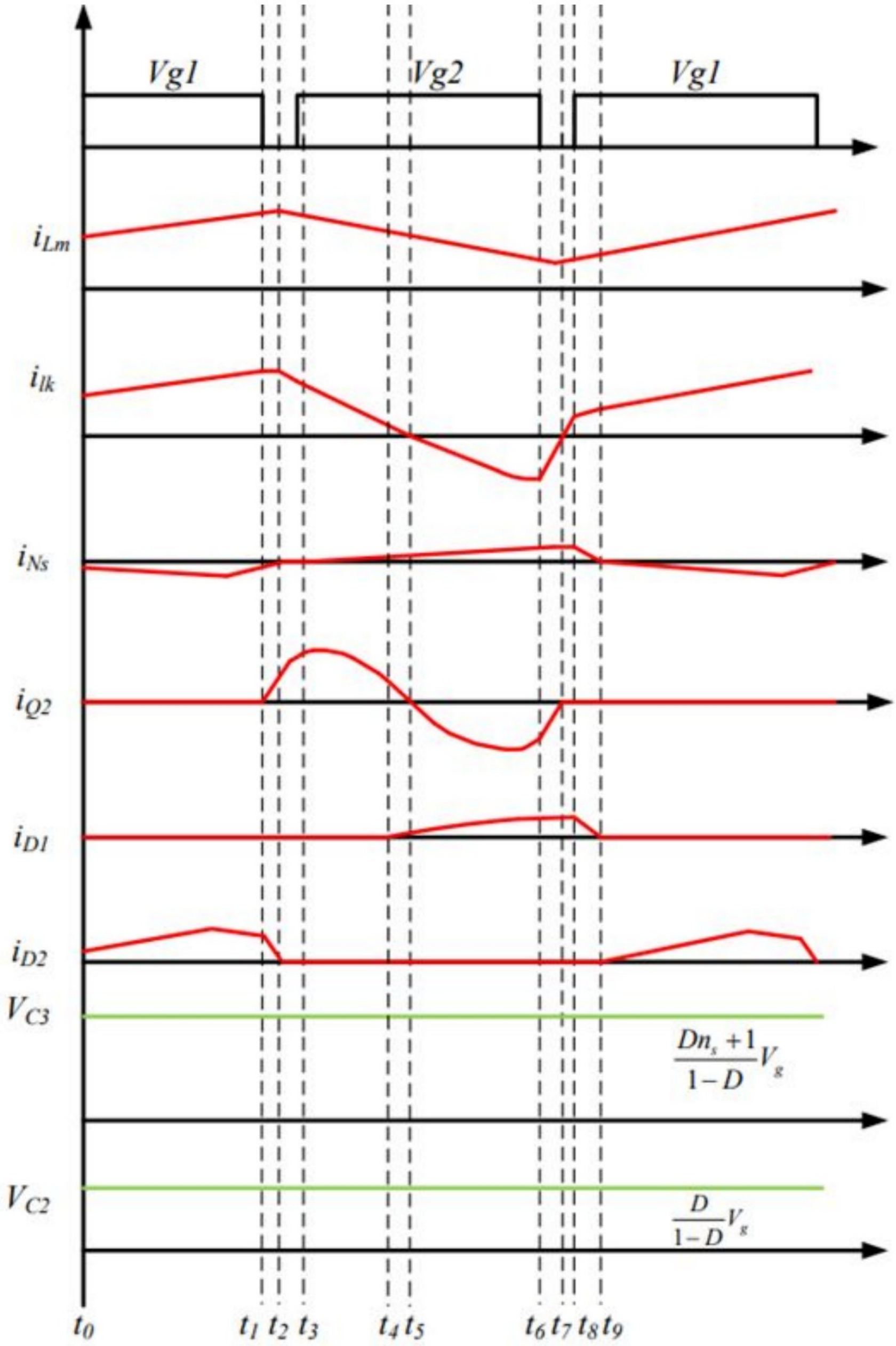


Figure 4.2: Theoretical waveform diagrams of the main device.[29]

4.1 Operating Principle:

The converter's theoretical waveform diagram is represented in Fig. 4.2 based on the above hypotheses. V_{g1} and V_{g2} are the gate signals of the Q_1 and Q_2 switches, respectively in the waveform. In one switching period there are 9 operating modes; simplified equivalent circuits are given in Fig.4.3 for each mode. The modes of operation are as follows:

Mode 1 ($t_0 - t_1$):

The Q_1 switch is enabled in this mode as the Q_2 switch is disabled. Diode D_2 is conducted as D_1 and D_3 remain out of conduction. The current path is displayed as Fig. 4.3 (a).

The V_g power supply charges the L_m inductor and the L_{lk} leakage inductor. The current magnetizing iLm and leakage inducer current range are steadily increasing. The $V_{\_g}$, C_2, C_3 and the secondary winding voltage are in series for the C_{02} output condenser. C_{01} output condenser provides load power. The current of the magnetizing inductor can be shown in the following: [29]

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{Lm}}{L_m}(t - t_0) \tag{4.1}$$

Where,

$$V_{Lm} = \frac{L_m}{L_m + L_k} V_g = kV_g \tag{4.2}$$

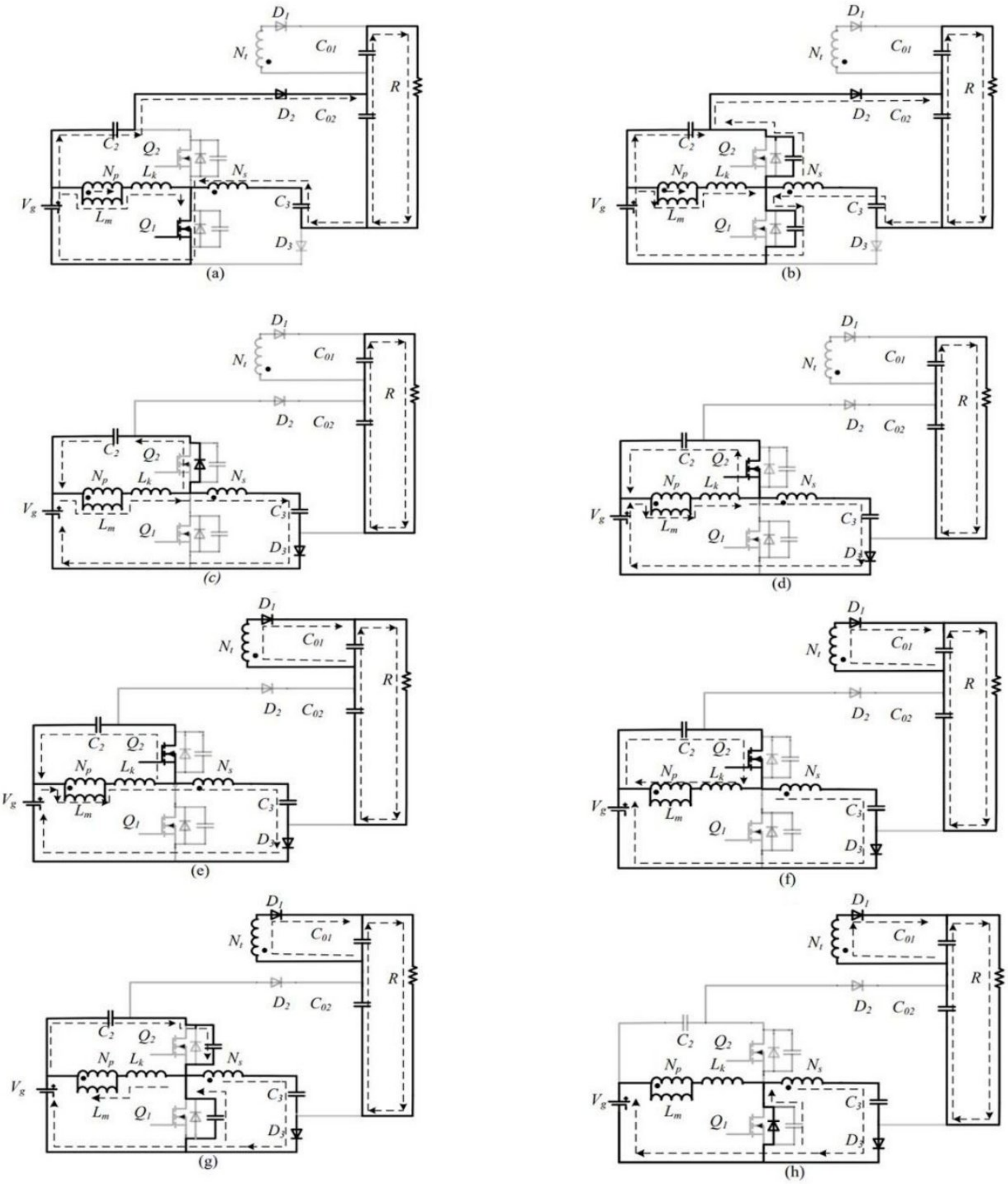


Figure 4.3: Different modes of the proposed converter during one switching period. (a) Mode 1 ($t_0 - t_1$). (b) Mode 2 ($t_1 - t_2$). (c) Mode 3 ($t_2 - t_3$). (d) Mode 4 ($t_3 - t_4$)(e) Mode 5 ($t_4 - t_5$). (f) Mode 6 ($t_5 - t_6$). (g) Mode 7 ($t_6 - t_7$). (h) Mode 8 ($t_7 - t_8$). (i) Mode 9 ($t_8 - t_9$). [29]

$$i_{Lk}(t) = i_{Lk}(t_0) + \frac{V_g - V_{Lm}}{L_k}(t - t_0) \tag{4.3}$$

The voltage of the C_{02} output capacitor can be derived as follows [29]:

$$V_{C02}(t) = V_{C3}(t) + V_g(t) + V_{C2}(t) + V_{Ns}(t) \tag{4.4}$$

Mode 2 ($t_1 - t_2$):

This mode starts with $t=t_1$ when the Q_1 switch is switched off. The current of the leakage inductor starts to charge the parasite capacitor Q_1 and discharge the parasite capacitor Q_2 . The voltage at drain sources in the Q_1 rises from 0 to V_g+V_{C2} and the voltage at drain sources in the Q_2 decreases from V_g+V_{C2} to 0.

The $V_{ds}.Q_1$ drain-source voltage and the i_{lk} leakage inductor current are obtained by [29],

$$V_{ds.Q1} = V_g(1 - cos\ (\omega_1(t - t_1))\ ) + i_{lk}(t_1)Z_1 sin\ (\omega_1(t - t_1)) \tag{4.5}$$

$$i_{lk}(t_1) \approx i_{lk}(t_1)\, cos\ (\omega_1(t - t_1))\ + \frac{V_g - V_{ds.Q1}}{Z_1} sin\ (\omega_1(t - t_1)) \tag{4.6}$$

Where, $\omega_1 = 1/\sqrt{2C_{OSS}(L_m + L_k)}$ & $Z_1 = 1/\sqrt{(L_m + L_k)/2C_{OSS}}$.

The C_2, C_3 and secondary winding voltage source begin to charge the C_{02} output capacitor in series. The load is provided with energy by the C_{01} output capacitor. D_2 inherently gets disabled at the end of mode.

Mode 3 ($t_2 - t_3$):

If the current i_{D2} is null, this phase begins. At the same moment, the drain-source voltage of Q_1 approaches V_g+V_{C2} and the body diode of the switch Q_2 begins to operate. The voltage spike of the Q_1 switch can be absorbed by the C_2 capacitor. Magnetizing inductor L_m, leaked inductor L_{lk}.

And the C_2 switched capacitor forms a resonant circuit and the C_2 switched capacitor starts charging around the same time as the C_3 switched capacitor also starts charging, as seen in Fig.4.3(c). Charging current can be determined as follows for the switched capacitor C_2 [29]:

$$i_{C2}\ (t) \approx i_{lk}\,(t_2)\,cos\ (\omega_2\,(t-t_2))\ + \frac{V_{Lk}(t)}{Z_2} sin\ (\omega_2\,(t-t_2)) \qquad (4.7)$$

Where, $\omega_2 = 1/\sqrt{C_2(L_m + L_k)}$ & $Z_2 = 1/\sqrt{(L_m + L_k)/C_2}$

Q_2 should be switched on until the path of resonant current i_{C2}(t) reverses in order to obtain ZVS for the Q_2 transition.

Mode 4 ($t_3 - t_4$):

The gate signal for Q_2 at t_3 is high. The body diode of the transition Q_2 was executed prior t_3. The Q_2 switch thereby switches on under the state of ZVS. The routes of the currents are shown in Fig. 4 (d). In order to charge C_3, the input voltage source, the magnetizing inductor L_m, leakage inductor L_{lk} and the secondary winding are in series. The magnetizing inductor Lm and the leakage inductor L_{lk}, respectively, charge C_2. The C_{01} and C_{02} output capacitors provide the load with electricity.

Mode 5($t_4 - t_5$):

This phase begins when the diode D_1 is conducting. C_3 continues to be charged in series by the input voltage source, the magnetizing inductor L_m, leakage inductor L_{lk} and the secondary winding. The magnetizing inductor L_m and the leakage inductor L_{lk} charge C_2 simultaneously.

Mode 6 ($t_5 - t_6$):

This mode begins when the i_{lk} reaches zero. Hold on with D_1 and D_3. The present course of the i_{lk} varies during this interval. The magnetizing inductor L_m, the leakage inductor L_{lk}, charges the energy contained in the switched capacitor C_2. At the same time, the switch

capacitor C_3 and output capacitor C_{01}, respectively, are charged by winding N_s and N_t. This mode stops when the Q_2 switch is deactivated.

Mode 7 ($t_6 - t_7$):

The mode begins at t_6 when the Q_2 key is deactivated. During this point, a new resonant circuit is created by the leakage inductor L_{lk} and the parasitic capacitors of switches Q_1 and Q_2, and the parasitic capacitor of switch Q_1 begins to discharge, as shown in Fig.4.3 (g). The parasitic capacitor of the Q_2 switch continues to charge at the same time. Since the switch's parasitic capacitor is quite thin, the Q_1 drain source voltage is expeditiously declining. The Q_1 drain-source voltage can be extracted as follows [29]:

$$V_{ds.Q1} \approx V_d - \left(V_d - V_{ds.Q1}(t)\right) cos\ (\omega_3 (t - t_6)) + i_{lk}\ (t_6) Z_3 sin\ (\omega_3 (t - t_6)) \quad (4.8)$$

Where, $V_d = V_g + \left(\frac{V_g - V_{C3}(t)}{1+n_s}\right)$, $\omega_3 = 1/\sqrt{2C_{OSS}L_k}$ & $Z_3 = 1/\sqrt{L_k/2C_{OSS}}$

The phase stops when the Q_1 drain-source voltage reaches zero. The energy stored in the leakage inductor in this mode should be greater than the energy stored in the parasitic capacitor of the Q_1 switch in order to sense the ZVS of the Q_1 switch. Thus the, the prerequisite for achieving the ZVS of Q_1 is as follows [29]:

$$L_{lk} \geq \frac{C_{OSS} V_{ds.Q1}^2(t_6)}{i_{lk}^2(t_6)} \quad (4.9)$$

Mode 8 ($t_7 - t_8$):

As the parasitic capacitor of the Q_1 switch is totally discharged, this mode resumes. The body diode of the switch Q_1 works simultaneously. In order to accomplish ZVS for Q_1, the V_{g1} gate signal should be used during this period.

Mode 9 ($t_8 - t_9$):

The switch Q_1 is activated on at $t=t_8$ with ZVS. The magnetizing and leakage current begins

to rise linearly. The current of diode D_1 continues to decline. This cycle continues until the current i_{Ns} falls to zero and switches direction at t_9. After that, the operating modes replay again.

V. Steady state analysis and design of the proposed converter

5.1 Voltage Gain:

Only modes 1, 4, 5 and 6 are considered to simplify the steady-state analysis and other modes are neglected during the dead-time period. The non-ideal variables that influence the voltage gain predominantly include the coupling inductor leakage inductor, the coupling inductor parasitic resistor, the transfer on-state resistor, and the condenser corresponding sequence resistor.

When the Q1 switch is activated, the magnetizing inductor Lm and leakage inductor Llk are charged by the input voltage source Vg. Meanwhile, to charge the output capacitor C02, the input voltage source, C2, C3 and the secondary winding are in series. The equations can be written as follows, based on Kirchhoff's voltage law:

$$V_g - V_{Lm} - V_{lk} = 0 \tag{5.1}$$

$$V_{C3} + V_{Ns} + V_g + V_{C2} = V_{C02} \tag{5.2}$$

$$V_{Ns} = n_s V_{Lm} \tag{5.3}$$

$$V_{Nt} = n_t V_{Lm} \tag{5.4}$$

$$\frac{V_{Lm}}{K} = \frac{V_{lk}}{1-K} \tag{5.5}$$

Where k is the linked inductor coupling coefficient, which is equal to Lm/(Lm+Llk). Inductor $1 : n_S : n_t$ coupling ratio. The voltage paths are shown as shown in Fig.5.1.

When the Q1 switch is switched off, the Q2 switch is turned on. The C2 and C3 switching capacitors are charged in parallel. The equations can be obtained as follows, based on Kirchhoff's voltage law:

$$V_{C2} + V_{lk} + V_{Lm} = 0 \tag{5.6}$$

$$V_g - V_{Lm} - V_{lk} - V_{Ns} - V_{C3} = 0 \tag{5.7}$$

$$V_{Nt} + V_{C01} = 0 \tag{5.8}$$

The following equation can be given by applying the volt-second balance principle on Np, Nt and Ns:

$$\int_0^{DT} V_{Lm} dt + \int_{DT}^{T} V_{Lm} dt = 0 \tag{5.9}$$

$$\int_0^{DT} V_{Nt} dt + \int_{DT}^{T} V_{Nt} dt = 0 \tag{5.10}$$

$$\int_0^{DT} V_{Ns} dt + \int_{DT}^{T} V_{Ns} dt = 0 \tag{5.11}$$

Equations (5.12) can be obtained based on (5.1), (5.5), (5.6) and (5.9).

$$V_{C3} = \frac{D}{1-D} V_g \tag{5.12}$$

Centered on (5.1), (5.5), (5.7), (5.9), the C3 switched capacitor voltage can be expressed as the C3 switched capacitor voltage.

$$V_{C3} = V_g + \frac{Dk(\frac{1}{k+n_s})}{1-D} \tag{5.13}$$

Combining (5.4), (5.5), (5.8) and (5.10), it is possible to determine the following equation:

$$V_{C01} = \frac{kDn_t}{1-D} V_g \tag{5.14}$$

It can be obtained by incorporating (5.11), (5.12), (5.13) and (5.14):

$$V_{C02} = V_{C2} + V_g + V_{C3} = \frac{kn_s+2}{1-D} V_g \tag{5.15}$$

The output capacitors C01 and C02 are large enough, according to the above assumption, so their voltage is constant over one switching cycle. Thus, ultimately, the output voltage is derived as follows.

$$V_{out} = V_{C01} + V_{C02} = \frac{kDn_t+kn_s+2}{1-D} V_g \tag{5.16}$$

Voltage gain:

$$M = \frac{V_{out}}{V_g} = \frac{kDn_t+kn_s+2}{1-D} \tag{5.17}$$

The turn ratio of the inductor is set to 1:2:8. Obviously, the coupled inductor's coupling coefficient has virtually no effect on the voltage gain. In other words, there is absolutely no effect on voltage gain from the leakage inductor of the coupled inductor. The voltage gain can then be loosely determined as

$$M = \frac{Dn_t+n_s+2}{1-D} \tag{5.18}$$

Fig. 6 displays the proposed converter's voltage gain versus duty ratio and the converters in [20]-[24] under k=1 and n=2. The proposed converter is able to achieve higher voltage gain than other converters in [20]-[24] in the case of using the same converter and duty ratio, as three windings of the coupled inductor are used. By using a lower turn ratio, the proposed converter will achieve the same voltage gain, which is useful for minimizing the volume of the converter.

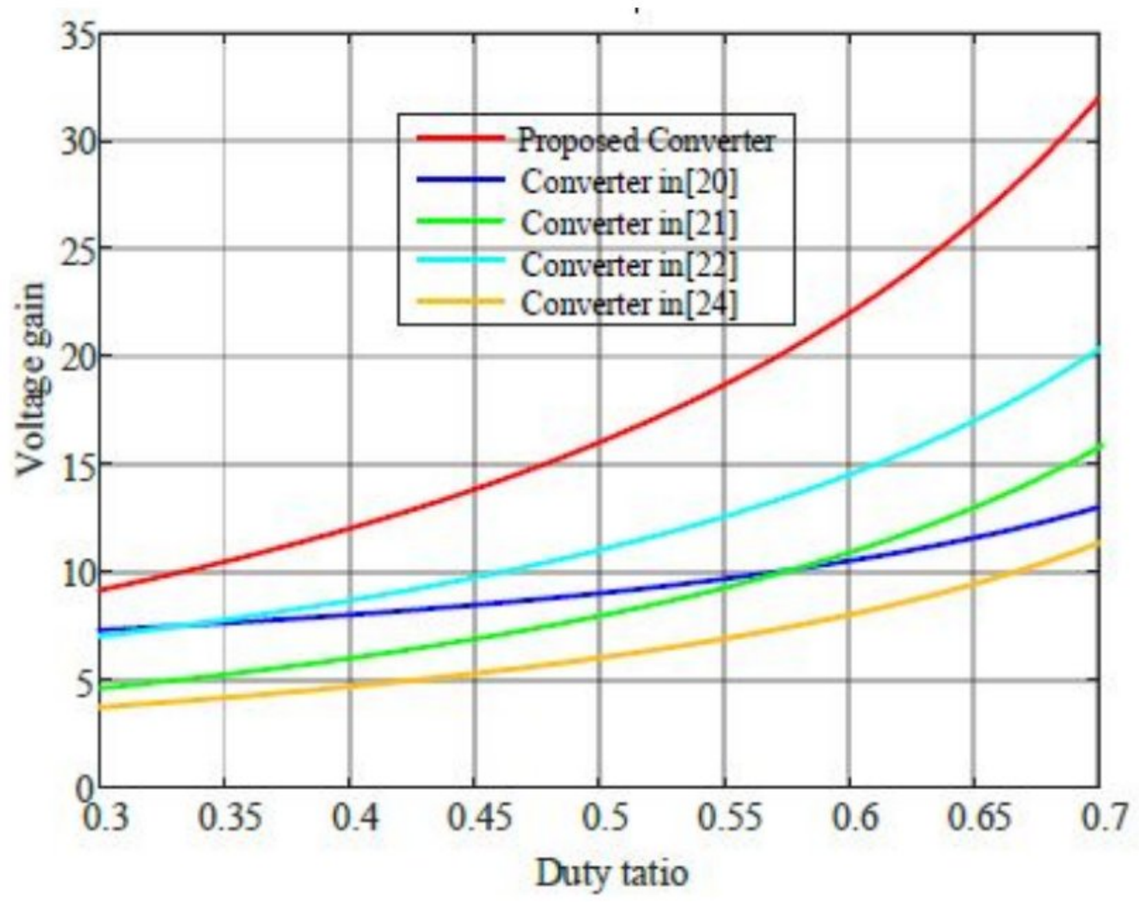


Fig. 5.1 The voltage gain versus duty ratio of the proposed converter, the converter in [20], the converter in [21], the converter in [22]

The comparison of the other characteristics is seen in Table 5.1 This can be clearly shown that the number of the device components of the proposed converter is almost the same as that of the converters in [20], [21] and [22], and is smaller than that of the converters in [23] and [24]. The converter suggested in [20] and [24] has almost the same switch voltage stress as the proposed converter, but the output diode voltage stress is greater than the proposed converter in this study. The voltage tension of all switches and diodes in [21], [22] and [23] is greater than the converter proposed. More specifically, for switches in [20], [21], and [22] and [23], soft switching cannot be accomplished, which results in significant switching losses. Hard switching will seriously affect the efficiency of the converter at [20], [20], [21], [22] and [23] stages. While ZCS can be realized by the converter in [24], the number of diodes is high, leading to a lot of loss of conduction of diodes.

TABLE 5.1 Comparisons of the proposed converter with reference [20] - [24]

Topology	**Proposed converter**	**Reference[ ]**	**Reference[ ]**
Voltage gain	$\frac{Dn_s+n_s+2}{1-D}$	$\frac{(2-D)(1+n)}{1-D}$	$\frac{2+nD}{1-D}$
Switches count	2	2	2
Diodes count	3	3	8
Capacitor count	4	4	5
Inductor count	1	1	2
Voltage stress of switch	$\frac{V_g}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
Voltage stress of output capacitor	Lower	Higher	Higher
Voltage stress of output diodes	$\frac{Dn_t}{1-D}V_g$	$\frac{1+n}{1-D}V_{in}$	$\frac{2+n(1+D)}{1-D}V_{in}$
Soft switching	ZVS	Hard switching	ZCS
Efficiency	$\eta = 95.3\%$ $P_{out} = 43.23W$	$\eta = 93.5\%$ $P_{out} = 160W$	$\eta = 94.55\%$ $P_{out} = 400W$

5.2 Voltage and Current Stresses:

Ideally, the voltage stresses of Q2, VD1 and VD3 are, with regard to Fig .4(a),

$$V_{Q2} = V_g + V_{C2} = \frac{1}{1-D}V_g \tag{5.19}$$

$$V_{D1} = V_{out} - V_{C2} - V_{C3} - (n_s + 1)V_g = \frac{Dn_t}{1-D}V_g \tag{5.20}$$

$$V_{D3} = V_{C02} - V_{C2} - V_g = \frac{n_s+1}{1-D}V_g \tag{5.21}$$

Ideally, the voltage stresses of Q1 and VD2 are identical in the same method.

$$V_{Q1} = V_g + V_{C2} = \frac{1}{1-D}V_g \tag{5.22}$$

$$V_{D2} = V_{C02} - V_{C2} - V_g = \frac{n_s+1}{1-D} V_g \tag{5.23}$$

Moreover, the voltage stress on the C2 and C3 switches is given by

$$V_{C2} = \frac{D}{1-D} V_g \tag{5.24}$$

$$V_{C3} = \frac{(1+Dn_s)}{1-D} V_g \tag{5.25}$$

By following the concept of the amp-second equilibrium of the output capacitors C01, C02 and the switched capacitors C2, C3, it is apparent that the average value of the output current through the diodes D1, D2 and D3 is equal to that of the output current. The peak currents of diodes D1, D2, D3 are therefore given by

$$I_{D1(peak)} = I_{D3(peak)} = \frac{2V_{out}}{(1-D)R} \tag{5.26}$$

$$I_{D2(peak)} = \frac{2V_{out}}{DR} \tag{5.27}$$

The current stress of switches

$$I_{Q1(peak)} = \frac{V_{out}(kDn_t+kn_s+2)}{(1-D)R} + \frac{V_{out}(1-D)D}{2(kDn_t+kn_s+2)(L_m+L_k)f_s} \tag{5.28}$$

$$I_{Q2(peak)} = \frac{V_{out}(1-D)\sqrt{(L_m+L_k)/C_2}}{kDn_t+kn_s+2} \tag{5.29}$$

VI. Result And Simulation

In order to verify the feasibility of the proposed converter we simulated the circuit in MATLAB simulink.We have plan to implement a 100W prototype in laboratory in future.The electrical specification is as follows:

$V_g = 25-45V$, $V_{out} = 380V$, $f_s = 100kHZ$ *and* $P_{out} = 100W$. The ratio of the coupled inductor was kept 1:2:8.A table is given below showing

Table-6.1: The parameters based on mathematical calculation.

Component	Specifications
MOSFETs	Simulink
D_1, D_2, D_3	Simulink
Switching Frequency	100kHZ
Turn Ratio	1:2:8
Magnetizing Inductor	120uH
C_2	1.68uH
C_3	0.62uH
C_{01}, C_{02}	100uH

6.1 Design of coupled inductor and switched capacitor:

1) *Coupled inductor Design:* Current ripple is kept under consideration to design coupled inductor.To function the circuit properly we need to put limit in maximum current ripple.By employing a coupled inductor maximum current ripple in limited to 20% of the maximum inductor current.By calculating it was observed that the for output power $P_{out} = 100W$ and input voltage $V_g = 25V$, the average inductor

current is the largest.The largest inductor current for previous assumption is $I_{L-max} = 4A$ and the ripple current $\Delta i_L = 0.8A$.

The expression of ripple current is as follows

$$\Delta i_L = \frac{V_g DT}{L_m} = \frac{D(1-D)TV_{out}}{L_m(2+n_s+Dn_t)} \tag{6.1}$$

Where D =Duty ratio

L_m =Magnetizing inductance

V_g =Input voltage

T =Chopping period

n_s, n_t=Turn ratio

V_{out}= Output voltage

Magnetizing inductance can be calculated as

$$L_m = \frac{D(1-D)TV_s}{L_m(2+n_s+Dn_t)} \tag{6.2}$$

2) *Switched Capacitor Design:*There are several categories of switched capacitor.There are two main factors that is kept in mind before choosing the specific one to work for our purpose.They are:1)voltage ripple and 2)output power lever.Switched capacitor can be calculated by utilising charge-second balance as

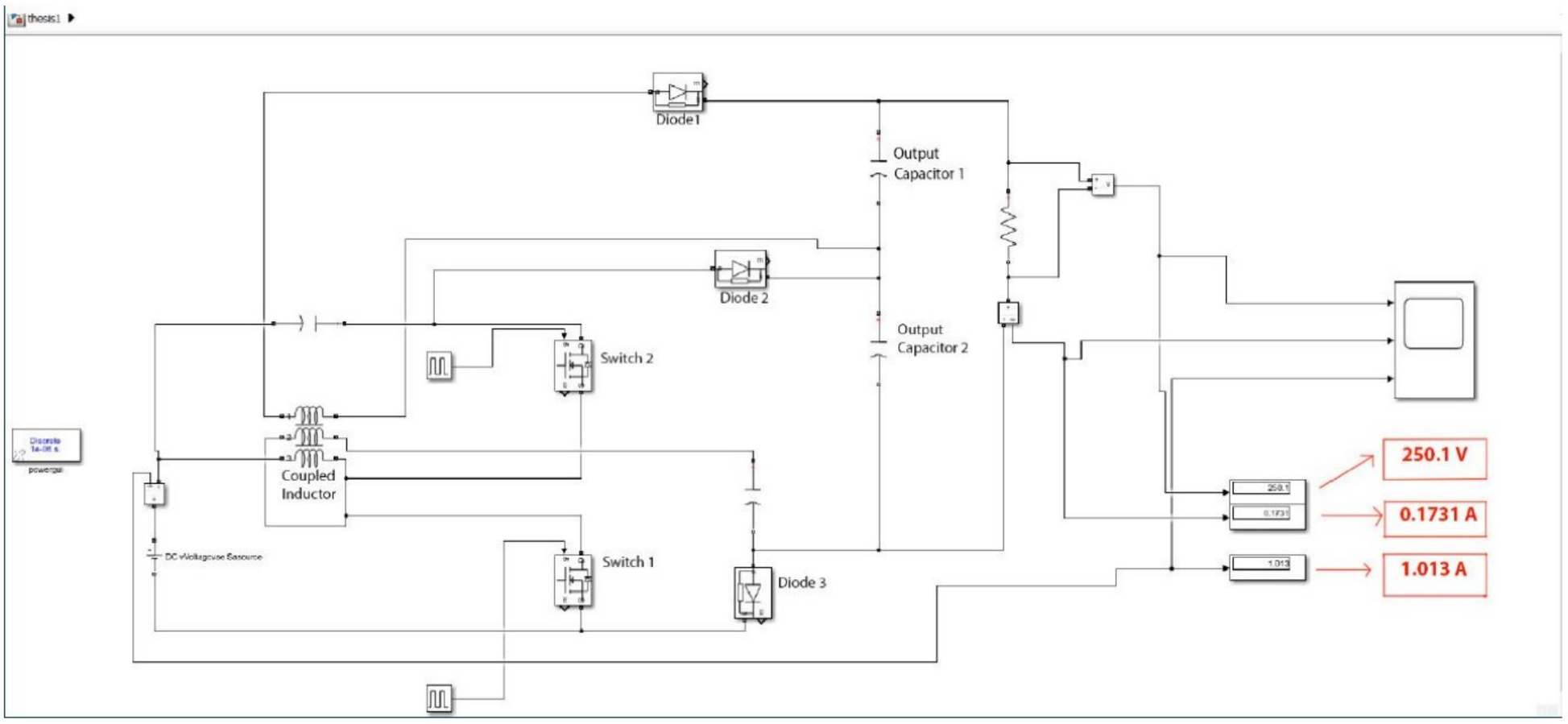
$$C_2 \geq \frac{I_{out}DT}{\Delta C_2}$$

$$C_3 \geq \frac{I_{out}DT}{\Delta C_3}$$

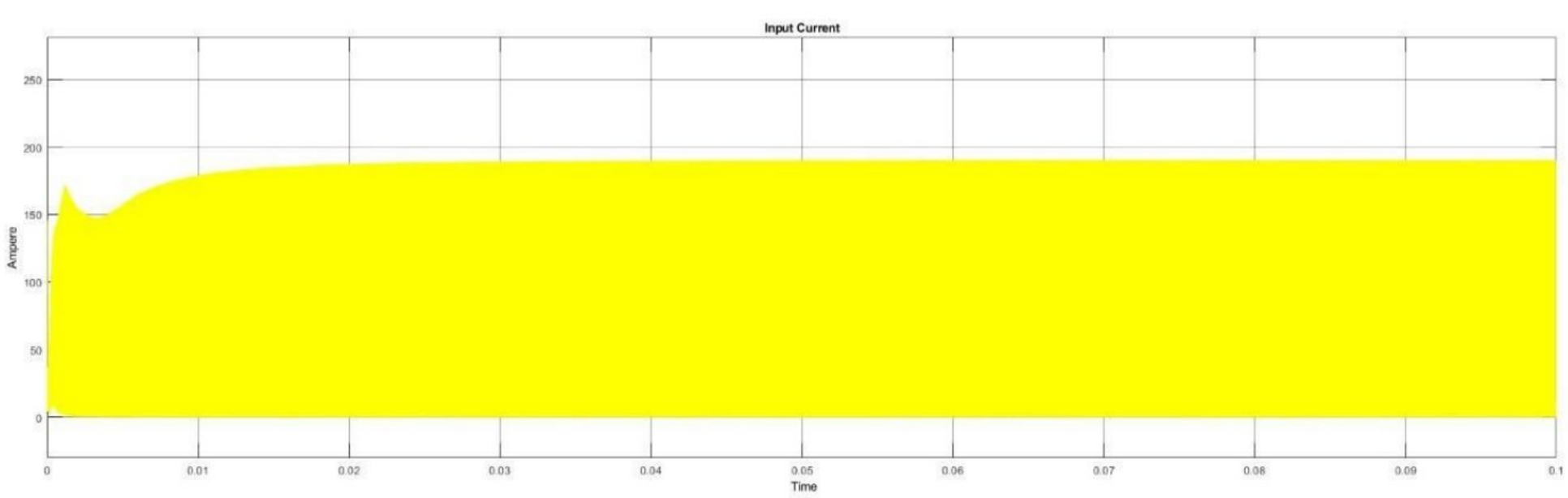
To keep maximum voltage ripple 1% of switched capacitor voltage, C_2 and C_3 were chosen accordingly. ΔC_2 and ΔC_3 are assumed ripple voltage of switched capacitor C_2 and C_3 accordingly.

6.2 Experimental Results:

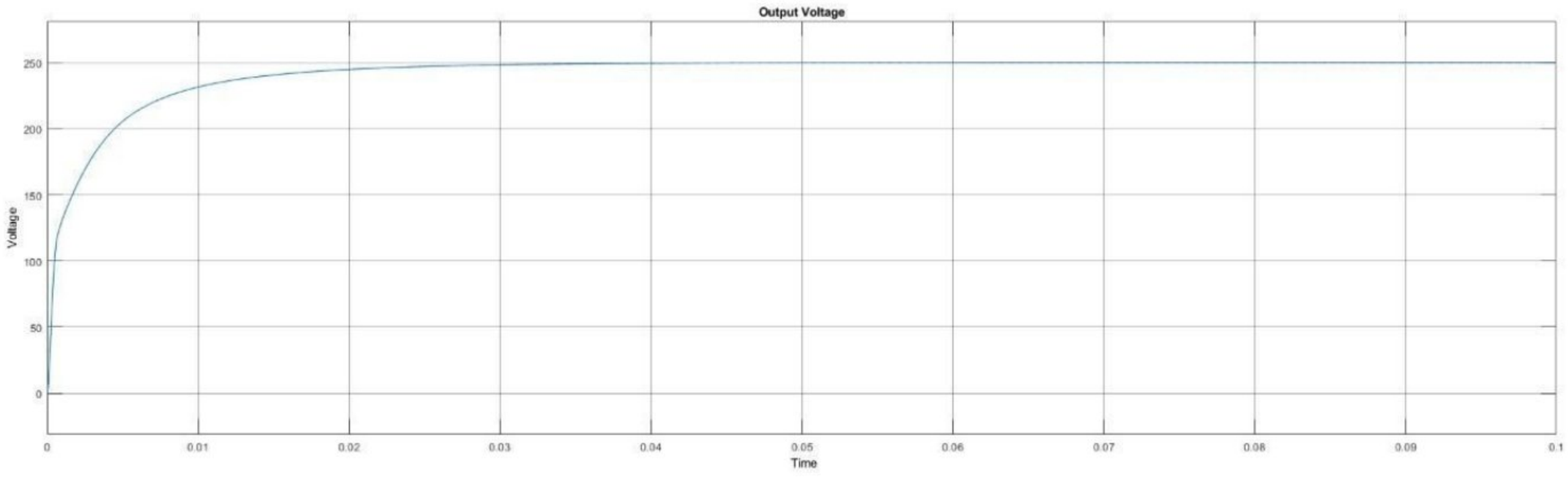
The proposed converter was simulated in MATLAB software.The screenshot of the circuit diagram is given in fig(6.1).



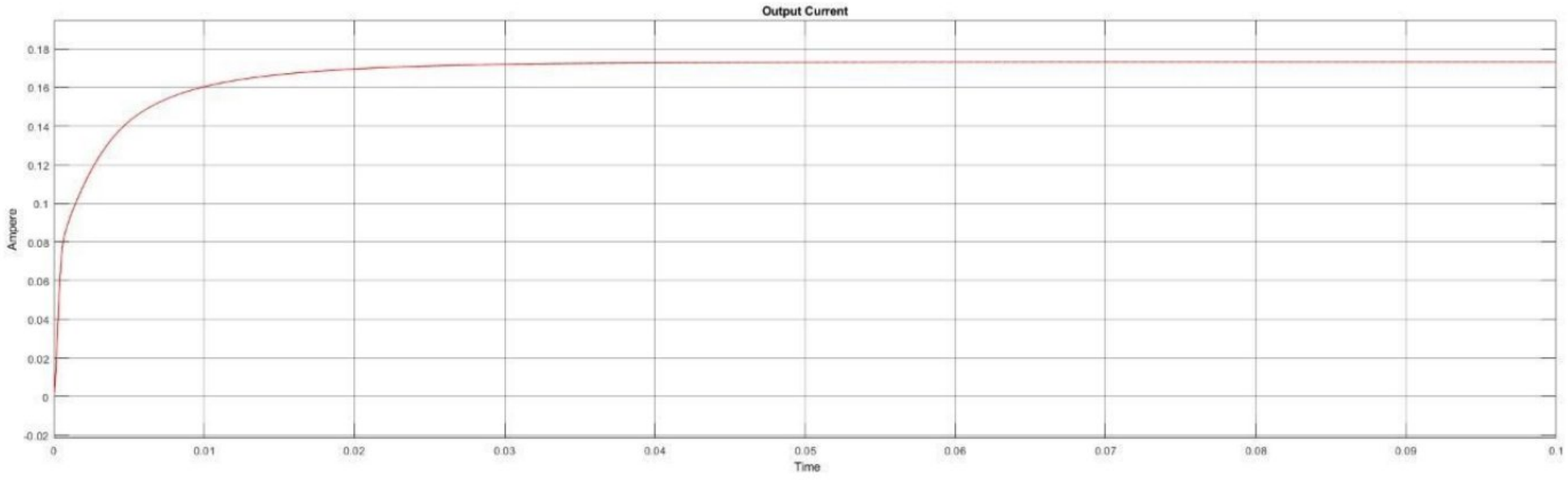
(a)



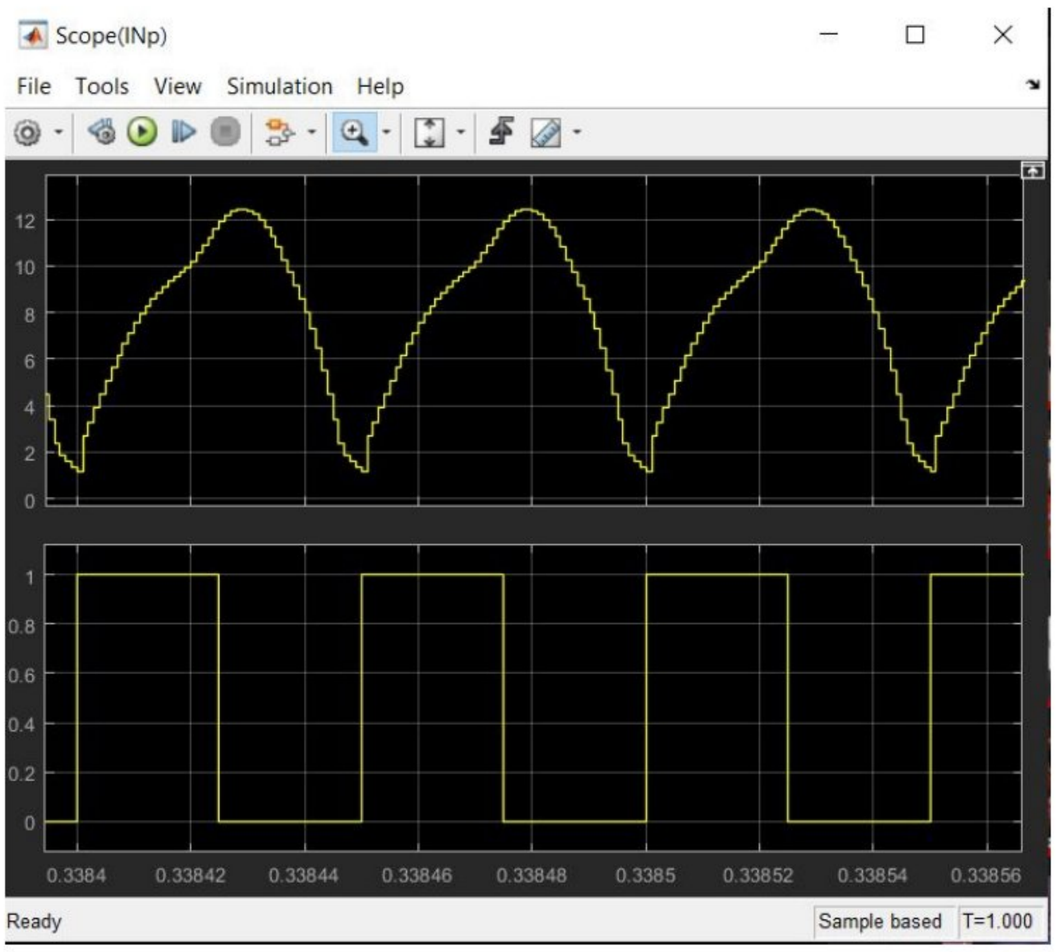
(b)



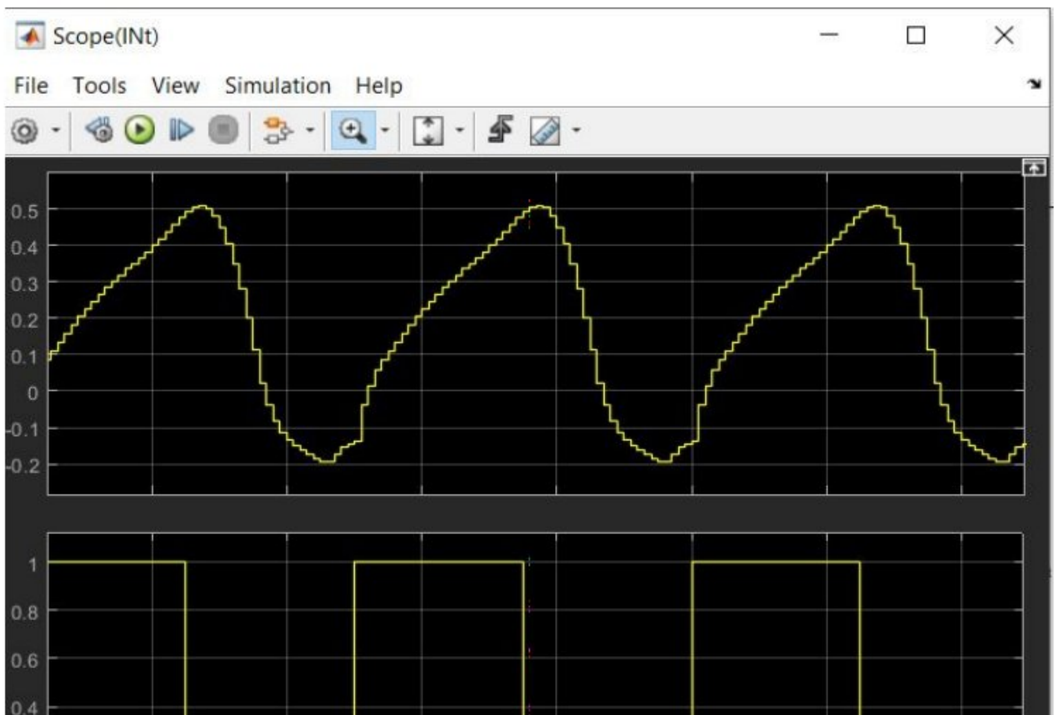
(c)



(d)



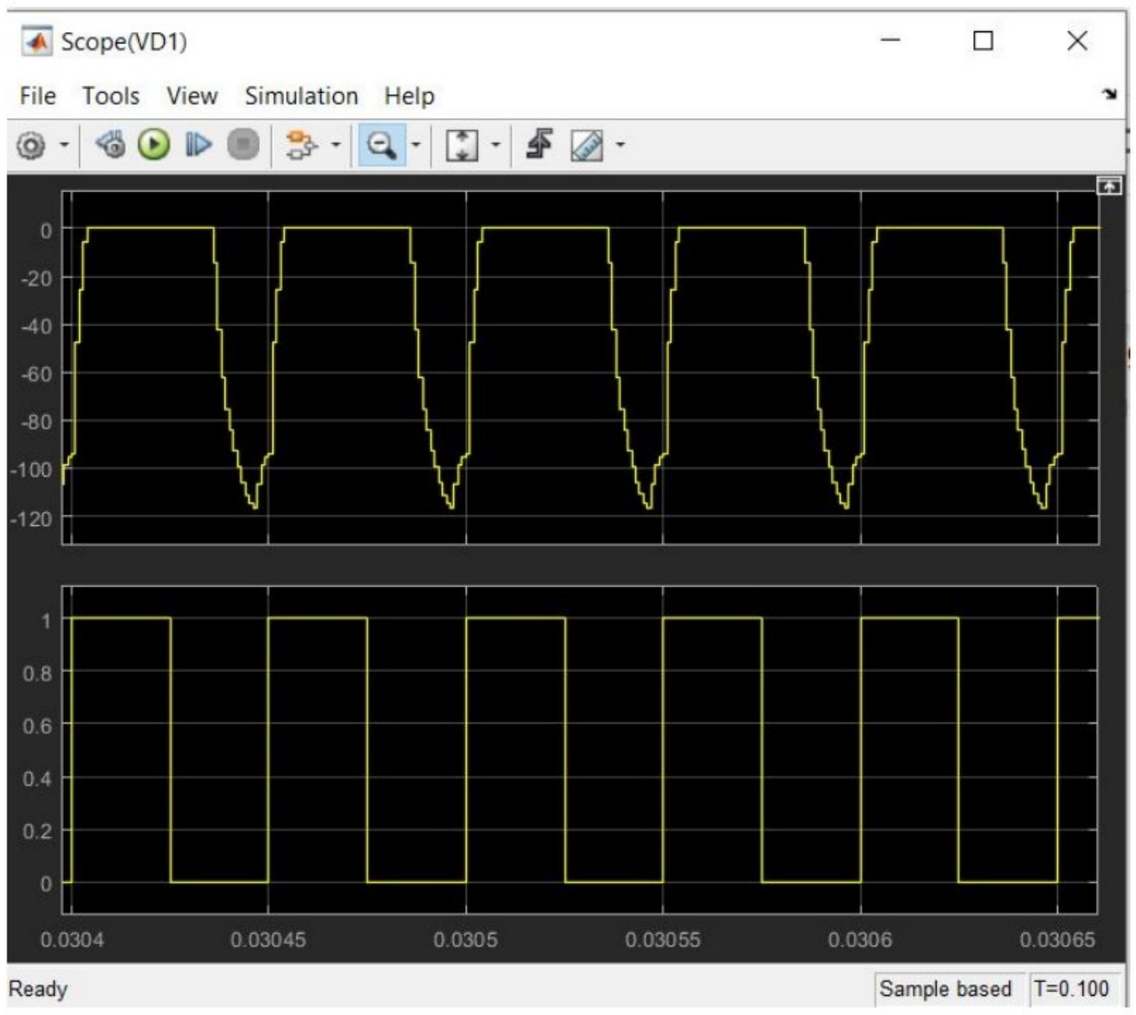
(e)



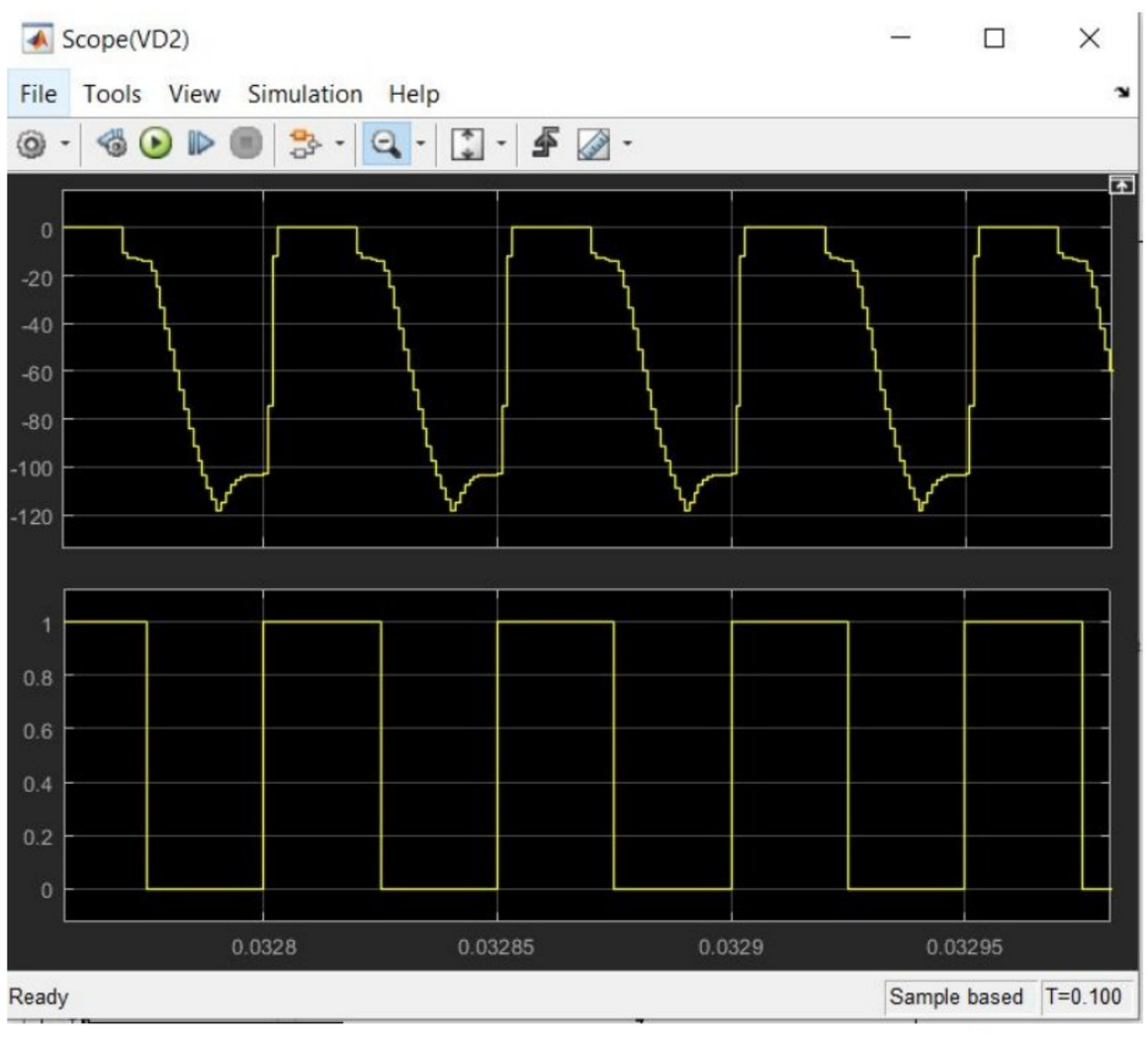
(f)

Fig.6.1 (a)Circuit diagram of the proposed converter.(b)Input current waveform.(c)Output voltage waveform.(d)Output current waveform.(e) V_{g1} and I_{Nt} waveform.(f) V_{g1} and I_{Np} waveform.

We get $P_{out} = 43.21W$ for input voltage $V_g = 45V$ .From _(c),(d) we see that output voltage is 250.1V and output current is 0.1731A respectively.Current through primary winding and secondary winding with V_{g1} are shown in fig_(e),(f).From above figures we see that the results are consistent with previously described steady-state analysis.



(a)



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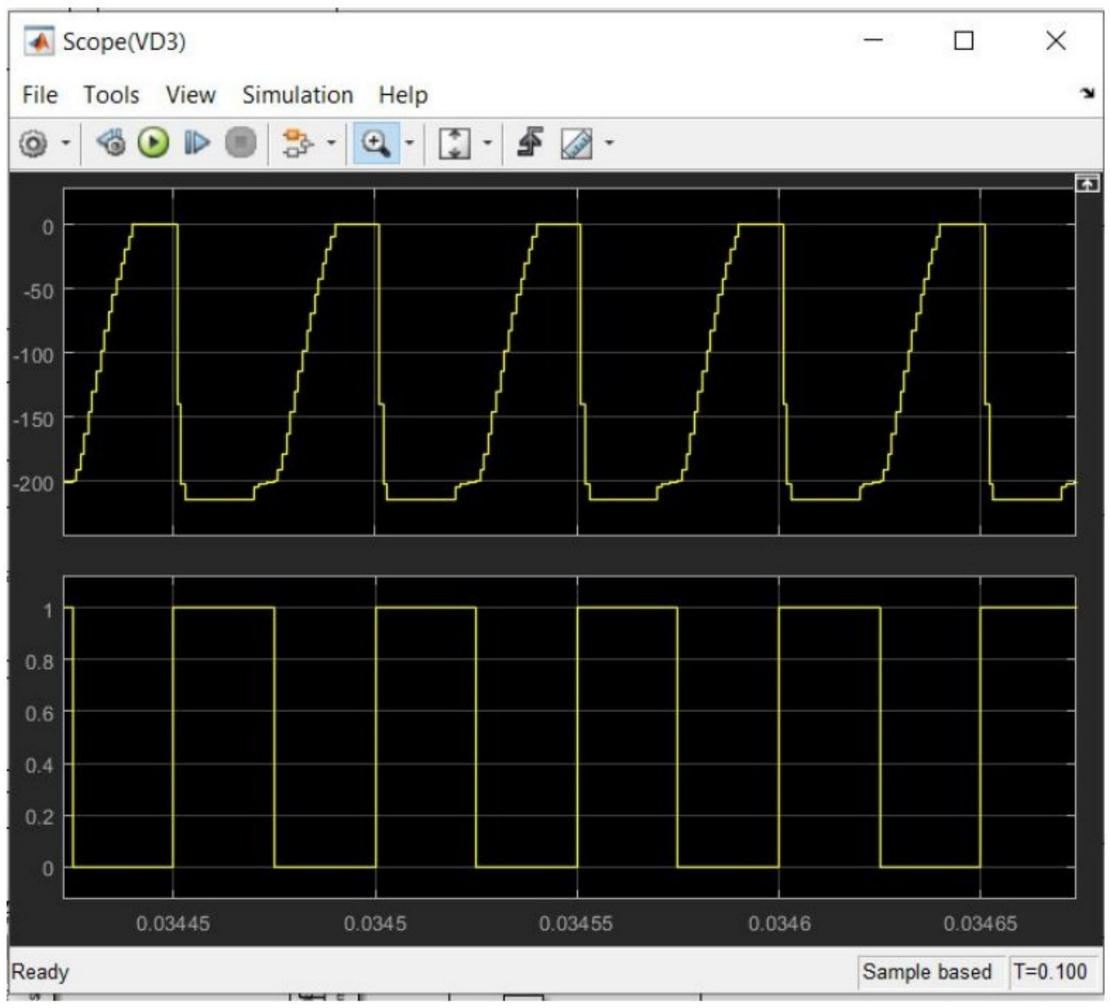
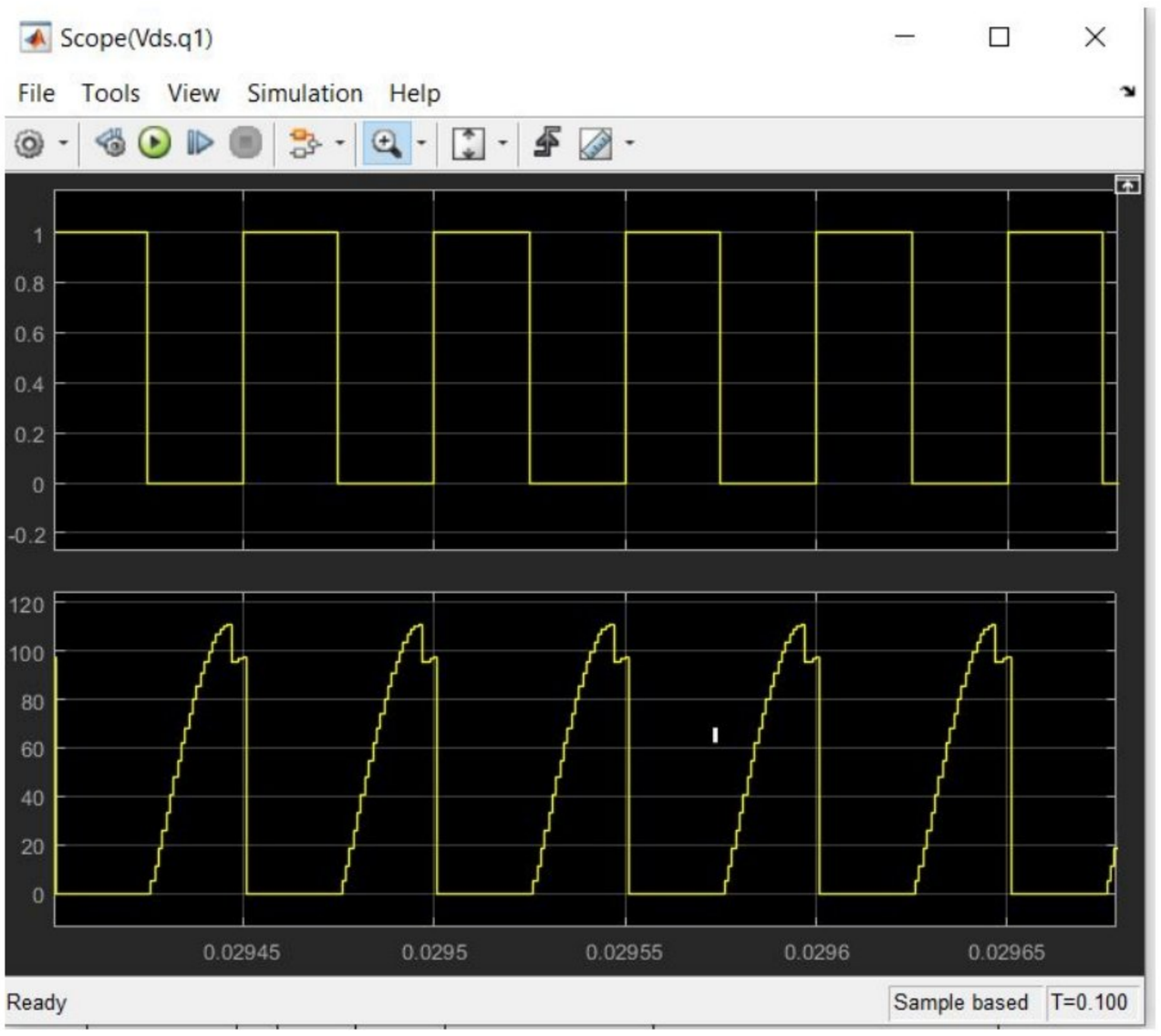


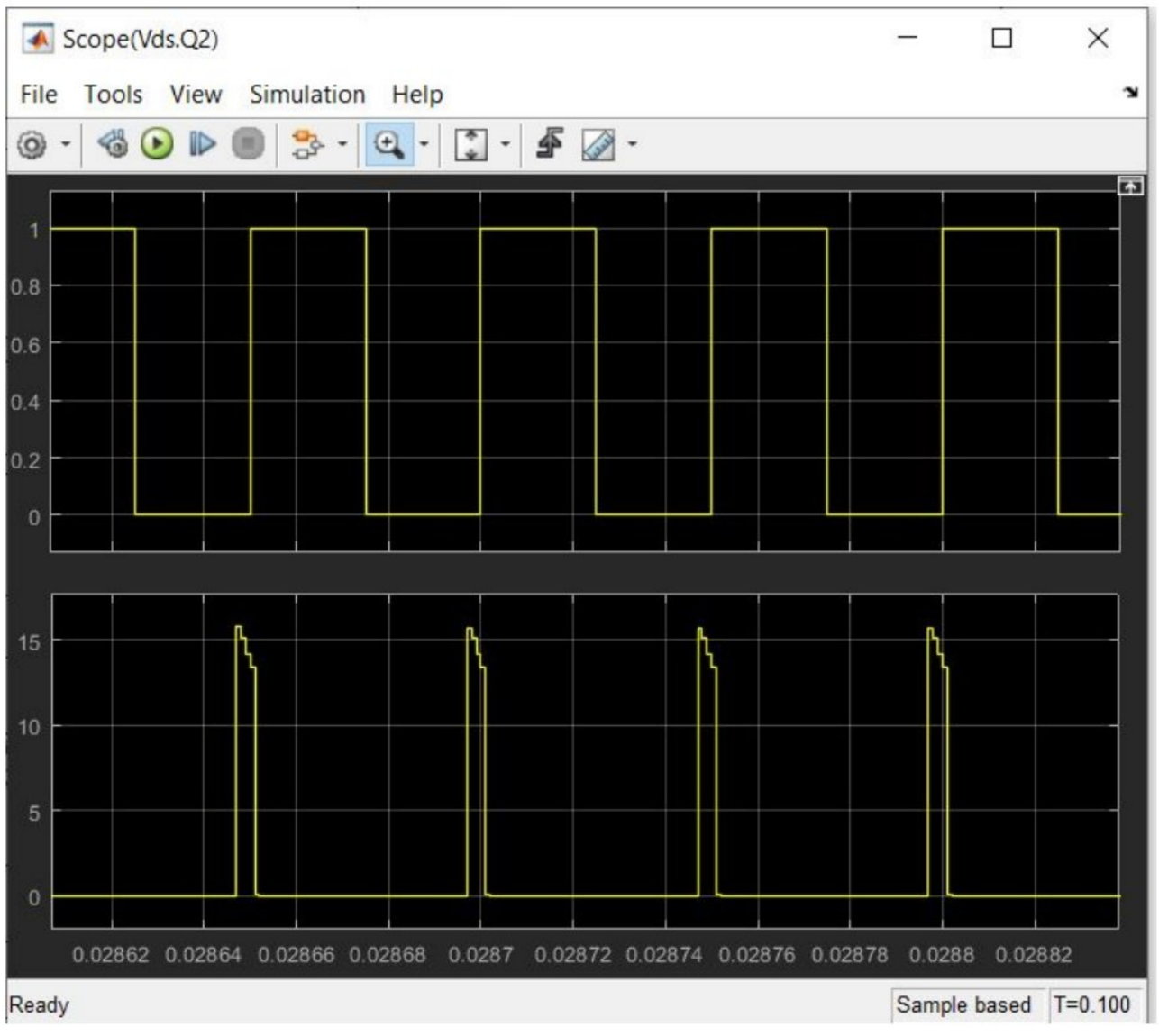
(c)

Fig 6.2. (a)Measured voltage waveform of $D_1, D_2,$ *and* D_3 .(a)The voltage of diode D_1 .(b)The voltage of diode D_2 .(c)The voltage of D_3 .

Voltage stress of D_1 is shown in the above figure. Due to leakage inductors there is a slight voltage spike in the voltage waveform.The other voltage stresses on D_2 and D_3 is also shown. The voltage in 9(b) and 9(c) are opposite to each other along with V_{g1}.



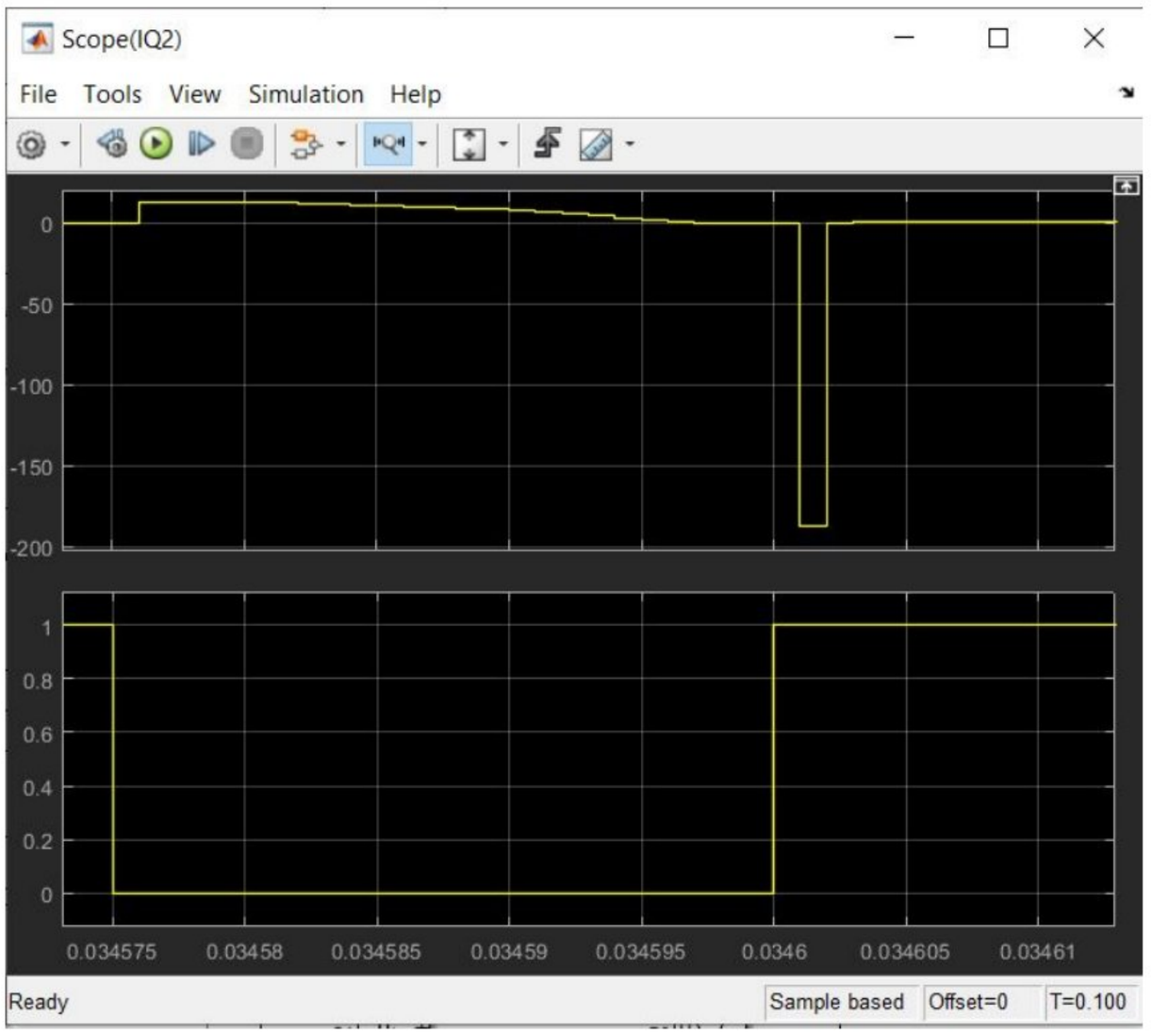
(a)



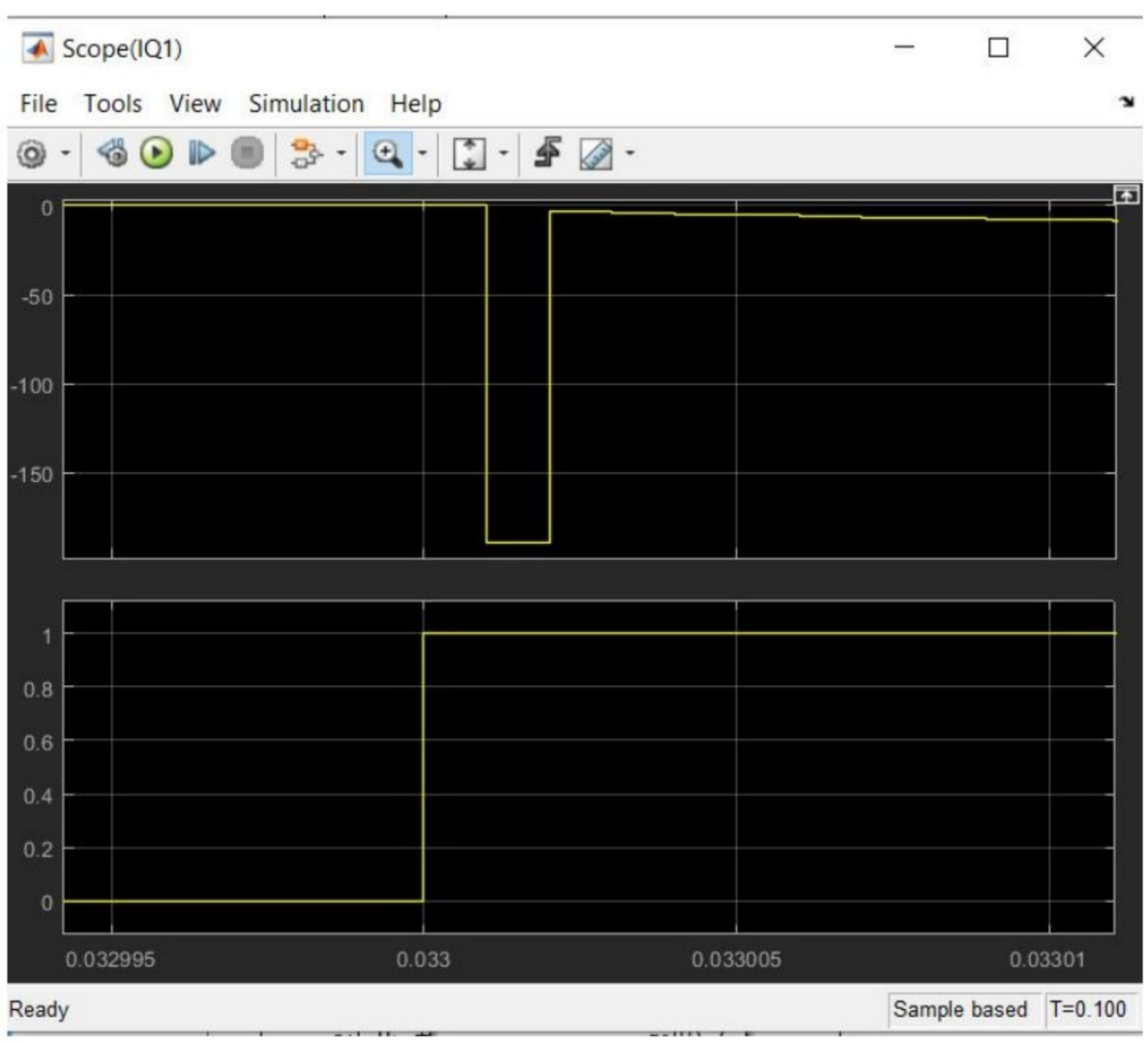
(b)

Fig6.3 .Measured waveform of switch 1 (Q_1) and switch 2 (Q_2) .(a)Gate signal and drain-source voltage of Q_1.(b)Gate signal and drain-source drain source voltage of switch 2.

From above figure drain source voltage of Q_1 and drain source voltage of Q_2 along with source voltage is shown accordingly.From the waveform we see that the drain-source voltage of switch Q_1 is almost 8 times bigger than the drain-source voltage seen by switch 2. The voltage spike is more sharp in switch 2 compared to switch 1. To observe the zero voltage switching more accurately we compared drain source current with source voltage. In Fig_6.4.



(a)



(b)

Fig 6.4 Measured waveform of the switch Q_1 and Q_2.(a)The gate signal and drain-source current of Q_1.(b)The gate signal and drain-source current of Q_2.

The drain-source current of Q1 is in the negative direction of that of the gate signal before it goes up.When the body diode conducts,it achieves ZVS and drain-source voltage is clamped

to zero.From the above graphs.It is clear that both Q_1 and Q_2 achieves zero-voltage switching.ZVS help improve efficiency and reduce electromagnetic induction.As the voltage stress is low in both of the switches ,it is economic and overall improve efficiency of the proposed converter.The voltage spike caused by Q_2 is absorbed by the parasitic capacitor C_2.

The conduction loss of the switch is achieved by [25]

$$P_{cond} = I_s^2 R_{DSon} \tag{6.3}$$

Where,

R_{DSon} =On-state resistance .

I_s =RMS value of current flowing through switch.

The switching loss is calculated by [26]

$$P_{on} + P_{off} = \frac{V_{DS} I_{on} t_{on}}{6T} + \frac{V_{ds} I_{off} t_{off}}{6T} \tag{6.4}$$

Where,

t_{on} =Turn-on transition time

t_{off} =Turn-off transition time

V_{ds} =Drain-source voltage

I_{on} =Turn-on current

I_{off} =Turn-off current

The loss in the diode is given [27]

$$P_{diode} = U_{D0} I_D \tag{6.5}$$

Where,

U_{D0} =Forward conduction voltage of diode.

I_D =Diode current.

Core loss can be calculated as [28]

$$P_{core} = K_{Fe} \left(\frac{V_{ave}}{8 f_e N_L A_e} \right)^{\beta} A_e l_m \tag{6.6}$$

Where,

K_{Fe}, β =Constant related to loss

N_L =Number of turns of inductor winding.

V_{ave} =The average voltage across the winding in positive half cycle

A_e =Effective cross-sectional area

I_m =Magnetic path length of the core.

The copper loss can be expressed as

$$P_{copper} = I_{rms}^2 R_{eff} \tag{6.7}$$

Where,

R_{eff} =Equivalent value of copper resistance

I_{rms} =Current flowing through winding.

Power loss of the capacitor

$$P_c = I_c^2 R_{ESR} \tag{6.8}$$

Where,

R_{ESR} =Equivalent series resistor of capacitor

I_c =RMS capacitor current.

According to reference,The loss of the proposed converter is relatively low compared to others.We also introduced ZVS in this proposed converter without compromising the components and efficiency.The highest efficiency we got was 95.3%.We also has a plan of building an experimental prototype in upcoming future and use it in practical scenario.

VII. Conclusion

A high step-up dc-dc boost converter is proposed in this project.The proposed converter is claimed to have high efficiency,low loss,soft switching.It is based on coupled inductor and switched capacitor.The capacitor is charged in parallel and discharged in series.To realize ZVS,the leakage energy of leakage inductor was utilized.Also low voltage stress was ensured in the semiconductor device.That's why it can be used in low voltage device comfortably.A low-voltage rated MOSFET with a low on-state resistance was used in this converter.The input current of the proposed converter which is extremely suitable for OV applications.Due to Covid-19,we could not implement it in hardware.We have a plan on implementing a 100W prototype to measure the cost and feasibility of using this converter in real life scenario.

Future work plans

- Focus on output voltage fluctuation issue than we are currently facing
- Leakage inductor energy utilization in a more efficient way
- Building an experimental prototype
- Using on PV and EV applications
- Experimenting with IGBTs,BJTs,GTOs to see how the switching works with these chips
- Building an experimental prototype and realize it's feasibility in real life application.

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