Development of a Novel Single Phase Non-isolated AC-DC Zeta Converter for Improved Power Quality

by

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CERTIFICATE OF APPROVAL

The thesis entitled **"Development of a novel single phase non-isolated AC-DC Zeta Converter for improved power quality"** submitted by Ferdous S. Azad, Student No. 152623 of Academic Year 2016-17 has been found as satisfactory and accepted as partial fulfillment of the requirement for the Degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on March 01, 2021.

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Dedicated to my dear parents

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LIST OF ABBREVIATIONS

PFC	Power Factor Correction
EMI	Electromagnetic Interference
SMPS	Switch Mode Power Supply
SEPIC	Single-ended Primary-inductor Converter
THD	Total Harmonic Distortion
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
IEEE	Institute of Electrical and Electronics Engineers
PF	Power Factor
PWM	Pulse Width Modulation
PI	Proportional- Integral
SSA	State Space Averaging

Acknowledgement

First, I offer my gratitude to the Almighty ALLAH Subhanahu Wa Ta'la for giving me the capability to do this work with good health.

I am very much grateful to my research supervisor, Professor Dr. Golam Sarowar for his support and guidance throughout the course of this work. He has created a research environment for which I was able to explore many ideas without constraint. I have gained a wealth of knowledge and experience in science and engineering through his direction that is beyond value to my future endeavors.

As I am currently doing a job, the journey was not easy for me to complete my thesis work unless I got continuous support from my family. I am thankful to my family members especially to my parents for their continuous support throughout my entire academic life. I would also like to acknowledge the support from some of my friends who have been a constant source of inspiration all along this work.

Abstract

Switched-mode power converters have been studied broadly and used in industrial products. The classification comes as Buck, Boost, and Buck-Boost for the basic topology in which a single inductor is used. Converters with higher-order topology like Cûk, SEPIC, and Zeta used two inductors. A new topology of single-phase single switch non-isolated AC-DC Zeta converter is presented in this research work. Different studies are carried out to analyze the result and suitable parameter values are tuned. The proposed converter provides better conversion efficiency than the conventional converter throughout the variation of the duty cycle. Maximum efficiency of 98.09% is achieved for 20% duty cycle. The proposed converter offered a lower input power factor than the conventional converter for lower and higher duty cycles. Suitable feedback control in a closed-loop system improved the input power factor. The proposed converter with a PFC controller provides a very high input power factor (0.99) which is almost close to unity. The proposed converter has lesser total harmonic distortion (THD) of the input current in comparison with the conventional one for higher duty cycles but for lower duty cycles the conventional converter shows better performance. Again, using the feedback controller, the THD of the input current is kept close to IEEE Standards for the proposed converter. The proposed converter with feedback controller provides higher conversion efficiency, reduced THD of input current, and quality power factor. Dynamic response of the proposed converter has also been observed. The proposed converter can maintain the desired level of output voltage with sudden changes in load. Simulation results for the analysis of the proposed circuit are obtained using PSIM Professional

Chapter 1
Introduction

1.1 Introduction

With the advancement of technology, AC-DC converters are heavily used in industrial, commercial, transportation, utility and domestic applications. Telecommunications equipment, microprocessors and computer peripherals need DC supply to operate. Electric vehicle technology, that is used as an alternative of conventional vehicles need DC supply. DC power supply is also required in operating sensitive electronic devices, relays, DC motors, fusion process, chemical process, industrial cranes, industrial robots, battery chargers, separating magnets, electrolyte cells, electro refining, forklift trucks, mine haulers, marine hoists and so on. In many cases this DC supply comes from AC source. For this reason AC-DC conversion for different applications and voltage levels are studied in the past.

A basic AC-DC conversion scheme consists of input filter, AC-DC converter and DC-DC converter is shown in the figure 1.1. Power factor correction using active filtering is needed to overcome low input PF as it shapes the input current to draw nearly sinusoidal current in phase with voltage. In AC-DC conversion, input current THD, input power factor and conversion efficiency are the important aspects that should be taken care of.

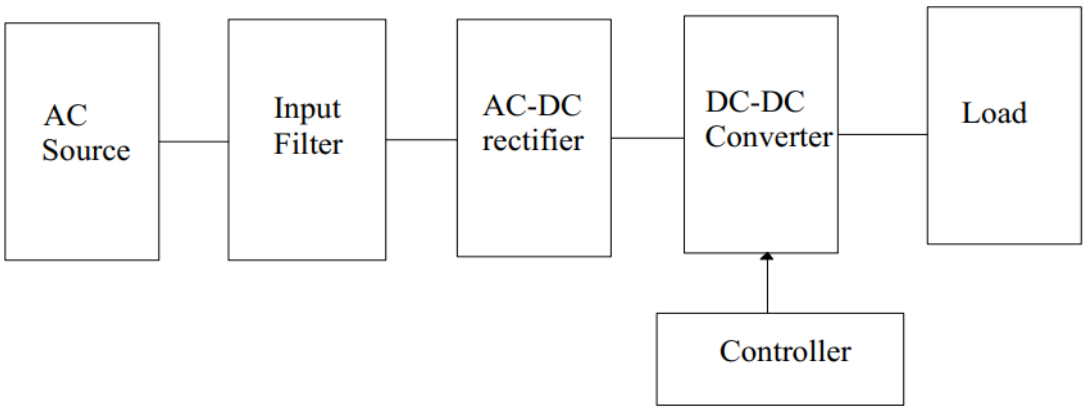


Figure.1.1: A basic block diagram of AC-DC conversion scheme

1.2 Background

Traditionally, full wave rectifier with bridge configuration is used for AC-DC power conversion that has the property of simple structure and low cost. However, these rectifiers have some drawbacks that includes pulsating input current, high electromagnetic interference (EMI), low input power factor, harmonic pollution at power system and so on [1] [2]. Harmonic pollution is detrimental to power supply that can cause malfunction or damage to sensitive electric devices. The harmonics present in power supply needs to be within a tolerable limit prescribed either by IEEE 519-1992 or IEC 61000-3-2/IEC 61000-3-4 standard [3].

Many methods have been proposed to mitigate harmonic pollution in the recent years. In general, input passive filters consisting of large inductor and capacitor are used to reduce current distortion (THD) sacrificing performances like efficiency and power factor [4]. Again, use of bulky inductor and capacitor are not suitable for high power application. Then active filters are introduced to solve problems of passive filters [5, 6]. The method involves a DC-DC converter in between rectifier and load. The required input filter is smaller than traditional passive filter and hence power factor is improved[7, 8]. Different topologies like Buck, Boost, Buck-Boost, Cûk etc. are investigated as DC-DC converter for the method, among which Boost converter is the common [9-16]. The DC-DC converter use unidirectional switch for switching purpose, which may be a BJT, MOSFET or IGBT.

In Boost AC-DC converter topology in [17, 18], Boost stage must operate in critical conduction mode (CCM). For CCM operation switch must be on at the time boost diode current approaches zero. With the change of source voltage or load, switching frequency needs to be adjusted in DC-DC operation. Constant average current mode in Boost diode is another approach in Boost converter topology [19]. In order to keep track of average current, current sensor is used and duty cycle is modulated over the line cycle to maintain constant current level. Unidirectional Boost converters are highly used in electronic ballasts, power supplies, EVs, variable-speed ac motor drives in compressors, refrigerators, pumps, fans etc. [20-22]. On the other hand, Bidirectional Boost Converters are extensively used in battery charging and discharging in line interactive

UPS, battery energy storage systems (BESS), and transport applications such as metro and traction. This converter is also used for utility interface with nonconventional energy sources such as solar PVs, wind, etc.[23-26]. Bridgeless AC-DC Boost converter [27-31] is implemented in the recent years to minimize number of semiconductor diodes and reverse-recovery problems associated with it, but number of switches are more than one in most of these configurations.

AC-DC Buck converter topology is a combination of diode bridge rectifier with step down chopper. Input and output filters are also present to reduce harmonics in supply side and reduce ripple at output stage. Step down AC-DC converters are also developed, both isolated and non-isolated, using rectifier with filter and different combinations of DC-DC converters [32-36]. High-frequency transformer isolation is needed to reduce the size, cost, weight, and volume of transformer used for isolation and voltage-matching. Isolated Buck converters have advantageous features such as high PF, decreased harmonic component in the ac side, and also provide controllable dc output voltage[26, 37]. AC-DC buck converters are used mainly in small-rating dc motor speed control, battery charging, self-regulating power supply, etc.

Buck-Boost topologies are implemented using both isolated [10, 38-41] and non-isolated [42-44] circuit configurations to step up and down the input voltage for wide range of applications. High-frequency transformer isolation provides voltage adjustment for better control, compactness, reduction in weight and size, losses, and their suitability to the wide variation of applications. Moreover, it needs only a single switch as in [38, 39] which is inherently capable of giving regulated dc output with reduced ripple and high input PF and low total harmonic distortion at the ac mains through proper control techniques. Some Buck-Boost converters using soft switching techniques using resonant circuits was implemented in the past [45-47]. It was used to reduce switching stresses and losses in the devices for operation at high switching frequency and to further reduce the size of magnetics and energy storage elements.

AC-DC Buck-Boost converters with Continuous conduction mode (CCM) operation [39, 48] was proposed with better efficiency and stable gain for non-variable load applications. Control techniques is often complex and high voltage stress of switching

devices is seen for this type of converters. On the other hand, Discontinuous Conduction mode (DCM) operation[49, 50] can reduce the inductor size, reduce voltage stress in switches and simpler controller is sufficient. The problem with DCM operation is that they suffer from current stress that can limit rated power. Buck-Boost bidirectional power flow converters are often a good choice in various applications such as automotive energy harvesting, battery storage systems etc.[51-53]. However, these converters need more switches and semiconductor diodes compared to unidirectional topologies and controller needed for these are complex and costly.

AC-DC Cûk converter is another step-up step-down converter used for power quality improvement that has more than one inductor and capacitor in the circuit topology [54-57]. Cûk converter requires low value intermediate capacitance in order to transfer energy to output capacitor and load resistance. Open loop Cûk provides output voltage ripple and also phase differences between input voltage and input current under input voltage variation[56]. Hysteresis current controller based Cûk converter was implemented for power factor correction [58]. Sliding current control [59], voltage controlled [60, 61] and modified one cycle control [62] Cûk converter was also used as PFC in the recent years. Cûk converter is heavily used in many applications such as PV systems [63, 64], LED driver [65, 66] , electric vehicles [67], motor controllers [68, 69] etc.

Single Ended Primary Inductor Converters, known as SEPIC converters, can provide non-inverting output voltage greater than (Boost mode) or less than (Buck mode) input voltage. SEPIC converter offers isolation between source and output load, inherent inrush current limitation during startup and overload conditions, reduced input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology [70-72]. Bridgeless SEPIC converters are investigated for better performance, reduced semiconductor diodes and less conduction losses [57, 73, 74]. Studies have been carried out in recent years to use SEPIC converters in different applications such as aircraft application [75], on-board battery charger [76], welding application [77], LED drivers [78], motor drives [79, 80] etc. Control strategy of SEPIC converters is complex due to increased number of inductors and capacitors. Fractional order PID controller [81] ,

ANFIS controller [82], Fuzzy logic based controller [83] are some examples used in the recent past as controller for SEPIC converters.

The Zeta converter, also known as Inverse SEPIC converter is a fourth order converter constructed using a switch, semiconductor diode, two capacitors and two inductors. A PWM feedback loop is needed to regulate output voltage that can be stepped up or down[84]. Zeta converter with high frequency transformer isolation can provide safety in the system but the topology has high transistor voltage stress because of resonance caused by HF transformer leakage inductance and capacitance of transistor switch. An isolated Zeta converter with two-transistor and two clamping diodes on primary side of transformer was proposed that is capable of reduce the transistor voltage stress[85]. DUAL-ZETA converter proposed in [86] can reduce the output voltage ripple and share load as two converters work simultaneously but out of phase. A bridgeless Zeta converter with isolation proposed in [87] used interleaved topology to reduce diode losses and output ripple. Fuzzy Logic Controller was used for discontinuous mode operation for the converter. Authors in [88] proposed a Zeta converter for step down operation in electric vehicles application; wherein two stage conversion process and two PI controller was used. Transformer-less AC-DC Zeta converter was used for Permanent magnet synchronous motor using direct torque control technique [89]. Applications of Zeta converter was mainly low power applications with stepped down output voltage; i.e., Led driver [87], electric vehicle battery charger [88], PV applications [90] etc.

Although Zeta converter is not a new topology but it has gained less attention over the years. Transformer-less AC-DC Zeta topology with both Buck and Boost mode operation able to provide high power quality is the target of this thesis. In this thesis, a new single phase single switch non-isolated AC-DC converter is reported.

The proposed converter can chop input current by using only one switch. This topology is different from conventional DC-DC regulated rectifiers because switching of input current ensures input AC current to be almost in phase with supply voltage without any additional control scheme. This would result in nearly sinusoidal input current shape with using of small EMI filter. This proposed converter can provide both step up and

step down DC output voltage with high efficiency power conversion. Feedback controllers are also used to maintain certain voltage level with high input PF and low THD. Dynamic response of the proposed converter is also analyzed to verify converter response under different load switching.

1.3 Converter Performance

The key converter performance parameters are conversion efficiency, input power factor and input current THD. The proposed converter is tested with this performance parameters.

The efficiency of a converter permits us to compare the effectiveness of rectification [91]. It is defined as the ratio of output power (dc) and input power (ac). Efficiency should be higher for a good converter.

$$\% \, efficency = \frac{P_{out,dc}}{P_{in,ac}} \times 100 \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.1)$$

The input power factor of an AC-DC converter plays a vital role in converter design because it determines how efficiently the converter utilizes the input AC power. It is defined as the ratio of the real power to the apparent power drawn by a load from an AC source. If the input voltage source is sinusoidal, then power factor can be expressed as the product of the distortion power factor and displacement power factor. Distortion power factor K_D is given by the following equation

$$K_D = \frac{I_{rms1}}{I_{rms}} \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.2)$$

Where, I_{rms1} is the fundamental component of input current and I_{rms} is the total rms current.

Again, displacement factor D_F can be defined as follows

$$D_F = cos\, \varphi \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.3)$$

Here, φ is called the displacement angle. It is the angle between fundamental component of input current and voltage.

So total power factor can be expressed as

$$PF = K_D * D_F \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.4)$$

$$PF = \frac{I_{rms1}}{I_{rms}} * cos\,\varphi \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.5)$$

A power factor of one indicates that the input current is in purely sinusoidal shape and is in phase with the input voltage. Power factor less than one means higher rating of VA is needed for a source than the load needs [92].

Total Harmonic Distortion (THD) is defined as the ratio of the square root of the summation of the square of all non-fundamental harmonics of a waveform to fundamental component of the same waveform. If rms value of fundamental component is I_{s1} and distortion component is $I_{distortion}$, then %THD can be expressed as follows

$$\%THD = \frac{I_{distortion}}{I_{s1}} * 100 \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.6)$$

Here, distortion component can be expressed as

$$I_{distortion} = \sqrt{{I_s}^2 - {I_{s1}}^2} \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.7)$$

When the harmonics of input current of a converter increases, the shape of the current waveform is distorted and source power is polluted. The relation between THD and PF can be written as

$$\%\,THD = \sqrt{\left({}^{1}/_{K_D}\right)^2 - 1} * 100 \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.8)$$

From this K_D can be expressed as

$$K_D = \frac{1}{\sqrt{\left(\frac{\%\,THD}{100}\right)^2 + 1}} \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.9)$$

The displacement PF can be made unity with the help of capacitors or inductors but making K_D unity is difficult. If D_F is unity then power factor is expressed as

$$PF = K_D = \frac{1}{\sqrt{\left(\frac{\%\,THD}{100}\right)^2 + 1}} \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad (1.10)$$

1.4 Thesis Objective

The main objective of this thesis is to develop a new topology single phase single switch non-isolated AC-DC Zeta converter for both step up and step down operation. The proposed converter was designed to attain the following features;

i) To ensure sinusoidal input current wave shape for close to unity power factor operation.
ii) To achieve conversion efficiency more than 90% for all the duty cycles.
iii) To maintain the THD of input current according to the standard IEEE-519 [3].
iv) To develop converter topology for step-up and step-down operation with suitable control mechanism and achieve fast dynamic response.

1.5 Thesis Organization

This study focuses on development of a novel Single Phase non-isolated AC-DC Zeta Converter to improve efficiency, input PF and reduce THD of the system.

- In chapter 2, open-loop analysis of conventional AC-DC converters are done with the variation of duty cycle.
- In chapter 3, working principle of proposed converter is analyzed. Ideal voltage gain expression of proposed converter is obtained in this chapter. Voltage gain, overall efficiency, input power factor and total harmonic distortion (THD) are analyzed with variation of duty cycle, load and frequency. Simulation results are also provided.
- In chapter 4, comparison between proposed and conventional converter is shown. Both numerical values and graphical representations are provided.
- In chapter 5, details of feedback controller of proposed converter is analyzed. Small signal transfer function is obtained for the converter. The dynamic

response of the converter is inspected and related simulation results are also provided.

- In chapter 6, the conclusion and the concise summary of the thesis is given. Some recommendations have also been provided along with discussing scopes of future works.

Chapter 2
AC-DC Switched Mode Converters

2.1 Conventional AC-DC topologies

There are various topologies investigated for AC-DC conversion process. On the basis of how the devices are switched there are three types of converters.

i) **Line frequency converter:** Here, the devices are switched on and off at line frequencies of 50 or 60Hz.
ii) **Switching converters:** Here, the controllable switches in the converter are turned on and off at a frequency higher than line frequency. Modern power electronic switches (e.g. BJT, MOSFET, IGBT etc.) can operate at high frequencies. By applying higher switching frequency, we can reduce the size of inductors and capacitors. In addition to that, the dynamic characteristics of converters improve with the increase of operating frequencies.
iii) **Resonant converters:** Here, the controllable switches are turned on and off at zero voltage or zero current.

Switched mode AC-DC converters have different configurations and thus classified into six main topologies. They are:

1. AC-DC Buck Converter
2. AC-DC Boost Converter
3. AC-DC Buck-Boost Converter
4. AC-DC Cûk Converter
5. AC-DC SEPIC Converter
6. AC-DC ZETA Converter

2.2 AC-DC Buck Converter

The step-down AC-DC converter, commonly known as a buck converter, is shown in Figure 2.1. The buck converter is used in power electronics system to step down the

input voltage signal from a higher potential to a lower potential. The circuit consists of an inductor to store energy. The switch is used to control the power flow. An input filter is used with the conventional circuit to reduce harmonics. Typical waveforms of the converter are shown in Figure 2.2. It can be seen that the input current (Iin) has high harmonic components. The output voltage is below the average input voltage, thus Buck mode of operation is achieved.

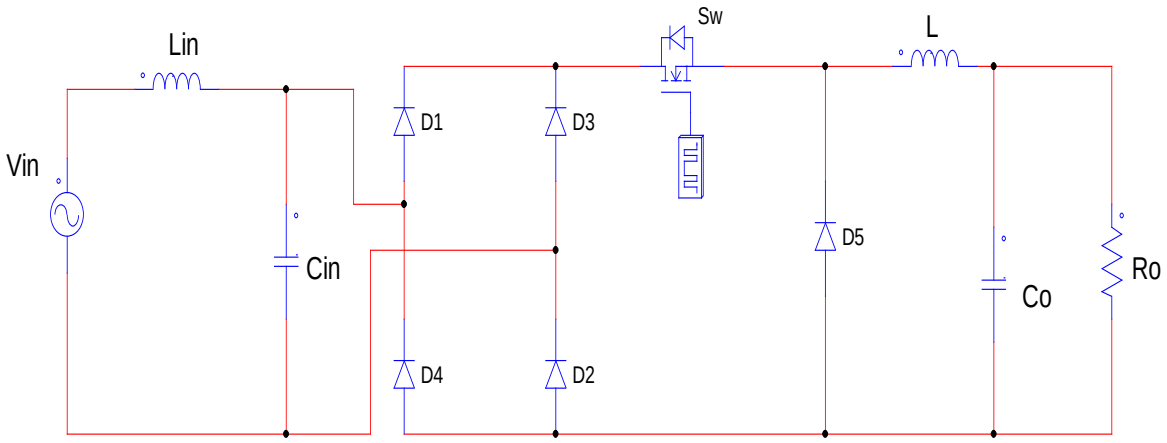


Figure 2.1: Single phase AC-DC Buck converter

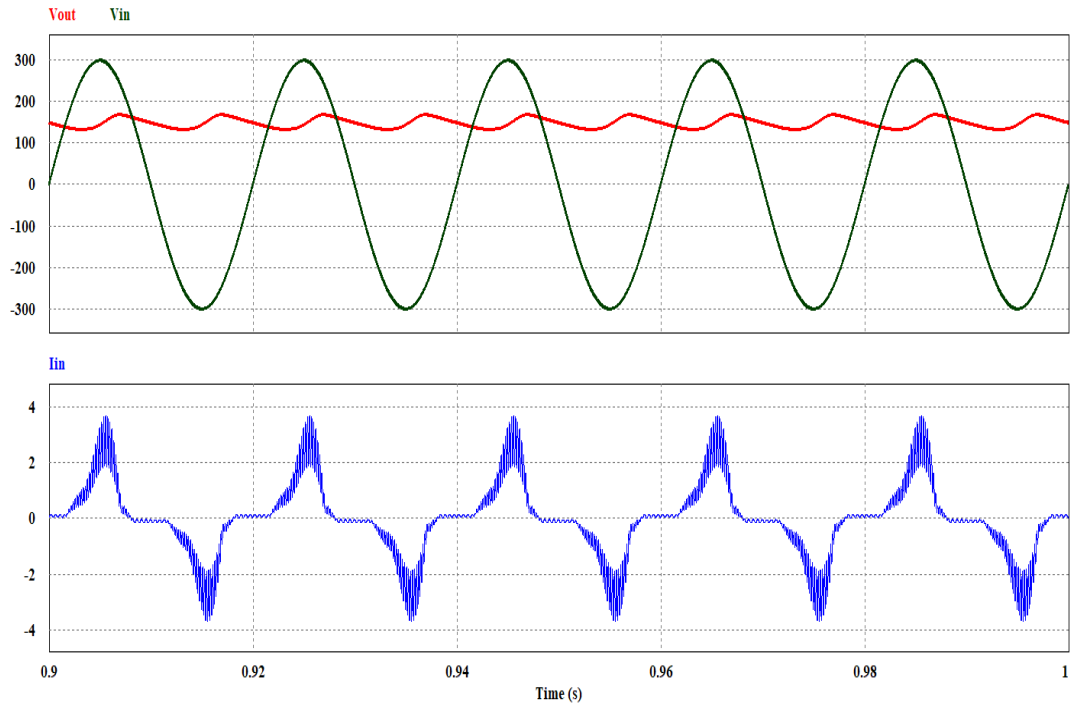


Figure 2.2: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional Buck converter at 50% duty cycle

2.2.1 Open loop analysis of AC-DC Buck Converter

The simulation of the conventional AC-DC Buck converter with input filter has been performed using PSIM software. The simulation results obtained are presented in Table 2.2. Here MOSFET is acting as the switching device. The value of different circuit components are tabulated in Table 2.1. The parameter values are taken from [93] and throughout the book same reference are used for different topologies.

Table 2.1 Parameters used for AC-DC Buck converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L)	5mH
Capacitance (Cin)	1 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.2 Performance Analysis of AC-DC Buck Converter under Duty Cycle Variation

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average Output Voltage (V)**	**Voltage Gain**
0.1	81.74	22.78	0.57	29.38	0.14
0.2	94.22	42.12	0.82	58.87	0.28
0.3	96.61	53.28	0.84	89.01	0.42
0.4	97.36	61.87	0.83	119.30	0.56
0.5	97.63	68.79	0.82	149.00	0.70
0.6	97.76	73.61	0.80	177.30	0.84
0.7	97.81	75.92	0.78	203.62	0.96
0.8	97.81	77.58	0.77	227.93	1.07
0.9	97.83	77.78	0.75	251.04	1.18

It can be seen from Table 2.2 that the THD of input current is high and power factor is also low for Buck converter. Efficiency of Buck converter is good for most of the duty cycles.

2.3 AC-DC Boost Converter

Boost converter is used in applications where the required output voltage is higher than input voltage. A full wave rectifier based single phase AC-DC Boost converter with input filter is shown in Figure 2.3. Here the inductor L stores and transfers energy to the load from input via diode bridge rectifier. When switch is ON inductor is charged and when switch is OFF inductor discharged its energy. An input filter on AC side is used to reduce the harmonics component of the system. MOSFET is used as switching device. Typical waveforms of input voltage, output voltage and input current are shown in Figure 2.4. It can be seen that the output voltage is higher than the input voltage for 50% duty cycle. The shape of input current is not in phase with input voltage, thus low input PF is achieved.

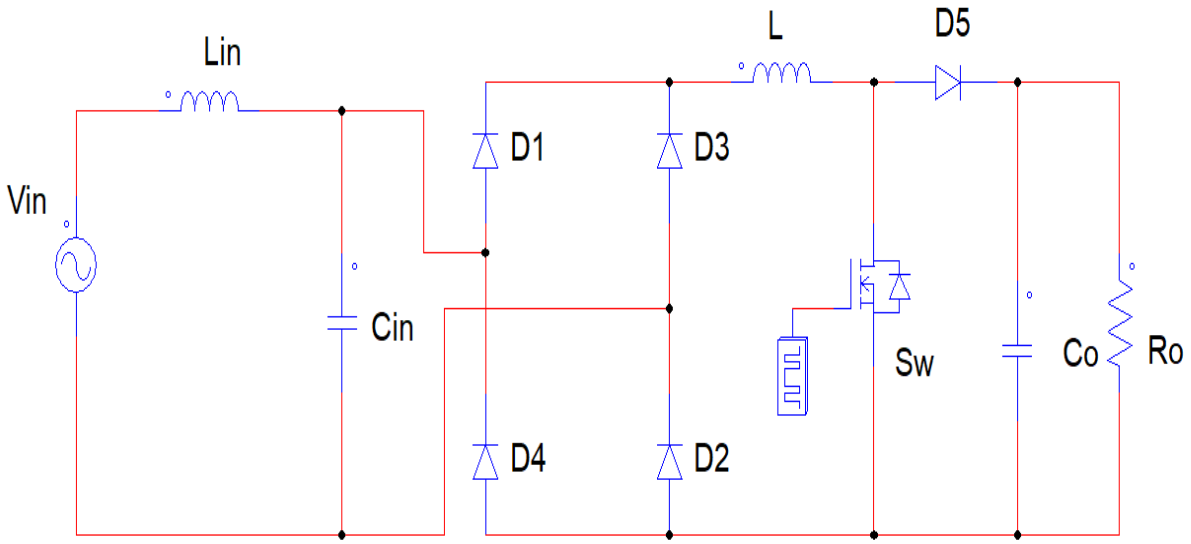


Figure 2.3: Single phase AC-DC Boost converter

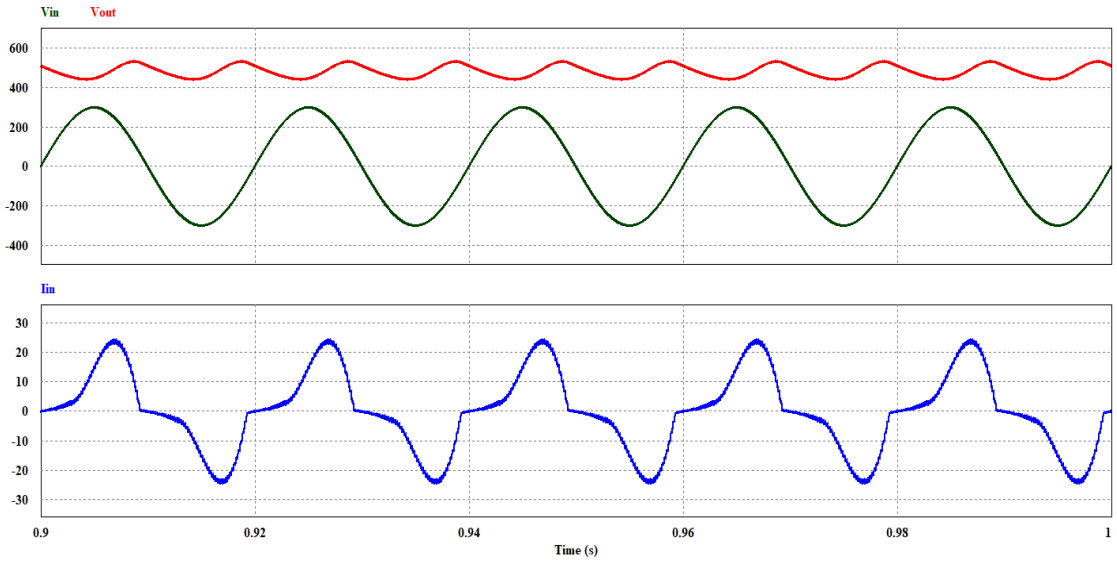


Figure 2.4: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional Boost converter at 50% duty cycle

2.3.1 Open loop analysis of AC-DC Boost Converter

The open loop simulation results are presented in Table 2.4. The value of different circuit components are tabulated in Table 2.3. It can be observed that the input PF is low and THD is also on the higher side for most duty cycle variations. The voltage gain is always greater than unity for boost mode of operation.

Table 2.3 Parameters used for AC-DC Boost converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L)	5mH
Capacitance (Cin)	1 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.4 Performance Analysis of AC-DC Boost Converter under Duty Cycle Variation

Duty cycle	Efficiency (%)	Input current THD (%)	Input Power Factor	Average Output Voltage (V)	Voltage Gain
0.1	98.78	70.01	0.76	303.02	1.43
0.2	98.76	61.65	0.78	335.31	1.58
0.3	98.74	54.03	0.80	375.01	1.77
0.4	98.72	47.19	0.81	424.02	2.00
0.5	98.70	40.94	0.81	485.10	2.29
0.6	98.65	34.11	0.79	562.24	2.65
0.7	98.57	25.21	0.74	660.19	3.11
0.8	98.41	13.00	0.63	771.75	3.64
0.9	97.87	9.00	0.40	839.83	3.96

2.4 AC-DC Buck-Boost Converter

Buck-Boost converter can provide both step up and step down output. The conventional Buck-Boost converter provides output voltage that has negative polarity; thus it's called inverting Buck-Boost converter. If the duty cycle is less than 50% then the converter works in Buck mode and it the duty cycle is more than 50% then it works in Boost mode.

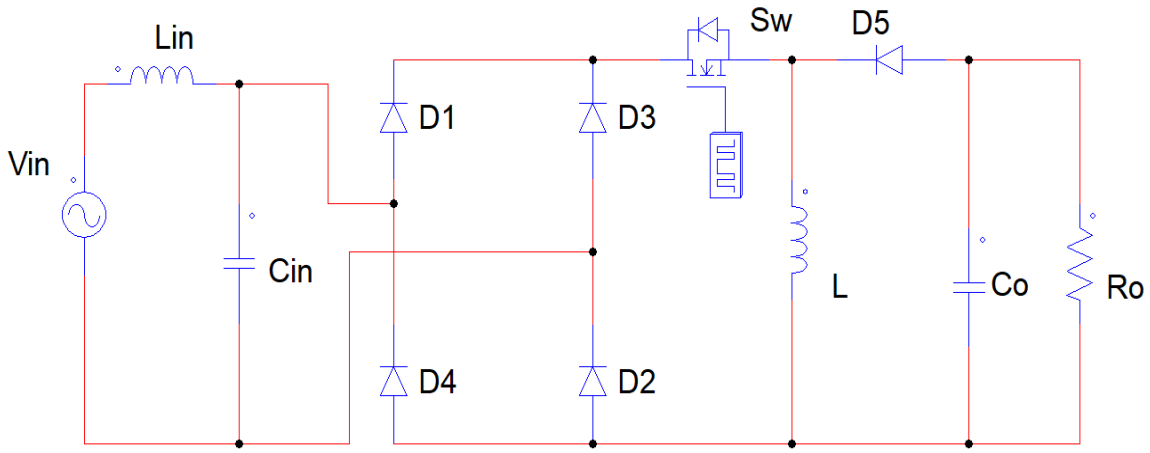


Figure 2.5: Single phase AC-DC Buck-Boost converter

Typical waveforms of input voltage, output voltage and input current are shown in Figure 2.6. The output voltage is negative as there is phase difference between input and output. Input current, Iin has high harmonic components and THD is high.

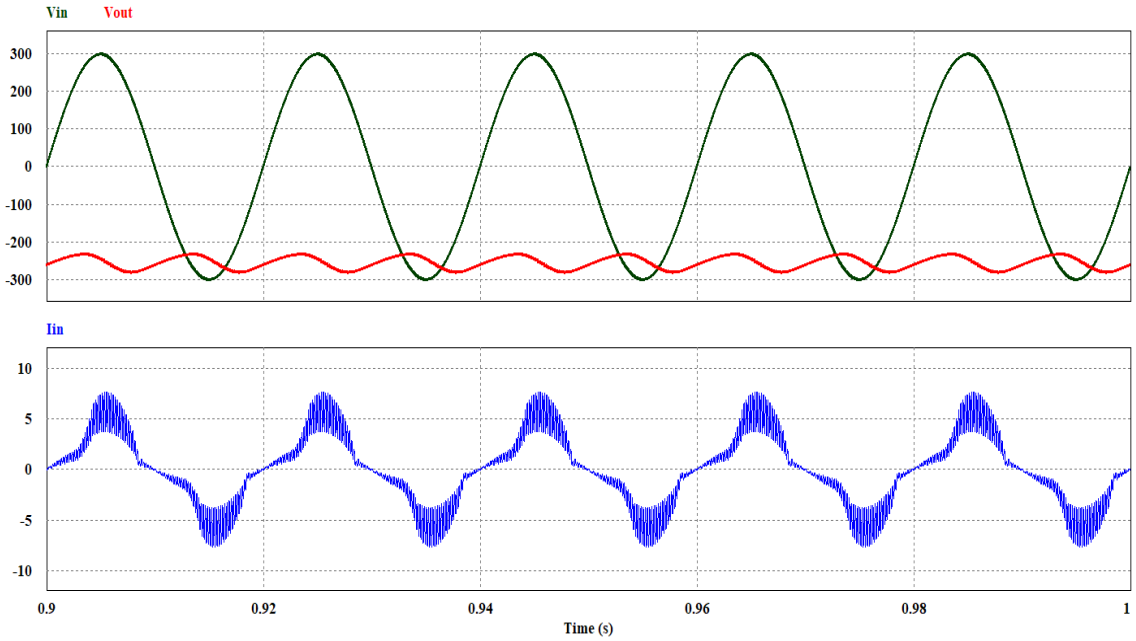


Figure 2.6: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional Buck-Boost converter at 50% duty cycle

2.4.1 Open loop analysis of AC-DC Buck-Boost Converter

The open loop simulation results of Buck Boost converter with input filter are presented in Table 2.6. The value of different circuit components are tabulated in Table 2.5.

Table 2.5 Parameters used for AC-DC Buck-Boost converter

Parameters	Value
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L)	5mH
Capacitance (Cin)	1 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.6 Performance Analysis of AC-DC Buck-Boost Converter under Duty Cycle Variation

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average Output Voltage (V)**	**Voltage Gain**
0.1	80.64	26.89	0.64	32.26	0.15
0.2	93.39	45.20	0.85	72.44	0.34
0.3	95.66	50.96	0.87	123.89	0.58
0.4	96.05	51.88	0.87	191.32	0.90
0.5	95.77	40.28	0.92	254.27	1.20
0.6	95.09	30.83	0.94	316.79	1.49
0.7	94.14	23.25	0.94	412.53	1.94
0.8	91.97	13.93	0.89	564.07	2.66
0.9	84.69	10.57	0.79	882.19	4.16

It can be observed from Table 2.6 that the input PF good for some duty ratios and THD is low for high duty ratios. Conversion efficiency of this converter is good except for duty cycle 0.1 and 0.9.

2.5 AC-DC Cûk Converter

A single phase Cûk converter is presented in Figure 2.7. DC-DC Cûk converter is connected with full bridge diode rectifier and MOSFET is used for high frequency switching. Cûk converter provides output voltage that is higher or lower than input voltage, but the polarity is negative like Buck-Boost topology. Cûk topology is a fourth order converter that has two inductors and two capacitors in DC-DC stage. Input filter is used for reduced EMI and harmonics effect. Typical waveforms of input voltage, output voltage and input current are shown in Figure 2.8. The output voltage has negative polarity whereas the input current, Iin has high harmonic components and THD is high for 50% duty cycle.

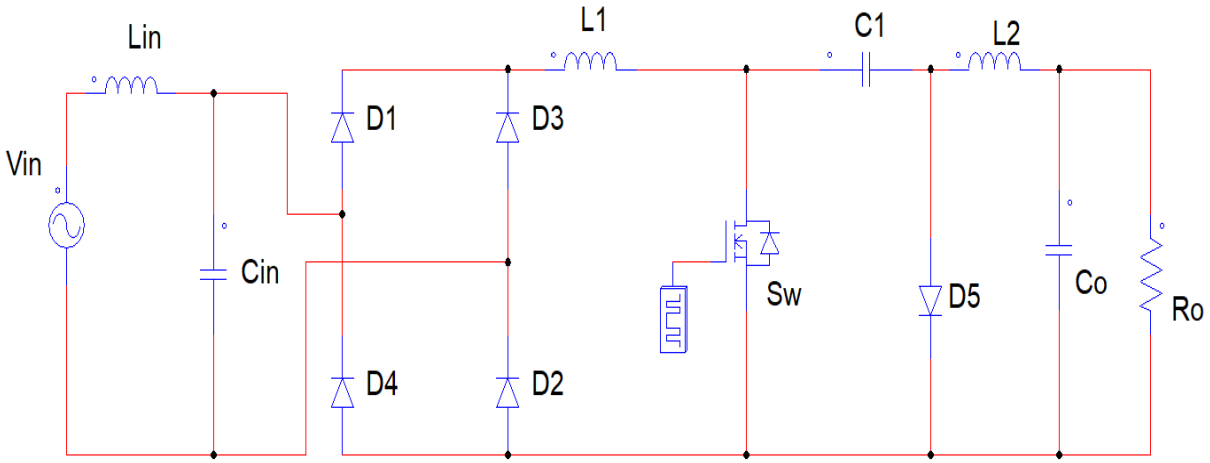


Figure 2.7: Single phase AC-DC Cûk converter

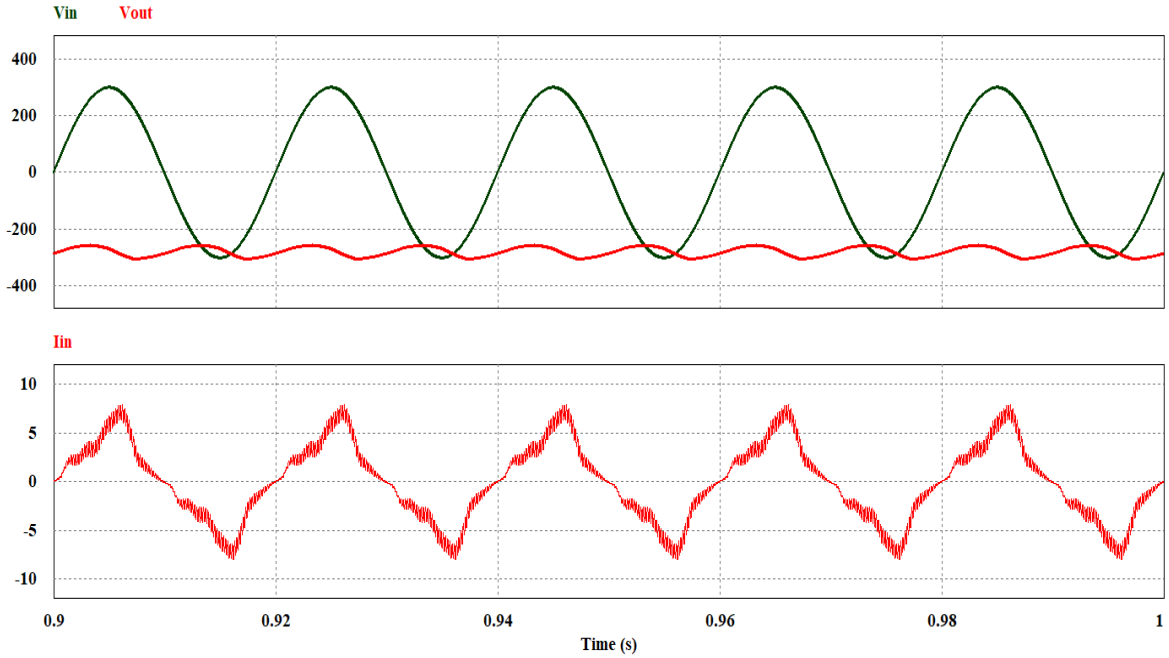


Figure 2.8: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional Cûk converter at 50% duty cycle

2.5.1 Open loop analysis of AC-DC Cûk Converter

The open loop simulation results of Cûk converter with input filter are presented in Table 2.8. The value of different circuit components are tabulated in Table 2.7. It can be observed that the input PF is good for some duty ratios and THD is low for high duty ratios. Conversion efficiency is good for all duty cycles except very low duty cycle of 0.1.

Table 2.7 Parameters used for AC-DC Cûk converter

Parameters	Value
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L1)	5mH
Inductor (L2)	5mH
Capacitance (Cin)	1 µF
Capacitance (C1)	4.5 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.8: Performance Analysis of AC-DC Cûk Converter under Duty Cycle Variation

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average Output Voltage (V)**	**Voltage Gain**
0.1	90.62	38.54	0.79	51.78	0.24
0.2	96.07	34.79	0.90	101.68	0.48
0.3	97.43	27.26	0.93	152.76	0.72
0.4	97.85	21.52	0.93	203.89	0.96
0.5	98.23	29.89	0.90	279.72	1.32
0.6	98.34	36.40	0.87	394.46	1.86
0.7	98.25	31.92	0.83	544.42	2.57
0.8	97.88	18.03	0.72	729.18	3.44
0.9	96.40	9.08	0.44	839.52	3.96

2.6 AC-DC SEPIC Converter

Single-ended primary-inductor converter (SEPIC) is a type of AC-DC converter which can provide voltage at output to be greater than or less than voltage at input. SEPIC topology is similar to conventional Buck-Boost converter, but has advantages of having non-inverted output voltage. Switching device within the converter controls the output

voltage of the SEPIC converter. Figure 2.9 shows a conventional SEPIC converter. It can be seen from Figure 2.10 that the output voltage has same polarity as input voltage. The input current has high harmonic components, thus THD is high.

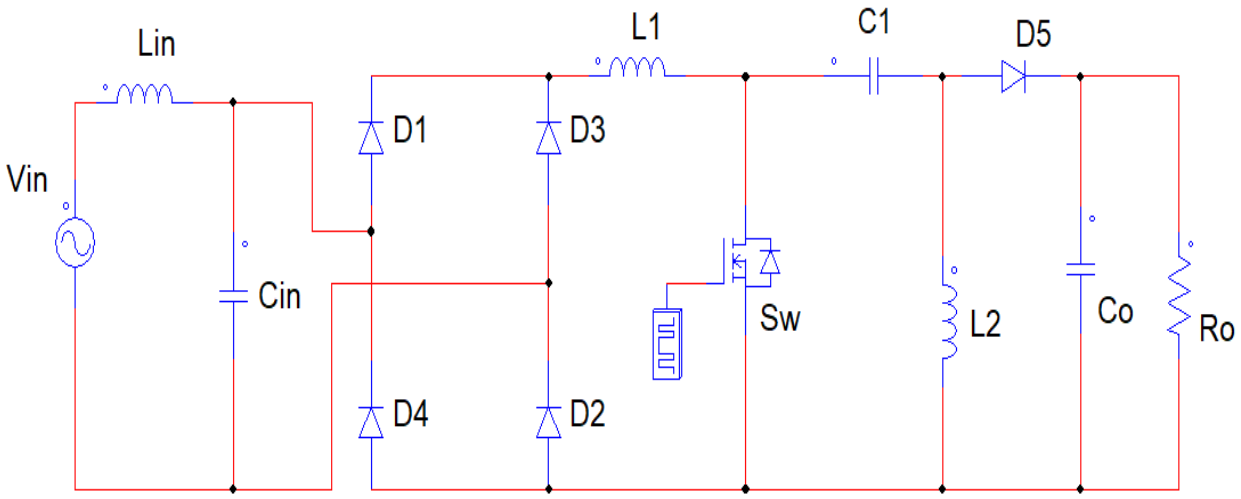


Figure 2.9: Single phase AC-DC SEPIC converter

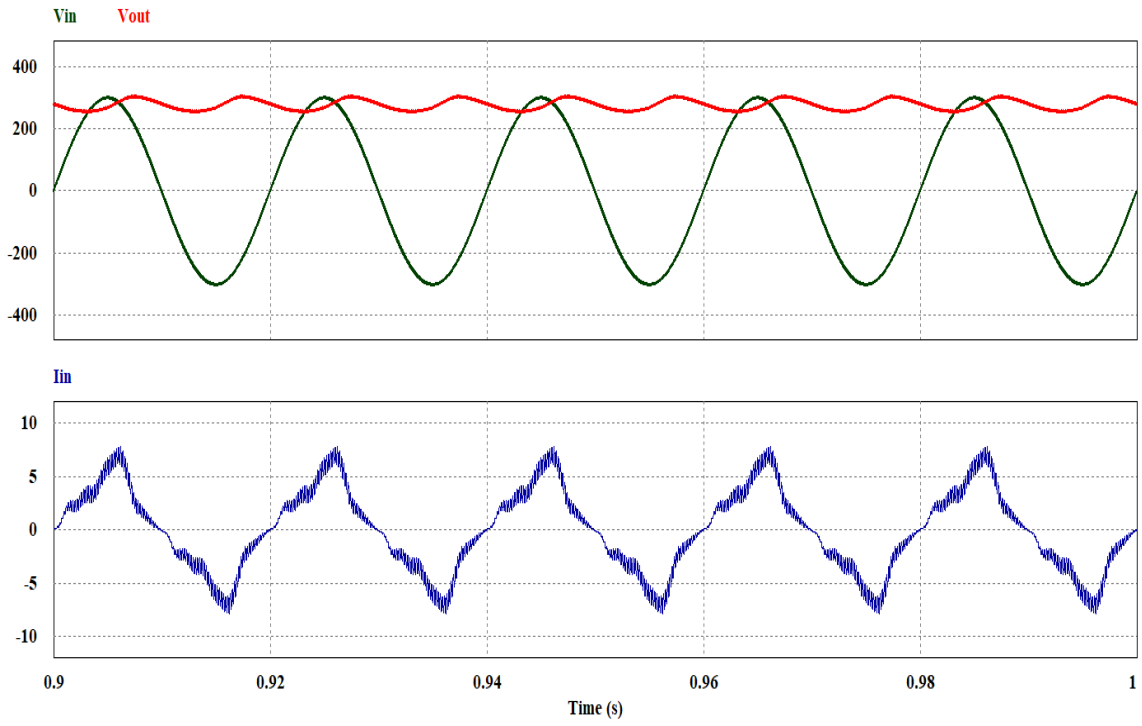


Figure 2.10: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional SEPIC converter at 50% duty cycle

2.6.1 Open loop analysis of AC-DC SEPIC Converter

The open loop simulation results of SEPIC converter with input filter are presented in Table 2.10. The value of different circuit components are tabulated in Table 2.9. It can be observed that the input PF is good for some duty ratios and THD is low only for high duty ratios. Conversion efficiency is found good for all duty cycles except 0.1.

Table 2.9 Parameters used for AC-DC SEPIC converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5 mH
Inductor (L1)	5 mH
Inductor (L2)	5 mH
Capacitance (Cin)	1 µF
Capacitance (C1)	4.5 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.10: Performance Analysis of AC-DC SEPIC Converter under Duty Cycle Variation

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average Output Voltage (V)**	**Voltage Gain**
0.1	90.88	38.57	0.80	51.77	0.24
0.2	96.26	34.95	0.91	101.65	0.48
0.3	97.51	27.54	0.94	152.30	0.72
0.4	97.93	21.69	0.93	203.50	0.96
0.5	98.29	29.12	0.91	277.96	1.31
0.6	98.39	36.12	0.88	393.43	1.85
0.7	98.28	31.83	0.84	544.47	2.57
0.8	97.90	18.09	0.72	730.67	3.44
0.9	96.39	9.08	0.44	839.61	3.96

2.7 AC-DC Zeta converter

Zeta converter, also known as inverse SEPIC converter, is a fourth order converter that can provide both step up and step down output voltage. Figure 2.11 shows a conventional AC-DC Zeta converter with input filter. MOSFET is used as switch for this circuit. Typical waveforms of input voltage, output voltage and input current are shown in Figure 2.12. The output voltage has same polarity as input voltage. The waveform of input current has high harmonic components.

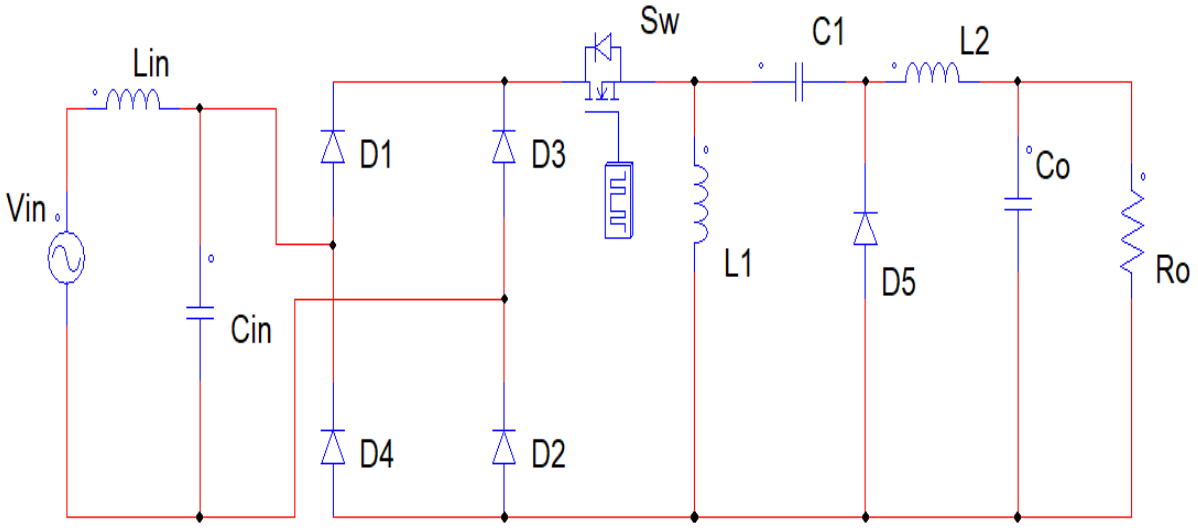


Figure 2.11: Single phase AC-DC Zeta converter

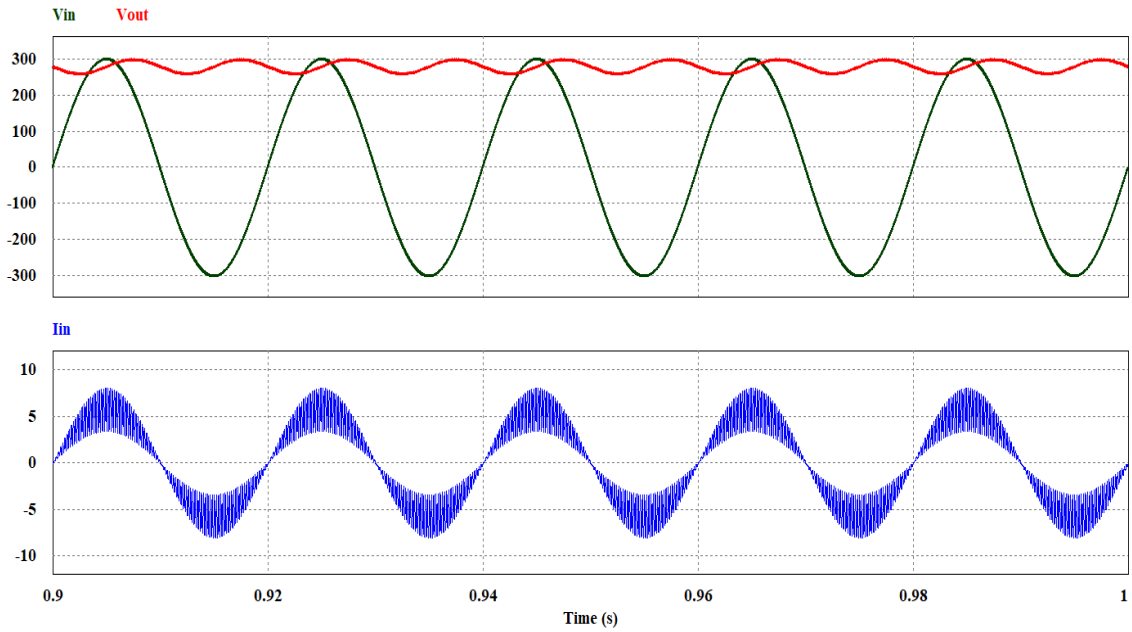


Figure 2.12: Input and output voltage (upper Figure) and input current (lower Figure) of the conventional Zeta converter at 50% duty cycle

2.7.1 Open loop analysis of AC-DC Zeta Converter

The open loop simulation results of Zeta converter with input filter are presented in Table 2.12. The value of different circuit components are tabulated in Table 2.11. It can be observed that the input PF is good for most of the duty ratios. THD is within tolerable limit for most of the duty ratios. Conversion efficiency is found good for all duty cycles.

Table 2.11: Parameters used for AC-DC Zeta converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5 mH
Inductor (L1)	2 mH
Inductor (L2)	2 mH
Capacitance (Cin)	1 µF
Capacitance (C1)	10 µF
Output capacitance (Co)	220 µF
Load Resistor (Ro)	100 ohm

Table 2.12: Performance Analysis of AC-DC Zeta Converter under Duty Cycle Variation

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average Output Voltage (V)**	**Voltage Gain**
0.1	94.95	37.01	0.90	68.29	0.32
0.2	96.19	35.48	0.94	149.79	0.71
0.3	94.91	33.66	0.95	223.03	1.05
0.4	95.10	32.13	0.95	246.02	1.16
0.5	94.58	28.60	0.96	281.70	1.33
0.6	95.12	23.30	0.97	336.05	1.58
0.7	95.76	18.82	0.97	444.57	2.10
0.8	96.63	17.24	0.95	645.34	3.04
0.9	95.79	6.82	0.74	950.46	4.48

Chapter 3
Proposed single-phase AC-DC Zeta Converter

A novel single phase single switch bridgeless Zeta AC-DC converter is proposed in this chapter. PSIM professional software is used for simulation of the proposed converter. The operation of the topology is described in this chapter. The waveforms of input voltage (V_{in}), output voltage (V_o) and input current (I_{in}) are given. Detailed data table the proposed converter are tabulated in this chapter for different duty ratio. Also, comparison between conventional and proposed converter is shown for different load and switching frequency variation.

3.1 Proposed AC-DC Zeta converter

The proposed converter is shown in Figure 3.1. This single phase single switch AC-DC Zeta converter can provide non-inverting output voltage in both step up and step down modes. This topology has no isolation between source and load. There are five inductors (Lin, L1, L2, L3 and L4), five capacitors (Cin, C1, C2, C3 and C4), six diodes and a MOSFET switch (S1) in this topology. Input inductor (Lin) and capacitor (Cin) act as input filter for this circuit. C3 and C4 are output capacitor. Resistor R_0 is used as load.

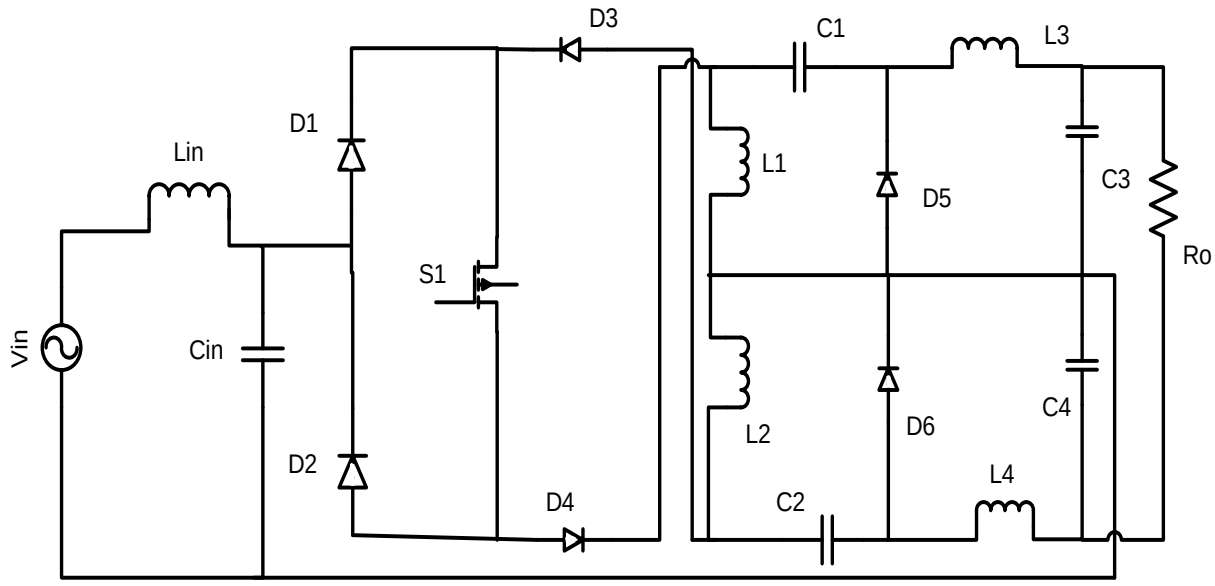
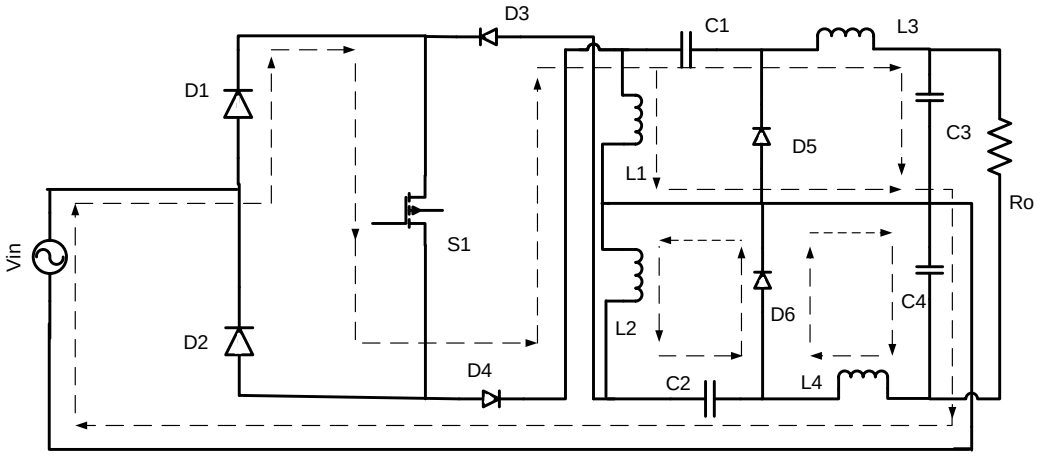


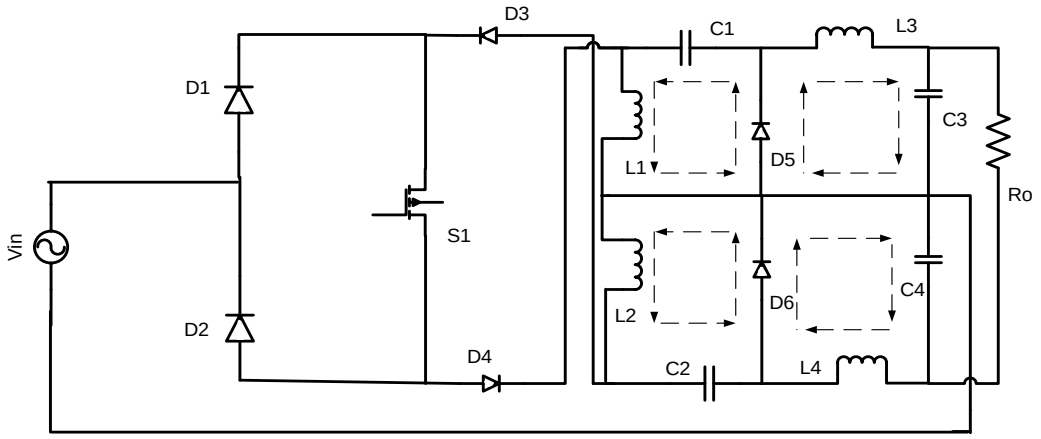
Figure 3.1: Proposed single phase single switch AC-DC converter

3.2 Principle of Operation

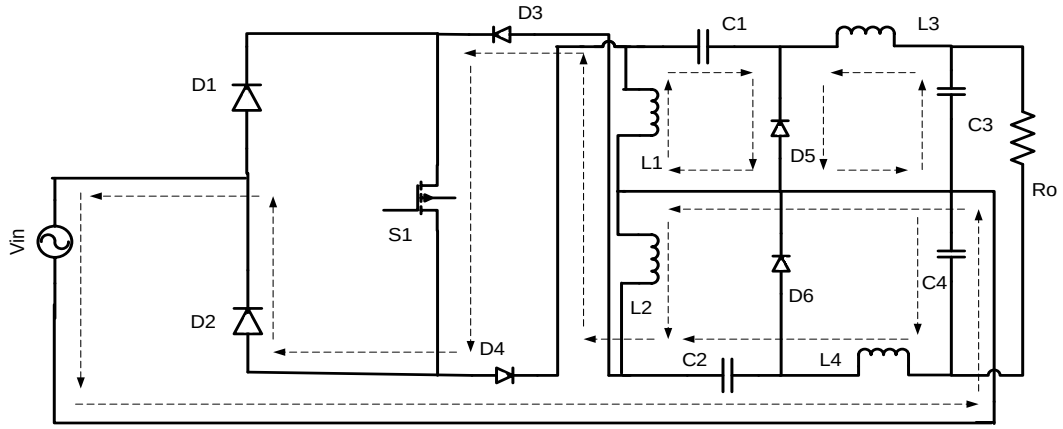
The proposed AC to DC converter has four operating states – positive and negative half cycles each with switch ON and OFF condition. The four modes of operation of the proposed converter are provided in the figures 3.2 (a) - 3.2 (d).



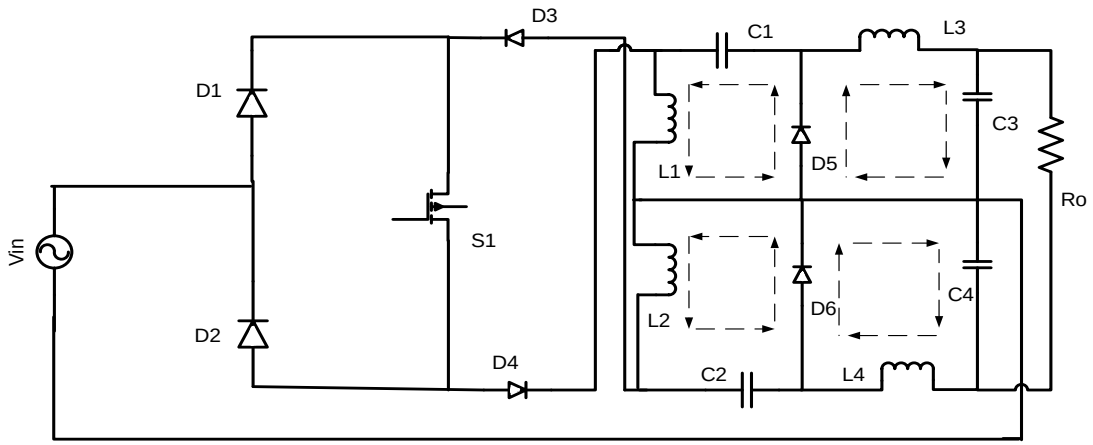
(a)



(b)



(c)



(d)

Figure 3.2: Four Modes of Operation of Proposed Converter; (a) Mode 1: Proposed circuit in positive half cycle when S1 is ON (b) Mode 2: Proposed circuit in positive half cycle when S1 is OFF (c) Mode 3: Proposed circuit in negative half cycle when S1 is ON (d) Mode 4: Proposed circuit in negative half cycle when S1 is OFF.

Mode 1: When S1 is on for positive half cycle, D1 and D4 is ON whereas D2 and D3 is OFF. Inductor L1 and L3 is charged. C2 and L2 creates a loop, and L4 and C4 also creates a loop as D6 is ON.

Mode 2: When switch S1 is OFF for positive half cycle of input, Vin is isolated from the main circuit. C3 and C4 is charged by L3 and L4 respectively.

Mode 3: When S1 is on for negative half cycle, diode D1 and D4 is OFF whereas D2 and D3 is ON. L2 and L4 is charged in this cycle.

Mode 4: For negative cycle and S1 OFF condition, source is isolated from the main circuit. C3 and C4 is charged again by L3 and L4 respectively.

3.3 Volt second balance of proposed converter

Ideal voltage gain expression is obtained for the proposed converter without input filter. When switch S1 is ON, the voltage across inductor L1 is

$$v_{L1} = v_{in} \tag{3.1}$$

When switch is OFF,

$$v_{L1} = v_{C1} \tag{3.2}$$

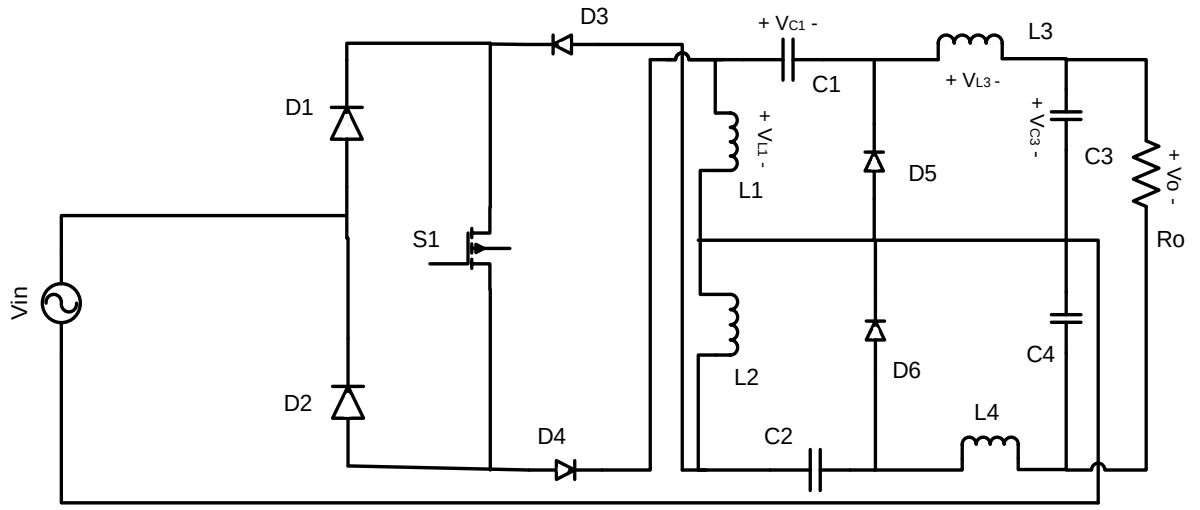


Figure 3.3: Proposed converter showing voltage across L1, C1, L3, C3 and V_O

Volt-sec balance over one switching cycle will not be equal to zero since the input signal is sinusoidal. Volt-sec balance for one switching cycle can be written as

$$\int_{ti}^{t_i+T_{sw}} v_{L1}\, dt = \int_{t_i}^{t_i+DT_{sw}} v_{in}\, dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{C1}\, dt \tag{3.3}$$

Here T_{sw} is switching time period and DT_{sw} is switch ON time.

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^{N} \int_{ti}^{t_i+T_{sw}} v_{L1}\, dt = 0$$

$$\Rightarrow \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} v_{in}\, dt + \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{C1}\, dt = 0 \tag{3.4}$$

Suppose,

$$v_{in} = V_{inmax} \sin(\omega t - \theta_{in})$$

$$v_{C1} = V_{C1max} \sin(\omega t - \theta_{C1})$$

Now from equation (3.4), we obtain

$$\sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} v_{in}\, dt = \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -v_{C1}\, dt$$

$$\Rightarrow \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} V_{in\,max} \sin(\omega t - \theta_{in})dt = \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -V_{C1max} \sin(\omega t - \theta_{C1})\, dt$$

$$\Rightarrow \sum_{n=1}^{N} [-\frac{V_{in\,max}}{\omega} \cos(\omega t - \theta_{in})]_{t_i}^{t_i+DT_{sw}} = \sum_{n=1}^{N} -\Big[-\frac{V_{C1max}}{\omega} \cos(\omega t - \theta_{C1})\Big]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\Rightarrow \sum_{n=1}^{N} V_{in\,max} [\cos(\omega t - \theta_{in})]_{t_i}^{t_i+DT_{sw}} = \sum_{n=1}^{N} -V_{C1max} [\cos(\omega t - \theta_{C1})]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\Rightarrow \sum_{n=1}^{N} V_{in\,max}[\cos(\omega t_i + \omega DT_{sw} - \theta_{in}) - \cos(\omega t_i - \theta_{in})]$$

$$= \sum_{n=1}^{N} -V_{C1max}\ [\cos(\omega t_i + \omega T_{sw} - \theta_{C1}) - \cos(\omega t_i + \omega DT_{sw} - \theta_{C1})$$

[Using trigonometric identity, $\cos A - \cos B = 2 \sin \frac{A+B}{2}\ sin \frac{B-A}{2}$]

$$\Rightarrow \sum_{n=1}^{N} 2\, V_{in\,max} \sin\Big(\omega t_i - \theta_{in} + \frac{\omega DT_{sw}}{2}\Big) \sin(-\frac{\omega DT_{sw}}{2})$$

$$= \sum_{n=1}^{N} -2\, V_{C1\,max} sin(\frac{\omega T_{sw} + \omega DT_{sw}}{2} + \omega t_i - \theta_{C1}) \sin(\frac{\omega DT_{sw} - \omega T_{sw}}{2})$$

$$\Rightarrow \sum_{n=1}^{N} -V_{in\,max} \sin\Big(\omega t_i - \theta_{in} + \frac{\omega DT_{sw}}{2}\Big) \sin(\frac{\omega DT_{sw}}{2})$$

$$= \sum_{n=1}^{N} V_{C1max} \sin(\frac{\omega T_{sw} + \omega DT_{sw}}{2} + \omega t_i - \theta_{C1}) \sin\frac{\omega T_{sw}(1-D)}{2}$$

$$\Rightarrow \sum_{n=1}^{N} V_{C1\,max} \sin(\frac{\omega T_{sw}(1+D)}{2} + \omega t_i - \theta_{C1})$$

$$= \frac{\sin(\frac{\omega DT_{sw}}{2})}{\sin\frac{\omega T_{sw}(1-D)}{2}} \times \sum_{n=1}^{N} - V_{in\,max} \sin\Big(\omega t_i - \theta_{in} + \frac{\omega DT_{sw}}{2}\Big)$$

$$\Rightarrow \sum_{n=1}^{N} V_{C1max} \sin(\frac{\omega T_{sw}(1+D)}{2} + \omega t_i - \theta_{C1})$$

$$= \frac{\frac{\sin\left(\frac{\omega D T_{sw}}{2}\right)}{\frac{\omega D T_{sw}}{2}} \times D}{\frac{\sin\frac{\omega T_{sw}(1-D)}{2}}{\frac{\omega T_{sw}(1-D)}{2}} \times (1-D)} * \sum_{n=1}^{N} -2\, V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right)$$

Using the following identities,

$i) \lim_{\theta \to 0} \frac{sin\theta}{\theta} = 1$ And

$ii) \frac{\omega D T_{sw}}{2} \to 0\ as\ T_{sw} \to 0$

$iii)\ \frac{\omega T_{sw}(1+D)}{2} \to 0\ as\ T_{sw} \to 0$

We get,

$$\Rightarrow \sum_{n=1}^{N} V_{C1max} \sin(\ \omega t_i - \theta_{C1}) = -\frac{D}{1-D} \times \sum_{n=1}^{N} V_{in\,max} \sin(\omega t_i - \theta_{in}) \qquad (3.5)$$

Again at the output stage for inductor L3,

When the switch is ON,

$$v_{L3} = v_{in} - v_{C1} - v_{C3} \qquad (3.6)$$

When the switch is OFF

$$v_{L3} = -v_{C3} \qquad (3.7)$$

The volt sec balance for one cycle can be expressed as

$$\int_{ti}^{t_i+T_{sw}} v_{L3}\ dt = \int_{t_i}^{t_i+DT_{sw}} (v_{in} - v_{C1} - v_{C3})\, dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -v_{C3}\, dt \qquad (3.8)$$

Again for N cycle of line frequency,

$$\sum_{n=1}^{N} \int_{ti}^{t_i+T_{sw}} v_{L3}\, dt = 0$$

$$\Rightarrow \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} (v_{in} - v_{C1} - v_{C3})\, dt + \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -v_{C3}\ dt = 0$$

$$\Rightarrow \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} (v_{in} - v_{C1} - v_{C3})\, dt = \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{C3}\ dt \qquad (3.9)$$

Suppose,

$$v_{C3} = V_{C3max} \sin(\omega t - \theta_{C3})$$

Then,

$$\sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} V_{in\,max} \sin(\omega t - \theta_{in}) dt - \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} V_{C1\,max} \sin(\omega t - \theta_{C1}) dt$$

$$- \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} V_{C3\,max} \sin(\omega t - \theta_{C3}) dt$$

$$= \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} V_{C3max} \sin(\omega t - \theta_{C3})\ dt$$

$$\Rightarrow \sum_{n=1}^{N} \left[-\frac{V_{in\,max}}{\omega} \cos(\omega t - \theta_{in})\right]_{t_i}^{t_i+DT_{sw}} + \sum_{n=1}^{N} \left[\frac{V_{C1\,max}}{\omega} \cos(\omega t - \theta_{C1})\right]_{t_i}^{t_i+DT_{sw}}$$

$$+ \sum_{n=1}^{N} \left[-\frac{V_{C3\,max}}{\omega} \cos(\omega t - \theta_{C3})\right]_{t_i}^{t_i+DT_{sw}}$$

$$= \sum_{n=1}^{N} \left[-\frac{V_{C3\,max}}{\omega} \cos(\omega t - \theta_{C3})\right]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\Rightarrow \sum_{n=1}^{N} V_{in\,max}[\cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega DT_{sw} - \theta_{in})]$$

$$- \sum_{n=1}^{N} V_{c1\,max}[\cos(\omega t_i - \theta_{C1}) - \cos(\omega t_i + \omega DT_{sw} - \theta_{C1})]$$

$$- \sum_{n=1}^{N} V_{C3\,max}[\cos(\omega t_i - \theta_{C3}) - \cos(\omega t_i + \omega DT_{sw} - \theta_{C3})]$$

$$= \sum_{n=1}^{N} V_{C3\,max}[\cos(\omega t_i + \omega DT_{sw} - \theta_{C3}) - \cos(\omega t_i + \omega T_{sw} - \theta_{C3})]$$

$$\Rightarrow \sum_{n=1}^{N} 2\, V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right) \sin\left(\frac{\omega D T_{sw}}{2}\right)$$
$$- \sum_{n=1}^{N} 2\, V_{C1\,max} \sin\left(\omega t_i - \theta_{C1} + \frac{\omega D T_{sw}}{2}\right) \sin\left(\frac{\omega D T_{sw}}{2}\right)$$
$$- \sum_{n=1}^{N} 2\, V_{C3\,max} \sin\left(\omega t_i - \theta_{C3} + \frac{\omega D T_{sw}}{2}\right) \sin\left(\frac{\omega D T_{sw}}{2}\right)$$
$$= \sum_{n=1}^{N} 2\, V_{C3\,max} sin\left(\frac{\omega T_{sw} + \omega D T_{sw}}{2} + \omega t_i - \theta_{C3}\right) \sin\left(\frac{\omega T_{sw} - \omega D T_{sw}}{2}\right)$$

$$\Rightarrow \sin\left(\frac{\omega D T_{sw}}{2}\right) \left[\sum_{n=1}^{N} V_{in\,max} \sin\left(\frac{\omega D T_{sw}}{2} + \omega t_i - \theta_{in}\right) - \sum_{n=1}^{N} V_{C1\,max} \sin\left(\frac{\omega D T_{sw}}{2}\right.\right.$$
$$\left.\left. + \omega t_i - \theta_{C1}\right) - \sum_{n=1}^{N} V_{C3\,max} \sin\left(\frac{\omega D T_{sw}}{2} + \omega t_i - \theta_{C3}\right)\right]$$
$$= \sin\left(\frac{(1-D)\omega T_{sw}}{2}\right) \times \sum_{n=1}^{N} V_{C3\,max} \sin\left(\omega t_i - \theta_{C3} + \frac{(1+D)\omega T_{sw}}{2}\right)$$

$$\Rightarrow \sum_{n=1}^{N} V_{C3max} \sin\left(\frac{\omega T_{sw}(1+D)}{2} + \omega t_i - \theta_{C3}\right)$$
$$= \frac{\dfrac{\sin\left(\frac{\omega D T_{sw}}{2}\right)}{\frac{\omega D T_{sw}}{2}} \times D}{\dfrac{\sin\frac{\omega T_{sw}(1-D)}{2}}{\frac{\omega T_{sw}(1-D)}{2}} \times (1-D)}$$
$$\times \left[\sum_{n=1}^{N} V_{in\,max} \sin\left(\frac{\omega D T_{sw}}{2} + \omega t_i - \theta_{in}\right) - \sum_{n=1}^{N} V_{C1\,max} \sin\left(\frac{\omega D T_{sw}}{2}\right.\right.$$
$$\left.\left. + \omega t_i - \theta_{C1}\right) - \sum_{n=1}^{N} V_{C3\,max} \sin\left(\frac{\omega D T_{sw}}{2} + \omega t_i - \theta_{C3}\right)\right]$$

Using following the identities,

$i) \lim_{\theta \to 0} \frac{sin\theta}{\theta} = 1$

$ii) \frac{\omega D T_{sw}}{2} \to 0\ as\ T_{sw} \to 0$

$iii)\ \frac{\omega T_{sw}(1+D)}{2} \to 0\ as\ T_{sw} \to 0$

We get,

$$\sum_{n=1}^{N} V_{C3max} \sin(\ \omega t_i - \theta_{C3}) = \frac{D}{1-D} \times \sum_{n=1}^{N} V_{in\ max} \sin(\ \omega t_i - \theta_{in}) - \frac{D}{1-D} \times \sum_{n=1}^{N} V_{C1\ max}\ \sin(\omega t_i - \theta_{C1})\ - \frac{D}{1-D} \times \sum_{n=1}^{N} V_{C3\ max}\ \sin(\omega t_i - \theta_{C3}) \quad (3.10)$$

Putting the value,

$$\sum_{n=1}^{N} V_{C1max} \sin(\ \omega t_i - \theta_{C1}) = -\ \frac{D}{1-D} \times \sum_{n=1}^{N} V_{in\ max} \sin(\omega t_i - \theta_{in})$$

And $V_{C3max}\ \sin(\omega t_i - \theta_{C3}) = \frac{1}{2} V_{omax} \sin(\omega t_i - \theta_o)$ in equation (3.10),

$$\Rightarrow \sum_{n=1}^{N} V_{C3max} \sin(\ \omega t_i - \theta_{C3}) + \frac{D}{1-D} \times \sum_{n=1}^{N} V_{C3\ max}\ \sin(\omega t_i - \theta_{C3}) = \frac{D}{1-D} \times \sum_{n=1}^{N} V_{in\ max} \sin(\ \omega t_i - \theta_{in}) + \frac{D}{1-D} \times \frac{D}{1-D} \times \sum_{n=1}^{N} V_{in\ max}\ \sin(\omega t_i - \theta_{in})$$

$$\Rightarrow \frac{1}{1-D} \times \sum_{n=1}^{N} \frac{1}{2} V_{0max} \sin(\omega t_i - \theta_0)\ = \frac{D}{(1-D)^2} \times \sum_{n=1}^{N} V_{in\ max}\ \sin(\omega t_i - \theta_{in})$$

$$\Rightarrow \sum_{n=1}^{N} V_{0\ max} \sin(\ \omega t_i - \theta_0) = \frac{2D}{1-D} \times \sum_{n=1}^{N} V_{in\ max} \sin(\omega t_i - \theta_{in})$$

Thus the average value of output voltage can be expressed as

$$V_{Oavg} = \frac{1}{\pi} \int_0^{\pi} V_{0\ max}\ sin\theta d\theta$$

$$\Rightarrow V_{Oavg} = \frac{1}{\pi} \int_0^{\pi} V_{in\ max} \times \frac{2D}{1-D}\ sin\theta d\theta$$

$$\Rightarrow V_{Oavg} = \frac{V_{in\ max}}{\pi} \times \frac{2D}{1-D}\ [-cos\theta]_0^{\pi}$$

$$\Rightarrow V_{Oavg} = \frac{2V_{in\,max}}{\pi} \times \frac{2D}{1-D} \tag{3.11}$$

The expression in equation (3.11) shows that the DC-DC conversion factor is $\frac{2D}{1-D}$ which allows both buck and boost mode of operation. The ideal voltage gain is compared with simulated results and tabulated in Table 3.1. Figure 3.4 shows graphical representation of theoretical and simulated voltage gains for duty cycle variation. For high duty ratios, the difference between the theoretical and simulated results is higher. But for low duty ratios both the gains are comparable.

Table 3.1: Voltage gain comparison under duty ratio variation

Duty cycle	**Voltage Gain (Theoretical)**	**Voltage Gain (simulation)**
0.1	0.20	0.25
0.2	0.45	0.57
0.3	0.77	0.95
0.4	1.20	1.33
0.5	1.80	1.63
0.6	2.70	2.05
0.7	4.21	2.66
0.8	7.21	3.38
0.9	16.22	4.68

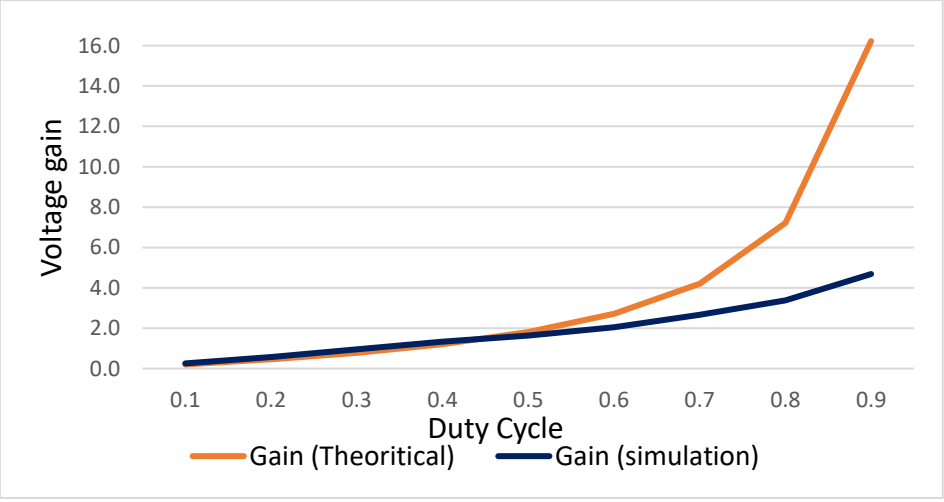


Figure 3.4: Voltage gain from theoretical and simulation results for duty cycle variation

3.4 Open loop analysis of proposed converter

The proposed converter is simulated for duty cycles 0.1 to 0.9. The circuit parameters are chosen suitably for better results in open loop analysis.

Table 3.2: Parameters used for proposed converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L1)	4 mH
Inductor (L2)	4 mH
Capacitance (Cin)	1 µF
Capacitance (C1)	10 µF
Capacitance (C2)	10 µF
Output capacitance (C3)	110 µF
Output capacitance (C4)	110 µF
Load Resistor (Ro)	100 ohm

Table 3.3: Performance of proposed converter for different duty ratio

Duty cycle	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Average voltage output (V)**	**Voltage Gain**
0.1	97.05	51.46	0.67	53.73	0.25
0.2	98.09	61.67	0.75	120.18	0.57
0.3	97.78	45.91	0.87	202.47	0.95
0.4	96.96	33.33	0.95	282.04	1.33
0.5	95.63	27.27	0.96	345.38	1.63
0.6	95.88	22.56	0.97	434.47	2.05
0.7	95.49	17.44	0.97	564.61	2.66
0.8	95.21	17.35	0.96	717.70	3.38
0.9	95.06	6.57	0.75	993.16	4.68

It is evident from the Table 3.2 that the proposed converter has efficiency range 95.06% to 98.09%. It has good efficiency for all duty cycles, which is a great attribute for a converter. Also it has good input PF except for some duty cycles. The proposed converter can give step down output up to 30% duty ratio and step up output for rest of the duty ratios. THD of input current decreased with the increase of duty cycles.

3.4.1 Open loop analysis under load variation

The load of proposed converter is varied from 50 ohm to 500 ohm for duty cycles D=0.3, D=0.5 and D=0.7 and results are shown in Table 3.4, Table 3.5 and Table 3.6 respectively.

Table 3.4: Performance under load variation of proposed converter for D=0.3

Load (Ω)	**Efficiency (%)**	**Input Current THD (%)**	**Input Power Factor**	**Average output voltage (V)**	**Voltage Gain**
50	97.05	44.92	0.88	148.03	0.70
100	97.78	45.91	0.87	202.47	0.95
150	96.79	48.90	0.87	243.54	1.15
200	96.68	52.01	0.87	276.25	1.30
250	96.76	41.07	0.92	283.67	1.34
300	96.53	34.84	0.94	289.82	1.37
350	96.24	33.07	0.94	301.27	1.42
400	96.11	33.02	0.94	321.63	1.52
450	95.88	33.01	0.94	340.75	1.61
500	95.72	33.01	0.94	358.89	1.69

Table 3.5: Performance under load variation of proposed converter for D=0.5

Load (Ω)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Average output voltage (V)	Voltage Gain
50	96.08	27.63	0.96	240.84	1.14
100	95.63	27.27	0.96	345.38	1.63
150	95.67	27.46	0.96	424.55	2.00
200	95.42	27.55	0.96	490.80	2.31
250	95.23	27.62	0.96	547.99	2.58
300	95.02	27.70	0.96	598.19	2.82
350	94.70	27.78	0.96	644.54	3.04
400	94.67	27.91	0.96	686.30	3.24
450	94.44	28.09	0.96	723.81	3.41
500	94.25	28.19	0.96	755.78	3.56

Table 3.6: Performance under load variation of proposed converter for D=0.7

Load (Ω)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Average output voltage (V)	Voltage Gain
50	95.71	19.23	0.97	365.61	1.72
100	95.49	17.44	0.97	564.61	2.66
150	93.66	17.82	0.96	683.91	3.22
200	93.53	18.35	0.96	784.87	3.70
250	93.25	18.76	0.96	869.55	4.10
300	93.09	19.22	0.96	946.05	4.46
350	92.72	19.51	0.96	1015.09	4.79
400	92.64	19.82	0.96	1083.41	5.11
450	92.13	20.09	0.96	1145.36	5.40
500	92.14	20.28	0.96	1209.09	5.70

From table 3.4, table 3.5 and table 3.6, the key points are as follows

- With the increase of load, the proposed converter is capable of providing good efficiency for different duty cycles
- THD is decreased significantly with load for D=0.3
- Power factor is also improved for D=0.5 and remained almost unchanged for other duty cycles
- Output voltage is increased, hence the gain of the proposed converter also increased.

To analyze the effect of inductive load with the proposed converter, an R-L load is considered instead of purely resistive load. It is considered that an inductor value of 1m H is connected in series with 100 ohm as load. The Table 3.7 shows the performance of proposed converter under R-L load.

Table 3.7 : Performance under R-L load of proposed converter

Duty cycle	**Efficiency (%)**	**Input Current THD (%)**	**Input Power Factor**	**Average output voltage (V)**	**Voltage Gain**
0.1	95.45	54.33	0.68	53.58	0.25
0.2	97.88	61.41	0.74	120.01	0.57
0.3	98.14	45.79	0.87	204.36	0.96
0.4	98.40	33.39	0.95	282.10	1.33
0.5	98.45	27.29	0.96	353.98	1.67
0.6	97.55	22.59	0.97	431.95	2.04
0.7	96.88	17.43	0.97	577.56	2.72
0.8	96.44	17.44	0.96	714.21	3.37
0.9	95.66	6.50	0.75	1009.39	4.76

Now, the effect of R-L load shown in Table 3.7 and resistive load shown in Table 3.3 are compared and shown in Figure 3.5 to Figure 3.7.

It is evident from the Figure 3.5 to 3.7 that the inclusion of inductive load doesn't change the performance parameters significantly. The efficiency of proposed converter for R-L load is slightly higher than the purely resistive load. THD and input PF are almost similar for both R load and R-L load.

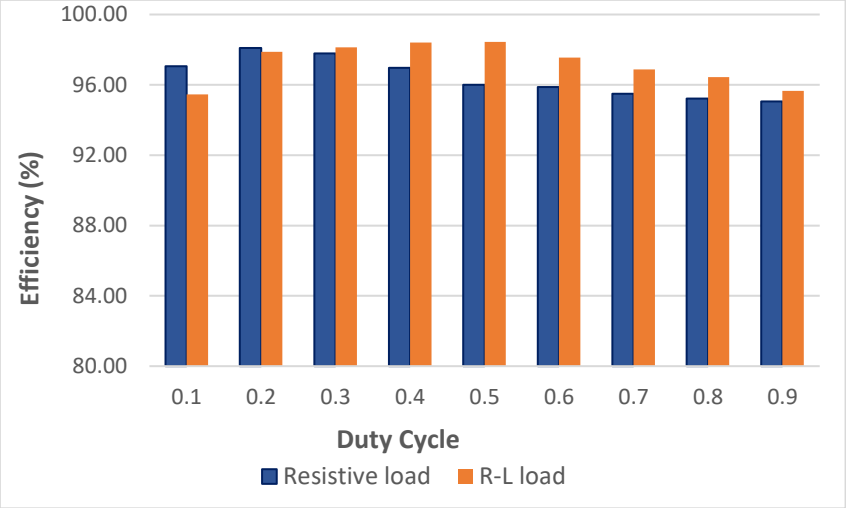


Figure 3.5: Comparison of efficiency between resistive load and R-L load for different duty cycles

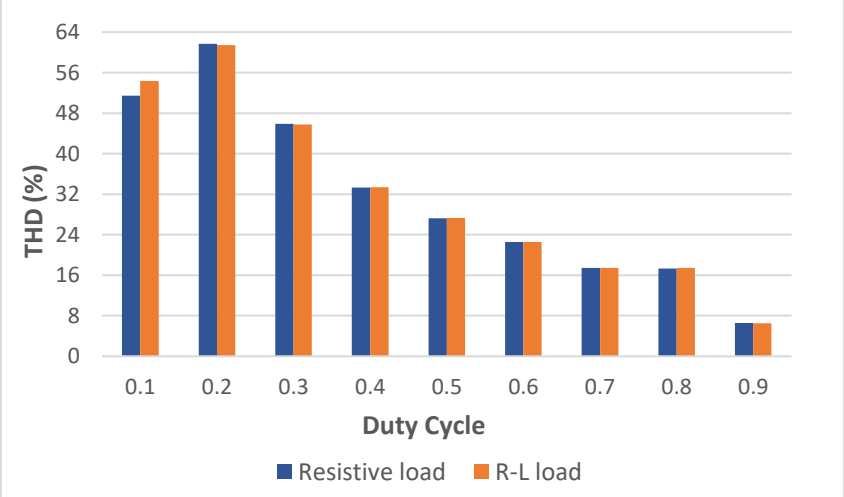


Figure 3.6: Comparison of THD between resistive load and R-L load for different duty cycles

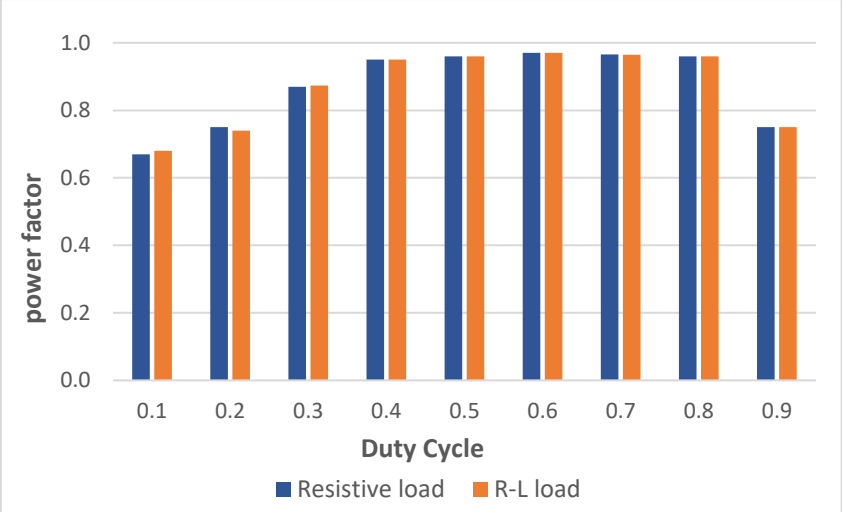


Figure 3.7: Comparison of input power factor between resistive load and R-L load for different duty cycles

3.4.2 Open loop analysis under switching frequency variation

The performance of proposed converter is tested under switching frequency variation. The switching frequency is varied from 5 kHz to 100 kHz for D=0.3, D=0.5 and D=0.7 and results are shown in Table 3.7, Table 3.8 and Table 3.9.

Table 3.8: Performance under frequency variation of proposed converter for D=0.3

Frequency (Hz)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Average output voltage (V)	Voltage Gain
5k	97.78	45.91	0.87	202.47	0.95
10k	97.16	63.98	0.68	166.89	0.79
20k	94.83	67.56	0.62	149.78	0.71
30k	91.78	67.02	0.61	144.40	0.68
40k	95.52	69.19	0.58	144.28	0.68
50k	94.49	69.50	0.58	143.27	0.68
60k	95.85	70.93	0.57	143.55	0.68
70k	96.24	70.55	0.57	143.13	0.67
80k	96.66	72.43	0.56	142.87	0.67
90k	96.98	70.98	0.56	142.62	0.67
100k	96.99	72.26	0.56	142.12	0.67

Table 3.9: Performance under frequency variation of proposed converter for D=0.5

Frequency (Hz)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Average output voltage (V)	Voltage Gain
5k	95.63	27.31	0.96	345.38	1.63
10k	95.85	38.75	0.90	418.86	1.97
20k	94.99	48.03	0.82	429.70	2.03
30k	92.96	49.94	0.81	417.01	1.97
40k	90.71	50.01	0.80	407.65	1.92
50k	89.87	51.40	0.80	403.23	1.90
60k	91.38	47.72	0.80	409.69	1.93
70k	92.54	49.56	0.80	413.30	1.95
80k	92.59	50.01	0.79	410.10	1.93
90k	94.19	49.33	0.79	419.06	1.98
100k	96.49	52.04	0.79	429.53	2.02

Table 3.10: Performance under frequency variation of proposed converter for D=0.7

Frequency (Hz)	Efficiency (%)	Input Current THD (%)	Input Power Factor	Average output voltage (V)	Voltage Gain
5k	95.49	17.44	0.97	564.61	2.66
10k	93.66	13.90	0.95	789.40	3.72
20k	90.64	17.11	0.95	904.53	4.26
30k	87.25	17.24	0.95	912.56	4.30
40k	90.26	17.70	0.95	956.38	4.51
50k	91.13	17.57	0.94	976.22	4.60
60k	93.28	17.72	0.94	995.42	4.69
70k	94.39	17.55	0.94	1008.80	4.76
80k	94.94	17.58	0.94	1014.97	4.78
90k	95.58	17.79	0.94	1023.19	4.82
100k	95.43	17.68	0.94	1024.46	4.83

From Table 3.7, Table 3.8 and Table 3.9, the key points are

- Efficiency doesn't decrease much with the increase of switching frequency for most of the cases.
- THD increased in most of the cases.
- PF is also decreased but in tolerable rate for high frequencies.
- Voltage gain is improved for D=0.5 and D=0.7 as they provide step up output
- Voltage gain is decreased for D=0.3 as it provides step down output.

3.5 Simulation Results

Typical input voltage (Vin), input current (Iin) and output voltage (Vo) waveforms of the proposed single-phase AC-DC Zeta converter topology is presented here. Figure 3.8 shows the typical input voltage waveform of the proposed converter. The input voltage has peak value of 300V (50 Hz). The subsequent sections illustrate waveforms of proposed converter for duty cycle variation, load variation and switching frequency variation.

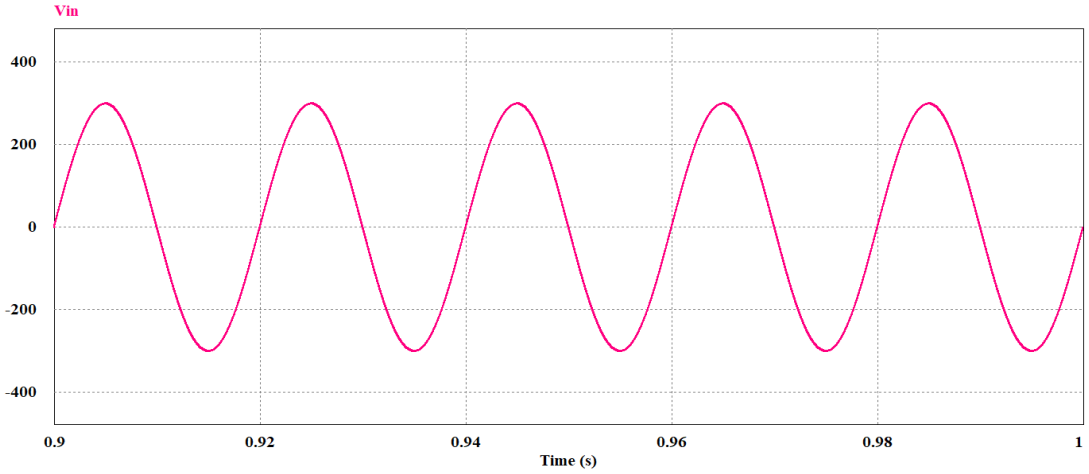


Figure 3.8: Typical input voltage waveform for proposed converter

3.5.1 Simulation results of proposed converter for duty cycle variation

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle 0.2, frequency 5 kHz and load 100 ohm in Figure 3.9-3.11. It can be observed from Figure 3.10 and 3.11 that the input current has high harmonic components.

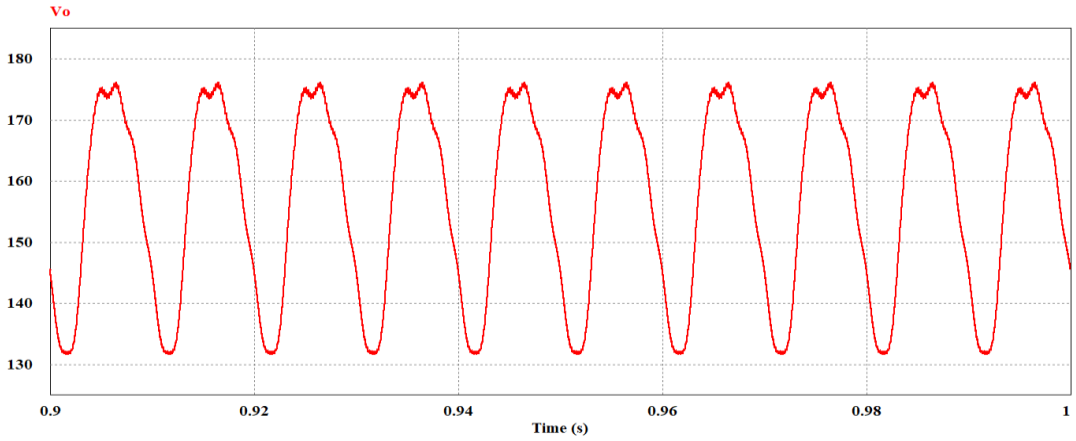


Figure 3.9: Waveform of output voltage of proposed converter at D=0.2, f_s=5 kHz and R_o=100 ohm.

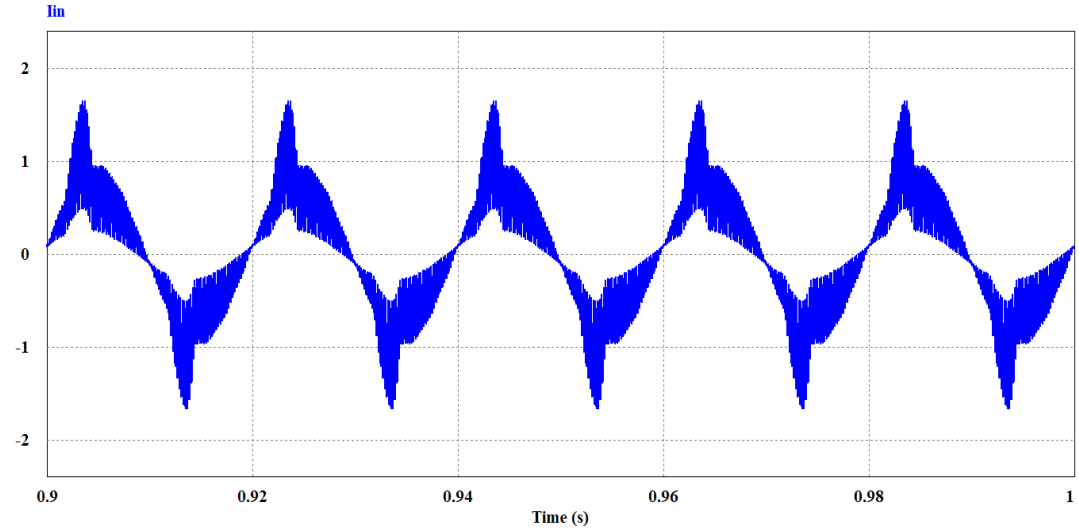


Figure 3.10: Waveform of input current of proposed converter at D=0.2, f_s=5 kHz and R_o=100 ohm.

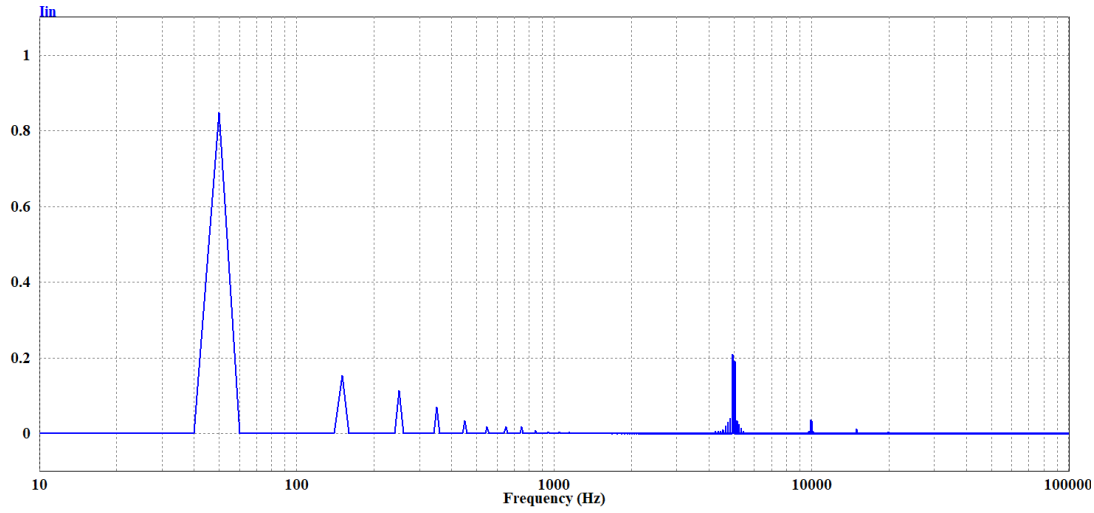


Figure 3.11: Input current spectrum of proposed converter at D=0.2, f_s=5 kHz and R_o=100 ohm.

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.8, frequency =5 kHz and load 100 ohm in Figure 3.12-3.14. The waveform of output voltage, Vo shows that the output voltage has high ripple peaks. The harmonic components of input current, Iin is lower compared to D=0.2.

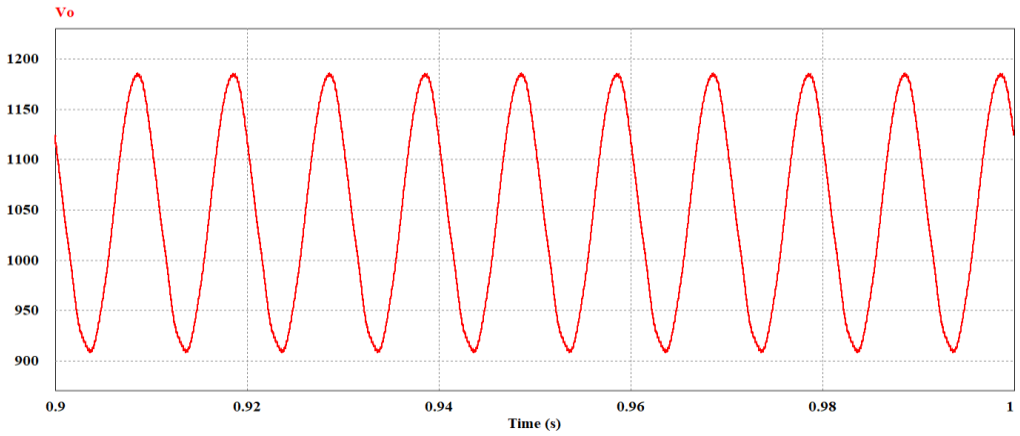


Figure 3.12: Waveform of output voltage of proposed converter at D=0.8, f_s=5 kHz and R_o=100 ohm.

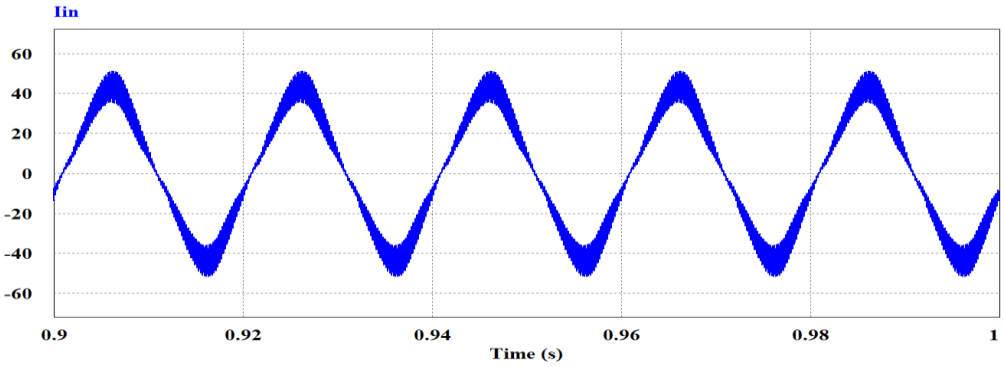


Figure 3.13: Waveform of input current of proposed converter at D=0.8, f_s=5 kHz and R_o=100 ohm.

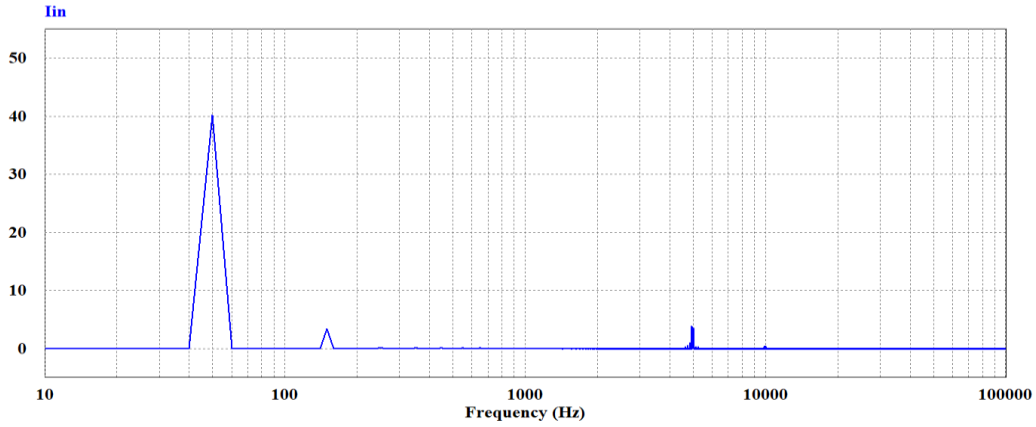


Figure 3.14: Input current spectrum of proposed converter at D=0.8, f_s=5 kHz and R_o=100 ohm.

3.5.2 Simulation results of proposed converter for load variation

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.3, frequency 5 kHz and load 50 ohm in Figure 3.18-3.20. For load variation, the output voltage has high ripples. The input current has fairly good harmonic components as seen from Figure 3.17.

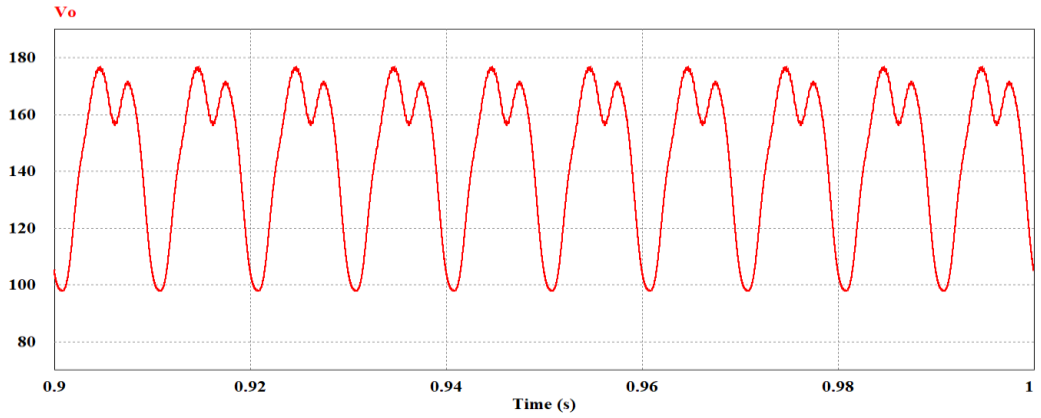


Figure 3.15: Waveform of output voltage of proposed converter at load=50 ohm, D=0.3 and fs=5 kHz

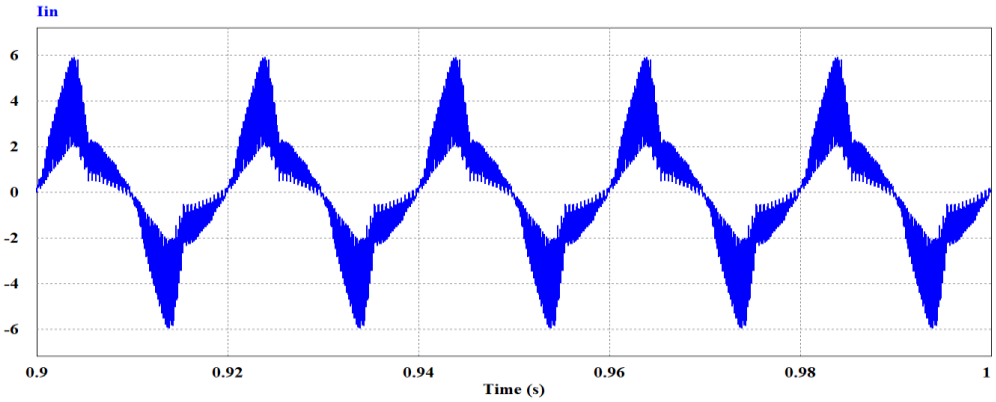


Figure 3.16: Waveform of input current of proposed converter at load=50 ohm, D=0.3 and fs=5 kHz

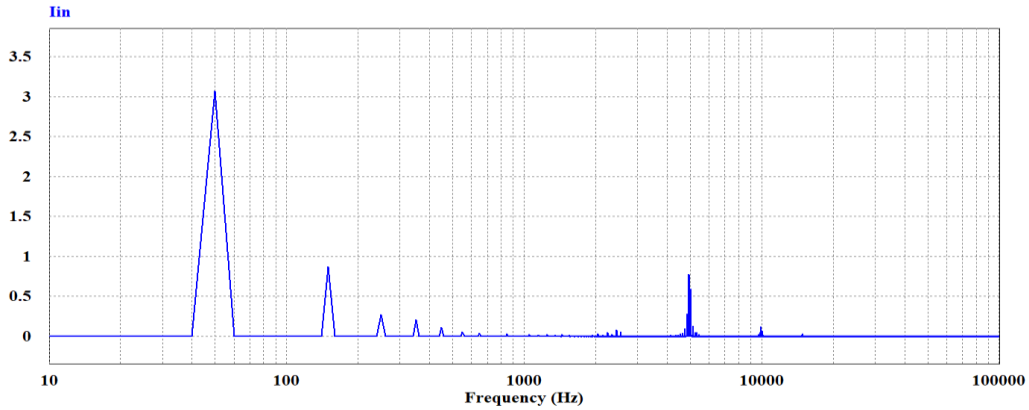


Figure 3.17: Input current spectrum of proposed converter at load=50 ohm, D=0.3 and fs=5 kHz

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.3, frequency 5 kHz and load 300 ohm in Figure 3.18-3.20. The output voltage waveform has low ripple as compared to low load of 50 ohm. Harmonic components of Iin are also low as depicted in Figure 3.20.

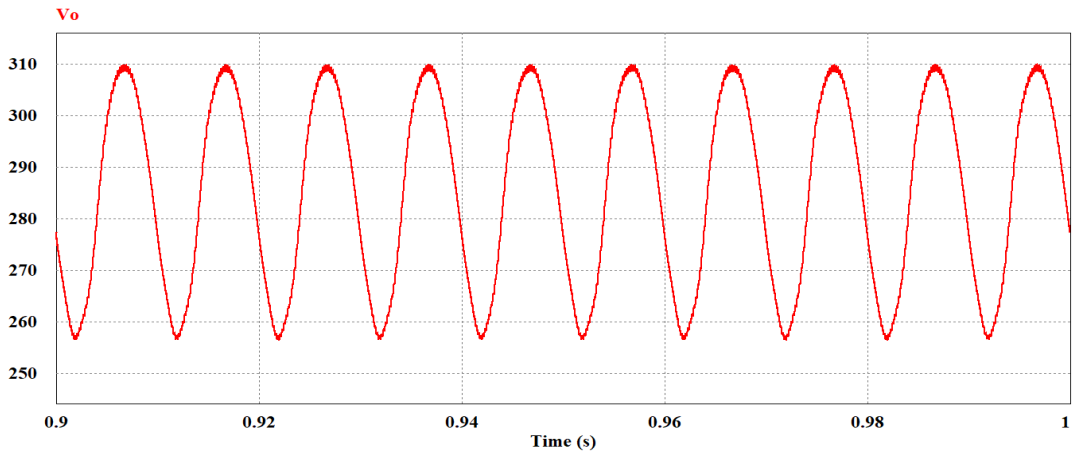


Figure 3.18: Waveform of output voltage of proposed converter at load=300 ohm, D=0.3 and fs=5 kHz

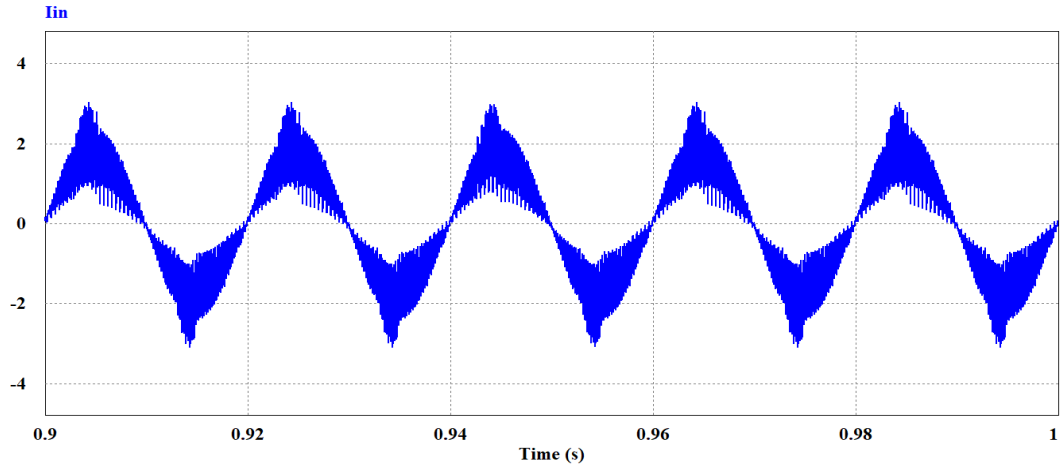


Figure 3.19: Waveform of input current of proposed converter at load=300 ohm, D=0.3 and fs=5 kHz

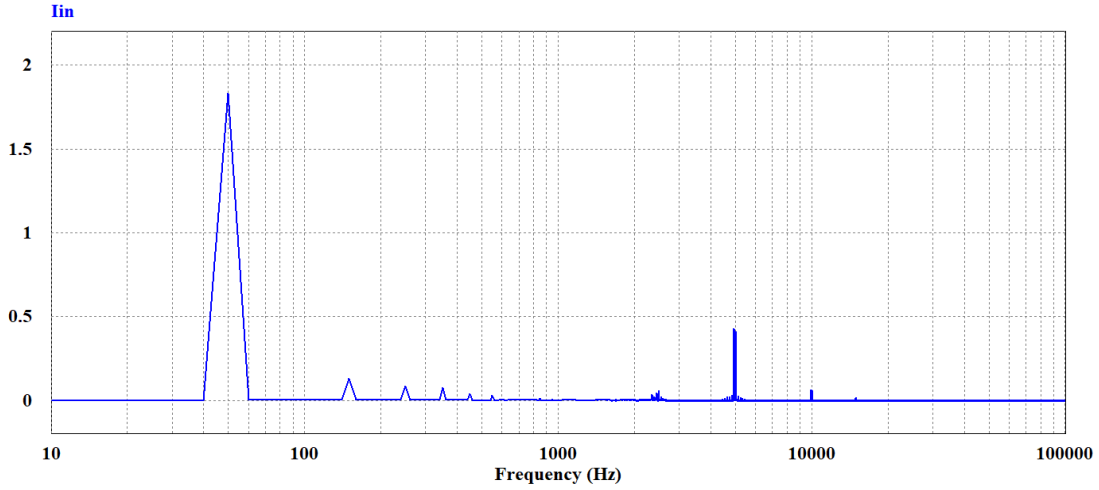


Figure 3.20: Input current spectrum of proposed converter at load=300 ohm, D=0.3 and fs=5 kHz

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.7, frequency 5 kHz and load 50 ohm in Figure 3.21-3.23. It is observed that the input current has low harmonic components.

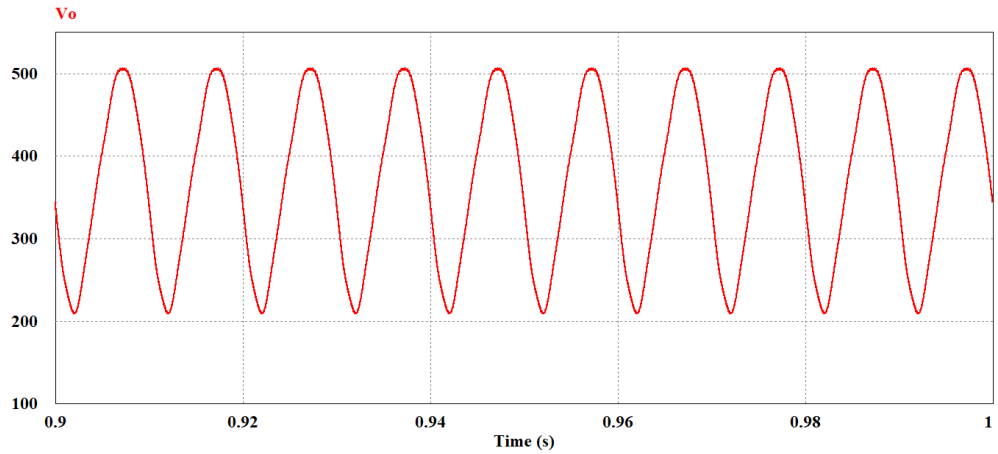


Figure 3.21: Waveform of output voltage of proposed converter at load=50 ohm, , D=0.7 and fs=5 kHz

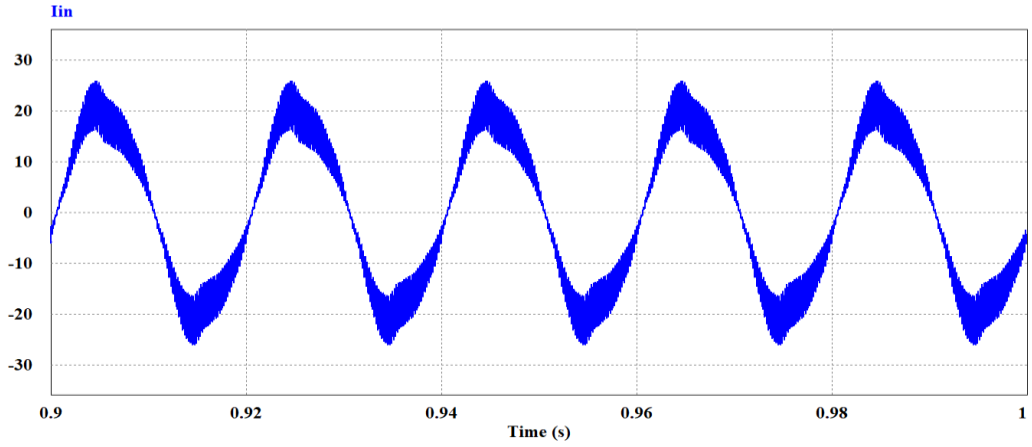


Figure 3.22: Waveform of input current of proposed converter at load=50 ohm, D=0.7 and fs=5 kHz

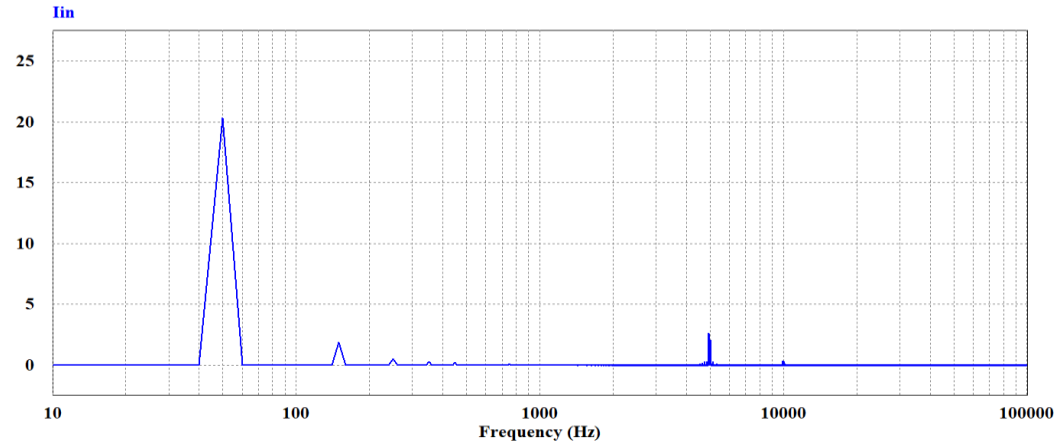


Figure 3.23: Input current spectrum of proposed converter at load=50 ohm, D=0.7 and fs=5 kHz

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.7, frequency 5 kHz and load 300 ohm in Figure 3.24-3.26. It is observed that the output voltage has low ripple percentage and the input current has very low distortions due to harmonics.

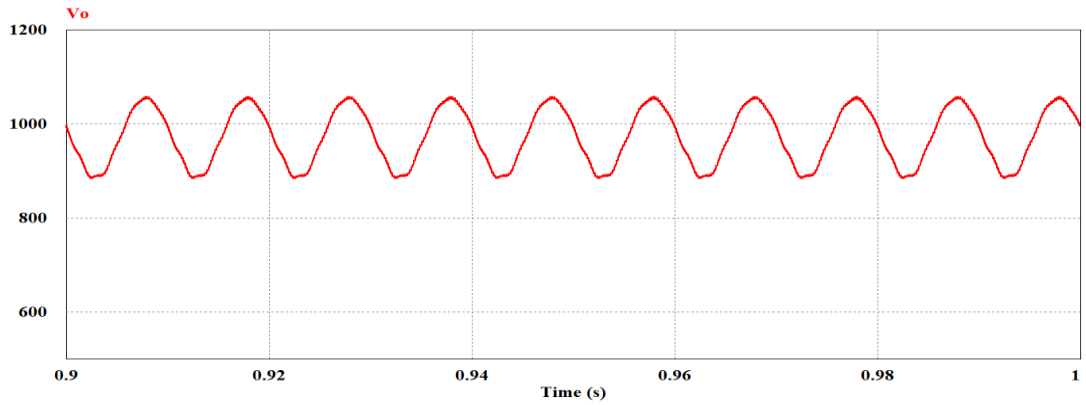


Figure 3.24: Waveform of output voltage of proposed converter at load=300 ohm, D=0.7 and fs=5 kHz

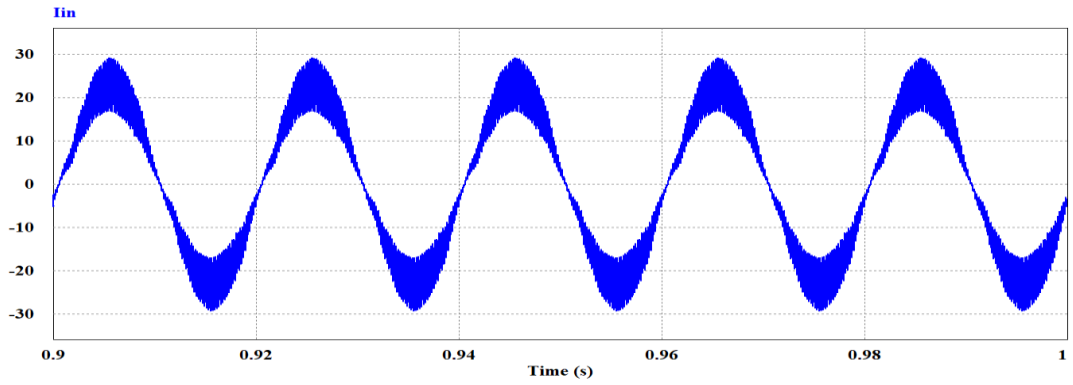


Figure 3.25: Waveform of input current of proposed converter at load=300 ohm, D=0.7 and fs=5 kHz

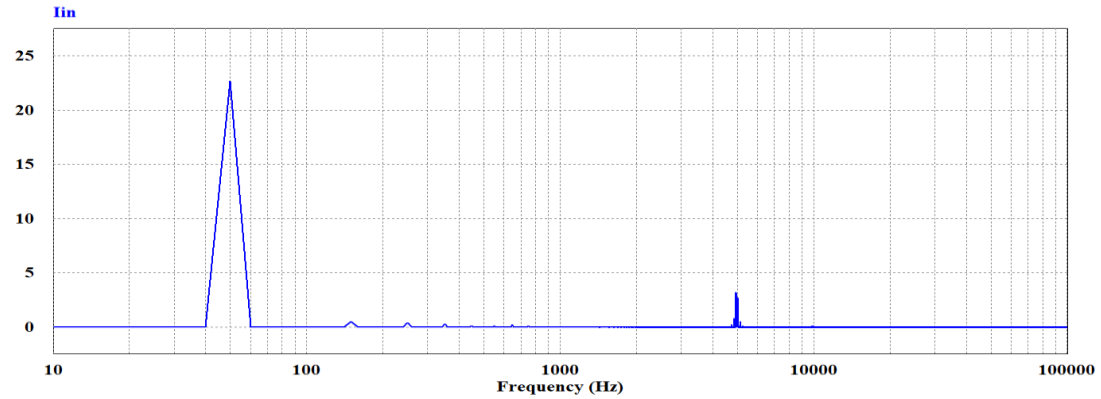


Figure 3.26: Input current spectrum of proposed converter at load=300 ohm, D=0.7 and fs=5 kHz

3.5.3 Simulation results of proposed converter for switching frequency variation

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.3, frequency 10 kHz and load 100 ohm in Figure 3.27-3.29. It is shown that the output has high ripples and input current, Iin has high distortion components.

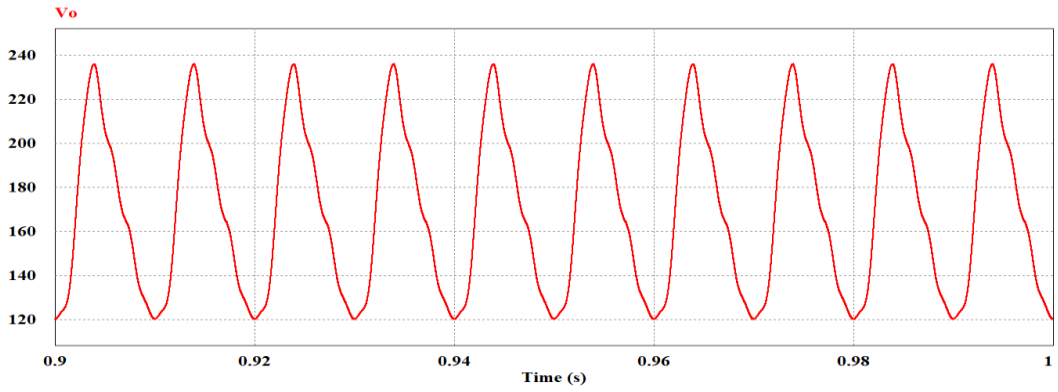


Figure 3.27: Waveform of output voltage of proposed converter at fs=10 kHz, D=0.3 and load=100 ohm

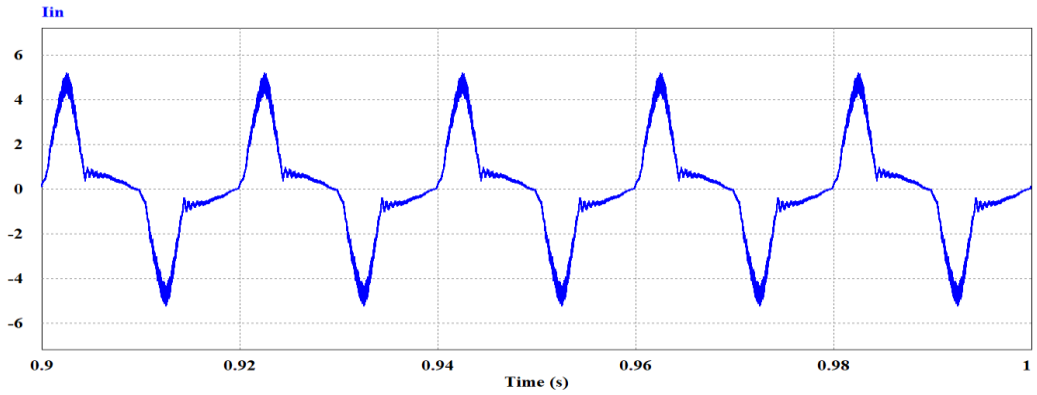


Figure 3.28: Waveform of input current of proposed converter at fs=10 kHz, D=0.3 and load=100 ohm

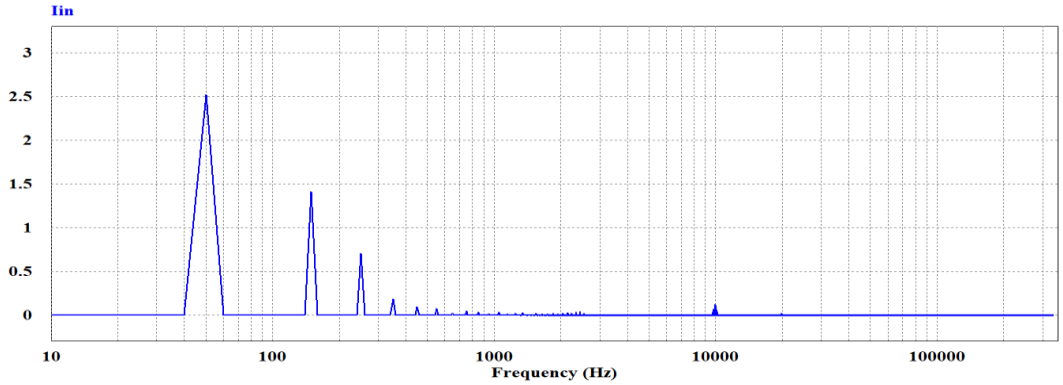


Figure 3.29: Input current spectrum of proposed converter at fs=10 kHz, D=0.3 and load=100 ohm

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.3, frequency 40 kHz and load 100 ohm in Figure 3.30-3.32. It is shown that the output has high ripples and input current, Iin has high harmonic components.

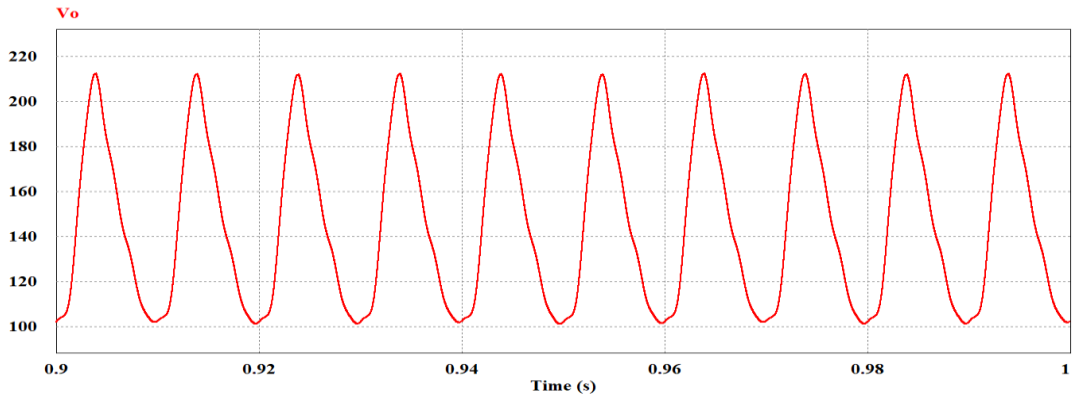


Figure 3.30: Waveform of output voltage of proposed converter at fs=40 kHz, D=0.3 and load=100 ohm

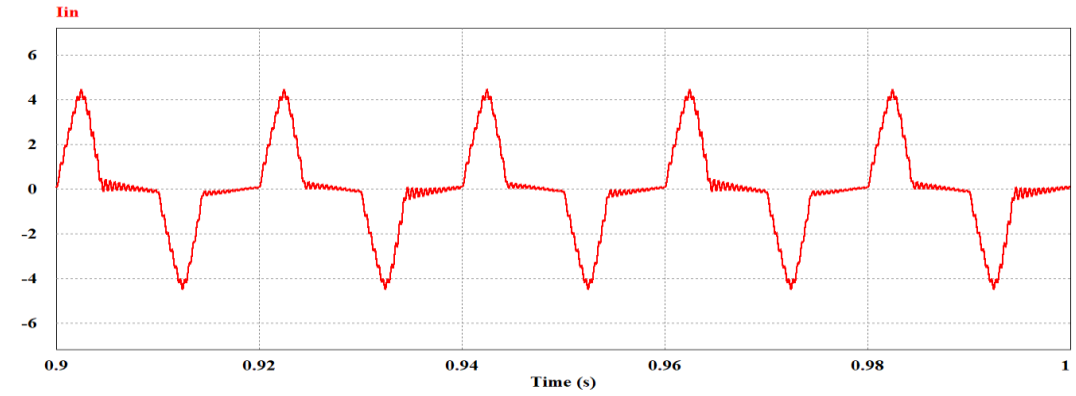


Figure 3.31: Waveform of input current of proposed converter at fs=40 kHz, D=0.3 and load=100 ohm

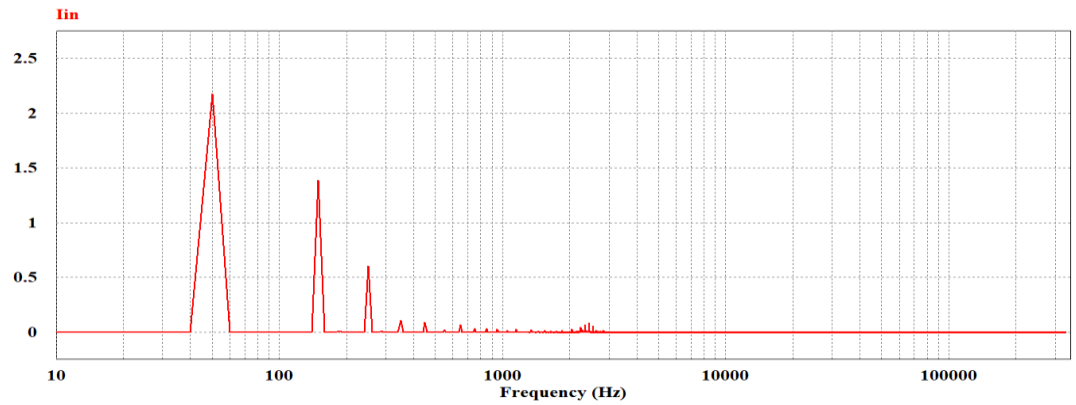


Figure 3.32: Input current spectrum of proposed converter at fs=40 kHz, D=0.3 and load=100 ohm

Simulated waveforms of output voltage, input current and input current spectrum are shown for duty cycle D=0.3, frequency 70 kHz and load 100 ohm in Figure 3.33-3.35. It is shown that the output has high ripples and input current, Iin has high harmonic components.

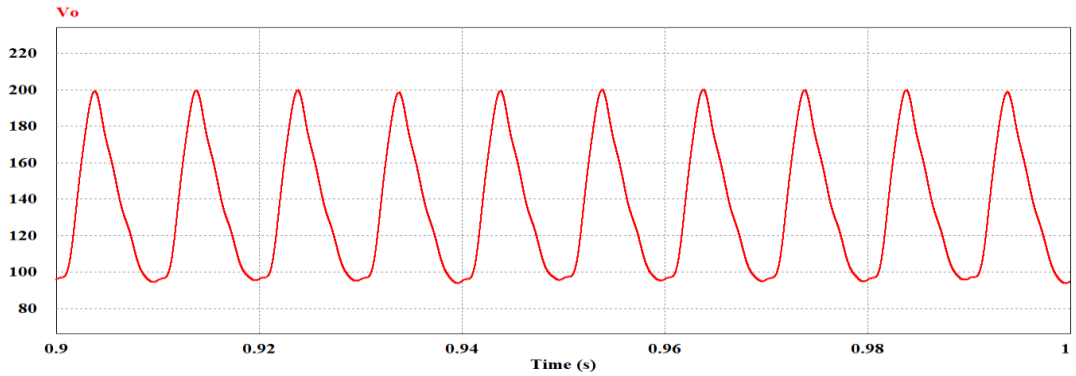


Figure 3.33: Waveform of output voltage of proposed converter at fs=70 kHz, D=0.3 and load=100 ohm

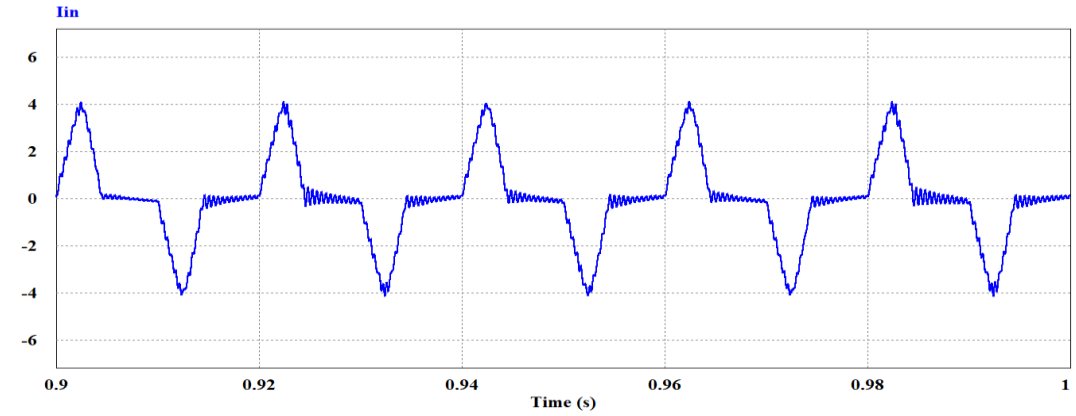


Figure 3.34: Waveform of input current of proposed converter at fs=70 kHz, D=0.3 and load=100 ohm

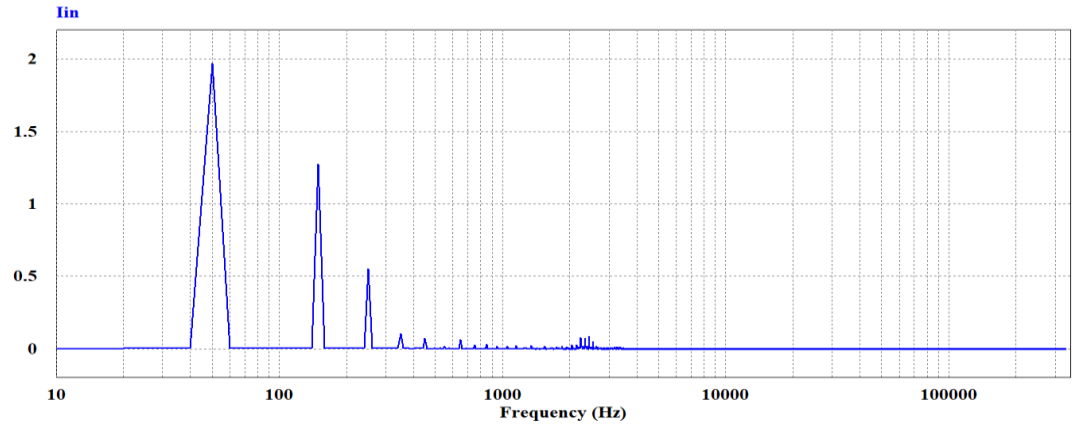


Figure 3.35: Input current spectrum of proposed converter at fs=70 kHz, D=0.3 and load=100 ohm

Chapter 4
Analysis and quantitative comparison of proposed AC-DC Zeta converter

In this chapter, comparison between proposed and conventional converter is presented with the help of numerical data tables and graphical representations. The conventional Zeta converter presented in [89] is compared with proposed converter. The comparison is necessary to validate the feasibility of using this converter. Both the converters are simulated with same parameters for any given variation. The key points from this simulation are also presented in this chapter.

4.1 Comparison of proposed converter with conventional converter under duty cycle variation

The proposed converter is compared with conventional Zeta converter for duty cycle variation. Duty cycle is varied from 0.1 to 0.9 and performance of both converters is tabulated in Table 4.1. The load is 100 ohm and switching frequency is 5 kHz for this comparison.

Table 4.1: Performance comparison under duty cycle variation for Fs= 5 kHz and Ro=100 Ω

Duty Cycle	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Input Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Input Power Factor	Voltage Gain
0.1	97.05	51.46	0.67	0.25	94.95	37.01	0.90	0.32
0.2	98.09	61.67	0.75	0.57	96.19	35.48	0.94	0.71
0.3	97.78	45.91	0.87	0.95	94.91	33.66	0.95	1.05
0.4	96.96	33.33	0.95	1.33	95.10	32.13	0.95	1.16
0.5	95.63	27.27	0.96	1.63	94.58	28.60	0.96	1.33
0.6	95.88	22.56	0.97	2.05	95.12	23.30	0.97	1.58
0.7	95.49	17.44	0.97	2.66	96.30	19.49	0.98	2.11
0.8	95.21	17.35	0.96	3.38	96.63	17.24	0.95	3.04
0.9	95.06	6.57	0.75	4.68	95.79	6.82	0.74	4.48

The key points from the comparison under duty ratio variation for proposed converter topology and conventional Zeta converter are given below

- The proposed converter has better efficiency for D=0.1 to D=0.6
- THD of proposed converter decreases with D and almost equal with conventional converter from D=0.4 to D=0.9
- Both converters have good PF in duty ratio range 0.5 to 0.8
- The voltage gain of proposed topology is better for most instances of duty ratios than conventional topology.

Comparison of efficiency (%), input current THD (%), input power factor and voltage gain between proposed and conventional converter are illustrated in Figure 4.1, Figure 4.2, Figure 4.3 and Figure 4.4 respectively.

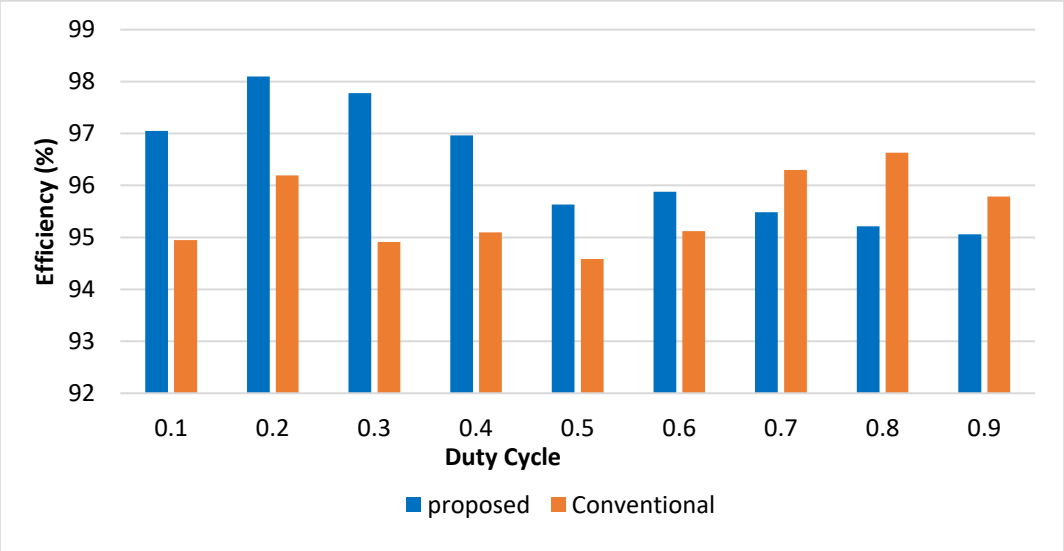


Figure 4.1: Comparison of efficiency (%) between proposed and conventional converter with variation of D at fs=5 kHz and load=100 ohm

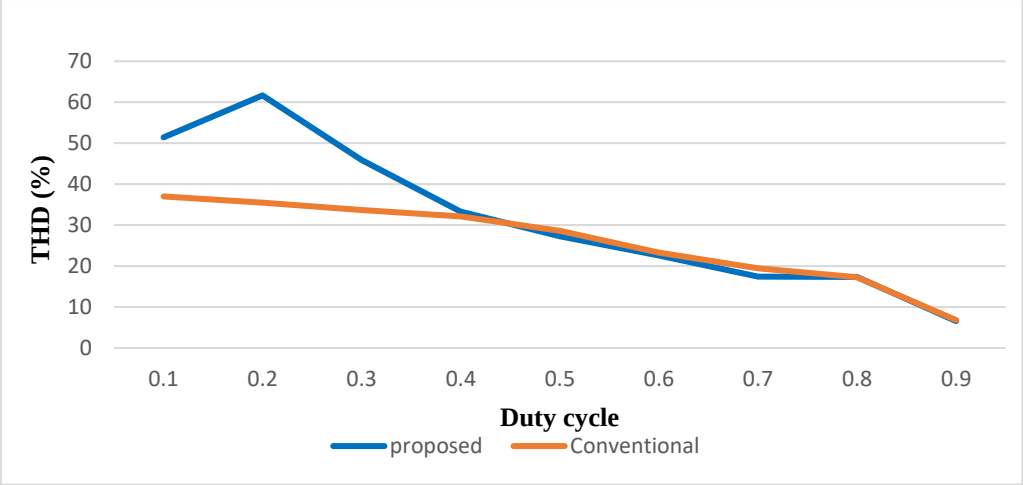


Figure 4.2: Comparison of input THD (%) between proposed and conventional converter with variation of D at fs=5 kHz and load=100 ohm

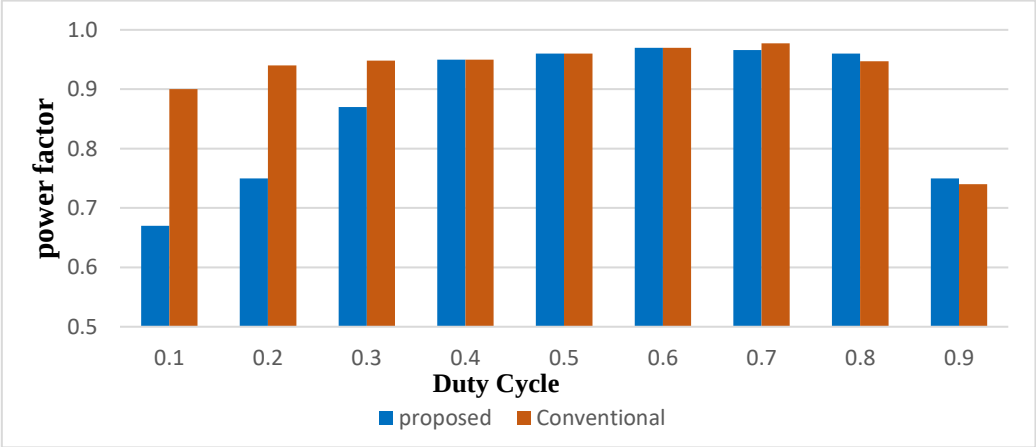


Figure 4.3: Comparison of input power factor between proposed and conventional converter with variation of D at fs=5 kHz and load=100 ohm

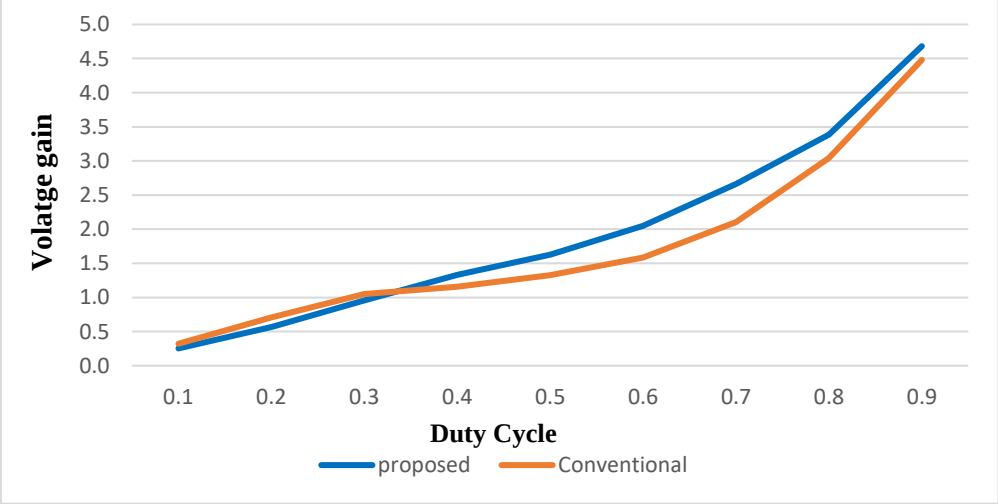


Figure 4.4: Comparison of voltage gain between proposed and conventional converter with variation of D at fs=5 kHz and load=100 ohm

4.2 Comparison of Proposed Converter under Load Variation

The proposed converter topology is compared with conventional ZETA converter for different load variation. Load Ro is varied from 50Ω to 500Ω for duty ratio D=0.3, D=0.5 and D=0.7. The switching frequency is fixed at 5 kHz. The results are shown in Table 4.2 for D=0.3, Table 4.3 for D=0.5 and Table 4.4 for D=0.7. The graphical analyses of the results are depicted in Figure 4.5 to Figure 4.16.

Table 4.2: Performance Comparison of Proposed converter and conventional converter under Load variation (for duty ratio of 0.3 and fs=5 kHz)

Load (Ω)	**Proposed Converter**				**Conventional Converter**			
	Efficiency (%)	**Input current THD (%)**	**Input Power Factor**	**Voltage Gain**	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Voltage Gain**
50	97.05	44.92	0.88	0.70	96.11	33.62	0.95	0.75
100	97.78	45.91	0.87	0.95	94.91	33.66	0.95	1.05
150	96.79	48.90	0.87	1.15	94.50	33.58	0.95	1.29
200	96.68	52.01	0.87	1.30	93.90	33.57	0.95	1.48
250	96.76	41.07	0.92	1.34	93.32	33.57	0.95	1.65
300	96.53	34.84	0.94	1.37	92.50	33.58	0.95	1.80
350	96.24	33.07	0.94	1.42	91.60	33.56	0.95	1.93
400	96.11	33.02	0.94	1.52	90.93	33.59	0.95	2.06
450	95.88	33.01	0.94	1.61	90.10	33.58	0.95	2.17
500	95.72	33.01	0.94	1.69	89.42	33.58	0.95	2.28

Table 4.3: Performance Comparison of Proposed converter and conventional converter under Load variation (for duty ratio of 0.5 and fs=5 kHz)

Load (Ω)	Proposed Converter				Conventional Converter			
	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain
50	96.08	27.63	0.96	1.14	95.86	28.21	0.96	0.97
100	95.63	27.27	0.96	1.63	94.58	28.60	0.96	1.33
150	95.67	27.46	0.96	2.00	93.97	28.57	0.96	1.62
200	95.42	27.55	0.96	2.31	93.06	28.55	0.96	1.86
250	95.23	27.62	0.96	2.58	92.04	28.55	0.96	2.07
300	95.02	27.70	0.96	2.82	91.02	28.53	0.96	2.25
350	94.70	27.78	0.96	3.04	89.84	28.53	0.96	2.41
400	94.67	27.91	0.96	3.24	89.21	28.50	0.96	2.57
450	94.44	28.09	0.96	3.41	88.23	28.51	0.96	2.71
500	94.25	28.19	0.96	3.56	87.36	28.56	0.96	2.84

Table 4.4: Performance Comparison of Proposed converter and conventional converter under Load variation (for duty ratio of 0.7 and fs=5 kHz)

Load (Ω)	Proposed Converter				Conventional Converter			
	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain
50	95.71	19.23	0.97	1.72	95.84	18.89	0.98	1.65
100	95.49	17.44	0.97	2.66	96.30	19.49	0.98	2.11
150	93.66	17.82	0.96	3.22	93.58	18.40	0.98	2.43
200	93.53	18.35	0.96	3.70	92.90	17.85	0.98	2.69
250	93.25	18.76	0.96	4.10	92.12	18.01	0.98	2.97
300	93.09	19.22	0.96	4.46	91.66	18.04	0.98	3.24
350	92.72	19.51	0.96	4.79	90.93	18.03	0.98	3.48
400	92.64	19.82	0.96	5.11	90.32	18.08	0.98	3.70
450	92.13	20.09	0.96	5.40	89.59	18.10	0.98	3.91
500	92.14	20.28	0.96	5.70	89.16	18.08	0.98	4.11

The key points from the comparison under load variation for proposed converter topology and conventional ZETA converter are given below

- The proposed topology has better efficiency than conventional topology in almost all loads at different duty cycles.
- THD is on the higher side for the proposed converter for some cases and lower side for some cases.
- Power factor of proposed converter is equal in all load conditions when D=0.5. PF is slightly lower for D=0.3 and D=0.7.
- Achievable voltage gain is better for proposed converter than conventional converter for different loads when D=0.5 and D=0.7. On the other hand conventional has better gain when D=0.3.

Comparison of efficiency (%) between proposed and conventional converter for load variation is shown in Figures 4.5-4.7 for duty cycles D=0.3, D=0.5 and D=0.7 respectively.

Comparison of input current THD (%) between proposed and conventional converter for load variation is shown in Figures 4.8-4.10 for duty cycles D=0.3, D=0.5 and D=0.7 respectively.

Comparison of input power factor between proposed and conventional converter for load variation is shown in Figures 4.11-4.13 for duty cycles D=0.3, D=0.5 and D=0.7 respectively.

Comparison of voltage gain between proposed and conventional converter for load variation is shown in Figures 4.14-4.16 for duty cycles D=0.3, D=0.5 and D=0.7 respectively.

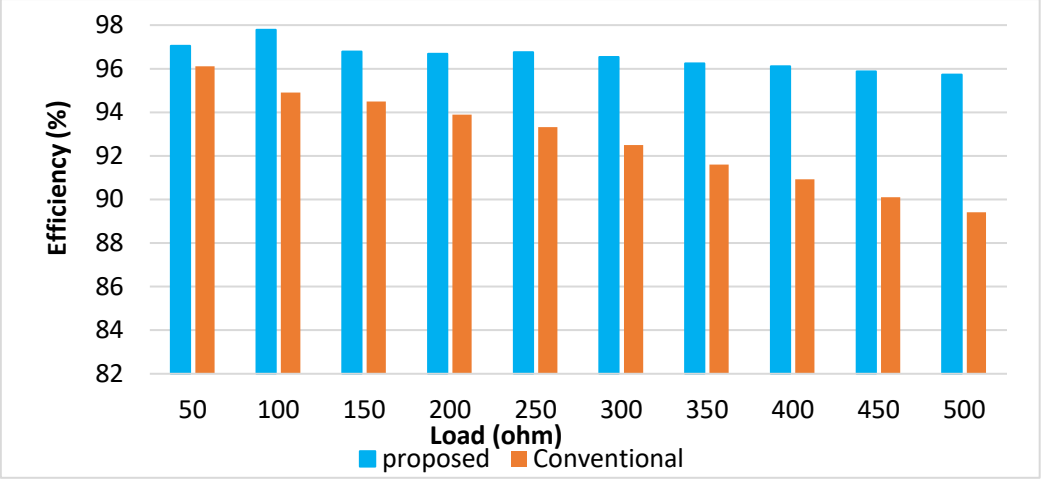


Figure 4.5: Comparison of efficiency between proposed and conventional converter for load variation at fs=5 kHz and D=0.3

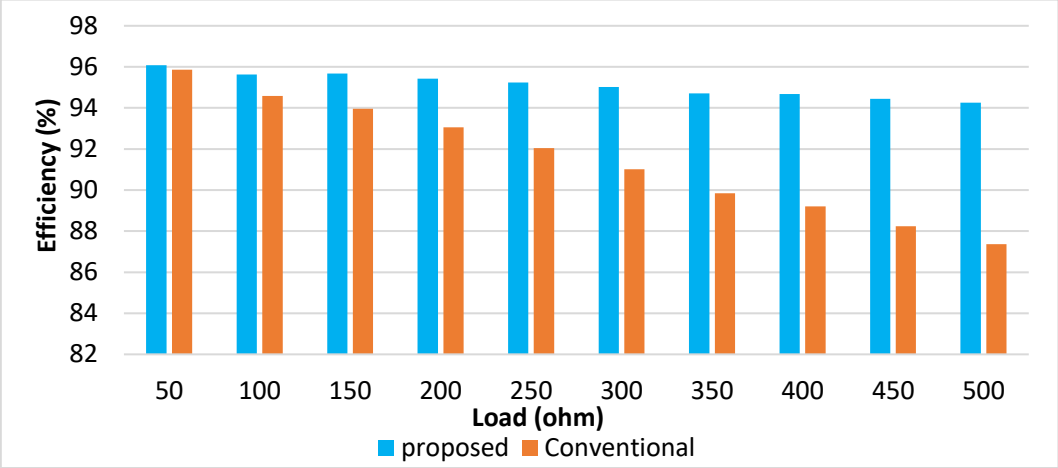


Figure 4.6: Comparison of efficiency between proposed and conventional converter for load variation at fs=5 kHz and D=0.5

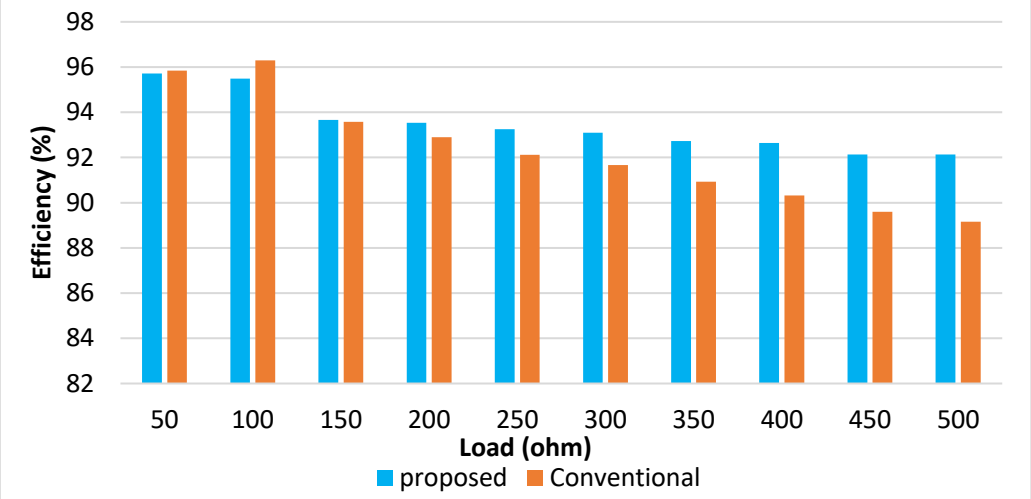


Figure 4.7: Comparison of efficiency between proposed and conventional converter for load variation at fs=5 kHz and D=0.7

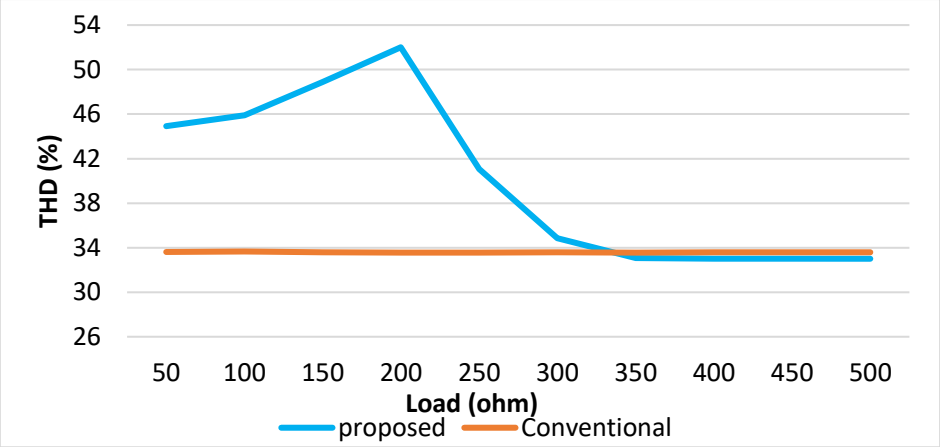


Figure 4.8: Comparison of THD between proposed and conventional converter for load variation at fs=5 kHz and D=0.3

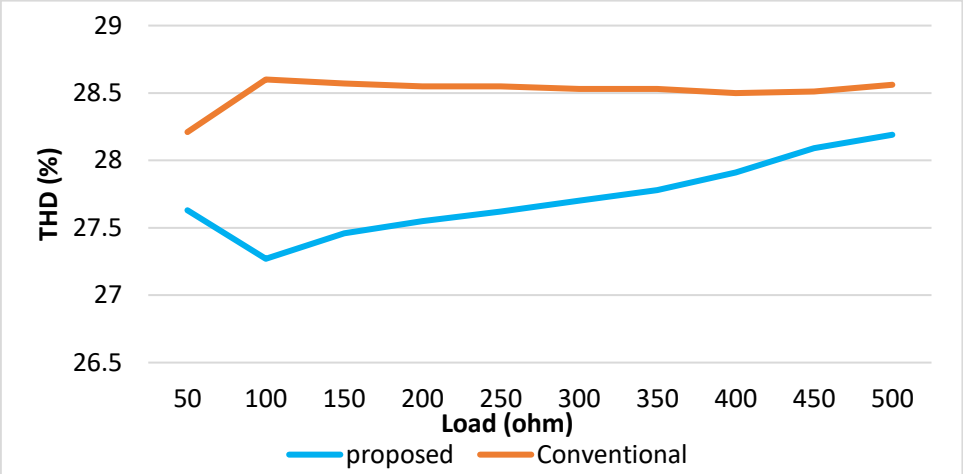


Figure 4.9: Comparison of THD between proposed and conventional converter for load variation at fs=5 kHz and D=0.5

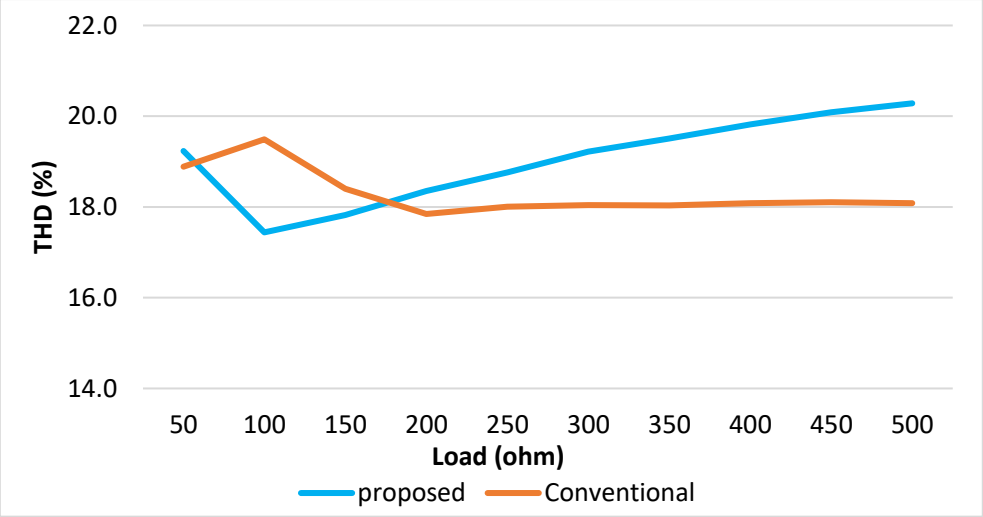


Figure 4.10: Comparison of THD between proposed and conventional converter for load variation at fs=5 kHz and D=0.7

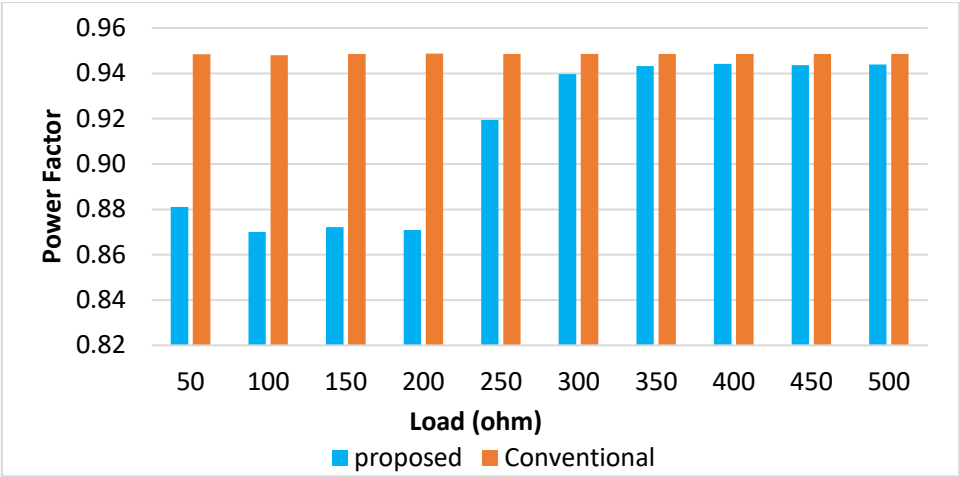


Figure 4.11: Comparison of power factor between proposed and conventional converter for load variation at fs=5 kHz and D=0.3

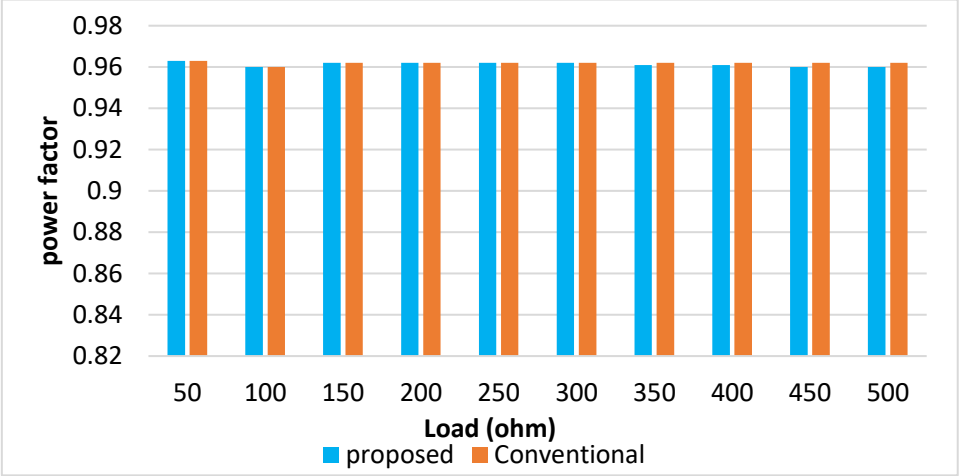


Figure 4.12: Comparison of power factor between proposed and conventional converter for load variation at fs=5 kHz and D=0.5

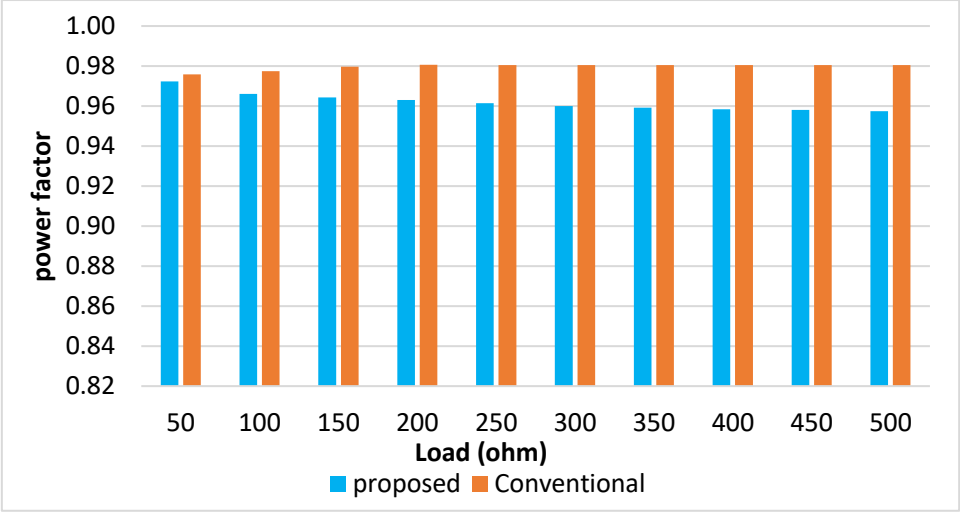


Figure 4.13: Comparison of power factor between proposed and conventional converter for load variation at fs=5 kHz and D=0.7

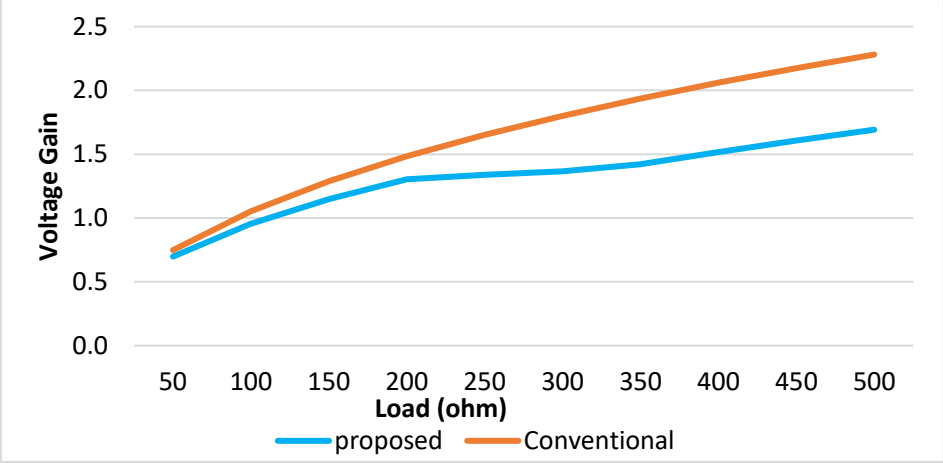


Figure 4.14: Comparison of voltage gain between proposed and conventional converter for load variation at fs=5 kHz and D=0.3

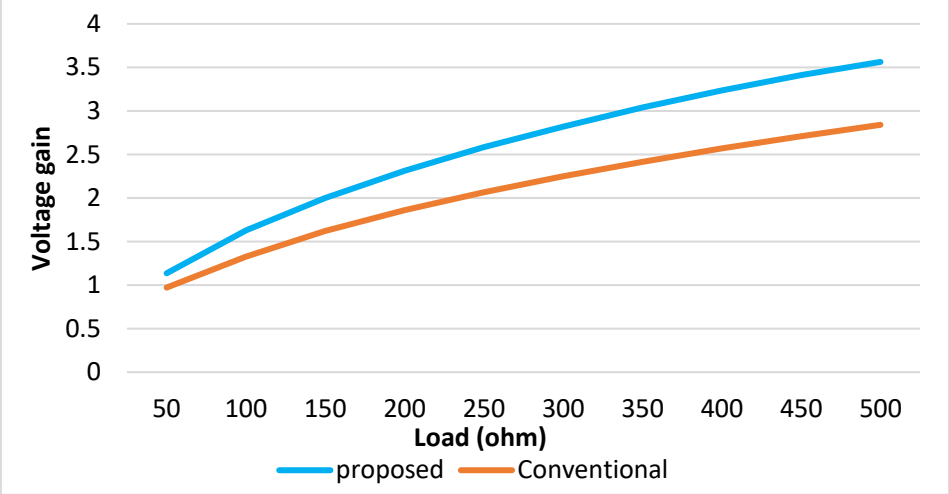


Figure 4.15: Comparison of voltage gain between proposed and conventional converter for load variation at fs=5 kHz and D=0.5

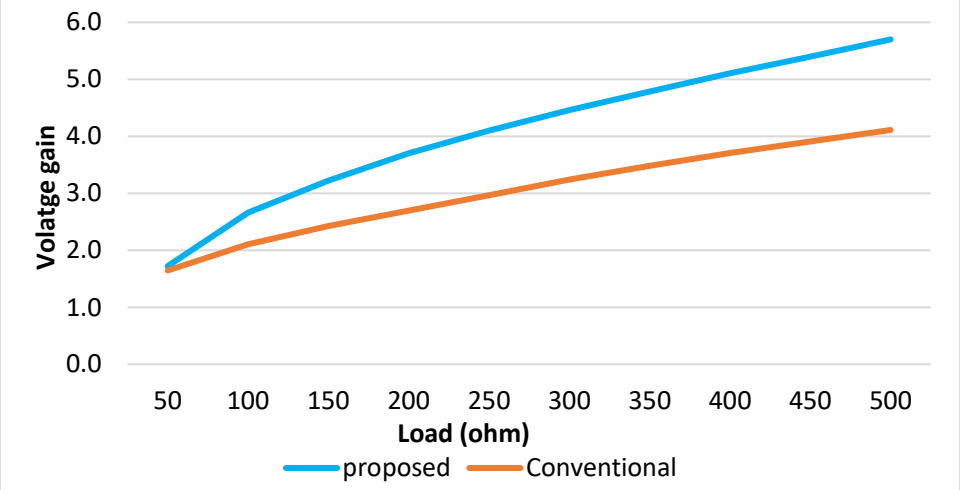


Figure 4.16: Comparison of voltage gain between proposed and conventional converter for load variation at fs=5 kHz and D=0.7

4.3 Comparison of Proposed Converter under switching frequency (fs) variation

The proposed converter topology is compared with conventional converter for different switching frequency variation. Switching frequency is varied from 5 kHz to 100 kHz for duty ratio of D=0.3, D=0.5 and D=0.7.The load resistance, Ro is fixed at 100 ohm. Other circuit parameters are kept unchanged for both circuits. The results are shown in Table 4.5 for D=0.3, Table 4.6 for D=0.5 and Table 4.7 for D=0.7. The graphical analysis is depicted in Figure 4.17 to Figure 4.28. The results are evaluated in terms of efficiency, input current THD, power factor and voltage gain.

Table 4.5: Performance comparison of proposed converter and conventional converter under frequency variation (for duty ratio, D=0.3 and load=100 ohm)

Frequency (Hz)	**Proposed Converter**				**Conventional Converter**			
	Efficiency (%)	**Input current THD (%)**	**Input Power Factor**	**Voltage Gain**	**Efficiency (%)**	**Input current THD (%)**	**Input Power Factor**	**Voltage Gain**
5k	97.78	45.91	0.87	0.95	94.91	33.66	0.95	1.05
10k	97.16	63.98	0.68	0.79	94.87	7.03	0.97	0.70
20k	94.83	67.56	0.62	0.71	90.33	42.84	0.88	0.59
30k	91.78	67.02	0.61	0.68	85.76	69.58	0.81	0.59
40k	95.52	69.19	0.58	0.68	88.49	73.04	0.78	0.59
50k	94.49	69.50	0.58	0.68	90.11	80.56	0.76	0.58
60k	95.85	70.93	0.57	0.68	92.42	88.51	0.74	0.59
70k	96.24	70.55	0.57	0.67	93.03	86.89	0.73	0.59
80k	96.66	72.43	0.56	0.67	93.70	92.11	0.72	0.59
90k	96.98	70.98	0.56	0.67	94.25	93.06	0.71	0.59
100k	96.99	72.26	0.56	0.67	94.26	92.89	0.71	0.59

Table 4.6: Performance comparison of proposed converter and conventional converter under frequency variation (for duty ratio, D=0.5 and 100 ohm load)

Frequency (Hz)	Proposed Converter				Conventional Converter			
	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain
5k	95.63	27.31	0.96	1.63	94.58	28.60	0.96	1.33
10k	95.85	38.75	0.90	1.97	93.81	29.38	0.95	1.47
20k	94.99	48.03	0.82	2.03	93.87	56.83	0.84	1.33
30k	92.96	49.94	0.81	1.97	91.63	62.86	0.81	1.30
40k	90.71	50.01	0.80	1.92	89.20	66.89	0.80	1.28
50k	89.87	51.40	0.80	1.90	88.11	71.62	0.80	1.27
60k	91.38	47.72	0.80	1.93	90.00	74.73	0.78	1.28
70k	92.54	49.56	0.80	1.95	91.18	69.97	0.78	1.29
80k	92.59	50.01	0.79	1.93	91.36	71.66	0.77	1.28
90k	94.19	49.33	0.79	1.98	92.93	75.01	0.77	1.29
100k	96.49	52.04	0.79	2.02	94.79	75.95	0.76	1.30

Table 4.7: Performance comparison of proposed converter and conventional converter under frequency variation (for duty ratio, D=0.7 and 100 ohm load)

Frequency (Hz)	Proposed Converter				Conventional Converter			
	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain	Efficiency (%)	Input current THD (%)	Input Power Factor	Voltage Gain
5k	95.49	17.44	0.97	2.66	96.30	19.49	0.98	2.11
10k	93.66	13.90	0.95	3.72	94.87	23.18	0.96	2.54
20k	90.64	17.11	0.95	4.26	93.09	38.34	0.85	2.58
30k	87.25	17.24	0.95	4.30	91.29	41.89	0.83	2.52
40k	90.26	17.70	0.95	4.51	93.36	43.36	0.81	2.52
50k	91.13	17.57	0.94	4.60	94.00	43.95	0.80	2.53
60k	93.28	17.72	0.94	4.69	95.34	43.82	0.79	2.54
70k	94.39	17.55	0.94	4.76	96.07	44.42	0.79	2.55
80k	94.94	17.58	0.94	4.78	96.40	44.35	0.79	2.56
90k	95.58	17.79	0.94	4.82	96.81	44.73	0.78	2.56
100k	95.43	17.68	0.94	4.83	96.76	45.03	0.78	2.56

The key points from the comparison under frequency variation for proposed converter topology and conventional Zeta converter are given below

- The efficiency of proposed converter is better than conventional converter for all switching frequency of D=0.3 and D=0.5 but is lower than conventional one when D=0.7.
- Input current THD is lower for most cases of load for different duty ratios.
- For D=0.5 and D=0.7, power factor of proposed one is better than conventional one for most cases of loads. For D=0.3, the conventional converter achieves higher PF.
- Achievable output voltage is high for proposed converter in comparison with conventional converter for different loads and for different duty cycles.

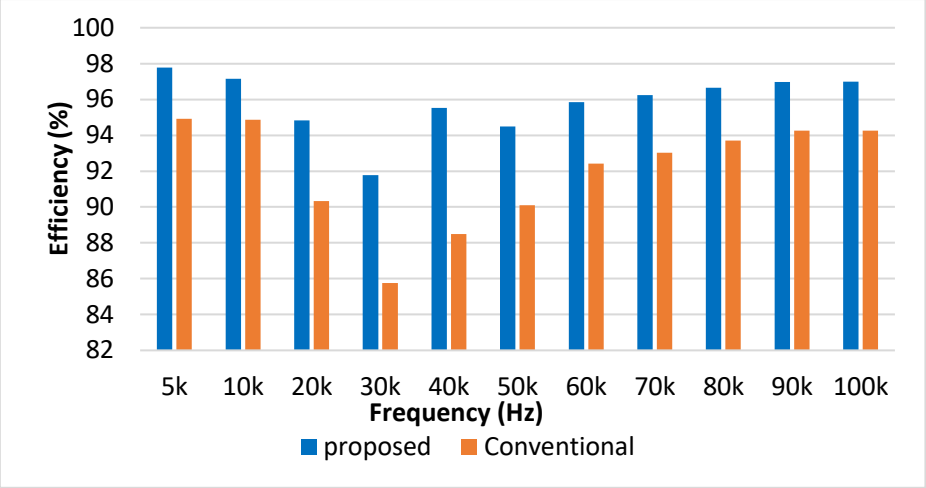


Figure 4.17: Comparison of efficiency between proposed and conventional converter under frequency variation at D=0.3 and Ro=100 ohm

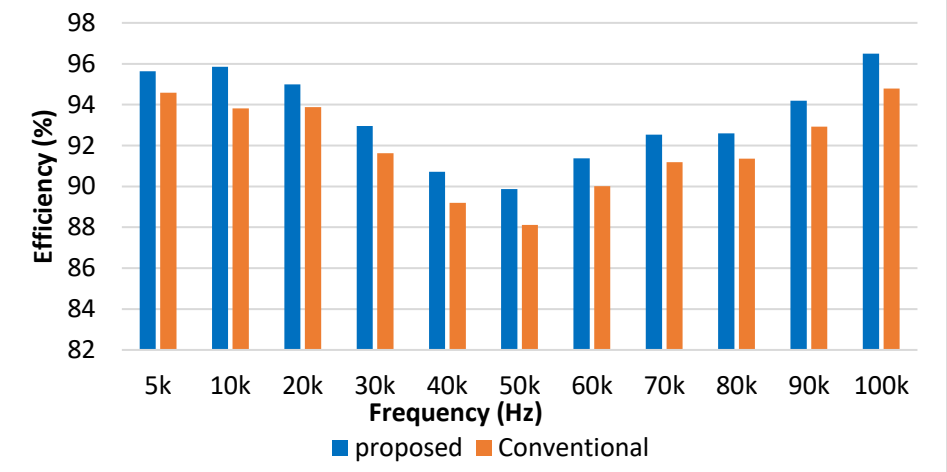


Figure 4.18: Comparison of efficiency between proposed and conventional converter under frequency variation at D=0.5 and Ro=100 ohm

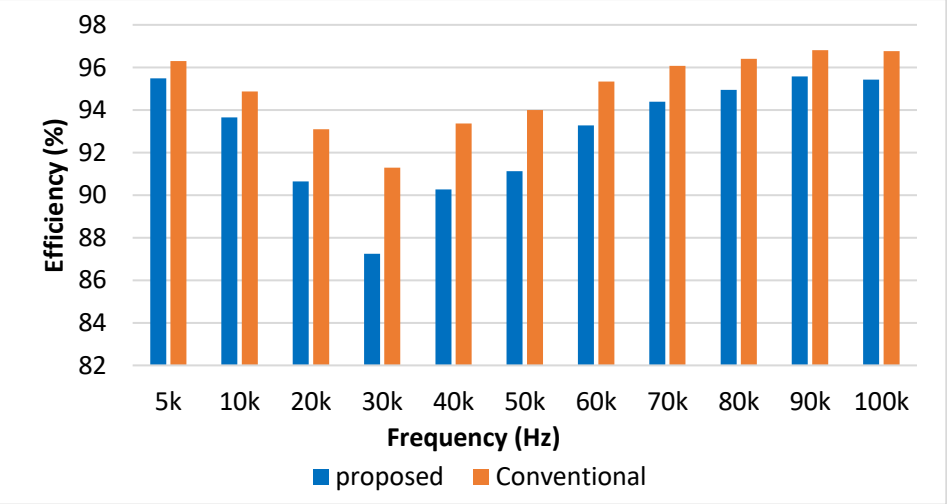


Figure 4.19: Comparison of efficiency between proposed and conventional converter under frequency variation at D=0.7 and Ro=100 ohm

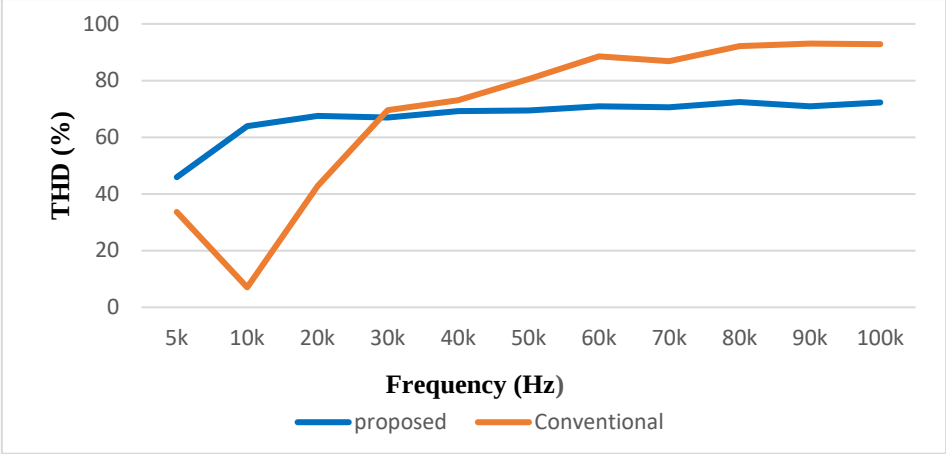


Figure 4.20: Comparison of THD between proposed and conventional converter under frequency variation at D=0.3 and Ro=100 ohm

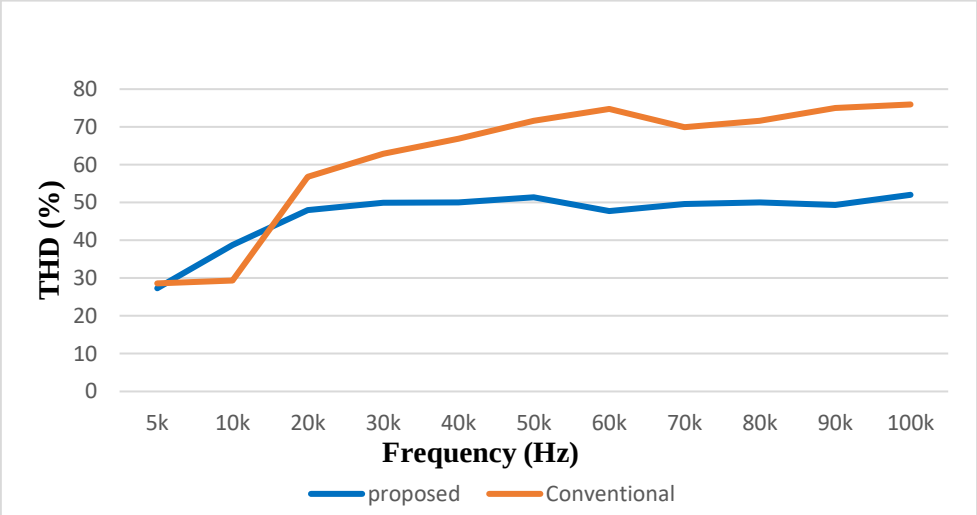


Figure 4.21: Comparison of THD between proposed and conventional converter under frequency variation at D=0.5 and Ro=100 ohm

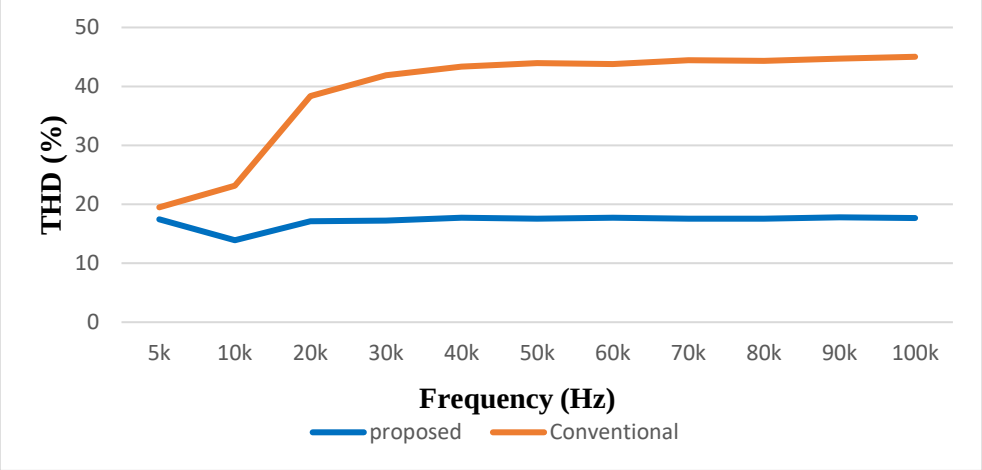


Figure 4.22: Comparison of THD between proposed and conventional converter under frequency variation at D=0.7 and Ro=100 ohm

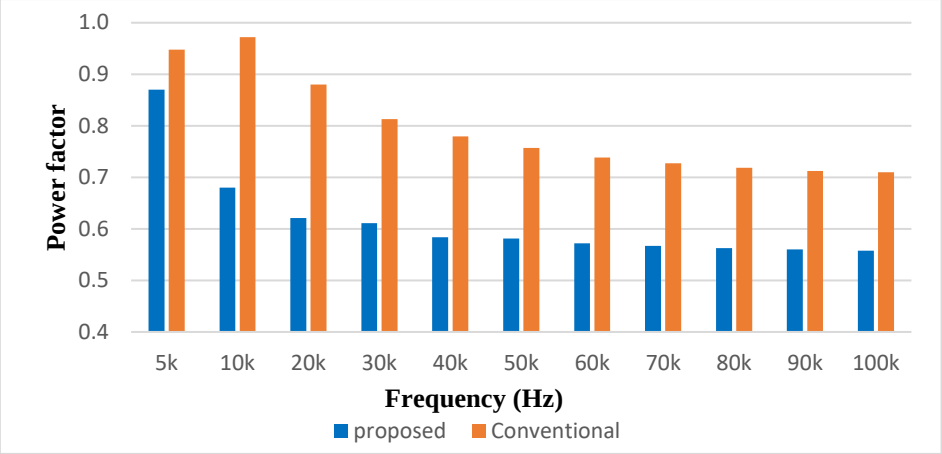


Figure 4.23: Comparison of power factor between proposed and conventional converter under frequency variation at D=0.3 and Ro=100 ohm

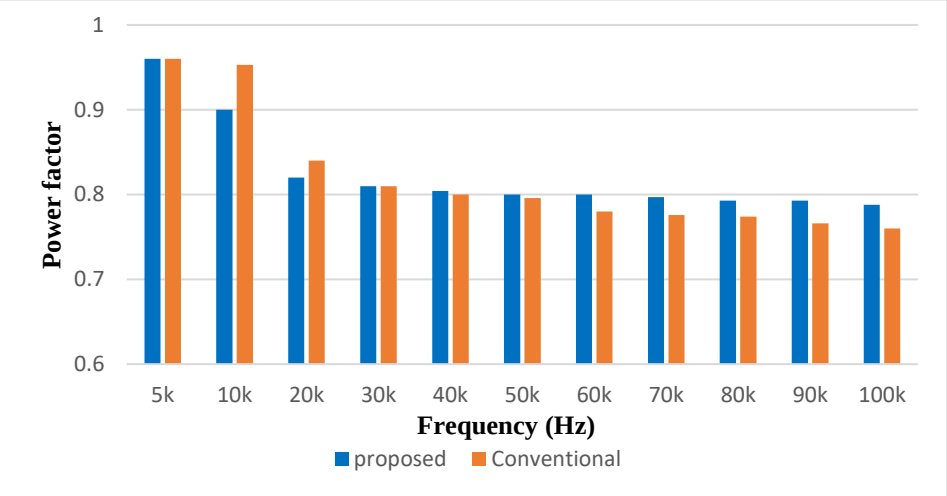


Figure 4.24: Comparison of power factor between proposed and conventional converter under frequency variation at D=0.5 and Ro=100 ohm

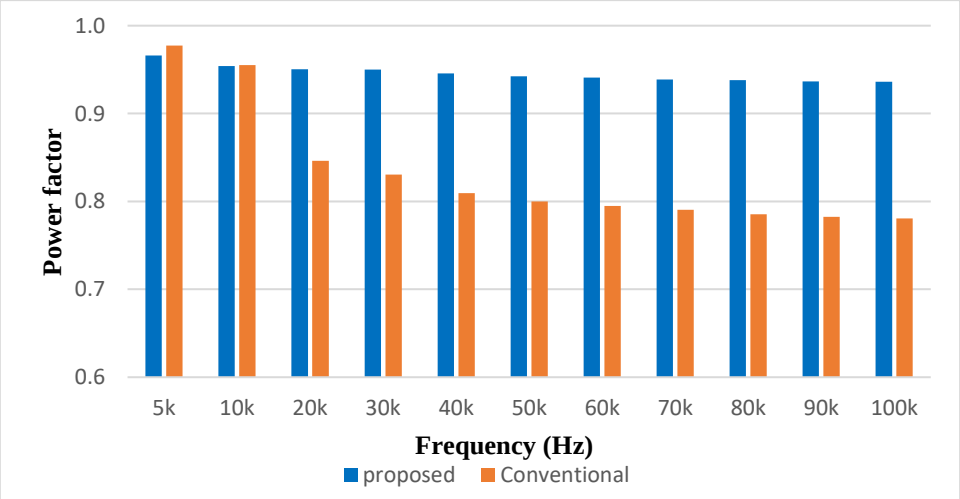


Figure 4.25: Comparison of power factor between proposed and conventional converter under frequency variation at D=0.7 and Ro=100 ohm

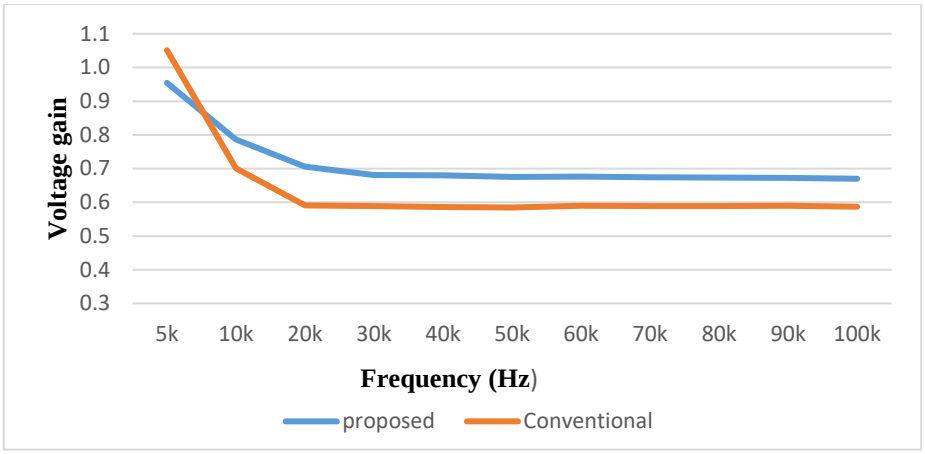


Figure 4.26: Comparison of voltage gain between proposed and conventional converter under frequency variation at D=0.3 and Ro=100 ohm

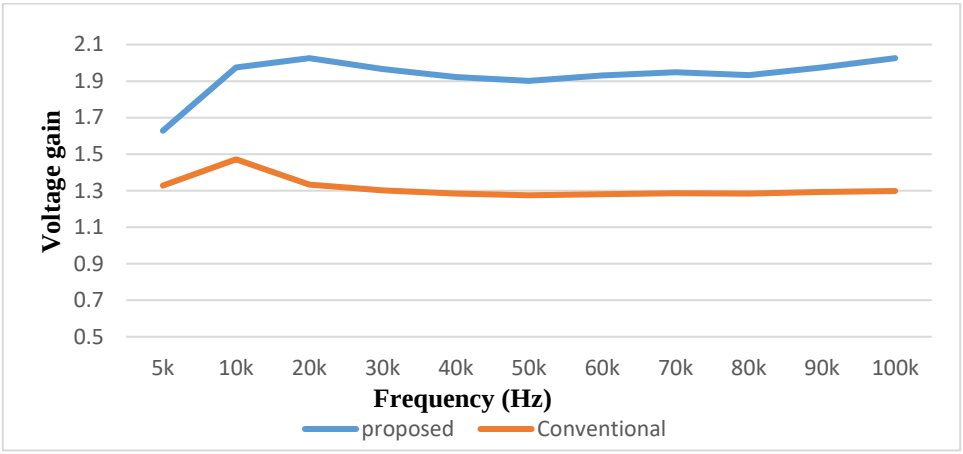


Figure 4.27: Comparison of voltage gain between proposed and conventional converter under frequency variation at D=0.5 and Ro=100 ohm

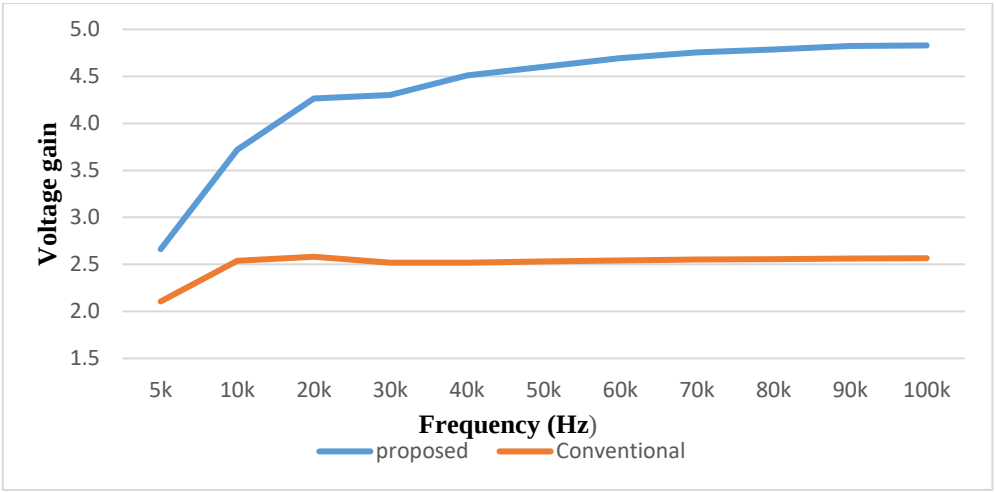


Figure 4.28: Comparison of voltage gain between proposed and conventional converter under frequency variation at D=0.7 and Ro=100 ohm

4.4 Comparison with recent AC-DC Converters

The proposed AC-DC Zeta converter is compared with recent step-up and step-down converters. The comparison is shown in Table 4.8. Three recent topologies of converters are selected for comparison. The converter topology in [94] has good conversion efficiency but THD is high. Topology in [95] has better THD and PF but efficiency is lower than proposed converter. The efficiency of recent converter in [96] is lower but THD and PF is good. It can be observed from the Table 4.8 that the proposed converter topology can match or outperform recent converters in terms of different performance parameters such as efficiency, THD and input PF.

Table 4.8 Comparison of proposed converter with recent converters

Converter Topology	**Maximum Conversion Efficiency (%)**	**Input current THD (%)**	**Input PF**
Proposed	98.1	12.3	0.99
Recent converter 1- [94], (2020)	98	16	0.98
Recent converter 2- [95] (2020)	94	9	0.99
Recent converter 3-[96] (2019)	91.46	10.5	0.99

Chapter 5
Feedback Controller and Dynamic Response of Proposed Converter

5.1 Feedback Control Techniques

Quality power factor is a must to maintain the power quality of electrical systems. There are several demerits of low power factor such as need for larger KVA rating of electrical equipment, increased conductor size, larger copper losses, poor regulation of voltage etc. Generally, the input power factor of conventional converters is very low for most of the duty ratios in open loop operation and is responsible for many problems in whole power system. Proper feedback controller design can achieve high input power factor and can improve overall performance of converter. The typical controller works in two loops. One is inner current control loop and the other is the outer voltage control loop. In this chapter, the feedback controller is designed for the proposed single phase AC-DC converter as shown in Figure 5.1.

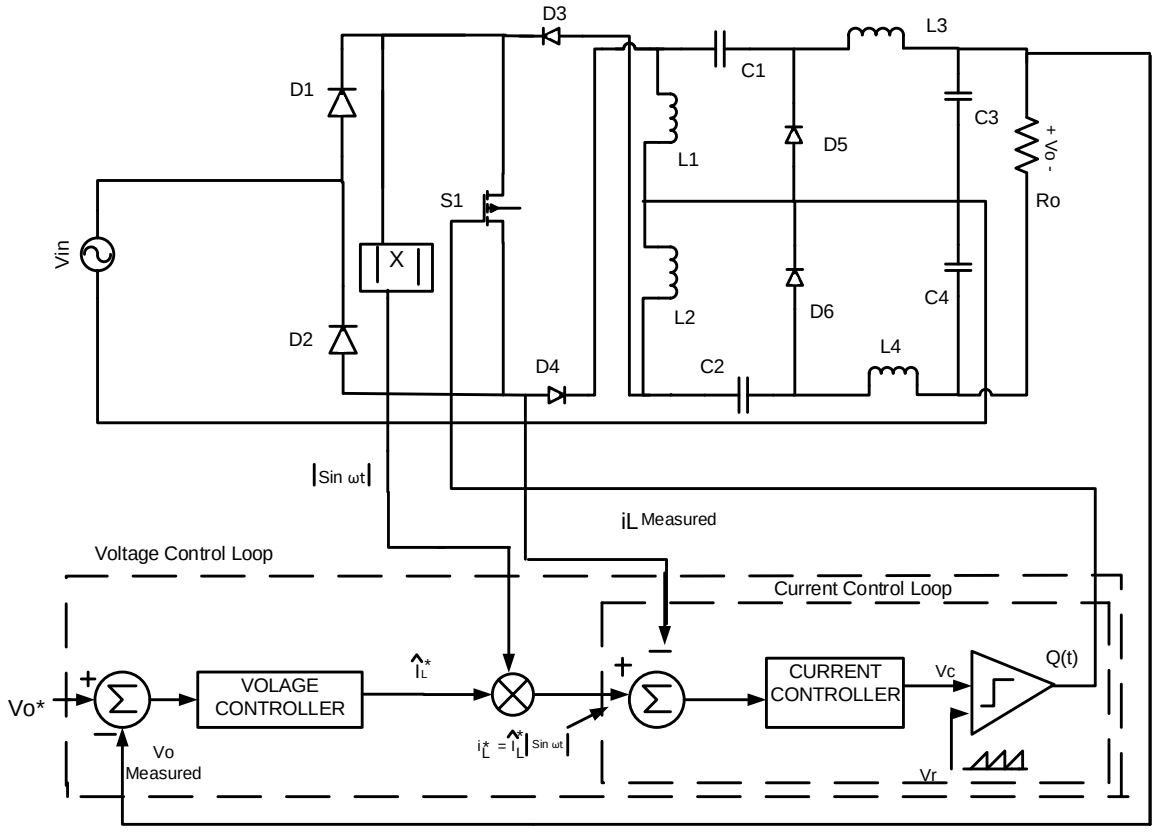


Figure 5.1: Proposed converter with feedback controller

5.2 Transfer function using State Space Averaging Technique

The converter has two states in each switching period.

(i) Switch is on for a time interval dT_{sw} and

(ii) Switch is off for a time interval (1-d) T_{sw}, where d is duty cycle and T_{sw} is switching period.

To model converters using steady state averaging (SSA) method state equations are obtained for both state of switch states [97]. When switch is on during time interval dT_{sw}, state-space equations of converter can be written as

$$\frac{dx(t)}{dt} = A_1\, x(t) + B_1\, u(t) \tag{5.1}$$

$$y(t) = C_1\, x(t) + E_1\, u(t) \tag{5.2}$$

Here x(t) is a state vector that contains all state variables such as capacitor voltage and inductor currents. u(t) and y(t) are called input vector and output vector respectively. Here A1, B1, C1 and E1 are 8x8 matrix, 8x1 matrix, 1x8 matrix and 1x1 matrix respectively.

When switch is OFF during time interval $(1\text{-}d)T_{sw}$, state-space equations of converter can be written as

$$\frac{dx(t)}{dt} = A_2\, x(t) + B_2\, u(t) \tag{5.3}$$

$$y(t) = C_2\, x(t) + E_2\, u(t) \tag{5.4}$$

The matrices A2, B2, C2 and E2 have co-efficients that describe the network connections during the time interval $(1\text{-}d)T_{sw}$.

Now the average of one switching period is

$$\frac{dx(t)}{dt} = A_{12}\, x(t) + B_{12}\, u(t) \tag{5.5}$$

$$y(t) = C_{12}\, x(t) + E_{12}\, u(t) \tag{5.6}$$

Here,

$$A_{12} = A_1 d + (1-d)A_2$$

$B_{12} = B_1 d + (1-d)B_2$

$C_{12} = C_1 d + (1-d)C_2$

$E_{12} = E_1 d + (1-d)E_2$

To obtain a small signal ac model, small perturbations are added to state space equations.

$x(t) = X + \hat{x}(t)$

$u(t) = U + \hat{u}(t)$

$y(t) = Y + \hat{y}(t)$

$d(t) = D + \hat{d}(t)$

Here $\hat{x}(t), \hat{u}(t), \hat{y}(t)$ and $\hat{d}(t)$ are small ac variations and the terms with capital letter denote DC values. Now for linearization the following conditions are to be met

$X > \hat{x}(t)$, $U > \hat{u}(t)$, $Y > \hat{y}(t)$ and $D > \hat{d}(t)$

Now from equations (5.5) and (5.6), small signal state space model can be found as

$$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{u}(t) + \{(A_1 - A_2)X + (B_1 - B_2)U\}\,\hat{d}(t) \quad (5.7)$$

$$\hat{y}(t) = C\hat{x}(t) + E\hat{u}(t) + \{(C_1 - C_2)X + (E_1 - E_2)U\}\,\hat{d}(t) \quad (5.8)$$

Wherein

$A = A_1 D + (1-D)A_2$

$B = B_1 D + (1-D)B_2$

$C = C_1 D + (1-D)C_2$

$E = E_1 D + (1-D)E_2$

Let,

$B_{ad} = (A_1 - A_2)X + (B_1 - B_2)U$

$E_{cd} = (C_1 - C_2)X + (E_1 - E_2)U$

Now taking Laplace transform of equations (5.7) and (5.8),

$$\hat{X}(s) = (sI - A)^{-1}[B\hat{u}(s) + B_{ad}\hat{d}(s)] \quad (5.9)$$

$$\hat{Y}(s) = C\ (sI - A)^{-1}\left[B\hat{u}(s) + B_{ad}\hat{d}(s)\right] + E\hat{u}(s) + E_{cd}\hat{d}(s) \quad (5.10)$$

Let us consider, input Vin, output Vo and duty ratio D. Then the small signal transfer functions are

$$\frac{\widehat{V_o}(s)}{\widehat{V_{in}}(s)} = C\ (sI - A)^{-1}B + E \quad (5.11)$$

$$\frac{\widehat{V_o}(s)}{\hat{d}(s)} = C\ (sI - A)^{-1}B_{ad} + E_{cd} \quad (5.12)$$

Now the circuit equations are obtained for DC-DC sections for small signal transfer function needed for controller.

When the switch S1 is On for dT_{sw} time the state equations are

$$\frac{di_{L1}}{dt} = \frac{V_{avg,r}}{L1}$$

$$\frac{di_{L2}}{dt} = \frac{-V_{C2}}{L2}$$

$$\frac{di_{L3}}{dt} = \frac{V_{avg,r} - V_{C1} - V_{C3}}{L3}$$

$$\frac{di_{L4}}{dt} = \frac{V_{C4}}{L4}$$

$$\frac{dV_{C1}}{dt} = \frac{i_{L3}}{C1}$$

$$\frac{dV_{C2}}{dt} = \frac{i_{L2}}{C2}$$

$$\frac{dV_{C3}}{dt} = \frac{i_{L3}}{C3}$$

$$\frac{dV_{C4}}{dt} = \frac{i_{L4}}{C4}$$

$$V_0 = V_{C3} + V_{C4}$$

Now, A_1, B_1, C_1 and E_1 can be expressed as follows,

$$A_1 = \begin{vmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L2 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/L3 & 0 & -1/L3 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L4 \\ 0 & 0 & 1/C1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/C3 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1/C4 & 0 & 0 & 0 & 0 \end{vmatrix}, B_1 = \begin{bmatrix} 1/L1 \\ 0 \\ 1/L3 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$C_1 = |0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1|$$

$$E_1 = [0]$$

When switch S1 is off in (1-d)T_{sw} time the equations are as follows

$$\frac{di_{L1}}{dt} = \frac{V_{C1}}{L1}$$

$$\frac{di_{L2}}{dt} = \frac{-V_{C2}}{L2}$$

$$\frac{di_{L3}}{dt} = \frac{-V_{C3}}{L3}$$

$$\frac{di_{L4}}{dt} = \frac{V_{C4}}{L4}$$

$$\frac{dV_{C1}}{dt} = \frac{i_{L1}}{C1}$$

$$\frac{dV_{C2}}{dt} = \frac{i_{L2}}{C2}$$

$$\frac{dV_{C3}}{dt} = \frac{-i_{L3}}{C3} - \frac{2V_{C3}}{RC3}$$

$$\frac{dV_{C4}}{dt} = \frac{-i_{L4}}{C4} - \frac{2V_{C4}}{RC4}$$

$$V_0 = V_{C3} + V_{C4}$$

Now, A_2, B_2, C_2 and E_2 can be expressed as follows,

$$A_2 = \begin{vmatrix} 0 & 0 & 0 & 0 & -1/L1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/L3 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1/L4 \\ 1/C1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1/C2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1/C3 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/C4 & 0 & 0 & 0 & 0 \end{vmatrix}, B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$C_2 = |0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1|$

$E_2 = [0]$

Now by using SSA technique, A, B, C and E are determined.

$$A = \begin{vmatrix} 0 & 0 & 0 & 0 & \frac{-(1-D)}{L1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-(1-D)}{L3} & 0 & \frac{-1}{L3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L4} \\ \frac{1-D}{C1} & 0 & \frac{D}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2D-1}{C3} & 0 & 0 & 0 & \frac{-2(1-D)}{RC3} & 0 \\ 0 & 0 & 0 & \frac{2D-1}{C4} & 0 & 0 & 0 & \frac{-2(1-D)}{RC4} \end{vmatrix}$$

$$B = \begin{bmatrix} D/L1 \\ 0 \\ D/L3 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$C = |0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1|$

$E = [0]$

Now the open loop transfer function, Go(s) can be found as follows,

$$Go(s) = \frac{5.43 \times 10^5 s^6 + 3.19 \times 10^7 s^5 + 1.16 \times 10^{13} s^4 + 7.075 \times 10^{14} s^3 - 4.84 \times 10^{19} s^2 - 2.28 \times 10^{21} s + 3.11 \times 10^{25}}{s^8 + 117.6 s^7 + 3.9 \times 10^7 s^6 + 4.59 \times 10^9 s^5 + 3.41 \times 10^{14} s^4 + 4.07 \times 10^{16} s^3 - 2.46 \times 10^{20} s^2 - 1.35 \times 10^{22} s - 4.21 \times 10^{25}}$$

5.3 Operating Principle of Single-Phase PFC controller

The proposed converter used MOSFET as switch and it is PWM at constant frequency. The current i_L through the inductor have the form of full wave similar to $|v_s(t)|$ as seen from Figure 5.2 where$i_L = \hat{I_L}|sin\omega t|$. $|v_s|$ represents the absolute value of the supply voltage. The output voltage V_0 of the proposed converter can be greater or less than the peak of supply voltage $\hat{V_s}$ depending on duty cycle, d.

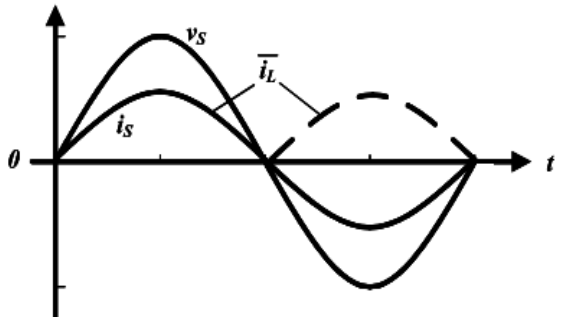


Figure 5.2: PFC waveforms

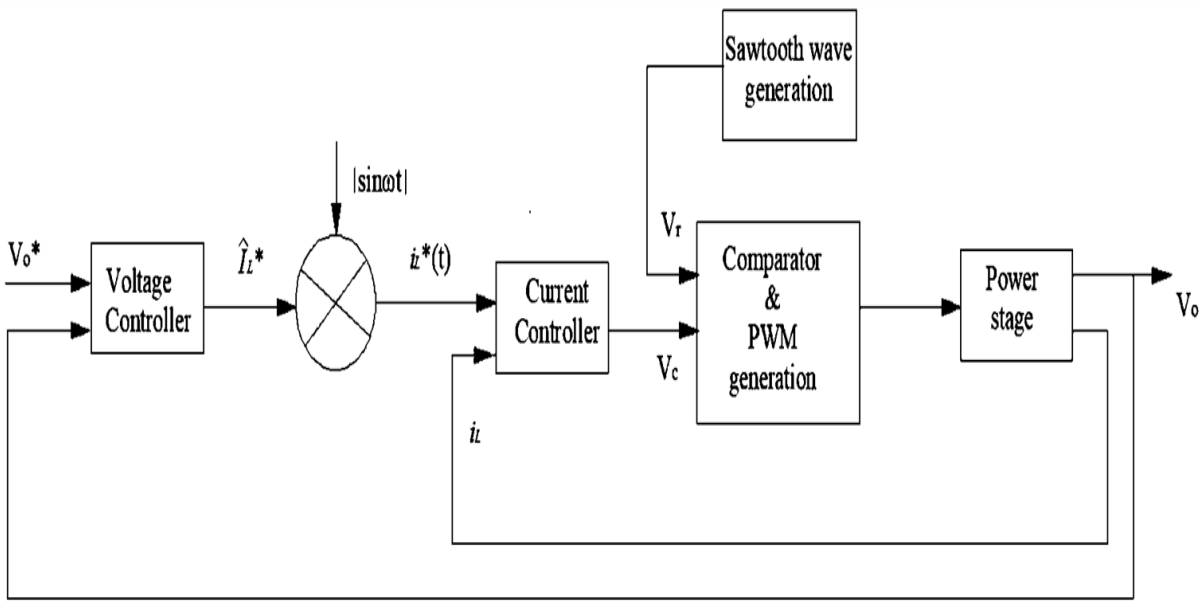


Figure 5.3: Control loop for proposed feedback control system

The main target of the control scheme is to draw a sinusoidal current that should be in phase with the converter input voltage. The inductor current reference $i_L{}^*(t)$ has the full rectified form as shown in Figure 5.2. The control system has two loops as shown in Figure 5.3. One is inner current loop and other is outer voltage loop. The inner loop ensures the form of inductor current. The outer loop controls the amplitude of $i_L{}^*(t)$ based on V_o and maintains the output voltage at a fixed preselected value. When the current of inductor is not sufficient for any load, Vo will drop below reference voltage Vo*. The voltage of control system in Figure 5.5 reshapes the amplitude of inductor current and thus Vo is maintained at its reference value. In this way voltage loop of controller maintains preselected output voltage for the converter. To follow the reference with little harmonics, average current control is used. The error signal produced from reference and measured inductor current is fed to a current controller. Then the control voltage Vc(t) is obtained from current controller. This voltage is compared with a ramp signal that is generated from a sawtooth wave generator with peak voltage of Vr at switching frequency and switching signal d(t) is generated as seen in Figure 5.4. This signal is then fed to MOSFET.

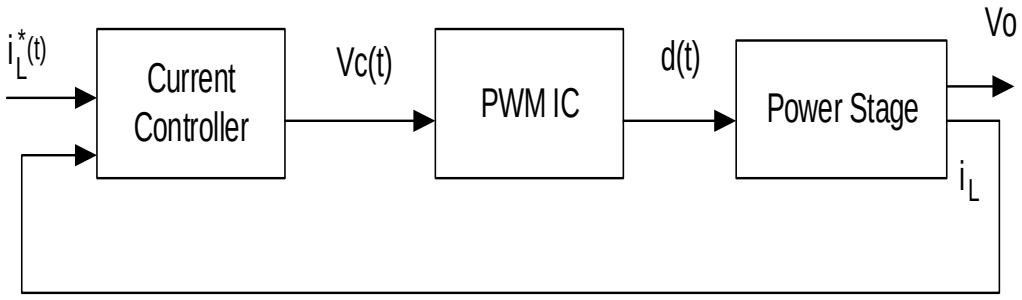


Figure 5.4: Current loop for the controller

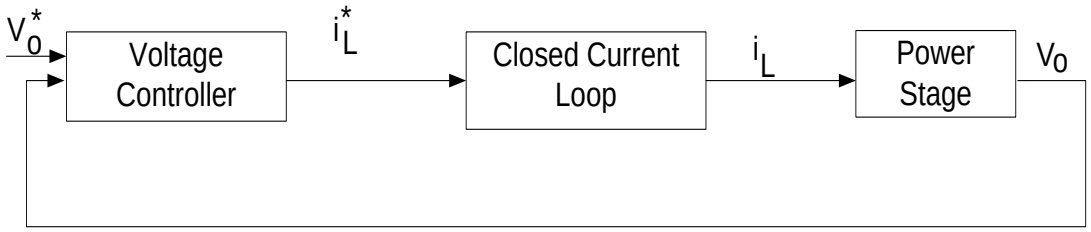


Figure 5.5: Voltage loop for the controller

5.4 Design of controller for current loop and voltage loop

To realize a current controller Proportional Integral (PI) controller is used in the feedback controller system. The circuit diagram of current loop PI controller is shown in Figure 5.6.

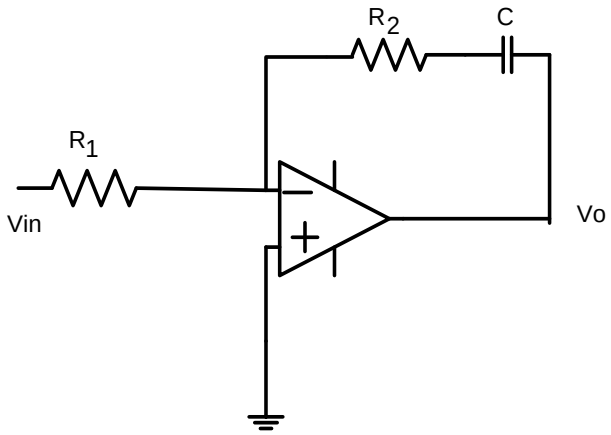


Figure 5.6*:* PI controller for current loop

The transfer function of the PI current controller, $H_{CC}(s)$ is derived as

$$H_{CC}(s) = -\frac{R_2}{R_1}\frac{(s+\frac{1}{R_2C})}{s} \tag{5.13}$$

Here, the PI controller is manually tuned and chosen values are $R_2 = 220k, R_1 = 10k$ and C=0.022uF.

So, from equation 5.13,

$$H_{CC}(s) = -\frac{220k}{10k}\frac{(s+\frac{1}{0.00484})}{s}$$

$$= \frac{-22s-4545.45}{s}$$

$$= -22 - \frac{4545.45}{s}$$

From the above equation we find K_{p1} = -22 and K_{i1} = - 4545.45.

The voltage controller is shown in Figure 5.7. The voltage controller yields the transfer function of

$$H_{VC}(s) = -\frac{\left(R_2 + \frac{1}{sC}\right) \parallel R_f}{R_1}$$

$$= -\frac{\frac{R_f R_2 sC + R_f}{R_2 sC + 1 + R_f sC}}{R_1} \tag{5.14}$$

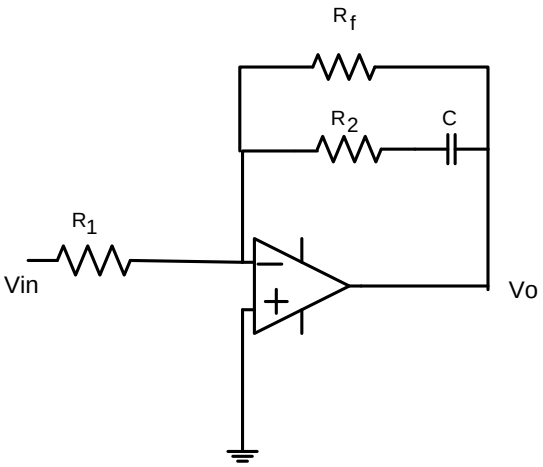


Figure 5.7: Voltage controller for feedback control

Here, $R_1 = R_2 = 10k$,$R_f = 12K$ and C = 0.01uF. So,

$$H_{VC}(s) = -\frac{R_f R_1 sC + R_f}{R_1^2 sC + R_1 + R_f R_1 sC}$$

After putting the values,

$$H_{VC}(s) = -\frac{1.2\,s + 12000}{s + 10000 + 1.2s}$$

$$= -\frac{1.2s + 12000}{2.2s + 10000}$$

5.5 Simulation with Designed Controller

Simulation has been done for the proposed converter with feedback controller. The parameters of the circuit are given in Table 5.1. The PFC Controller is designed to obtain an average output voltage of 900 V dc .The simulation results are given in Table 5.2. The input-output waveforms are shown in figure 5.8 and 5.9.

Table 5.1: Parameter for feedback controller of proposed converter

Parameters	**Value**
Input voltage (Vin) Peak	300 V peak
Switching Frequency (f_s)	5 kHz
Inductor (Lin)	5mH
Inductor (L1)	4 mH
Inductor (L2)	4 mH
Capacitance (Cin)	1 µF
Capacitance (C1)	10 µF
Capacitance (C2)	10 µF
Output capacitance (C3)	2m F
Output capacitance (C4)	2m F
Load Resistor (Ro)	100 ohm

Table 5.2: Results of the Simulation of the Converter with Feedback Controller (900V)

Performance Parameters	**Conventional Zeta converter**	**Proposed converter Without Feedback**	**Proposed converter With Feedback**
Efficiency (%)	90.63	92.34	**92.94**
Input Power Factor	0.97	0.95	**0.99**
Input Current THD (%)	14.13	16.42	**12.3**

It is evident from the Figure 5.8 that the input voltage and current are almost in phase and power factor is found to be 0.99 which is close to unity. Also the proposed converter with feedback operation can maintain desired average output voltage of 900V approximately as seen from Figure 5.9. The ratio of short circuit current, I_{sc} to fundamental frequency component of load current, I_1 is 88 for proposed converter. For I_{sc}/I_1 ratio on the range of 50-100, the tolerable THD range is 8-12% as per IEEE-519 standard [98]. THD with feedback controller is 12.3% which is very close to this standard.

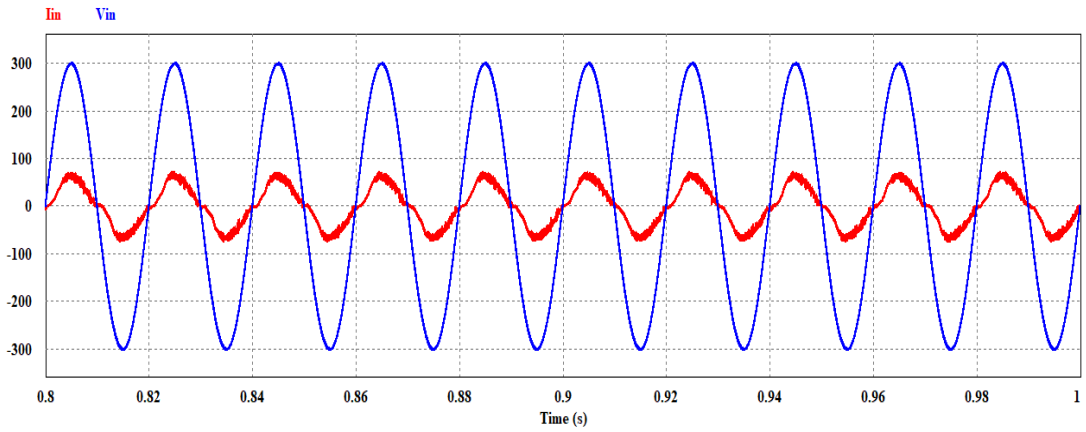


Figure 5.8: Waveform of input current and input voltage for proposed converter with feedback controller

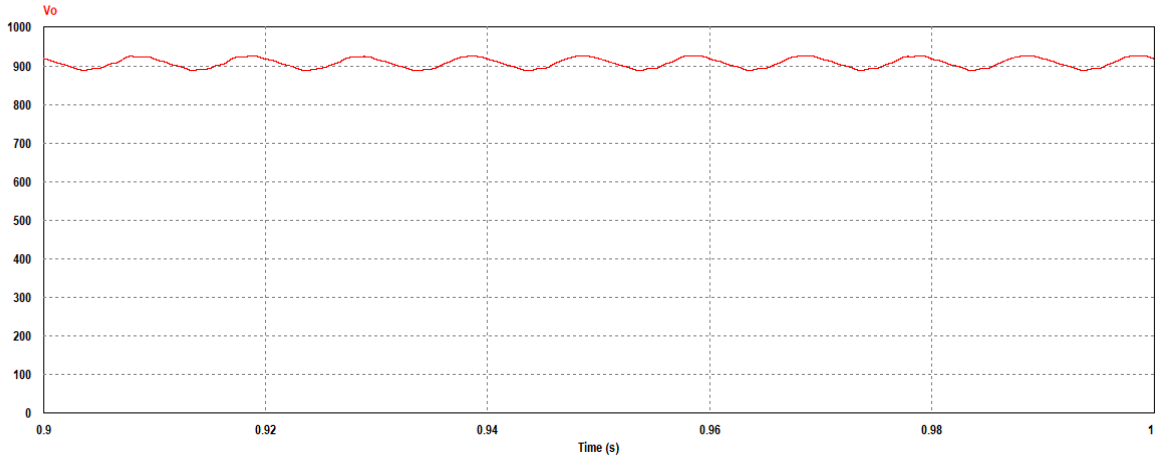


Figure 5.9: Waveform of output voltage for proposed converter with feedback controller

Ripple Calculation: Percentage ripple of output voltage is calculated for feedback response of proposed converter. From figure 5.9, it is evident that there the ripple percentage is low. The peak ripple is 17 V for the base voltage of 900 V. So the percentage ripple is 1.88% of base value.

5.6 Dynamic Response of proposed Converter

Dynamic behavior response is an important design consideration for AC-DC converters. Many converters suffer from problems to maintain required voltage level under sudden change of load. Therefore, dynamic response is observed for AC-DC converters to maintain desired average output voltage. The proposed converter with feedback controller can achieve stable dynamic response for load variations. Reference voltage was set to 900 V with initial load of 200 Ω. Simulation was carried out for

different load changes at different time. The load and time of change is shown in Table 5.3. Figure 5.10 shows the circuit arrangements for dynamic response.

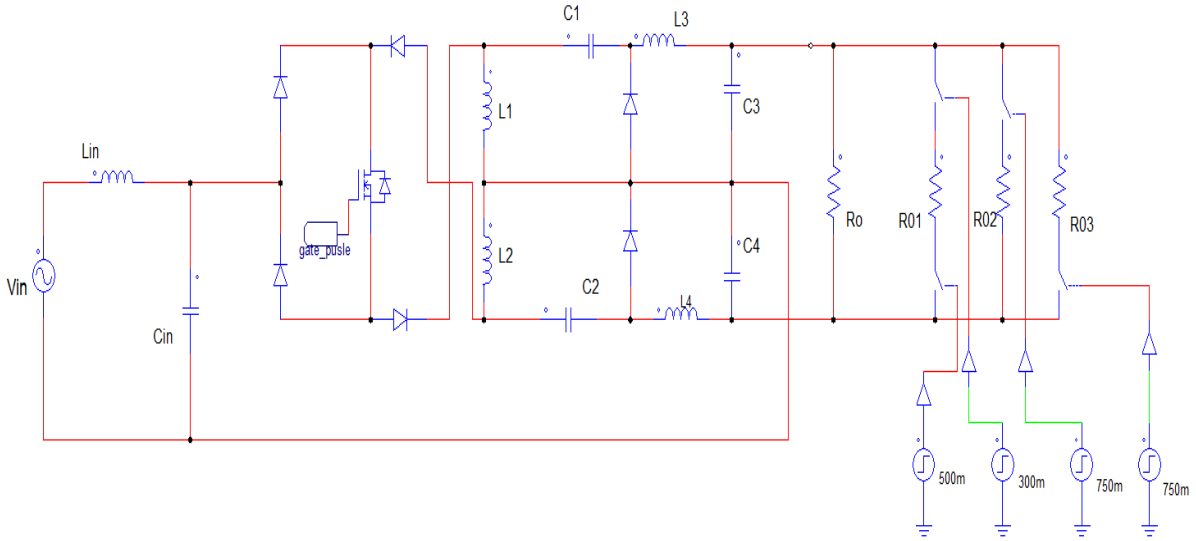


Figure 5.10: Circuit arrangement for dynamic response of proposed converter

The value of load resistances Ro, Ro1, Ro2 and Ro3 are chosen as 200 Ω, 100 Ω, 600 Ω and 200 Ω respectively. The effective load and time of change is shown in Table 5.3. Figure 5.11 illustrates the waveform of output voltage under dynamic load condition. It is observed that the proposed converter can maintain desired output voltage of 900 V dc.

Table 5.3: Load scheduling for dynamic response

Time (s)	**Load(Ω)**
0-0.3	200
0.3-0.5	66.6
0.5-0.75	100
0.75-1.0	150

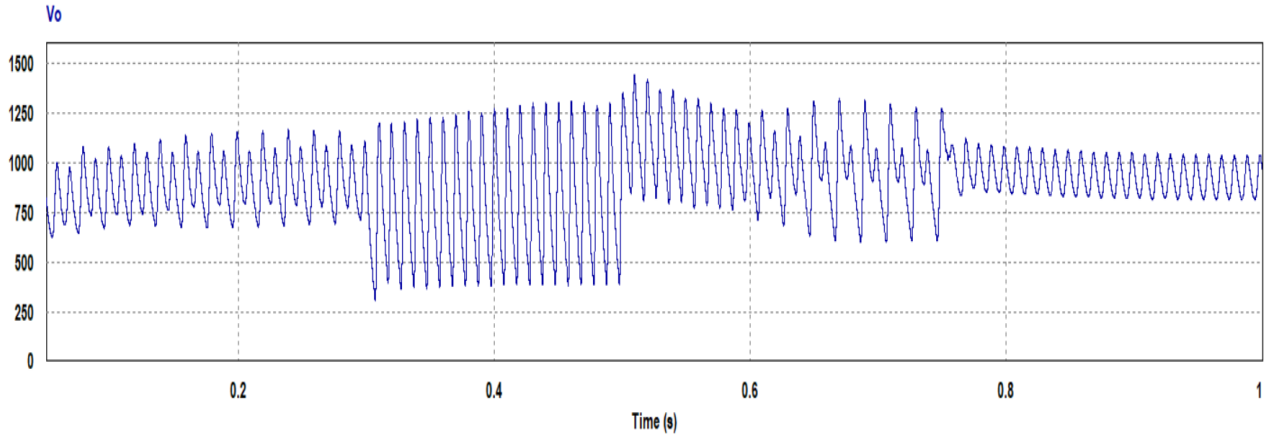


Figure 5.11: Waveform of output voltage for dynamic response

Chapter 6
Conclusion and Future Work

6.1 Summary

The proposed AC-DC Zeta converter can provide output in the same polarity with input signal and both step up and step down voltage can be achieved with good conversion efficiency and input PF. It is evident from the open loop data analysis that the proposed AC-DC converter gives better conversion efficiency throughout the duty ratio variation than the conventional converter. For lower and higher duty cycles, the proposed converter has some limitation in terms of input PF. This deficiency of input PF was overcome with the use of suitable closed loop controller which gives high input PF of 0.99. The closed loop controller gives higher efficiency even with high voltage gain than conventional converter. The proposed topology has high total harmonic distortion of input current in some of the duty cycle variations. Again, feedback controller solves this problem and the THD of input current was kept within the boundary set by IEEE standards. The voltage gain of proposed converter is better than conventional converter for most of the duty cycle variation. Highest achievable boost voltage gain is 4.68 for proposed converter whereas the conventional has gain of 4.48. It can be said that the proposed converter has some deficiency in terms of input PF and input current THD for some of the duty ratio variation, but with the use of suitable feedback controller these shortcomings are corrected. The use of closed loop feedback controller not only provides higher conversion efficiency but also gives better input current THD and PF.

A brief summary of the work discussed in this thesis book is given below:

Detailed literature survey on state of the art single phase AC-DC switched mode converters is carried out on Chapter 1. Brief introduction is given on power electronics systems, power factor and harmonic distortion on power.

In chapter 2, open loop analysis of conventional topologies of AC-DC converters are demonstrated. Different performance parameters like input current THD, input PF and efficiency are tabulated with the variation of duty cycle.

In chapter 3, an open loop performance analysis is carried out for the proposed AC- DC converter topology. Operating principle of the converter is described in details with suitable illustrations. Simulation results are tabulated and analyzed under different switching frequency variation, load variation and duty cycle variation. Graphical representation is also shown for all type of variations.

In chapter 4, detailed comparison between proposed converter and conventional converter is shown using tabulated data and graphical illustrations. Results are analyzed for different variations of duty cycle, switching frequency and load resistance. Proposed converter is compared with some recent works and result is shown.

In chapter 5, detailed analysis is carried out for the closed loop feedback controller used with the proposed converter. The dynamic response of the converter is inspected and relative simulation results are also provided. State space averaging technique is used to find out the transfer function to design the feedback controller.

6.2 Thesis Contribution

The contribution of this thesis work can be summarized as follows

- A new topology of AC-DC Zeta converter is proposed.
- Ideal voltage gain equation is obtained for the proposed converter.
- Performance analysis of proposed converter is carried out for duty cycle variation, load variation and switching frequency variation.
- Proposed converter is compared with conventional converters and some recent converters.
- Suitable controller is designed for the proposed converter.

6.3 Future Works

With the present state of the work, several future goals can be attained.

- Small signal analysis can be done to determine the AC equivalent circuit modeling.
- Conduction power loss at semiconductor diodes and the switching power loss at the switches can be calculated theoretically.
- Hardware implementation can also be carried out with suitable laboratory arrangements to validate this work.

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