Nano-Integrable Optical Logic Gate Implementation in Photonic Crystal Waveguide Using Beam Interference Principle

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CERTIFICATE OF APPROVAL

The submitted thesis entitled,"**Nano-Integrable Optical Logic Gate Implementation in Photonic Crystal Waveguide Using Beam Interference Principle**" submitted by Md. Istiac Ahmed, St. No. 170021069, Mohammed Radoan, St. No. 170021132, Md. Arefin Rabbi Emon, St. No. 170021134 of Academic Year 2017-18 has been found as satisfactory and accepted as partial fulfillment of the requirement for the Degree BACHELOR OF SCIENCE in ELECTRICAL AND ELECTRONIC ENGINEERING on April 20, 2022.

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Declaration of Authorship

We, the authors of this thesis entitled *"Nano-Integrable Optical Logic Gate Implementation in Photonic Crystal Waveguide Using Beam Interference Principle"*, declare that this book and all the findings presented in it are our own. We further confirm that:

- This thesis is submitted as the partial fulfillment of the Bachelor of Science in Electrical and Electronic Engineering degree at Islamic University of Technology (IUT).
- No part of this work has been submitted elsewhere for the award of any Degree or Diploma.
- We have always clearly attributed the sources when we have consulted the published work of others.

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List of Abbreviations

PhCs	Photonic Crystals
FEM	Finite Element Method
dB	Decibel
PCF	Photonic Crystal Fiber
EM	Electromagnetic
RF	Radio Frequency
LED	Light Emitting Diode
PCCS	Photonic Crystal Cavity Sensor
PhCWs	Photonic Crystal Waveguides
PBGs	Photonic Band Gaps
PhCRRs	Photonic Crystal Ring Resonators
SOA	Semiconductor Optical Amlifier
MMI	Multi-mode Interference
MZI	Mach-Zehnder Interferometer
ENIAC	Electronic Numerical Integrator And Computer
SPP	Surface Plasmon Polariton
MIM	Metal Insulator Metal
IMI	Insulator Metal Insulator
ERR	Elliptical Ring Resonator
BPSK	Binary Phase Shift Keying
TR	Transmission Ratio
CR	Contrast Ratio
ER	Extinction Ratio
RI	Refractive Index
IC	Integrated Circuit

Acknowledgment

"All praise and gratitude be to Allah, the most beneficent, the most merciful."

We can never deny the endless mercy bestowed upon us by the Almighty Allah (SWT). At the very beginning, therefore, we express our deepest gratitude to the Almighty for granting us the wisdom and capability to reach this far with the successful completion of this work. Alhamdulillah for everything!

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To conclude we would like to mention our parents as it was never possible to achieve our goals without their mental support.

Abstract

Optical logic gates are the best alternative to low-speed semiconductor-based integrated circuitry. Attractive features like small size, ultrahigh speed, tunability, reduced power consumption, and high selectivity have raised the demand for optical gates to a greater extent. By now research has ensured a promising field for optics-based technologies. However, the best logic gate arrangement is yet to be developed. In this work, a highly efficient photonic crystal waveguide-based structure has been proposed to implement all-optical AND-OR gates. The proposed structure implies the beam interference principle to carry out the logic operations. The proposed structure has a dimension of $8.4 \times 5.4\ \mu m^2$ with silicon nanorods embedded in the air background. Numerical analysis has been done using the Finite Element Method (FEM) in COMSOL Multiphysics software. Performance analysis shows that the optimized structural parameters give a high contrast ratio of 41.24 dB and 30.17 dB for OR and AND gates, respectively. Also, the extinction ratio has been found as high as 37.51 dB and 25.21 dB for OR and AND gates, respectively. These values have surpassed most of the recent works of all-optical logic gates. Simple design, high-performance factors, and compact size make the structure a suitable choice for on-chip integration.

Chapter 1

Introduction and Background

1.1 Nanophotonics: The Beginning

Back in the previous century, technologists put their utmost effort into reducing the device dimension. Along with gigantic size, the valve-based circuitry came with low operating speed. And the speed was also affected by continuous heating and delayed response. However, with the advent of semiconductor circuitry, it became possible to reduce the device dimension significantly to nm range. Nano-integrable semiconductor circuitry could attain GHz speed and offered transistor technologies. The underlying principle in semiconductors is to control the electron properties utilizing energy bands.

However, networking and communication applications demand higher operating speeds. Therefore, optical devices have become an attractive choice as it was always desirable to attain optical speed. Another reason for this is that the semiconductor technology is assumed to be limited due to heat dissipation difficulties in microchips [28]. It took a long time to develop a technology that can fusion light and nanodevices. Thus nanophotonics has made it possible to achieve both high speed and smaller dimensions. Nanophotonics is a multi-branch sector (Fig.1.1) offering different integration approaches [29].

Nanoscale confinement of radiation suggests light confinement in nanoscale geometries. It is possible only when the geometry has a significantly smaller dimension than the optical wavelength. The next approach is about nanomaterials that can combine photonic and electronic properties. Plasmonics and photonic crystals fall under this sector. The last approach, nanoscale photoprocesse, discusses the fabrication of photonic structures [1].

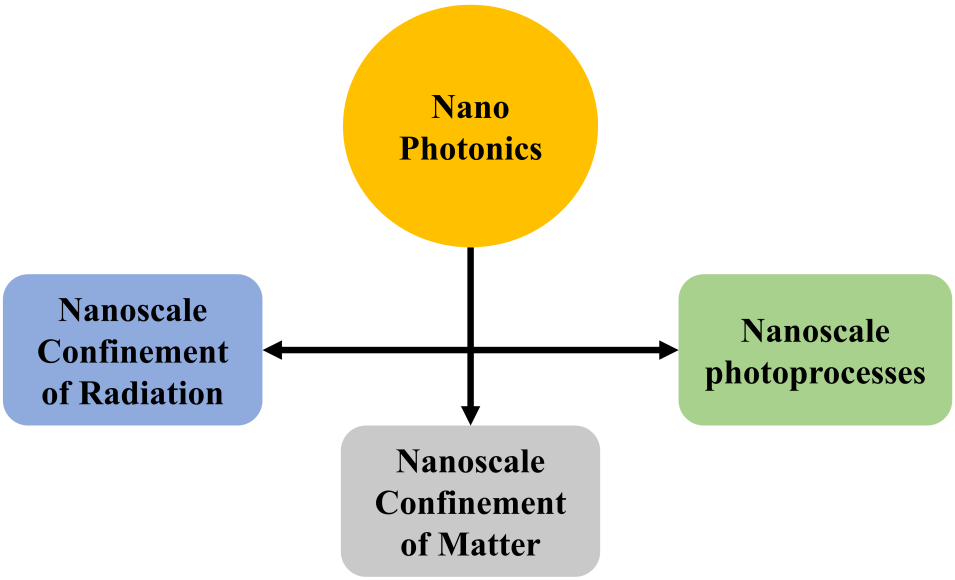


Figure 1.1: Branches of nanophotonics [1].

1.2 Photonic Crystals

As mentioned earlier, photonic crystals (PhCs) are examples of nanomaterials. PhCs are spurious materials having the property of periodically varying refractive indices. The periodicity is of the order of the incident light wavelength. Such a distinct structure has the unique capability of controlling photon properties and propagation in space [30]. PhCs are also widely named as 'Bandgap materials'. Such nomenclature is obvious as wave propagation through the PhCs is obstructed and controlled by creating energy bandgaps [31]. The periodicity in the crystal is obtained by the distribution of dielectric rods in the space and depending on the distribution over the space, photonic crystals can be one, two, and three dimensional [2].

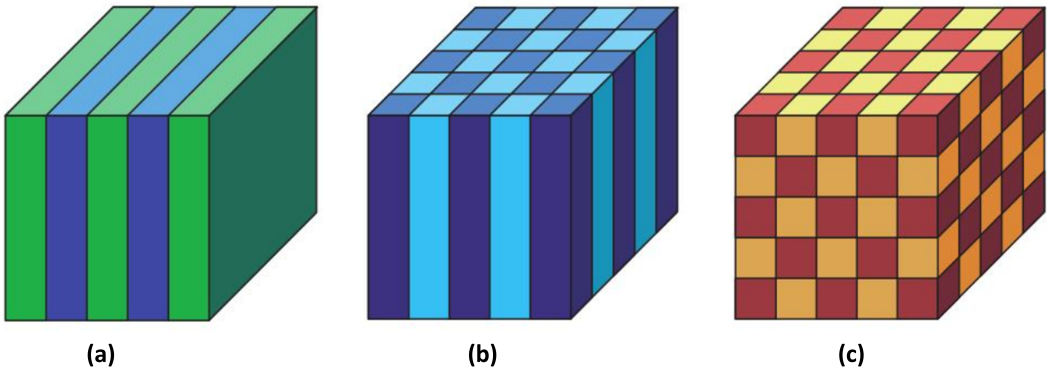


Figure 1.2: (a) One dimensional (1D), (b) two dimensional (2D), (c) three dimensional (3D) photonic crystal [2].

In practical scenarios, 1D crystals can be realized by stacking sheets of two different materials one after another; preferably placing dielectric sheets at a specific interval. 2D crystals may have dielectric cylinders or cuboids placed in the space while for 3D crystals, dielectric spheres or cubes can be stacked in the air medium [32].

1.2.1 Semiconductor of Light

All the functionalities of photonic crystals take place due to the periodic variation of the refractive index. The concept of guiding the photon path with such periodicity had arisen from the atomic structure of semiconductors [33].

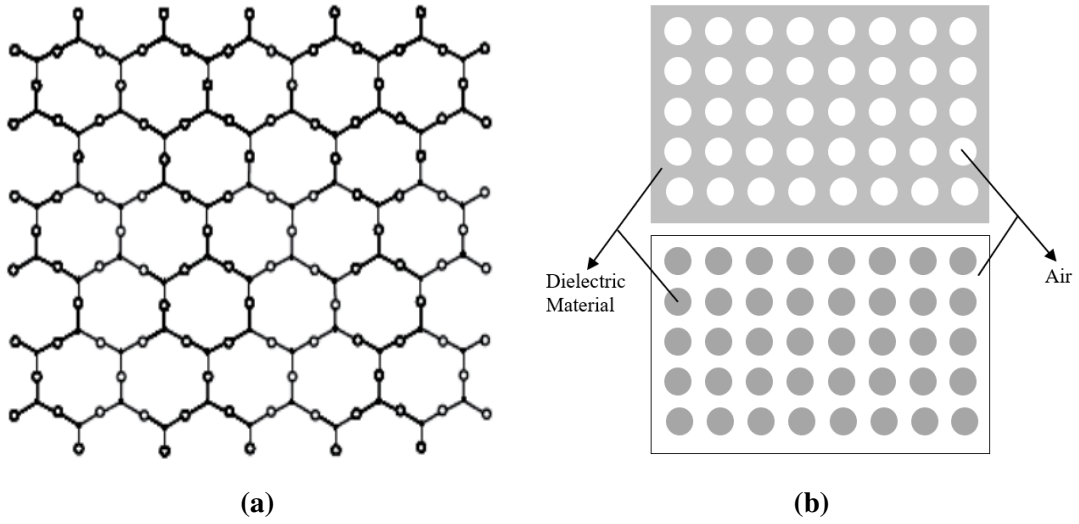


Figure 1.3: (a) Crystalline structure of semiconductor (Si) [3]. (b) 2D photonic crystal.

Quantum mechanics says that an electron exhibits its wave nature in the conduction process while passing through crystals. An electron witnesses a periodic array of atoms in its path. This periodic atomic arrangement sets up a periodic potential throughout the crystal. This periodic potential does not allow every wave to propagate within the crystal because not every wave possesses the energy to cross the potential barrier. Such a potential barrier is marked as an energy gap in the energy band structure.

The constituents and geometry of the crystal lattice greatly control the crystal's conduction properties. In semiconductor materials, the bandgap or potential barrier can be overcome by external excitations or by manipulating the inner structure. Therefore, a sufficient number of dopants are injected into the structure to gain control over the crystal conductivity which ultimately leads to the control of electron properties inside the crystal.

In a similar manner, photons face a periodic variation of refractive indices inside the photonic crystal. Therefore, a periodic dielectric function prevails in the photonic crystal and creates photonic bandgap in the energy band much similar to the elec-

tronic bandgap in semiconductors. With this, optical manipulation and control are gained by using photonic crystals. In Fig.1.4, an analogy has been presented between the semiconductor and photonic crystal bandgap. The position and the width of the bandgap can be adjusted by changing the lattice constant and dielectric constant ratio, respectively. Due to the capability of molding light, photonic crystal is termed as the '*Semiconductor of Light*' [4]. Again for the bandgap property, photonic crystal materials are familiarized as '*Bandgap Materials*'.

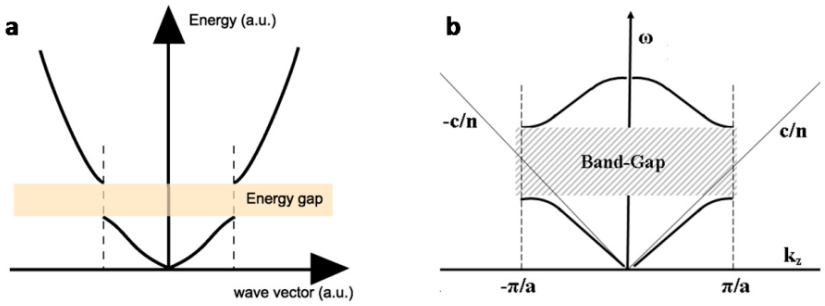


Figure 1.4: (a) Semiconductor bandgap. (b) Photonic crystal bandgap [4].

1.3 Photonic Crystal Applications

Gaining the ability to control light properties was a long-desired achievement in optics. Previously optical devices were operated based on the principle of reflection, absorption, and refraction only [34]. But now it has become possible to manipulate light as per requirement and it has opened a diverse application field with higher efficiency. Some of the applications of photonic crystals are mentioned below [35].

1.3.1 Optical Fibers

Photonic crystal fibers (PCF) is a class of 2D photonic crystals that has been stretched towards the homogeneous axis. PCFs are used to confine and guide lights. PCF sensors have been a wide area in optics.

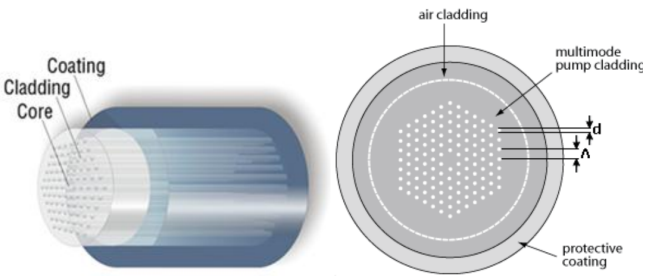


Figure 1.5: PCF structure with air cladding [5].

1.3.2 Nanoscopic Lasers

2D photonic crystals can form the tiniest surface-emitting lasers. A standing wave occurs due to Bragg's reflection and the EM field is perfectly distributed and defined at every lattice point. The optical beam is being diffracted perpendicular to the PhC plane [6].

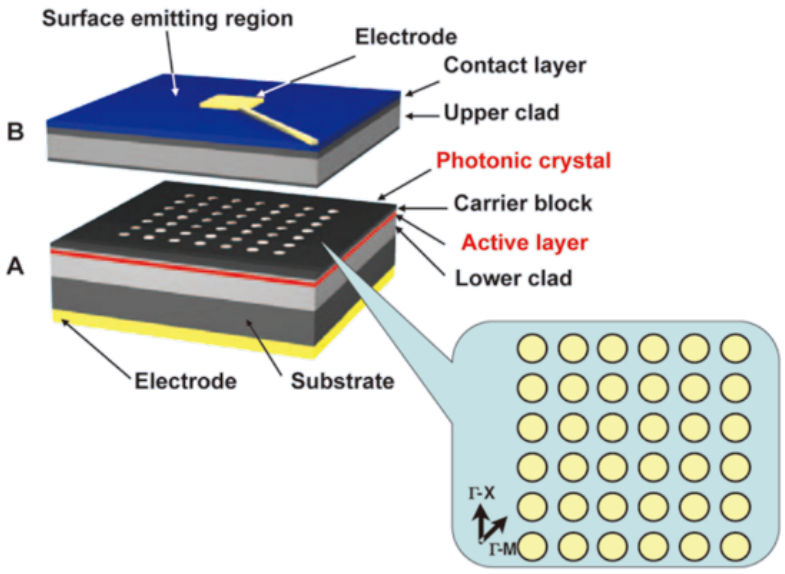
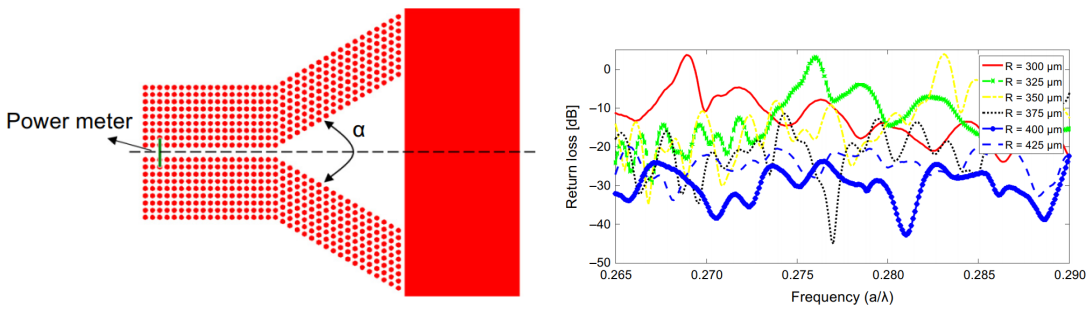


Figure 1.6: Photonic crystal laser structure [6].

1.3.3 RF Antennas

Due to the bandgap property, photonic crystals have been widely used to transmit electromagnetic radiation as signals for a specific operating wavelength. The low loss property of photonic crystals adds more significance to the construction of radio frequency antennas [7].



(a) **(b)**

Figure 1.7: (a) Proposed RF horn antenna. (b) Return Loss for different hole radius [7].

1.3.4 Photonic Crystal Mirrors

Photonic crystal slabs can be used to construct mirrors. When the incident light falls under the photonic bandgap, it gets reflected.

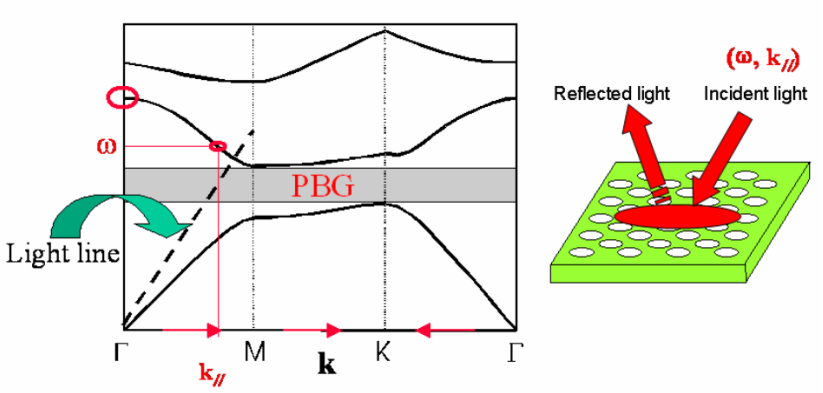
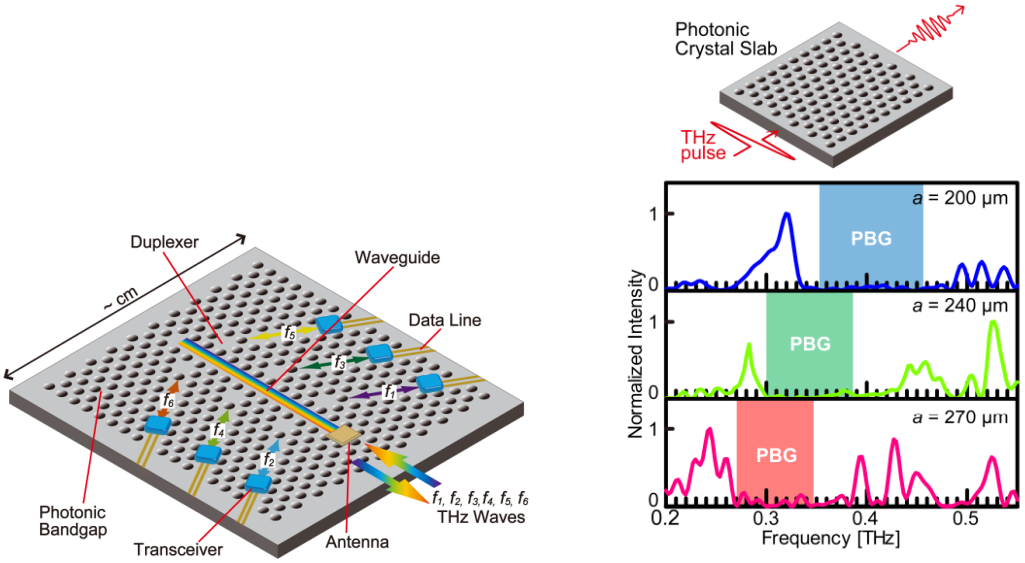


Figure 1.8: Operating principle of photonic crystal mirror [8].

1.3.5 Photonic Integrated Circuit

Nanoscale structure and ultralow absorption loss make photonic crystals an attractive choice for integrated circuits [9]. In a 2D photonic crystal slab, different components can be integrated. Implementing the concept, multiplexer [36], demultiplexer [37], channel drop filter [38], etc. can be constructed.



(a) **(b)**

Figure 1.9: (a) Schematic of a THz wave IC for a 6-channel photonic crystal frequency division multiplexing transreceiver. (b) Transmission spectra for varying lattice constant, a [9].

1.3.6 Photonic Crystal LEDs

Photonic crystal-based Light Emitting Diodes (LEDs) can enhance light extraction and make an increment of around 50% efficiency. A major amount of light absorbed inside the semiconductor can be extracted by incorporating a photonic crystal inside the conventional LED [10].

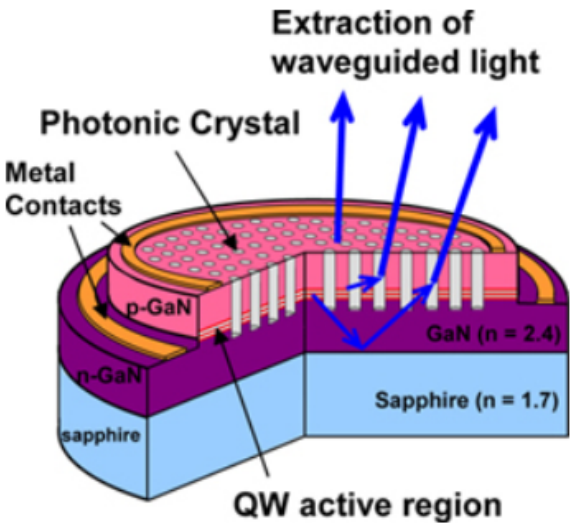
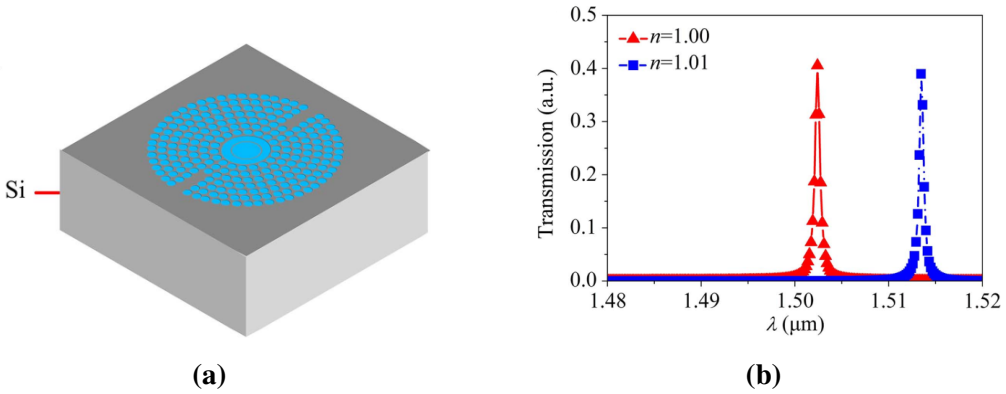


Figure 1.10: Photonic crystal incorporation inside an Indium-gallium-nitride (InGaN) LED [10].

1.3.7 Photonic Crystal Sensors

Photonic Crystal Cavity Sensors (PCCS) are widely studied and implemented mostly in chemical and biosensing applications. Such widespread usage of PCCS is due to quick response and high-performance factors [11].



(a) **(b)**

Figure 1.11: (a) 3D structure of the photonic crystal cavity sensor. (b) Transmission spectra for varying refractive index, η [11].

1.3.8 Photonic Crystal Filters

Optical filters have significant selectivity and noise cancellation. Photonic crystal sensors are highly appreciated because of their bandgap property which can provide a sharp output. Besides, waveguide-cavity coupling can lead to flexibility and adjustment in optical filter designing [12].

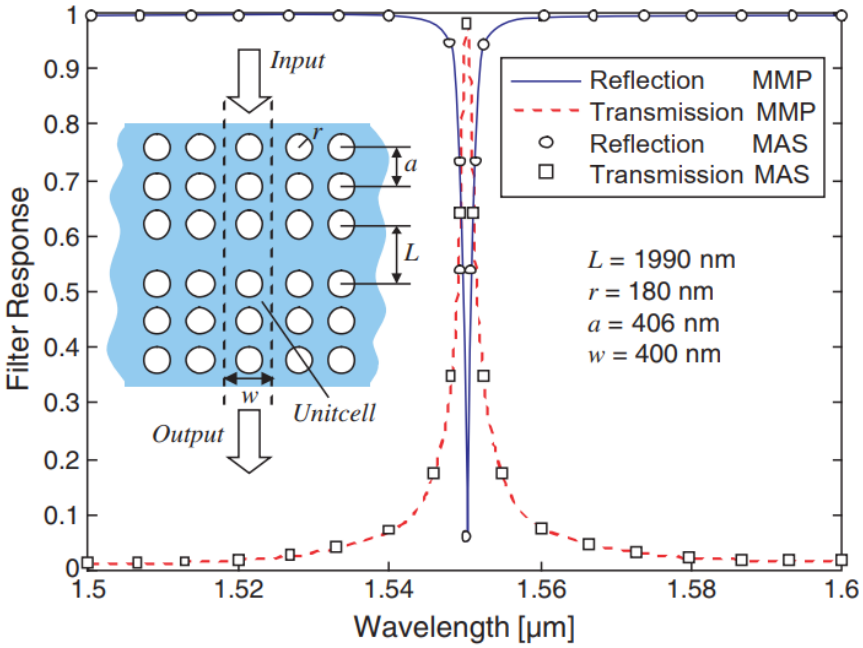


Figure 1.12: A PhC slab filter and its output specta [12].

1.4 Photonic Crystal Waveguides (PhCWs)

Photonic crystals (PhCs) are dielectric-based synthesized periodic structures. Air holes or solid rods are distributed periodically over the structure plane, where the gap between them is shorter than the wavelength of traveling light [39]. When light tries to travel through the holes or rod structure, it is reflected away. Alternatively, light can travel through a channel if is wider than the wavelength of traveling light [40]. Rajan *et al.* compared this with cutting a road for transportation [41]. This is the phenomenon of light localization which was hypothesized in 1987 and has recently been realized with photonic crystals [13]. These channel waveguides are made up of a succession of defects in the periodic lattices. And they use two significant photonic crystal properties: photonic band gaps (PBGs) and defect states [42]. Due to the inadequate optical alignment in traditional index-type waveguides, the guided light suffers significant radiation loss at sharp bends. It severely limits the adaptability of optical wiring and causes photonic circuits to grow to the cm^2 scale. The photonic crystal waveguide has

the ability to overcome this limitation [43]. These defects can be of two types; point defects and line defects.

1.4.1 Point Defects

Point defects can be created by creating a cavity in the periodic lattice. Light cannot propagate through the lattice; hence it is confined in the point cavity. Point defects can also be referred to as resonators [44]. The 3D structure of a photonic slab with a point defect is shown in Fig.1.13. The defect is created by removing air holes of a particular region introducing an aperiodicity in the structure. This defect or cavity is now wider than the wavelength of traveling light so light can propagate through this defect. But it cannot pass through the periodic region. As a result, the light is confined in the defect.

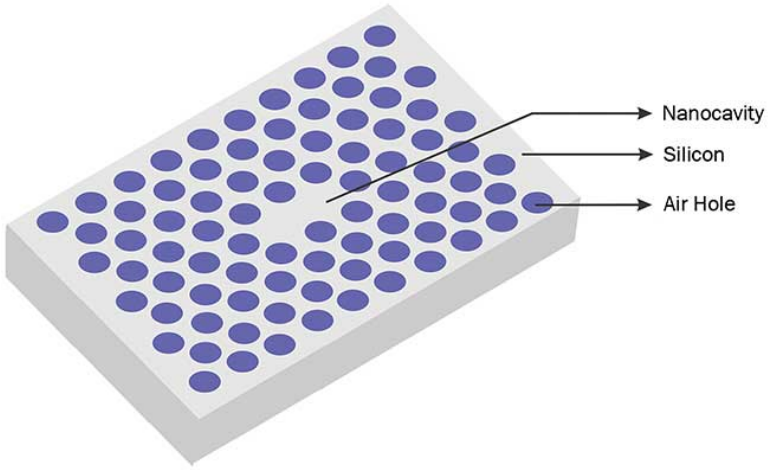
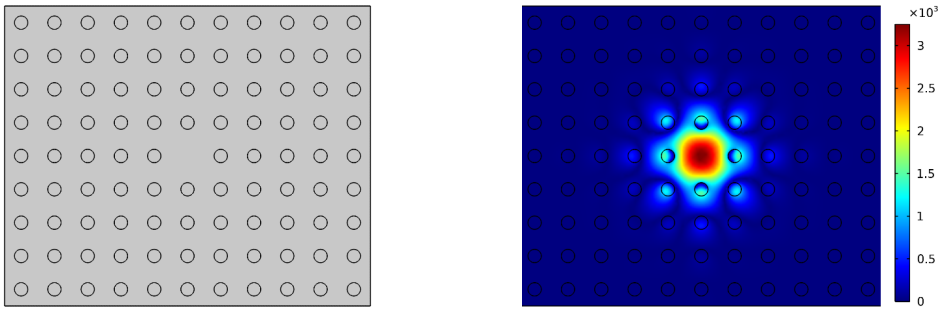


Figure 1.13: Cavity created in a photonic crystal slab through aperiodicity in the lattice [13].

This structure has been simulated in COMSOL Multiphysics, where a point defect has been introduced in a periodic lattice of silicon rods.



(a) **(b)**

Figure 1.14: (a) Photonic crystal structure with a point defect. (b) E-field distribution and light confinement in the cavity.

As observed in Fig.1.14, a cavity has been created and the light is being confined in that cavity without being able to leak to the outside wall. Because the light in

the forbidden frequency range is being reflected from the periodic lattice back to the confined defect. These cavities in PhCs are the building blocks of optical logic gates.

1.4.2 Line Defects

A line defect is like an extension of a point defect. While point defect creates a cavity, line defect creates a waveguide where the forbidden frequencies can be contained. In Fig.1.15, we can observe this defect which is composed of a succession of absent airholes in the photonic slab. Through these defects formed within the structure by disrupting the periodicity, light can be guided through them with negligible propagation loss for particular wavelengths [45].

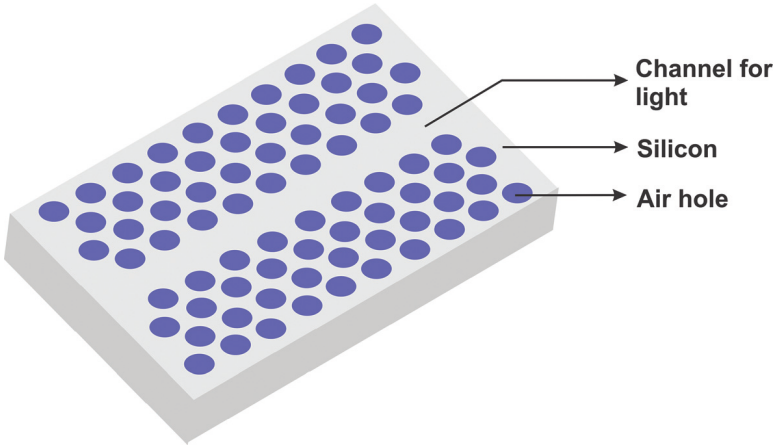
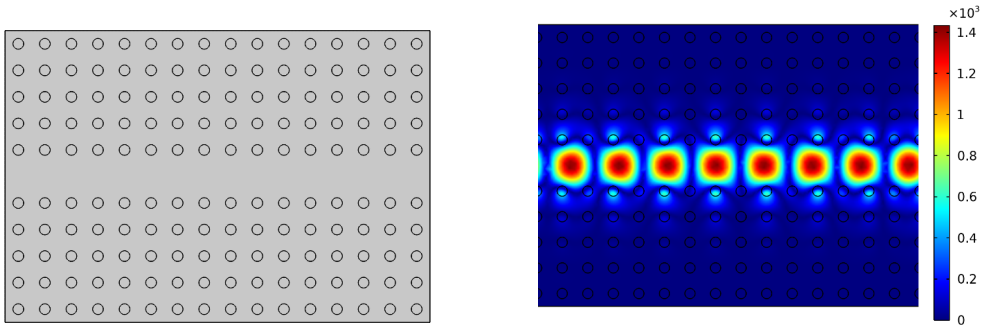


Figure 1.15: Channel waveguide created in a photonic crystal slab through line defect [13].

For illustrating this point, a 2D photonic crystal slab is modeled with silicon rods arranged periodically shown in Fig.1.16. Then a line defect is introduced by removing a row of dielectric rods from the slab. Inside the channel, a single guided mode band is introduced. The guided mode's field is tightly contained in the proximity of the defect and decays exponentially outwards [46].



(a) **(b)**

Figure 1.16: (a) Photonic crystal structure with a line defect. (b) E-field distribution and light confinement in the channel waveguide.

Photonic crystal waveguides are exciting because they offer a unique approach to steering optical light through narrow passageways in a tractable and efficient manner. There is nowhere else for light to go after it enters the waveguide. As a further venture, it is also studied what happens when the spacing is larger than the wavelength of traveling light. Theoretically, the light should leak through the spacing leading to significant propagation loss. And it is evident from Fig.1.17. The spacing between adjacent rods is called lattice constant. The lattice constant in this arrangement is adjusted to be larger than the required spacing for tight confinement of light at a specific wavelength.

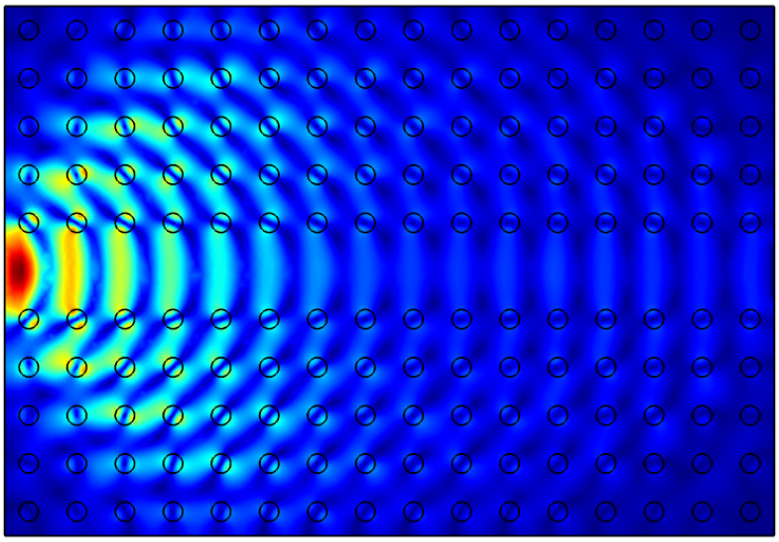


Figure 1.17: Propagation loss and leakage through photonic crystal.

In optical logic gates, having a high contrast ratio and minimal losses are critical. Changes in structural variables such as rod form and radius, cavity shape, lattice constant, and dielectric constant of rods lead to better control of loss features and an increase in contrast ratio. We will investigate these in the later sections for the optimization of our model.

1.5 Optical Logic Gates using PhCWs

The demand for high-speed computing while requiring low power is increasing day by day. Previously, this high-power consumption and slow speed were the disadvantages for optical communication systems. But now, researchers are working on optical logic gates that do not require optical to electrical conversion or vice versa which leads to an increase in the computing speed of the whole system. These devices are able to handle

high data rate and bandwidth. And they are made with photonic crystal waveguides (PhCWs). These waveguides are created by incorporating line or point defects into a structure that permits light to pass through in the frequency bandgap.

There are several approaches for designing all-optical logic gates. There are non-linear methods such as Kerr material, and Photonic Crystal Ring Resonator (PhCRRs). And there are linear methods like Semiconductor Optical Amplifier (SOA), Multi-mode Interference (MMI), and Mach-Zehnder Interferometer (MZI). But all of them have various disadvantages such as non-linear susceptibility, complex structure, high power requirement, low bit rate, less confinement of light, and dependency on the carrier's retrieval time [24].

To overcome these problems, photonic crystal waveguides are preferred. PhCWs have the advantages of small size, high speed, and strong confinement of light. The proposed structure, in this work consists of photonic crystal waveguides designed with an array of cylindrical silicon rods in the air as the background. One structure is used for all logic gates operation with required phase alterations in the applied control signal [18].

1.6 Literature Review

The history of logic functions started with electromagnetic relays [47]. Relays were just on-off switches. Their operational principle was majorly electro-mechanical and was prone to dangerous malfunctioning. However, vacuum tubes were the first programmable switches in history. They were also used in the ENIAC, one of the former computers [48]. Though it was a historical achievement but lacked fast response. Also, the tubes were gigantic in size, and most of the energy was used to waste as heat. Therefore, the system was quite inefficient compared to the demand for increased computational speed.

Semiconductor technology emerged with nano-scale integrable devices with high processing speed. Transistor logic gates indeed served the demand but now in this era, higher processing and computational speed are on demand. A major drawback of semiconductor-based integrated circuits and microchips is that the connecting copper trails lack the capability of high speed. Also at the connecting junctions, significant losses take place due to contact potential and heating issues [49].

Optical fibers could be a viable option to overcome these shortcomings but the macro-size of the fibers compared to the electronic circuitry made it difficult to integrate optics and electronics [50]. Therefore, there was a dire need to have a technology that can provide high operating and computational speed with minimum loss. And it must be nano-scale integrable.

Previously optical devices were operated by using the reflection, refraction, and absorption properties of light. There was no such technology to manipulate light so that photon energy can be utilized. Over the years different technologies have emerged to efficiently utilize light energy. A notable one is the Surface Plasmon Polariton (SPP) which made it possible to overcome the diffraction limit of light [51]. However, recent research has proved that optical logic gates have much more flexibility and efficiency than the traditional transistor-based logic gates. implementation techniques such as optical fibers, Kerr materials, photonic crystal ring resonators, plasmonic waveguides, semiconductor optical amplifiers, and several others have been studied to attain the best operation. Nevertheless, each of them has its own advantages and disadvantages. In this study, plasmonic waveguide and photonic crystal waveguide based optical gates will be highlighted.

1.6.1 Plasmonic Waveguide-based Optical Gates

Plasmonic waveguide-based structures follow the principles of surface plasmon polariton. Due to this, optical manipulation and light-matter interaction have been possible at the sub-wavelength level by overcoming the diffraction limit of light. Several structures have been developed to implement all-optical logic gates using plasmonic waveguides because of their high transmission rate. However, plasmonic waveguides have less light confinement, and different configurations such as Metal-Insulator-Metal (MIM), and Insulator-Metal-Insulator (IMI) have significant effects on the performance [52].

Nanodisk Resonator

In 2012, Dolatabady *et al.* propsoed a 2D plasmonic waveguide structure with nanodisk resonator. Using these structures they have evaluated XOR, XNOR, NAND, and NOT gates. They have also showed that the proposed gates can be cascades and hence different logic structures can be carried out [14].

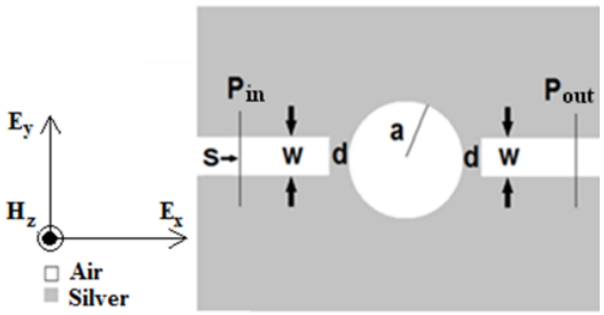


Figure 1.18: Basic structure of the nanodisk resonator [14].

The performance of the gates have been evaluated by calculating ON/OFF ratio which is defined as;

$$ON/OFFRatio = 10\log\left(\frac{P_{out|ON}}{P_{out|OFF}}\right) \tag{1.1}$$

The respective ON/OFF ratio has been tabulated in Table 1.1

Table 1.1: ON/OFF Ratio for Nanodisk Resonator Gates

Gate	ON/OFF Ratio
XOR	26 dB
XNOR	24 dB
NAND	23 dB
NOT	23 dB

Nonlinear Plasmonic Nanocavity

Yang et al. proposed all-optical logic gates based on nonlinear plasmonic nanocavity in 2017. This structure implemented XNOR, XOR, and NAND gate with a contrast ratio of 20 dB. The contrast ratio is defined as the average power ratio of logic state '1' to logic state '0' at the output port [15].

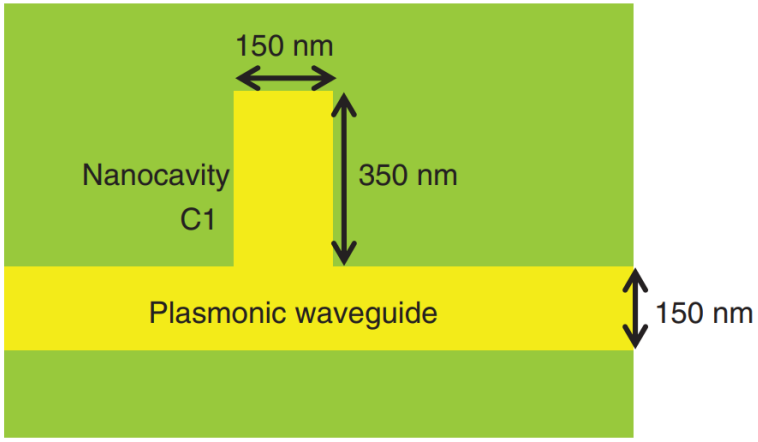


Figure 1.19: Schematic of the nonlinear plasmonic nanocavity [15].

Reconfigurable Logic Gates using Slot Waveguide

A reconfigurable plasmonic gate structure has been studied by Vladescu *et al.* in 2018. The structure is termed as slot waveguide constructed with graphene. Here the dielectric constant can be tuned and thus 1, 2, and 3-bit logic operations can be performed [16].

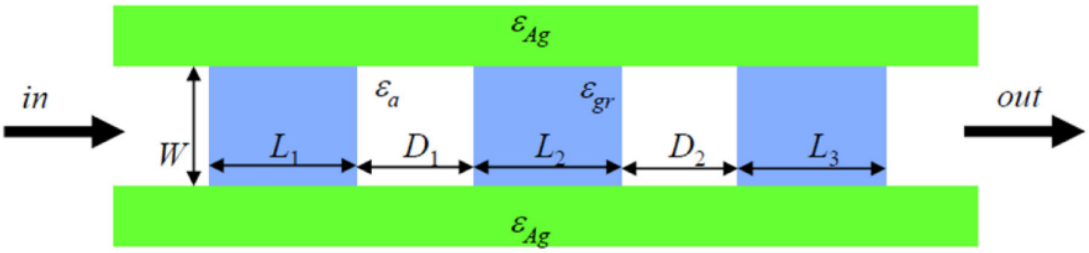


Figure 1.20: Schematic of the slot waveguide [16].

MIM Elliptical Ring Resonator

Haffar *et al.* has developed a MIM elliptical Ring Resonator (ERR) in 2021 to implement all-optical logic gates. This ERR has been utilized to demonstrate OR, XOR, AND, and NOT gate. The contrast ratio has been calculated as high as 28 dB [17].

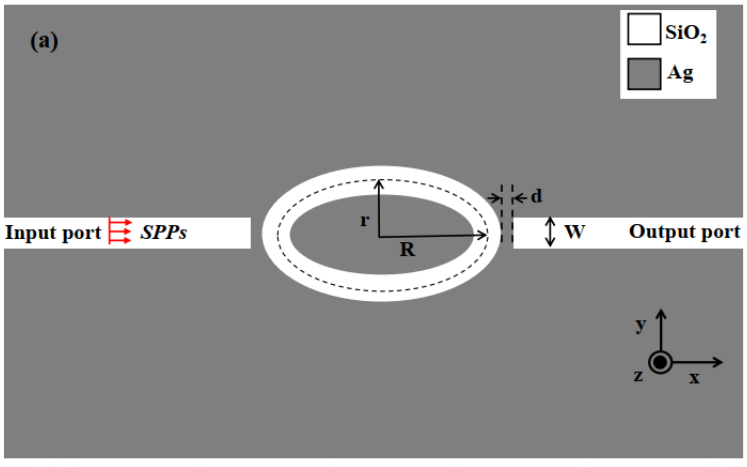


Figure 1.21: Proposed elliptical ring resonator [17].

1.6.2 PhCW-based Logic Gates

Logic gates using photonic crystal waveguides use several waveguides and defect cavities in different orientations to obtain the logic operations. The waveguides are interconnected and sometimes are cascaded to increase efficiency and to perform different combinational logic circuits [53].

All-optical Logic Gates using 2D Silicon PhC

Fu *et al.* have demonstrated a 2D silicon photonic crystal in 2013 to realize OR, XOR, NOT, XNOR, and NAND gate. The contrast ratio has been found to be as 20 dB with the feature of low power consumption. The authors have used beam interference principle [18].

Figure 1.22: Proposed schematic of 2D silicon PhC [18].

Y-shaped Photonic Crystal Waveguide

Rani *et al.* worked on a 2D Y-shaped structure to design AND gate in 2013. It has air holes in silicon substrate. The gate is found to operate at a bit rate of 0.830 Tbit/s [19].

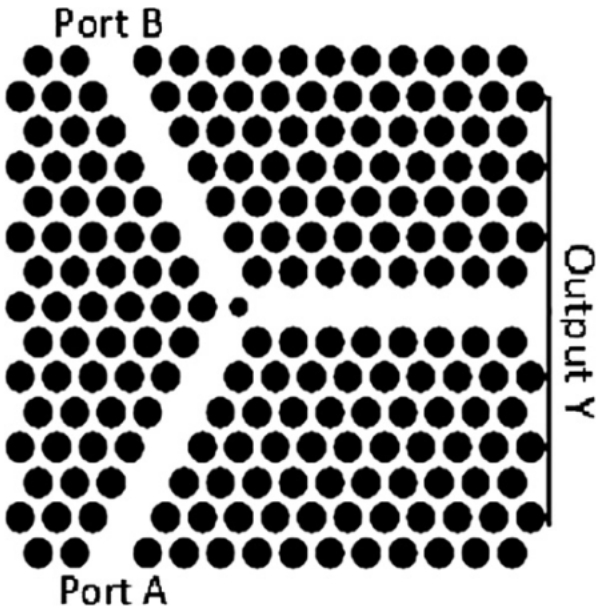


Figure 1.23: Proposed Y-shaped structure [19].

MMI-based 2D PhC All-optical Logic Gates for BPSK Signals

A SiO_2 based PhC has been developed with Si rods to process Binary Phase Shift-keyed (BPSK) signals. Multimode interference (MMI) has been implemented in an

arrangement of unequal waveguides. No external phase shifting arrangement is required for this structure and hence it is suitable for on-chip integration. The contrast ratio for the corresponding gates are presented in Table 1.2 [20].

Table 1.2: Contrast Ratio for the Gates

Gate	Contrast Ratio
XOR	21 dB
XNOR	17 dB
OR	13 dB
NAND	13 dB

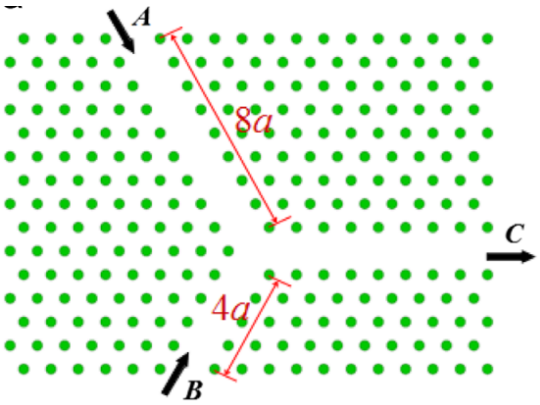
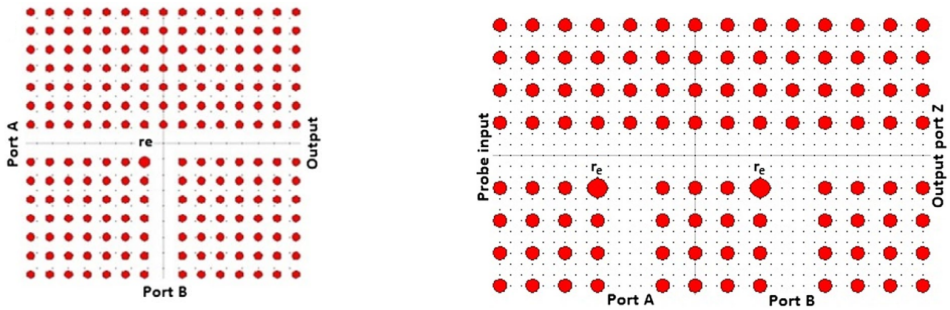


Figure 1.24: Schematic of the proposed MMI-based structure [20].

All-optical AND gate using T-shaped Waveguide

This structure is reported by Shaik *et al.* in 2015. They have demonstrated two configurations for implementing AND gate. One is of T shape without probe input and another is of double T shape with probe input. The gates show a contrast ratio of 5.74 dB and 9.66 dB, respectively. The authors expect this structure to be compatible with large-scale integration [21].



(a) **(b)**

Figure 1.25: AND gate (a) with probe input, (b) without probe input [21].

All-optical Full Adder

Swarnakar *et al.* developed this combinational logic circuit in 2018 implying beam interference. The structure is a 2D PhCW that combines T and W shaped waveguides. Here the authors have used the concept of junction rods to prevent back reflection. A maximum contrast raio of 3.74 dB was obtained for the full adder with a rapid response period of 1.06 ps [22].

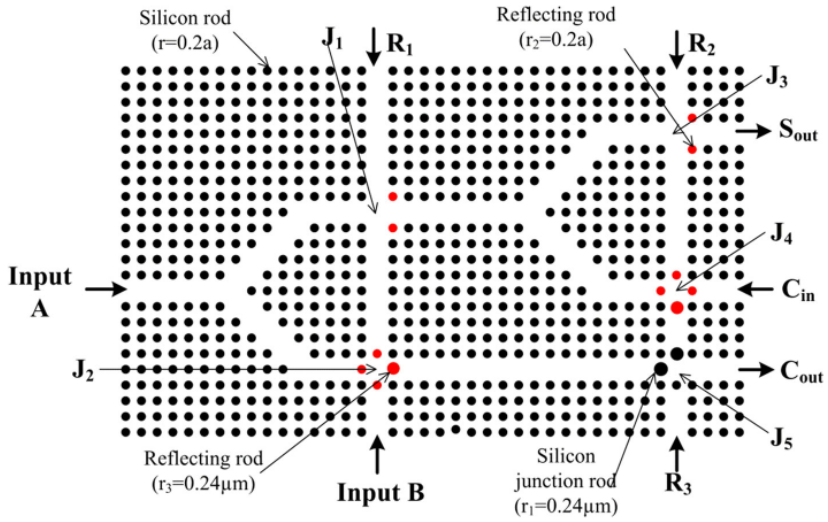


Figure 1.26: Full adder arrangement [22].

Tunable Bifunctional XOR and XNOR Gates

In 2020 Ibrahim *et al.* proposed a structure that can act as XOR and XNOR simultaneously. With a high contrast ration of 26 dB, the structure is found to be best fit for recent fabrication process. The gates offer small operating power, reduced size, and tunability [23].

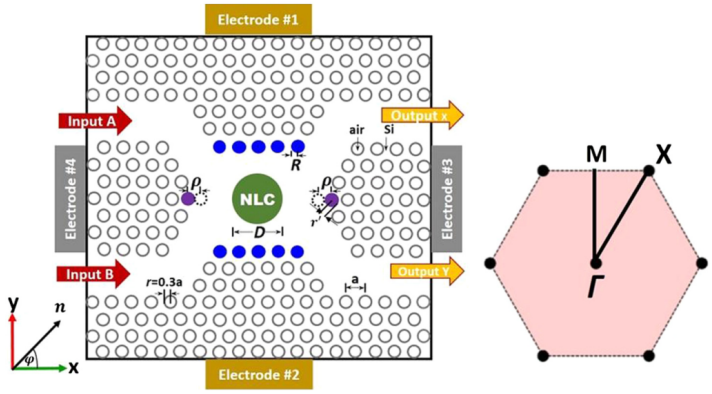


Figure 1.27: Proposed XOR/XNOR gate [23].

AOX Logic Gates using PhCs

Rao et al. came up with a PhCW-based structure that uses beam interference method to implement AND, OR, and XOR gates. The strucutre has air substrate with Si rods embedded within it. The contrast ratio for the respective gates are presented in Table 1.3 [24].

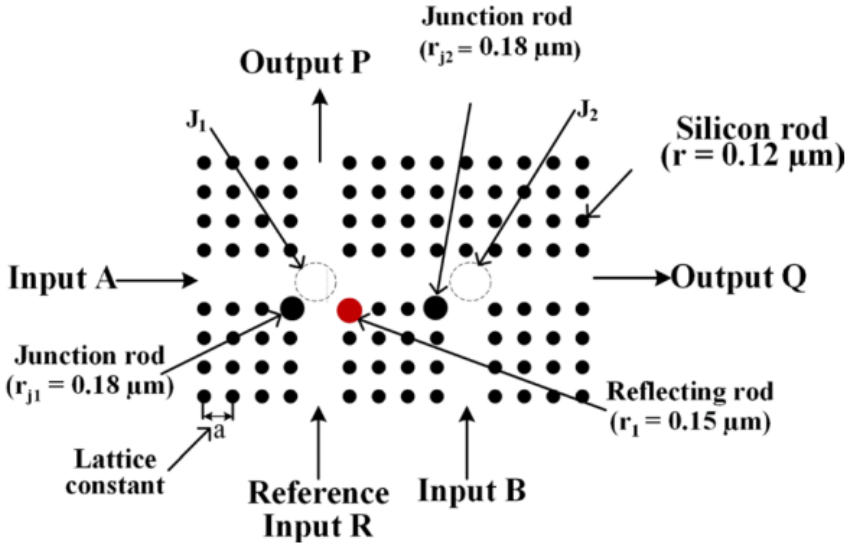


Figure 1.28: Schematic of the AOX gate [24].

Table 1.3: Contrast Ratio for AOX Gates

Gate	Contrast Ratio
AND	33.05 dB
OR	10.50 dB
XOR	8.29 dB

1.7 Thesis Objective

The prime objectives behind this works are;

- Proposing an on-chip all-optical logic gate using photonic crystal waveguide configuration implying beam interference method.
- Optimizing the structural parameters to obtain enhanced performance such as high contrast ratio, high extinction, and high transmission ratio.
- Developing such structure that minimizes the propagation loss.

1.8 Thesis Outline

Chapter 1 gives a brief introduction to the development of photonic crystals from the advent of nano-photonics. Photonic crystal waveguides and their working principles in realizing optical logic gates have been discussed elaborately. A comprehensive literature review on different optical logic gate technologies is presented. The chapter concludes with the thesis layout.

Chapter 2 defines different performance metrics related to optical gates. Transmission Ratio, Contrast Ratio, and Extinction Ratio have been discussed in detail.

Chapter 3 illustrates the detailed working principle of photonic crystal waveguide based optical logic gates. This dedicated section includes the primary introduction to interference mechanism and establishes the conditions for interference in photonic crystal waveguides.

Chapter 4 includes the the structural layout and parametes of the proposed sensor. Additionally this chapter presents the optimization process summarizes the optimized structural parameters with results.

Chapter 5 presents all the simulation results for the optical AND and OR gates. All the logic conditions along with performance analysis results have been included. Moreover, the truth tables for the optical gates have been derived.

Chapter 6 concludes the whole work by summarizing and comparing the proposed model with the recent research works. A sequence of steps for future works have been mentioned.

Chapter 2

Performance Metrics of Optical Logic Gates

The performance metrics are indicators of a structure's performance. This section defines three quality parameters for measuring the performance of optical logic gates (e.g., Transmission Ratio, Contrast Ratio, and Extinction Ratio). For all-optical logic gates, careful optimization of these parameters is critical. In the following sections, advancements in these features are carefully considered for a variety of applications of optical gates technology.

2.1 Transmission Ratio (TR)

The transmission ratio is calculated by dividing the average power at the output port by the average power at the input port. It's a widely utilized parameter in a variety of other fields. It is a measure of a system's efficiency. The expression for transmission ratio can be expressed as,

$$TR = \frac{P_{out}}{P_{in}}, \tag{2.1}$$

where, P_{out} is the average output output power, and P_{in} is the average input power. It is expressed as a percentage. The bigger the value, the more efficient the system is. However, it can be higher or lower for logic gates. It should be as low as feasible for the logic state '0' because there should be no transmission in this situation in an ideal world. The optimum scenario for logic state '1' is 100% transmission, thus the ratio should be as high as possible. For this condition, the transmission ratio is also an indication of transmission loss. To have minimal losses, this parameter needs to be maximized.

2.2 Contrast Ratio (CR)

Contrast ratio is the most dominant parameter for measuring the performance of logic gates. It is the ratio of power at the output port at high power or logic state '1' to low

power or logic state ‘0’. The expression for contrast ratio can be expressed as,

$$CR = 10 \log \frac{P_{1(avg)}}{P_{0(avg)}}. \tag{2.2}$$

CR is always measured in dB [54]. Any type of logic gate would benefit from having a higher contrast ratio. It is critical in the optical realm to have adequate contrast or variation between two logic states. This makes the system more resistant to human error and misinterpretation. When two states overlap, it becomes extremely difficult to tell the difference between high and low power, limiting the device’s performance. Hence, maximizing the contrast ratio is the highest priority when optimizing for these devices.

2.3 Extinction Ratio (ER)

Extinction ratio is closely related to the contrast ratio and it is also an indication of the separation between two logic states. It is defined as the ratio of minimum power at the output port for logic state ‘1’ to the maximum power at the output port for logic state ‘0’. The expression for extinction ratio can be expressed as,

$$ER = 10 \log \frac{P_{1(min)}}{P_{0(max)}}. \tag{2.3}$$

where, $P_{1(min)}$ is the minimum value for output intensity of logic state ‘1’, and $P_{0(max)}$ is the maximum value for output intensity of logic state ‘0’. It is also measured in dB [55].

The extinction ratio is always less than the contrast ratio since the lowest separation between the two states is used in this situation, whereas the concern for contrast ratio was the average separation. The extinction ratio can be thought of as the worst-case scenario for any logic gate. It is calculated to measure the risk factor and determine the smallest gap between two logic states. Ideally, if the contrast ratio is high, extinction ratio is also high. So, the optimization of both parameters goes hand in hand.

Chapter 3

Beam Interference Principle

In this work, the PhC-based optical logic gates have been implemented using the beam interference principle. Interference is a phenomenon that occurs when two waves collide while traveling across the same medium. This interaction between the waves is governed by the principle of superposition [56]. And when two waves interact, the principle of superposition says that the two waves merge by summing their displacements at every point of space and time, resulting in a wave with a larger, lower, or equal amplitude. This is analogous to when a little rock creates a ripple in the surface of a pond and it collides with another ripple pattern created by a second rock. When two wave crests overlap with each other, the resultant wave is equal to the sum of two individual waves. Alternately, a wave trough and wave crest coming together will cancel each other out. The linear wave equation can be used to understand the superposition principle. The linear wave equation for a transverse wave on a string can be expressed as [57],

$$\frac{\partial^2 y(x,t)}{\partial x^2} = \frac{1}{\nu^2}\frac{\partial^2 y(x,t)}{\partial t^2}. \tag{3.1}$$

For any wave function $y(x,t) = y(x \pm \nu t)$, with a linear function argument, $(x \pm \nu t)$ is a solution for the linear wave equation and also a linear wave function. And if wave functions $y_1(x,t)$ and $y_2(x,t)$ are solutions for the linear wave equation then the sum of the two functions $y_1(x,t)+y_2(x,t)$ is also a solution. A light wave can be characterized by its frequency, amplitude, and phase. These characteristics, among others, influence the interference pattern formed by two waves. The equation for interference between two monochromatic beams can be expressed as [58],

$$I(x,y) = I_1 + I_2 + 2\sqrt{I_1 I_2}\cos(\phi_1 - \phi_2), \tag{3.2}$$

$$I(x,y) = A_1^2 + A_1^2 + 2A_1 A_2 \cos(\phi_1 - \phi_2), \tag{3.3}$$

where, I denotes the irradiance, defined as the square of electric field amplitude, A,

$$I = A^2, \tag{3.4}$$

ϕ is the phase of the waves in radian, which is,

$$0 \leq \phi \leq 2\pi, \tag{3.5}$$

and $\phi_1 - \phi_2 = \Delta\phi$ is the phase difference between two beams.

Depending on the interference pattern of the two beams, there can be constructive and destructive interference.

3.1 Constructive Interference

This is a form of interference that happens anywhere along with the medium where the two interfering waves have the same displacement. If both waves have an upward displacement, the medium will have an upward displacement as the sum of the two interfering pulses' displacement. At every point where the two interfering waves are shifted upward, constructive interference is detected. It is also observed when both interfering waves are displaced downward [25]. This is shown in Fig.3.1 and in both cases, the superposition wave reaches a maximum height which is the sum of interfering waves' amplitudes.

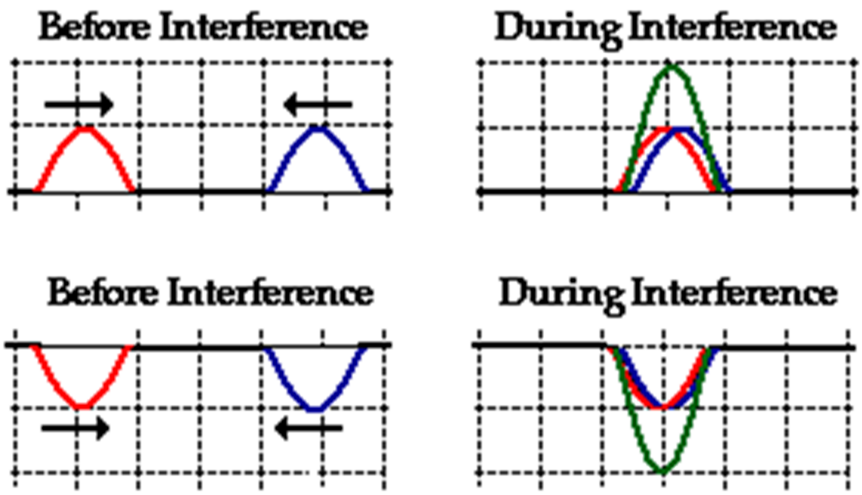


Figure 3.1: Constructive interference of upward and downward displacement [25].

3.2 Destructive Interference

This is a form of interference that occurs anywhere along with the medium where the two interfering waves have opposing displacements. It is exhibited in Fig.3.2 that when the crest of one wave collides with the trough of another, the waves partially cancel each other out. The waves will cancel each other totally if they are symmetrical. This can occur in two ways. Either by having a phase shift of $180°$ or a path difference of half-wavelength, $\frac{\lambda}{2}$.

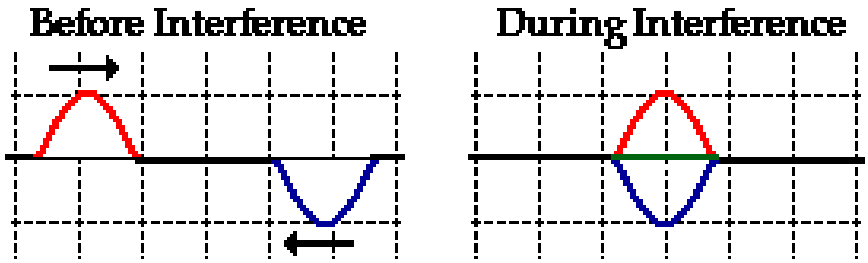


Figure 3.2: Destructive interference of two symmetrical waves [25].

3.3 Conditions for Interference

Constructive or destructive interference takes place inside the waveguide based on the phase angle and path covered by an incident light signal. The relation between phase difference and path difference can be expressed as,

$$\Delta\phi = \frac{2\pi}{\lambda} \cdot \Delta x, \tag{3.6}$$

where, $\Delta\phi$ is the phase difference and Δx denotes the path difference.

For constructive interference, according to the superposition principle, the phase difference should be $2k\pi$, where k is a non-negative integer. Using this condition in Eq. 3.6 we get,

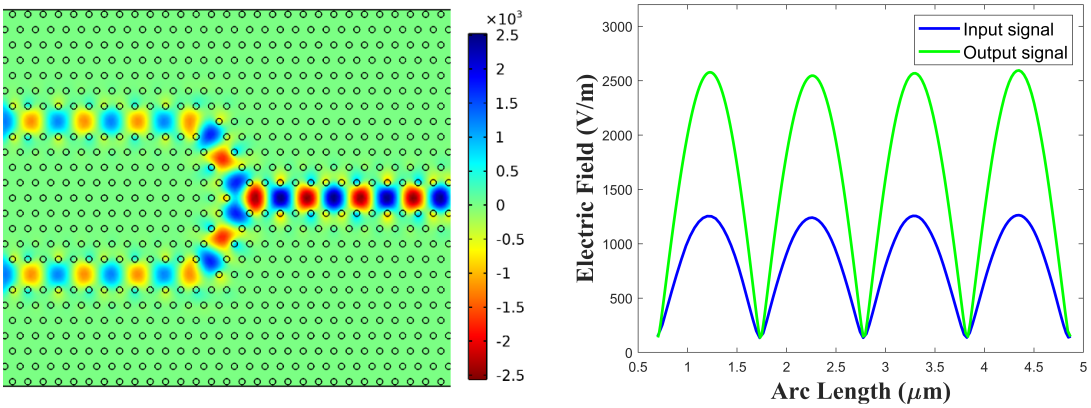
$$\Delta x = \frac{\lambda}{2\pi} \cdot \Delta\phi = \frac{\lambda}{2\pi} \cdot \pi k = \lambda k \tag{3.7}$$

Now, as previously discussed, the lattice constant, a is comparable to the wavelength of traveling light, λ. More precisely, the wavelength should be in the range of twice the lattice constant otherwise the light starts leaking as shown in Fig.1.17. So, the path difference for constructive interference in terms of the lattice constant is,

$$\Delta x = 2ka \tag{3.8}$$

When a constructive interference takes place, the signal is strengthened and propagated to the output side. We refer to this as logic state '1' or high power. And when

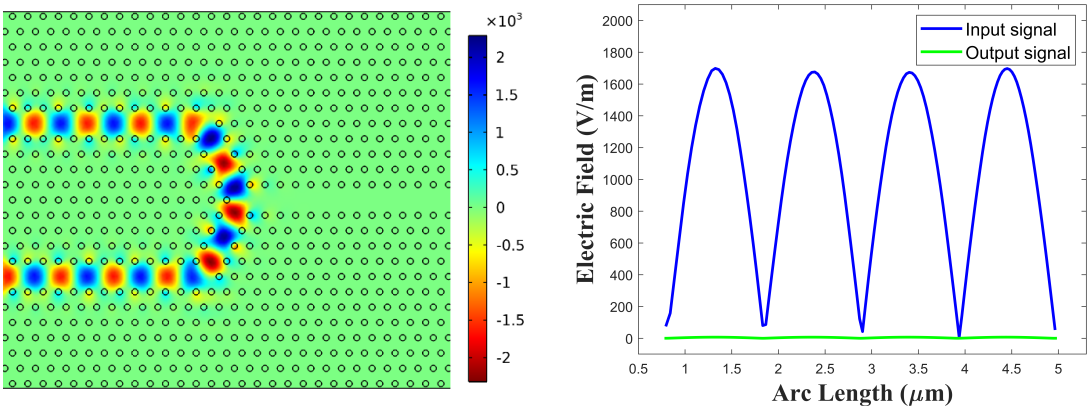
a destructive interference occurs, the two signals cancel each other out. So, no signal is propagated to the output port. We refer to this as logic state '0' or low power. We demonstrate this phenomenon in Fig.3.3 and Fig.3.4 by simulating a photonic crystal structure with a periodic lattice of dielectric rods and line defects. We input two signals with the same polarization and manipulate the phase difference between the signals to recreate a constructive or destructive interference.



(a) **(b)**

Figure 3.3: (a) Constructive interference of two signals, (b) input signal Vs. output signal for constructive interference.

As we can see in Fig.3.3(a) and Fig.3.3(b) for the constructive case, the output signal becomes more prominent than the input signal as the amplitude of the two signals is getting summed up. This leads to high power or logic state '1' on the output side.



(a) **(b)**

Figure 3.4: (a) Destructive interference of two signals, (b) input signal Vs. output signal for constructive interference.

And from Fig.3.4(a) and Fig.3.4(b), we can see for the destructive case, the output signal becomes almost zero as the amplitude of two signals are canceling each other. This leads to low or approximately zero power or logic state '0' on the output side.

Finally, as a summary, we can tabulate all the conditions required for constructive and destructive interference in terms of phase difference and path difference according to the superposition principle. The conditions are tabulated in Table 3.1

Table 3.1: Conditions for Constructive and Destructive Interference

Type	Phase difference ($\Delta\phi$)	Path difference (Δx)	Output power stage
Constructive	$2k\pi$ (where $k = 0, 1, 2, ...$)	$2ka$ (where $k = 0, 1, 2, ...$)	High power (logic state **'1'**)
Destructive	$(2k + 1)\pi$ (where $k = 0, 1, 2, ...$)	$2ka$ (where $k = 0, 1, 2, ...$)	Low power (logic state **'0'**)

3.4 Interference in Photonic Crystal Waveguides

Analyzing the conditions aummarized in Table 3.1, there can be primarily three methods to achieve desired logic operations in PhCWs discussed below;

3.4.1 Path Difference between Two Input Signals

Constructive or destructive interference can be created by introducing a $2ka$ and $(2k + 1)a$ amount of path difference between the two signals, respectively, as given in Table 3.1. Fu *et al.* [18] demonstrated this using silicon photonic crystal all-optical logic gates. Fig.4.10 exhibits the steady-state electric field distributions of the gates.

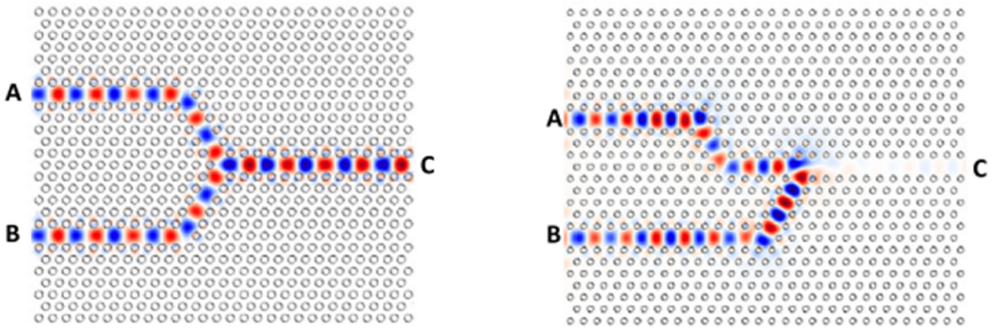


Figure 3.5: (a) Constructive interference, (b) destructive interference of input signals [18].

In Fig.3.5(a), the distance from A to junction and B to the junction is the same. This results in zero path difference. Hence, we get a constructive interference or logic state '1'. On the other hand, in Fig.3.5(b), the distance from A to the junction is one lattice constant, a, greater than the distance from B to the junction. As the path difference between two signals is an odd integer multiple of lattice constant or $(2k + 1)a$, this leads to destructive interference. The disadvantage of this method is that different

internal structural modifications are needed to create a different path difference each time.

3.4.2 Phase Difference between Two Input Signals

Constructive or destructive interference can be created by introducing a $2k\pi$ and $(2k+1)\pi$ amount of phase difference between the two signals, respectively, as given in Table 4.1. This is already demonstrated in Fig.3.3 and Fig.3.4, where one input signal was phase shifted by π or 180° to create a destructive interference while having no path difference between the signals. This approach has the disadvantage of requiring external phase shifters to change the input signal.

3.4.3 Usage of Extra Reference signal

This method requires the same conditions and principles as the two previous methods. But this time, they are applied to an extra reference signal. Rani *et al.* [26] demonstrated this when they proposed the design of all-optical logic gates in a two-dimensional triangular lattice composed of air holes in silicon.

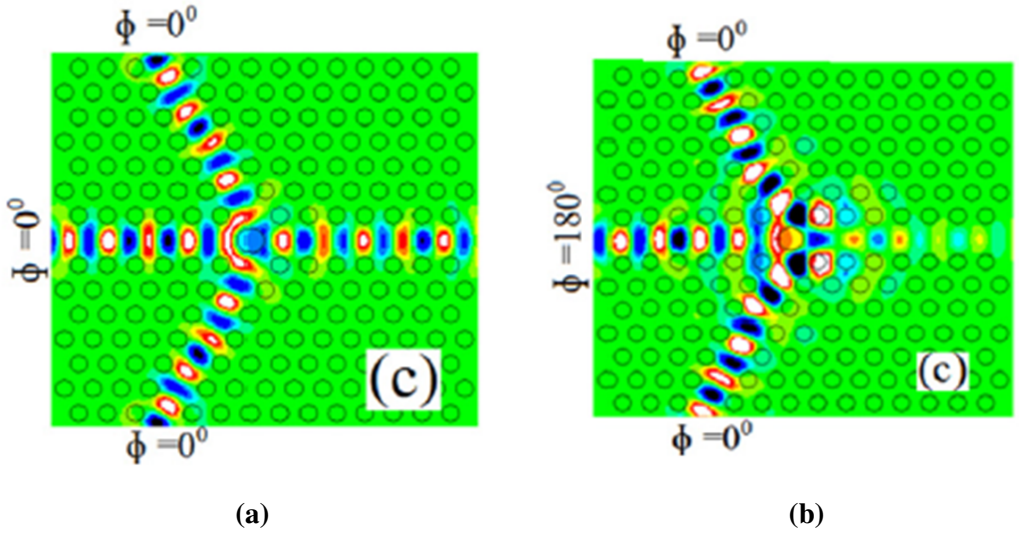


Figure 3.6: Using reference signal to vary the mode of operation. (a) Constructive interference with 0° phase-shifted reference signal, (b) destructive interference with 180° phase-shifted reference signal [26].

In Fig.3.6, two different modes are displayed just by phase-shifting the reference signal, keeping the input signals untouched. All the input signals are traveling the same path distance. This method has the advantage of always keeping the input signals preserved. Therefore, only the reference signal can be manipulated to get all the desired responses. For this reason, in our work, this technique is preferred over the others.

Chapter 4

Design, Optimization, and Performance Analysis of the Proposed Logic Gates

This section illustrates the design and optimization of the proposed logic gate structure. The proposed all-optical logic gates are designed to meet the high contrast ratio requirements for diverse photonic computing applications.

4.1 Structural Layout and Design Parameters

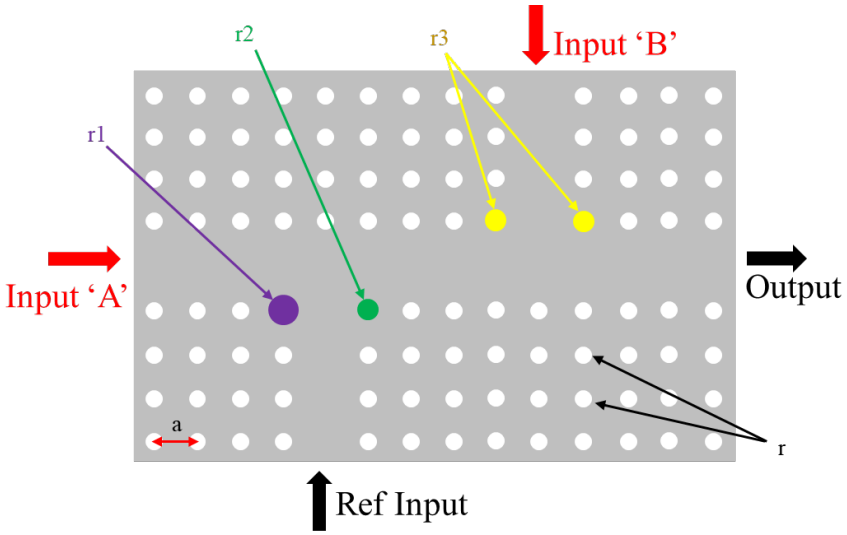


Figure 4.1: Two-dimensional (2D) model of the proposed logic gate.

The 2D structural layout of the proposed all-optical logic gate along with its input-output definition is shown in Fig.4.1. The gate consists of one horizontal waveguide and two vertical waveguides. And an array of cylindrical silicon rods in the air serves as the background for these photonic crystal waveguides. The silver color in Fig.4.1 denotes air and the white color is used to indicate the silicon rods.

Both AND and OR gate is implemented using only one structure in this work. The structural parameters of the design have been tabulated in Table 4.1. The optical

logic gates are operated at a resonant wavelength of 1550 nm which is in the optical communication range. Following the principle of superposition, the lattice constant is set to be in the range of half-wavelength, 600 nm. The lattice constant, a is defined as the distance between two adjacent silicon rods. The value for the radius of the silicon rods, r is set to be 120 nm. The colorful rods depicted in Fig.4.1 are differentiated as junction rods and they are used to reduce the unwanted back reflections into the input ports and also to get better output levels which in turn will improve the contrast ratio. Three different dimensions of junction rods have been found after optimization. They are r_1, r_2, and r_3 having a junction rod radius of 210 nm, 150 nm, and 150 nm, respectively.

Table 4.1: Structural Parameters for the Proposed Logic Gate

Parameter	Symbol	Values (nm)
Lattice constant	a	600
Radius of cylindrical silicon rods	r	120
Radius of junction rod 1	r_1	210
Radius of junction rod 2	r_2	150
Radius of junction rod 3	r_3	150

An extra reference input is used in addition to the two input signals. This reference input will always remain active, that is, it will always output signal of logic '1'. But, under different conditions, different phase shifts will be used for the reference input to get the desired output.

4.2 Parametric Optimization

As previously stated, having a high contrast ratio and minimal power loss are critical in all-optical logic gates. Optimization of structural parameters such as rod form and radius, cavity shape, lattice constant, and refractive index of rods can lead to better control of loss features and an increase in contrast ratio. For the purpose of this study, the radius of the junction rods and refractive index of the dielectric rods are optimized with these goals in mind.

Table 4.1 illustrates the final optimized values of the structural parameters. The values of three junction radius (r_1, r_2, and r_3) and refractive index, η of silicon rods have been optimized and fine-tuned to maximize contrast ratio and minimize propagation loss. The initial values of all junction rods are set to be equal to the radius of non-junction rods, r. And they also have been optimized in relation to the normalized value $(\frac{r_j}{r})$. The initial refractive index, η of silicon rods was chosen as 3.48. From

these initial conditions and values, the contrast ratio and transmission ratio were derived to be 21.89 dB and 42.18% respectively.

4.2.1 Junction Rod 1 Radius

The junction rod radius, r_1 has been first varied from 90 nm to 210 nm with a step-size of 15 nm while keeping other parameters fixed. It is evident from Fig.4.2(a) that the maximum contrast ratio is found at $(1.75 \cdot r)$ or 210 nm. The CR keeps pretty steady at first but starts fluctuating rapidly at a higher radius finally reaching its peak, 24.97 dB at 210 nm. Fig.4.2(b) exhibits the transmission ratio over the variation of radius. At $r_1 = 210$ nm, the transmission ratio is also found to be at its maximum, 45.4%. As a result, r_1 is chosen to be 210 nm.

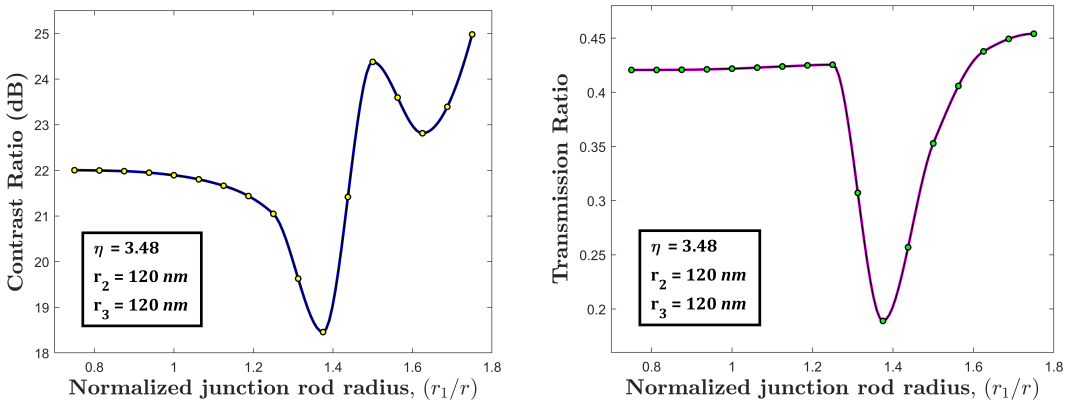


Figure 4.2: (a) Contrast ratio, (b) transmission ratio for the variation of r_1.

4.2.2 Junction Rod 2 Radius

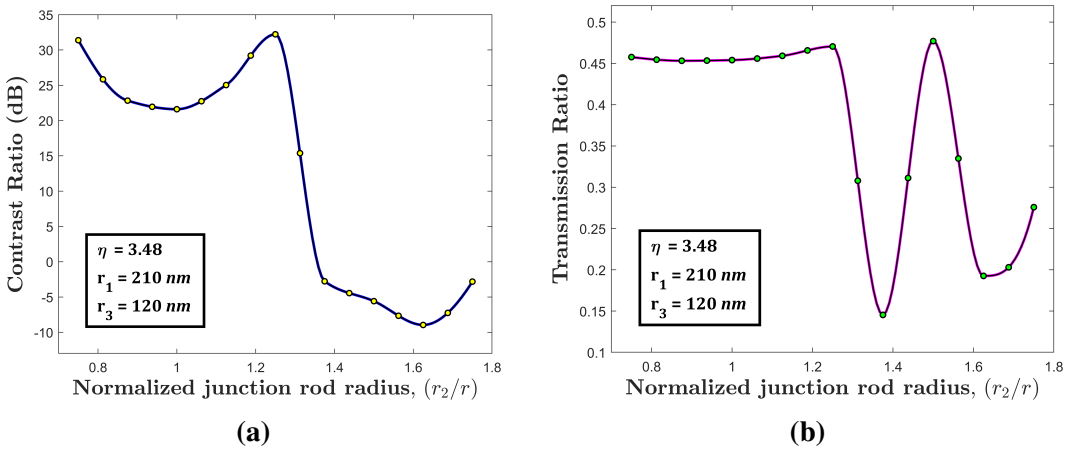


Figure 4.3: (a) Contrast ratio, (b) transmission ratio for the variation of r_2.

The junction rod radius, r_2 is optimized next. It is varied from 90 nm to 210 nm, same as r_1. From Fig.4.3(a), it can be clearly seen that, the curve peaks around $(1.25{\cdot}r)$ or 150 nm and starts dropping rapidly, even to the negative values, as r_2 increases. And in Fig.4.3(b), where the maximum transmission ratio is also observed at the same spot, this value of r_2 is shown to be ideal. This demonstrates that in this structure, r_2 is an important tuning parameter. So, the optimum value of r_2 is updated to 150 nm. The updated contrast ratio and transmission ratio is 31 dB and 47%

4.2.3 Junction Rod 3 Radius

After r_2, the radius of two junction rods at the right vertical waveguide, r_3 is varied. And the variation range is exactly like r_1 and r_2. During the optimization of this parameter, an interesting phenomenon is witnessed that is both the graph of contrast ratio and the graph of transmission ratio looks almost identical. In other words, the relation of these two quality parameters with r_3 is quite similar. This is an interesting finding since it suggests that there may be an underlying relationship between contrast ratio and transmission ratio that might be investigated further in the future. It can be observed in Figure 4.4 that the contrast ratio peaks at $(1.5 \cdot r)$ or 180 nm while the maximum transmission ratio is recorded at $(1.375 \cdot r)$ or 165 nm. Even though these could be considered optimized values in general, neither was ideal for satisfactory logic operation. For both of these values, undesirable output was obtained for some specific input combinations for both gates due to over absorption of input signals. For both contrast ratio and transmission ratio, the next maximum value is obtained at $(1.25 \cdot r)$ or 150 nm which is 32.68 dB and 49%, respectively. Thus, the optimized value for r_3 is 150 nm.

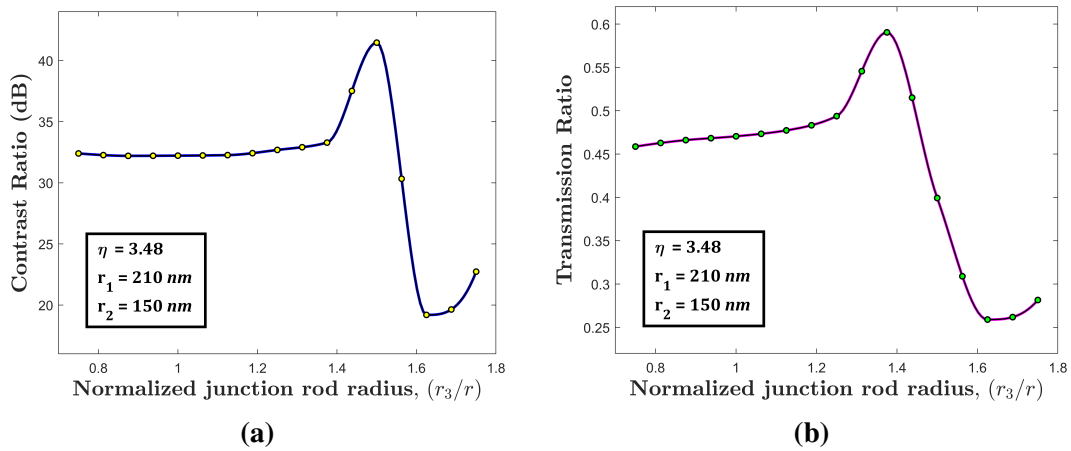
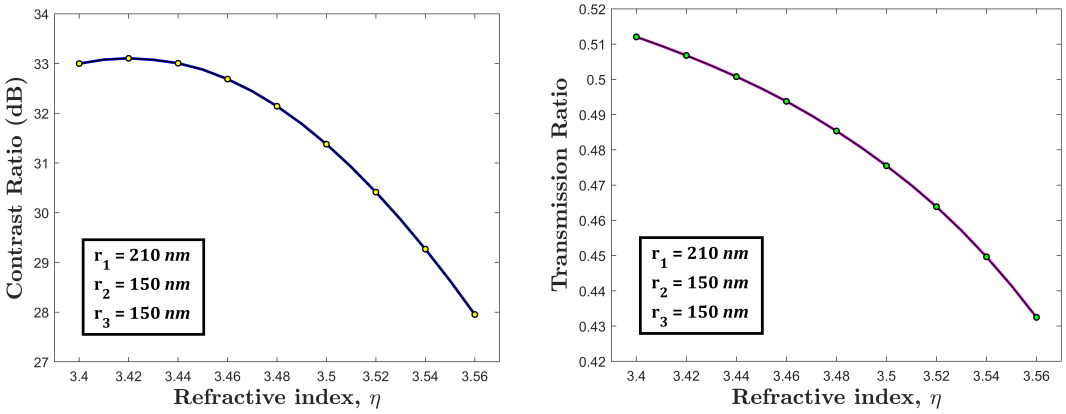


Figure 4.4: (a) Contrast ratio, (b) transmission ratio for the variation of r_3.

4.2.4 Variation of RI of Silicon Rods

The refractive index of silicon rods, η is then varied between 3.4 and 3.56 with a step-size of 0.02. It is observed from Fig.4.5(a) and Fig.4.5(b) that both the contrast ratio and transmission ratio start going down as refractive index increases after 3.44. Therefore, the optimized refractive index is 3.44. After this optimization, the new contrast ratio and transmission ratio is 33 dB and 50%.



(a) **(b)**

Figure 4.5: (a) Contrast ratio, (b) transmission ratio for the variation of RI, η.

4.2.5 Optimization Results

The entire design parameter optimization result is summarized in Table 4.2. The table shows that tweaking all parameters resulted in a rise of both quality parameters, but the change of r_2 and then r_1 provided the most substantial improvement. After the optimization procedure, the contrast ratio and transmission ratio rose by 50.7% and 18.5%, respectively.

Table 4.2: Structural Parameters and Performance Results for the Proposed Logic Gate

Parameter	Initial Value	Optimized Value	Performance before Optimization	Performance after Optimization
r_1	120 nm	210 nm	CR= 21.89 dB TR= 42.18%	CR= 24.97 dB TR= 45.40%
r_2	120 nm	150.00 nm	CR= 24.97 dB TR= 45.40%	CR= 31.00 dB TR= 47.00%
r_3	120 nm	150 nm	CR= 31.00 dB TR= 47.00%	CR= 32.68 dB TR= 49.00%
η	3.48	3.44	CR= 32.68 dB TR= 47.00%	CR= 33.00 dB TR= 50.00%

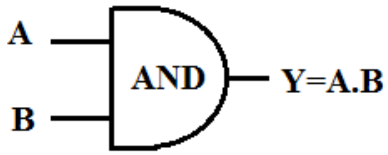
Chapter 5

Simulation Results

The FEM approach is used to validate the structural simulation. The suggested design's operation is tested utilizing various input combinations and the reference input signal. The beam interference effect is exploited for logic gate construction. This interference effect takes place within the waveguide based on the relative distance covered by input light signals and the beginning phase of delivered light beams. To obtain the required output, all possible input combinations are constructed and simulated.

5.1 All-optical AND Logic Gate

The AND gate represents multiplication. It is a logic gate with two or more inputs and a single output. AND gates use Boolean multiplication rules to operate. If any one of the inputs is low (logic state '0'), the output also becomes low. Only If all of the inputs become high (logic state '1'), the output will be high as well. The symbol and truth table of AND gate is given in Fig.5.1.



Inputs		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Figure 5.1: AND gate symbol and truth table [27].

5.1.1 Input Combination A=0, B=0

For the first combination for the AND gate, both of the inputs, A and B are set to be zero. But the reference input will be on with a phase shift of 0°. Although, here the phase shift is not of any importance because there is only one signal. As shown in Fig.5.2, for this case a low power or zero signal is received at the output port, which is the ideal case for this condition of AND gate. Again, the junction rods are being used to confine some light so that less amount of signal is propagated to the output side so that we get very little power output for Logic '0'. This in turn increases the contrast ratio for this design.

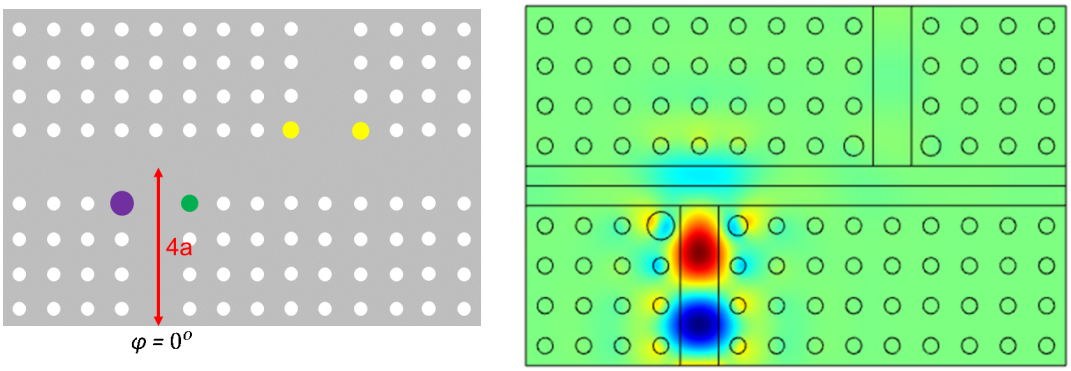


Figure 5.2: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=0 AND B=0.

5.1.2 Input Combination A=1, B=0

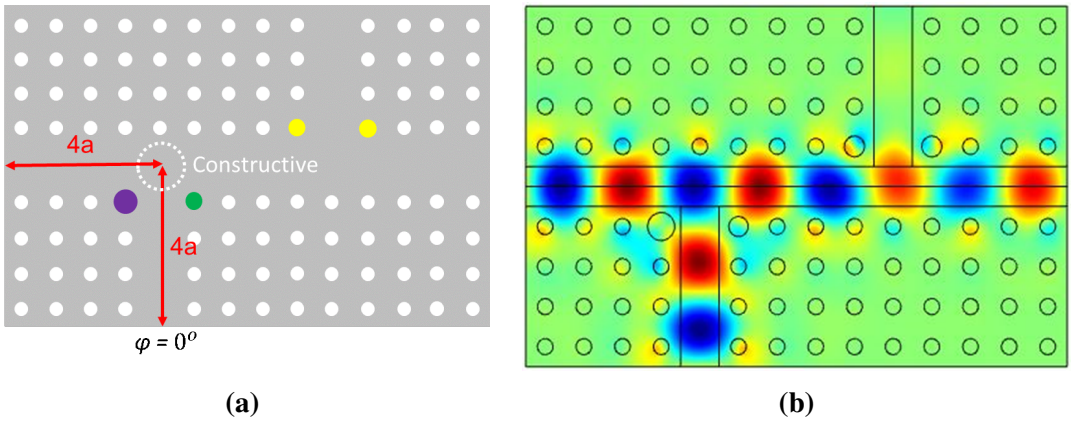


Figure 5.3: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=1 AND B=0.

The second combination is input A as '1' and Input B as '0'. Here, a 180° phase shift is introduced to the reference input. Here, both of the input covers the same

amount of distance $4a$. They would have a constructive interference if there was no phase shift. But due to the presence of a 180° phase shift, destructive interference in this region is observed in Fig.5.3 which is indicated by the black dotted circle. The phase shifts can also be observed from the electric field distribution. The red blobs are crests and the blue blobs are troughs. In input A, it is starting with a crest (red blob) and the reference input is starting with a trough (blue blob). So, they are indeed 180° phase shifted.

5.1.3 Input Combination A=0, B=1

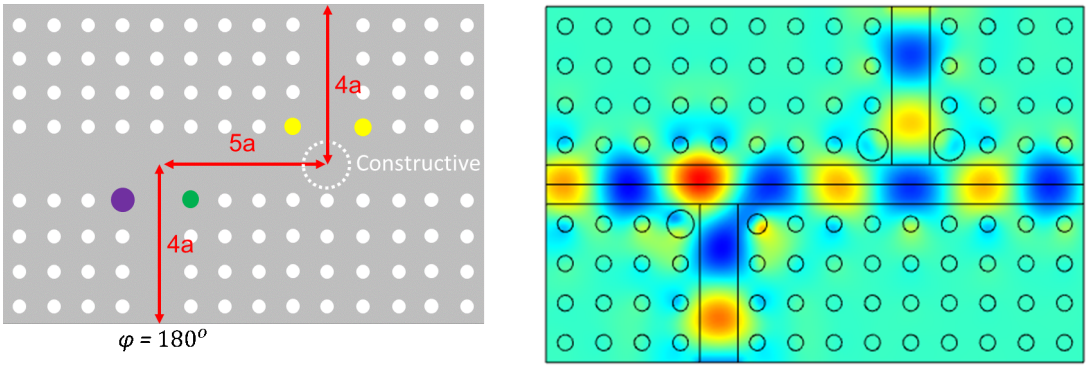
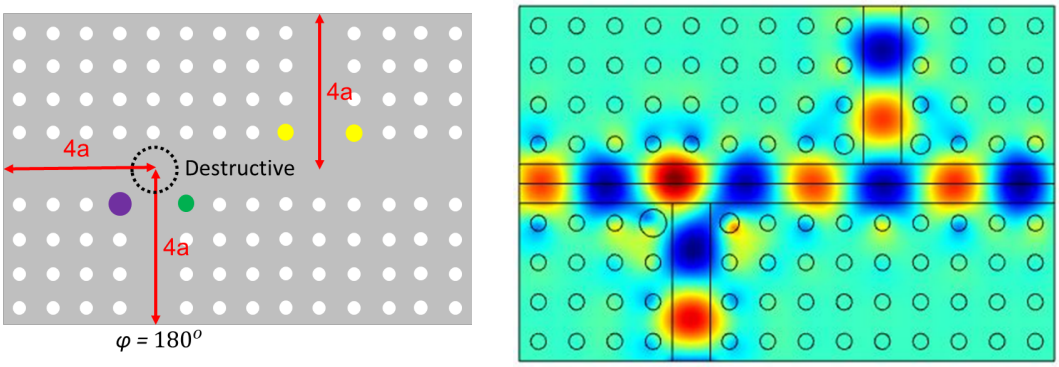


Figure 5.4: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=0 AND B=1.

The third condition is Input A as '0' and Input B as '1'. In the same way as before, here the common junction between the two active inputs is indicated by a dotted circle in Fig.5.4. The reference input is traveling a distance of $9a$, while Input B is traveling a distance of $4a$. As the path difference is an odd integer multiple of lattice constant or $2\pi k$, the two signals will spawn a destructive interference. That is why there is no signal present on the output side.

5.1.4 Input Combination A=1, B=1

And the last condition is both inputs having logic state '1'. Here, like before, the two inputs, input A and reference input cancel each other out due to destructive interference because of giving a 180° phase shift at the reference signal. That leaves the signal from input B to propagate uninterrupted to the output side in Fig.5.5. This results in high power or logic state '1'.



(a) **(b)**

Figure 5.5: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=1 AND B=1.

5.1.5 Obtained Truth Table and Transmission Ratio, TR

The transmission ratio for all combinations has been calculated using Eq.2.1 . The obtained truth table and transmission ratio after simulating all conditions along with the required phase shift in reference signal for the AND gate are given in Table 5.1.

Table 5.1: Obtained Truth Table and TR for AND gate

Input A ($\phi_A = 0°$)	**Input B** ($\phi_B = 0°$)	**Reference Input (R)**	**Reference Phase** (ϕ_R)	**Logic Output**	**TR**
0	0	1	0°	0	0.19427
1	0	1	180°	0	0.04736
0	1	1	0°	0	0.11879
1	1	1	180°	1	0.49376

5.1.6 Performance Analysis: CR and ER

In order to assess the performance of the gate, we have calculated two parameters, contrast ratio (CR) and extinction ratio (CR) defined in Eq.2.2 and Eq.2.3. Both of these parameters are representations of distinction between two logic states. The difference in output between logic '1' and logic '0' was evident in the electric field distributions in Fig.5.2 to Fig.5.5. Now, the waveguide signals for both logic states have also been plotted in Fig.5.6. where a huge difference between the amplitude of logic '1' and logic '0' is clearly evident.

The contrast ratio (CR) can be derived from the ratio of the mean value of output intensities for logic '1' and logic '0'. After analyzing the output power for both cases, the contrast ratio for this AND gate was found to be as high as 30.17 dB.

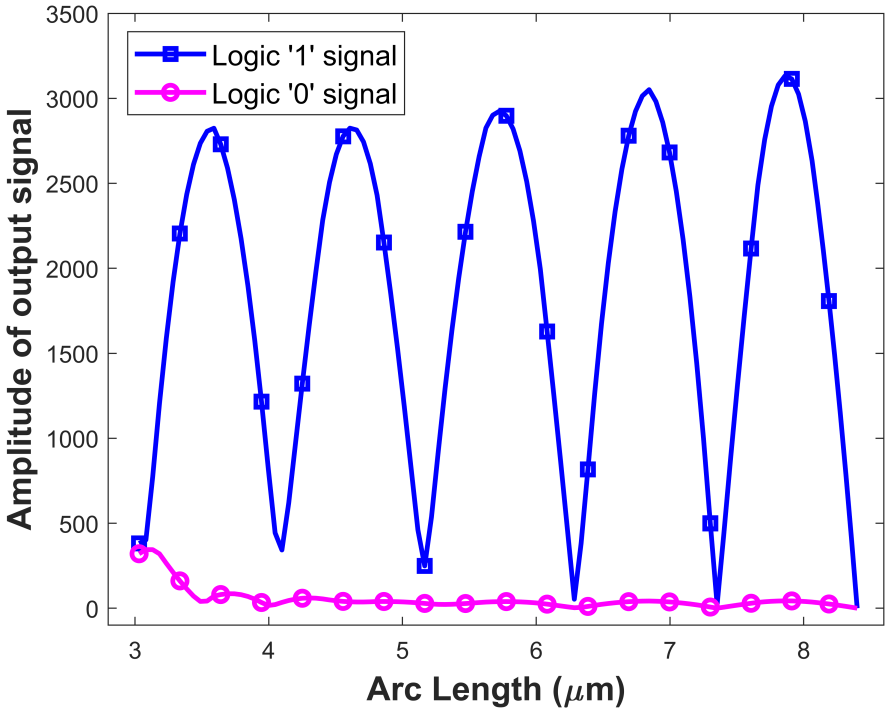
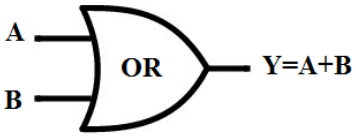


Figure 5.6: Line plot of waveguide signal for logic '1' and logic '0' (AND gate).

The extinction ratio (ER) can be derived from the ratio of minimum value of output intensity for logic state '1' and maximum value of output intensity for logic state '0'. And for this structure, after optimization, the maximum extinction ratio is found to be 25.21 dB.

5.2 All-optical OR Logic Gate

The OR gate represents addition. Like an AND gate, it can also have multiple numbers of input probes and a single output. OR gates use Boolean addition rules for their operation. The output only becomes low (logic state '0'), when both of the inputs are low. Otherwise, it generates a high (logic state '1') signal in all conditions. The symbol and truth table of AND gate is given in Fig.5.7.

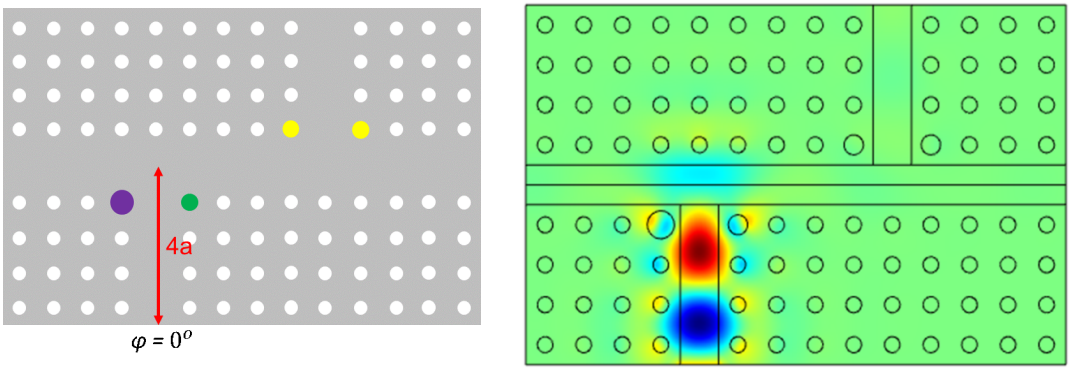


Inputs		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Figure 5.7: OR Gate symbol and Truth table [27].

5.2.1 Input Combination A=0, B=0

For the first combination for the OR gate, both of the inputs, A and B are set to be zero. But the reference input will be on with a phase shift of $0°$. For this condition, it is the same as the AND gate, as shown in Fig.5.8. A low power or zero signal is received at the output port. Again, because the junction rods are utilized to limit some light, less signal is transferred to the output side, resulting in very little power output for Logic '0'. This raises the contrast ratio for this design.

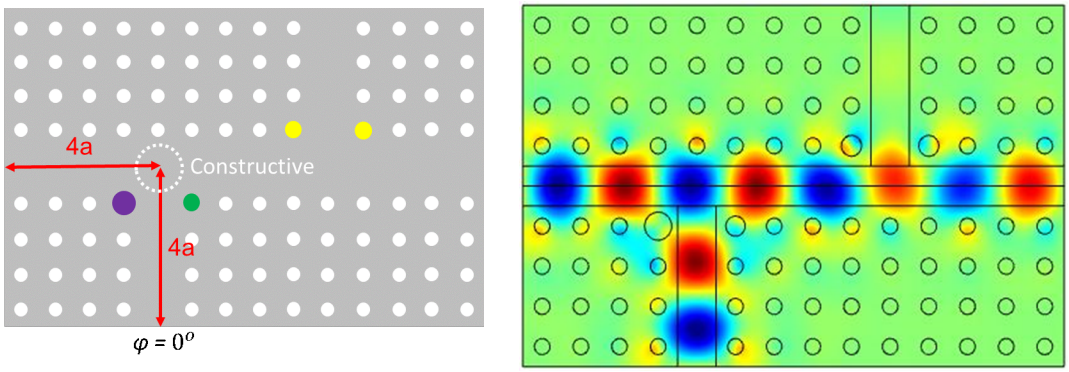


(a) **(b)**

Figure 5.8: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=0 OR B=0.

5.2.2 Input Combination A=1, B=0

The second combination is input A as '1' and Input B as '0'. Here, the input signals would have a constructive interference as no phase shift is introduced in the reference signal. This is indicated by the white dotted circle in Fig.5.9. The constructive interference generates a signal summing both individual signal amplitudes which leads to a high signal at the output side. This is the exact opposite scenario of the AND gate.



(a) **(b)**

Figure 5.9: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=1 OR B=0.

5.2.3 Input Combination A=0, B=1

For the third condition, Input A is set as low and Input B as high. And a $180°$ phase shift was introduced at the reference signal. The reference signal is traveling a distance of $9a$, and Input B is traveling a distance of $4a$. As the path difference is an odd integer multiple of lattice constant or $2\pi k$, a constructive interference is observed at the junction indicated by the white dotted circle, shown in Fig.5.10. So, an output of logic state '1' is found in this case.

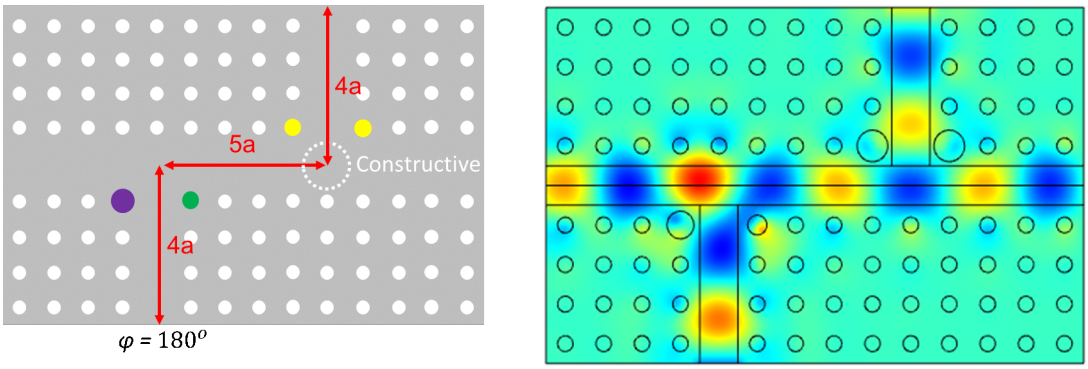


Figure 5.10: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=0 OR B=1.

5.2.4 Input Combination A=1, B=1

For the last condition, both Input A and Input B are active. This is the same as the AND gate described in section 5.1.4. A $180°$ phase shift is introduced at the reference signal again. This reference signal cancels out the signal from input A. Therefore, the signal from input B uninterruptedly becomes the output having logic state '1' in Fig.5.11.

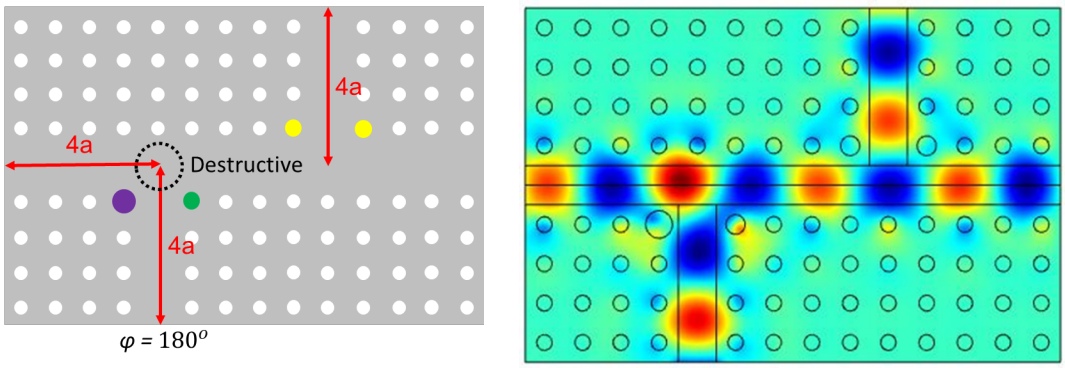


Figure 5.11: (a) Path covered by the input signals in terms of lattice constant, a, (b) corresponding electric field distribution for A=1 OR B=1.

5.2.5 Obtained Truth Table and Transmission Ration, TR

Table 5.2 shows the truth table and transmission ratio obtained after simulating all combinations, as well as the needed phase shift in the reference signal for the OR gate. A satisfactory and high transmission ratio has been found for the logic state '1' which led to an excellent contrast ratio for the OR gate.

Table 5.2: Obtained Truth Table and TR for OR gate

Input A ($\phi_A = 0°$)	**Input B** ($\phi_B = 0°$)	**Reference Input (R)**	**Reference Phase** (ϕ_R)	**Logic Output**	**TR**
0	0	1	0°	0	0.19427
1	0	1	0°	1	0.57691
0	1	1	180°	1	0.56221
1	1	1	180°	1	0.49376

5.2.6 Performance analysis: CR and ER

To evaluate the gate's performance, two parameters are established and evaluated: contrast ratio (CR) and extinction ratio (ER). A high value for both of these characteristics is desired for an all-optical logic gate. A higher value represents better performance, higher contrast between states, and less room for error and misinterpretation. Fig.5.12 shows the waveguide signals for both logic states, with a clear difference in amplitude between logic '1' and logic '0'.

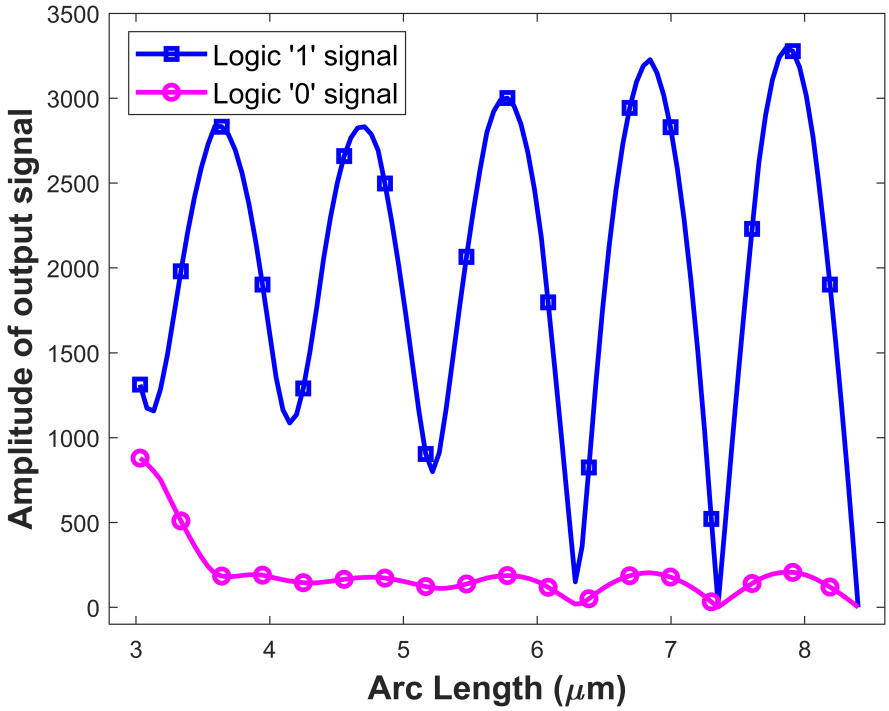


Figure 5.12: Line plot of waveguide signal for logic '1' and logic '0' (OR gate).

Now, after assessing the output power for both scenarios, the contrast ratio (CR) for the OR gate was determined to be extraordinarily high as 41.24 dB. The output extinction ratio (ER) for this structure was also revealed to be very high as 37.51 dB after optimization.

Chapter 6

Conclusion and Future Works

6.1 Conclusion

Optical electronics research has progressed significantly in recent decades. As technology advances, component sizes shrink, resulting in more sophisticated and larger integrated circuits. As a result, it necessitates specifically engineered components that are both tiny and efficient. One of the most important components for optical circuit integration is all-optical logic gates. These structures' modest size is a significant benefit that permits them to be used in optically integrated circuits. As a result of their low loss, excellent performance, and small size, photonic crystal waveguide-based optical logic gates are one of the most important optical components.

In this work, a highly efficient structure has been proposed for all-optical AND-OR gate. The proposed structure has two primary input ports and an additional reference input signal port. By varying the phase of the reference signal, desired output states have been obtained. The proposed structure is a photonic crystal waveguide having a dimension of $8.4 \times 5.4 \mu m^2$ with silicon nanorods in air background. Performance analysis shows that the optimized structural parameters give the Contrast ratio as 41.24 dB and 30.17 dB for OR and AND gate, respectively. Also, the extinction ratio has been found as 37.51 dB and 25.21 dB for OR and AND gate, respectively. These values have surpassed most of the recent works of all-optical logic gates. A comparative analysis of the previous works with the proposed model has been presented in Table 6.1.

The entire investigation has been carried out in COMSOL Multiphysics software implying Finite Element Method (FEM). The results have been verified by comparing them with the existing works.

The structure possesses a very simple geometry consisting of waveguides and holes only. Along with such simple geometry and high-performance metrics, the gate can

be highly preferred for on-chip applications. Furthermore, it is expected to help in realizing ultrahigh-speed all-optical signal processing and optical interconnection of networks.

Table 6.1: Comparative Analysis of the Recent All-optical Logic Gates

Ref.	Material	Dimension	RI	Contrast Ratio	Extinction Ratio
[17]	SiO_2	-	3.46	AND: 9.81 dB	-
[18]	Si	$24.62 \times 23.74\ \mu m^2$	-	AND-OR: 20 dB	-
[19]	Si	$5.28 \times 5.28\ \mu m^2$	3.5	AND: 6.017 dB	-
[20]	Si/SiO_2	$9.6 \times 7.7\ \mu m^2$	3.4/1.45	OR: 13 dB	-
[21]	Si	$8.88 \times 8.88\ \mu m^2$	3.46	AND: 19.46 dB	-
[22]	Si	$24 \times 14.4\ \mu m^2$	3.4	Full Adder: 8.74 dB	-
[24]	Si	$8.4 \times 5.4\ \mu m^2$	3.46	OR: 10.5 dB AND: 33.05 dB	-
[26]	Si	$5.28 \times 5.28\ \mu m^2$	3.5	OR: 5.42 dB AND: 8.76 dB	-
[55]	MRR	-	-	Fredkin GATE: 19.5 dB	Fredkin GATE: 12.2 dB
[59]	GaAs	$10 \times 13\ \mu m^2$	3.6	AND-XOR: 20.29 dB AND-OR: 16.70 dB	-
[60]	Si	$26.46 \times 21.6\ \mu m^2$	3.59	AND: 6 dB	-
[61]	Dielectric	$8.84 \times 8.84\ \mu m^2$	-	AND: 20.2 dB	-
[62]	MMI-based	-	-	OR: 22.3 dB	-
[63]	Dielectric/Air	$13.74 \times 8.46\ \mu m^2$	3.4	AND: 40 dB	-
[64]	Si	$14.4 \times 11.7\ \mu m^2$	3.4	AND: 6.79 dB	-
[65]	Si/SiO_2	$7.3 \times 7.7\ \mu m^2$	3.48/1.45	-	OR: 26.6 dB
[66]	Air/Ag	-	-	AND: 6 dB	-
[67]	Si	$12 \times 12\ \mu m^2$	3.46	AND: 10.96 dB	-
Proposed Work	**Si**	**$8.4 \times 5.4\ \mu m^2$**	**3.44**	**OR: 41.24 dB AND: 30.17 dB**	**OR: 37.51 dB AND: 25.21 dB**

6.2 Future Works

Though this work has offered a high performance there can be several sectors where improvements can be done. For future work, the design can be further improved, by the introduction of more junction rods and reflecting rods, and also through the tuning of different parameters, to obtain a greater contrast ratio and extinction ratio.

The design could also be improved or modified to obtain other logic operations, preferably the universal gates NAND and NOR. The universal optical logic gates could then be cascaded to obtain other logic operations, such as NAND gates cascaded to obtain AND operation. Cascading of logic operations other than universal gates could also be attempted. These designs could be further analyzed to investigate their effect on the performance parameters.

Another design could also be established where more than one reference signal is used which would grant more flexibility and control, and also allow a greater variety of logic operations in a single device. This could even facilitate the implementation of more complicated logic operations like a full adder, which are to be investigated.

However, we summarize the future works in the following sequence of steps that may lead to more advancement in the sector of photonic crystal based optical gates.

- Designing of other logic gates (XOR, XNOR, NOT)
- Design of universal gates (NAND, NOR)
- Further structural analysis and improvisations.
- Parametric optimization for enhanced contrast ratio. Machine learning can be used to increase accuracy in the optimization.
- Increasing practical field applicability

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