ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination — Summer Semester, A. Y. 2021-2022
Course No.: EEE 4483 — Time: 90 Minutes
Course Title: Digital Electronics and Pulse Techniques — Full Marks: 75

There are 3 (**three**) questions. Answer all 3 (**three**) questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets. Do not write on the question paper.

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1. a) Briefly describe the current hogging phenomenon in DCTL gates. **[5] (CO1, PO1)**

   b) In Fig. 1, gate G1 is a 3-input DTL NAND gate that has a fan-out equal to N (output of G1 is driving one of the inputs of N other similar 3-input NAND gates). If all the inputs of gate G1 is at logical HIGH state, determine the approximate value of N. [Here, $\beta = 50$ and $\sigma = 0.85$] **[10] (CO2, PO2)**

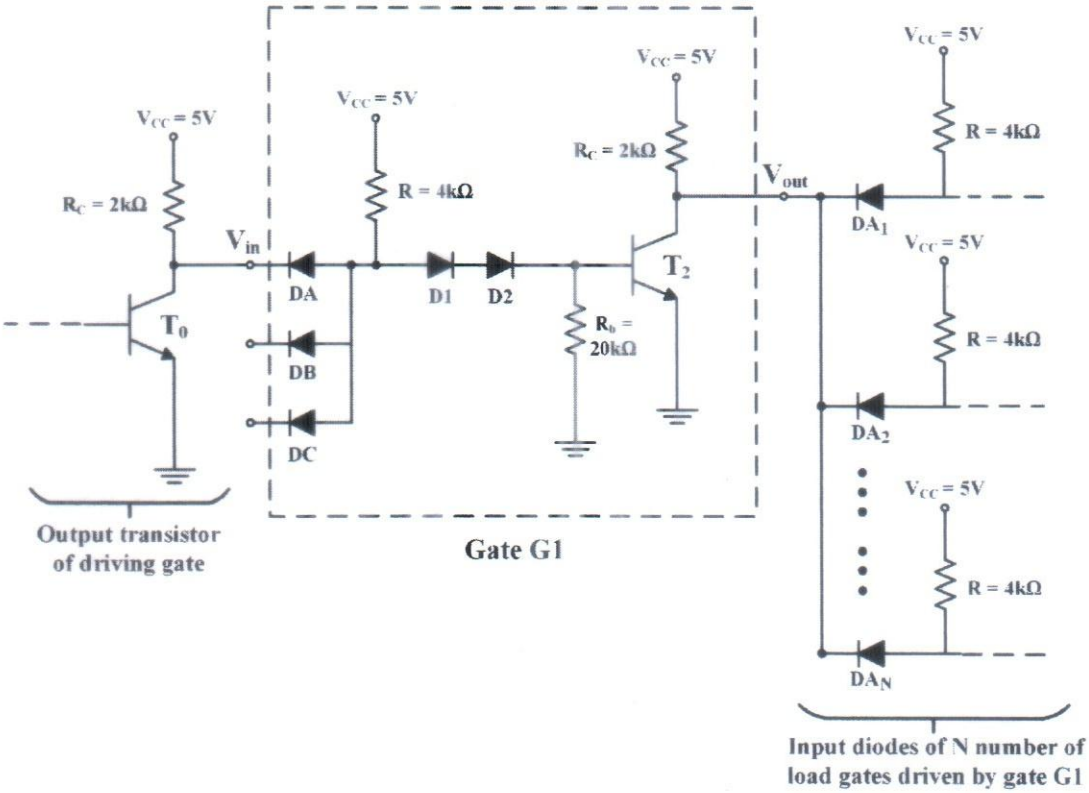

Fig. 1

   c) Sketch the circuit diagram of a 3-input TTL NAND gate with active pull-up. Specify the role of each transistor in the circuit and describe the overall operation of the circuit. **[10] (CO1, PO1)**

2. a) With proper reasoning, describe how TTL gates overcome the speed limitation of DTL gates. **[12] (CO1, PO1)**

b) Describe which type of logic circuit is presented in Fig. 2. For this circuit, sketch the input-output characteristics curve, determine the different input & output voltage levels and noise margins. [Here, $\beta = 50$, $\sigma = 0.85$, V_{BE}(Cut-in) = 0.65V, V_{BE}(Sat) = 0.7V, V_{CE}(Sat) = 0.2V] **[13] (CO2, PO2)**

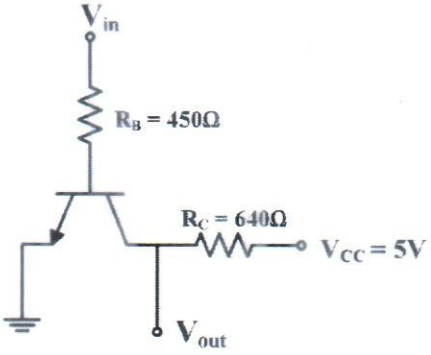

Fig. 2

3. a) Sketch the circuit diagram of the static CMOS design of the following circuit shown in Fig. 3. **[10] (CO2, PO2)**

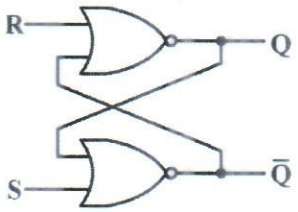

Fig. 3

b) Sketch the circuit diagram to implement the following Boolean expression using static CMOS logic. **[10] (CO2, PO2)**

$$F = \overline{(AB + \bar{C})D}$$

c) In Fig. 4, the I-V curves of nMOS and pMOS of a static CMOS inverter are shown for different values of input voltage (V_{in}) in a common coordinate set where the x-axis variable is the inverter output voltage (V_{out}) and y-axis variable is the current flowing from supply voltage towards the ground. With respect to Fig. 4, sketch the input (V_{in}) - output (V_{out}) characteristics curve of the CMOS inverter with proper labelling and highlight the different modes of operation of nMOS and pMOS along the curve. **[5] (CO2, PO2)**

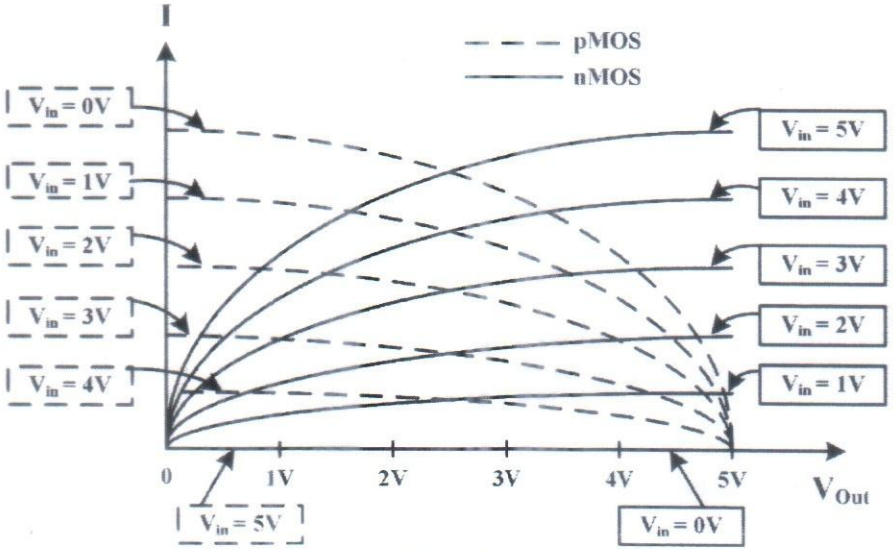

Fig. 4