ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination
Course No.: EEE 4483
Course Title: Digital Electronics and Pulse Techniques

Summer Semester, A. Y. 2021-2022
Time: 3 Hours
Full Marks: 150

There are **6 (six)** questions. Answer all **6 (six)** questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets.

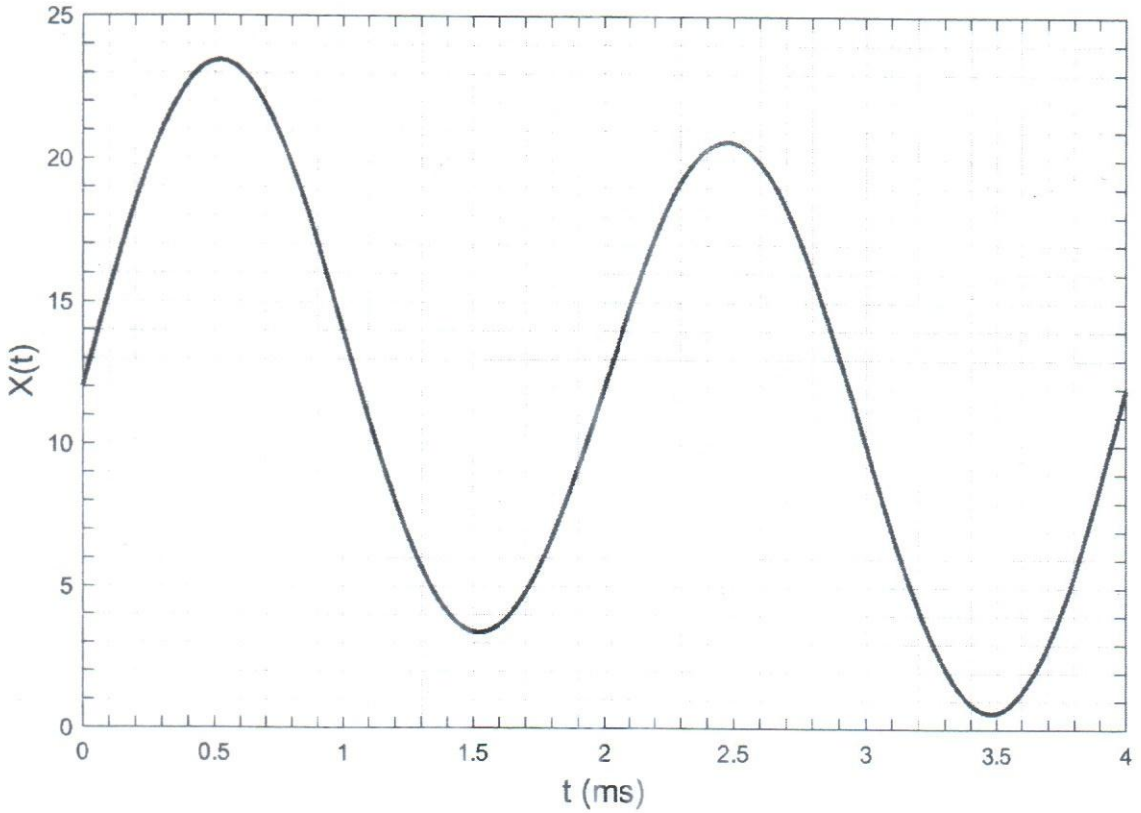

Fig. 1

1. a) In order to sample the signal X(t) shown in Fig. 1, an astable multivibrator circuit can be constructed using 555 timer to generate the necessary pulse wave. Consider the value of the capacitor in the RC timing circuit to be 4.7μF. **18 (CO2, PO2)**
   - (i) Sketch the circuit diagram of this astable multivibrator to generate a pulse wave of 50% duty cycle.
   - (ii) Derive the expression of the total time period.
   - (iii) Determine the values of the resistances in the RC timing circuit of this astable multivibrator to set the pulse wave frequency to 5kHz.
   - (iv) Sketch the waveshape of the generated pulse wave.

   b) Sketch the circuit diagram of a sample and hold circuit with an nMOS being the switching device to sample the signal X(t) shown in Fig. 1 using the pulse wave generated in Question 1(a). Briefly describe the working principle of the circuit and sketch the output waveform. **12 (CO2, PO2)**

2. a) The output signal of the sample and hold circuit of Question 1(b) is provided as one of the input to the comparators of a 4-bit Flash ADC with a reference voltage of 20V. Sketch the circuit diagram of this 4-bit Flash ADC. Describe the operating principle of this circuit. Find the equivalent digital form of the signal for the entire duration of 4ms. **14 (CO2, PO2)**

b) Sketch the circuit diagram of a 4-bit R-2R ladder DAC circuit and answer the following questions: **18 (CO2, PO2)**

(i) Derive the expression of the output voltage.

(ii) Describe what modification can be done to change the polarity of the output voltage.

(iii) Considering the modified circuit, determine the equivalent analog values for the digital data obtained in Question 2(a) and plot the wave shape of the reconstructed analog signal.

3. a) With suitable diagrams discuss the *Read*, *Write* and *Refresh* operation of a one transistor DRAM memory cell. **12 (CO1, PO1)**

b) Sketch the MOS-based NOR ROM memory cell array to store the data given in Table 1 along the bit lines. **10 (CO2, PO2)**

Table 1

BL[0]	BL[1]	BL[2]	BL[3]	BL[4]	BL[5]
0	1	0	1	0	0
1	0	0	1	1	1
0	1	0	0	0	1
1	1	1	0	1	1
1	0	1	0	1	0
0	0	1	0	0	0

4. a) With suitable diagram briefly discuss about Programmable ROM (PROM). **8 (CO1, PO1)**

b) Sketch the circuit diagram of a programmable array logic with 3 inputs and 3 outputs to implement the following Boolean functions. **8 (CO2, PO2)**

$$f1 = AB + A'BC'$$
$$f2 = B'C + ABC'$$
$$f3 = A + A'B$$

5. a) Define enhancement type MOSFET. Describe the different regions of operation of an enhancement type nMOSFET and draw it's typical IV characteristics graph. **12 (CO1, PO1)**

b) Define rise time, fall time and propagation delay related to the operation of logic gates. **6 (CO1, PO1)**

c) Sketch the circuit diagram of 3 input AND gate using Diode Logic and describe it's working principle. **7 (CO1, PO1)**

6. a) Sketch the circuit diagram of a CMOS inverter and describe its operating principle. Also mention some of the properties of this inverter design. **13 (CO1, PO1)**

b) In Fig. 2, an RTL-based NOT gate is working as the driver gate that has a Fan-out equal to N. Calculate the minimum voltage at the input side of each NOT gate guaranteed to be recognized as logic HIGH. Determine the value of N. What will be the effect on Fan-out if a noise margin of 0.5V is considered. [Here, $V_{BE}(Sat)$ = 0.75V, $V_{CE}(Sat)$ = 0.2V, $\beta = 50$, $\sigma = 0.85$] **12 (CO2, PO2)**

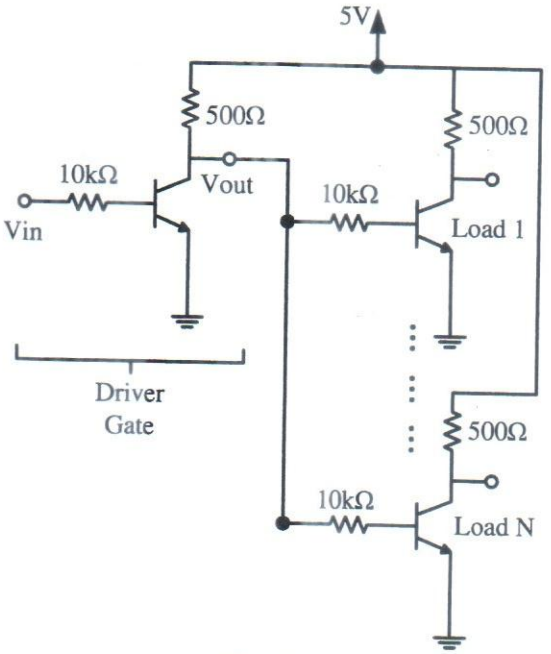

Fig. 2