ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination   Winter Semester, A. Y. 2022-2023
Course No.: EEE 4761   Time: 90 Minutes
Course Title: VLSI Circuits-I   Full Marks: 75

There are 3 (three) questions. Answer all 3 (three) questions. All the questions carry equal marks. Marks in the margin indicate full marks. Do not write anything on the question paper. The symbols have their usual meanings.

1. a) Explain the concept of full custom, and any of the semi-custom styles (among   **10**
        ASICs, FPGA, etc.) of VLSI system design. Distinguish the difference   (CO3, PO5)
        between full custom and semi-custom system design.

    b) Sketch the two input XOR logic using transistor-level design (TG) from the logic **15**
        circuit as shown in Figure 1. Determine the output using truth table.   (CO3, PO4)

Figure 1. Two input XOR Logic gate

2. a) Explain symbol, different colors, and lines used for drawing stick diagram.   **10**
        Sketch a stick diagram of pseudo-CMOS inverter using n-type transistors only   (CO1, CO2,
        as shown in Figure 2a.   PO2)

Figure 2a. Pseudo-CMOS inverter using n-type transistors

    b) Using the voltage transfer curve (VTC) of a CMOS inverter from Figure 2b,   **15**
        show the different operating regions and identify the location of the following (CO1, PO2)
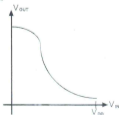   voltages: V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

Figure 2b. VTC curve of CMOS Inverter

3. a) For the given function; $F = A\overline{B}C + A\overline{B}\overline{C} + \overline{A}\overline{B}C$, determine the truth table, and if each of the gate is implemented as CMOS gate, determine the number of transistors needed to build this logic. **10** (CO3, PO4)

   b) For the following circuit in Figure 3, determine the unknown voltages: V_1, V_2, V_3, V_4, and V_{OUT}. Assume that, all the n-type transistors have same threshold voltage (V_T) of 1V, and supply voltage, V_{DD}=5V. Ignore the body effect. **15** (CO3, PO4)
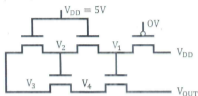

Figure 3: A pass transistor circuit