M.Sc. Engg. /Ph.D. (EE) October 10, 2023 (Afternoon)

27

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination | Winter Semester, A. Y. 2022-2023
Course No.: EEE 6237 | Time: 90 Minutes
Course Title: IC Processing and Fabrication Technology | Full Marks: 75

There are 4 (four) questions. Answer any 3 (three) questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write anything on the question paper. The symbols have their usual meanings.

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1. a) State various process steps to achieve silicon wafer from Silicon Ingot for MOSFET fabrication. Discuss several aspects of your preference of using either glass substrate or silicon wafer for semiconductor fabrication. **10**

   b) A typical Coplanar NMOS electronic device fabrication process is depicted in below Figure 1. Describe the process steps (lithography, etching, etc.) in brief. **15**

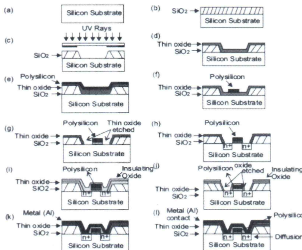

Figure: 1. Process flow for NMOS electronic device fabrication

2. a) Discuss how semiconductor chip is deferred from integrated circuit (IC). Illustrate the IC fabrication life cycle. **10**

b) Why interconnections engineering is so important to achieve optimal electrical behavior of an electronic circuit? Please discuss MOSFET contact resistance, interconnect Cu wire dishing issue, and interconnect wire capacitance impact as shown in Figure 2 on electrical performance. **15**

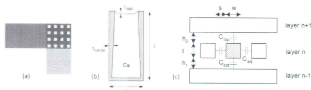

Figure: 2. IC Process issues: (a) contact resistance, (b) Cu wire dishing, and (c) wire capacitance.

3. a) Compare the diffusion and ion implantation processes in MOSFET fabrication with brief schematic figure. **10**

Or

Compare vacancy, interstitial, and intersticiality diffusion model in silicon. **10**

b) Given Figure 3 describes a typical open tube diffusion process. Discuss the process steps. Also, deduce flick's law of diffusion; (equation parameters have their conventional meaning.) **15**

$$\frac{dC}{dt} = D\frac{d^2C}{dx^2}.$$

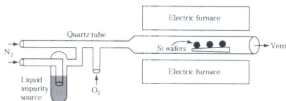

Figure: 3. Open-tube diffusion of impurity on Silicon wafer.

4. a) Why plasma enhanced chemical vapor deposition (PECVD) is preferred among other CVD process for insulator deposition? State some advantages of PECVD process. **10**

Or

Why semiconductor manufacturers in the world are considering atomic layer deposition (ALD) process? State some advantages of ALD process over other semiconductor thin film deposition techniques. **10**

b) With appropriate explanation, discuss one of the inexpensive semiconductor thin film deposition techniques (Spin coating). For reference, consider the below Figure 4 and state the process flow. List down some advantages and limitations of spin-coating deposition technique. **15**

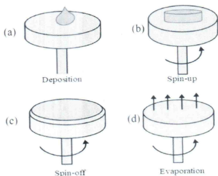

Figure: 4. A simple spin coating of semiconductor thin film on substrate.