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ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION
DURATION: 1 HOUR 30 MINUTES

WINTER SEMESTER, 2022-2023
FULL MARKS: 75

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.
Answer **all 3 (three)** questions. Figures in the right margin indicate full marks of questions whereas corresponding CO and PO are written within parentheses.

1. The development division of the company ABC is embarking on a project to create an application system intended for a wide-ranging user base. The development phase is expected to span two years. During the design phase of the application, they outlined the features and architecture of the system to ensure adaptability for the ever-increasing user base over the subsequent two years. Additionally, they planned to optimize only a certain number of features to be fast and efficient based on popularity. To handle the hardware failure issues, multiple servers will be set up also. The R&D division of the company, on the other hand, wants to integrate an enhancement on their existing processor that currently performs sorting queries. They decided to integrate the enhancement only if the overall performance of the processor becomes at least 3 times faster.

   a) Consider the application system being developed by the development division. With a brief explanation state the ideas incorporated into the system to enhance its performance. — 6 (CO1) (PO1)

   b) In the case of the R&D division, the enhancement to the processor will make the sorting task 29 times faster. Currently, the processor performs sorting 75% of the time. Calculate the overall speedup (improvement) achieved by the enhancement and asses whether the R&D team will incorporate the enhancement to the processor or not. — 10 (CO2) (PO1)

   c) What technological changes can you identify from Figure 1? Do you think the trend in the graph will continue to be the same over the next decade? Justify your answer. — 6 (CO1) (PO2)

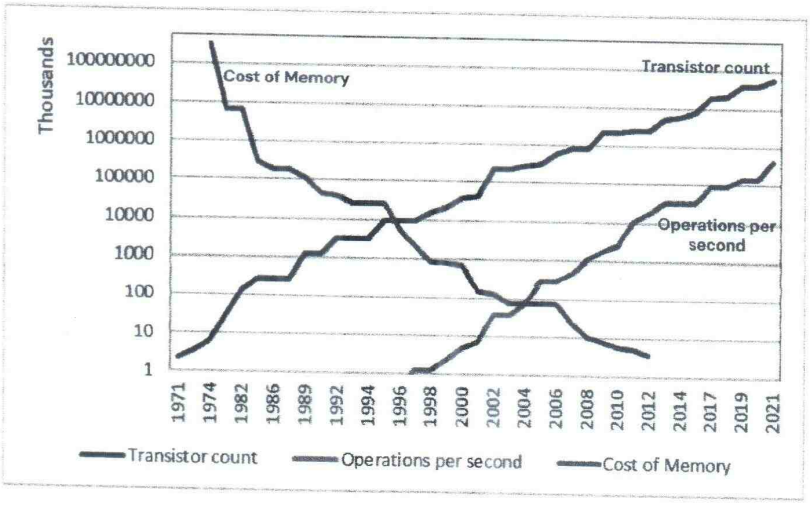

Figure 1: A graph for Question 1.c)

   d) What is Power Wall? — 3 (CO1) (PO1)

2. a) Suppose, in a RISC-V system, register $x7$ contains value 16. In the same register, you want to store the square of 16. Perform the task using a single RISC-V assembly instruction. 6 (CO3) (PO1)

b) Consider the data shown in Table 1 to design an interrupt mechanism to handle the given scenario and provide proper justification for choosing that mechanism. 14 (CO4) (PO3)

Table 1: Data for Question 2.b)

Programs	Duration of execution (s)	Arrival, t (s)	Priority
Execution of a C program	30	0	1
Keyboard input	6	11	5
Printer	5	8	3
Disk	12	15	3
Update Notice	3	20	2

Show each step of the execution process. Here higher value denotes a higher priority.

c) Which concepts would you consider when designing a general purpose computer? Briefly explain your design implementation. 5 (CO4) (PO1)

3. Consider the program shown in Code Snippet 1.

```
1  #include<stdio.h>
2  int main()
3  {
4      int i, m, a, c, d, t, q;
5      int p[] = {10, 50, 90, 35, 40};
6      i = 10;
7      m = t + q;
8      p[1] = m;
9      a = m + c + d;
10     if(a == i){
11         a = a + 5;
12     }else {
13         p[3] = i;
14     }
15 }
```

Code Snippet 1: A C program for Question 3.

a) Assume the values of array `p` from Code Snippet 1 above are stored in a RISC-V system. The base address of the array is 500. Show how the values are arranged in the memory and their corresponding memory addresses using a figure. You can represent the values of the array in hexadecimal instead of binary in the memory segments. 5 (CO3) (PO2)

b) The variables `i`, `m`, `a`, `c`, `d`, `t` and `q` in Code Snippet 1 correspond to the registers $x9$ through $x15$. The base address of the array is stored in $x23$. 8 + 7 (CO3) (PO2)

i. Convert the C program from line 6 to 16 into corresponding RISC-V instructions.

ii. Convert the RISC-V instructions generated for lines 6, 7, and 8 into machine codes. You can represent the values in hexadecimal instead of binary. The machine codes denoting the operation types of the instructions is not required.

c) RISC-V ISA does not have any explicit `NOT` instruction. How is this instruction implemented in RISC-V? Explain with an example. 5 (CO1) (PO1)