ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION WINTER SEMESTER, 2022-2023

DURATION: 1 HOUR 30 MINUTES FULL MARKS: 75

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

Answer **all 3 (three)** questions. Figures in the right margin indicate full marks of questions whereas corresponding CO and PO are written within parentheses.

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1. Dynamic Random Access Memory (DRAM) is a common type of computer memory used for temporary data storage. Several key steps are involved in performing a read operation in a DRAM module.

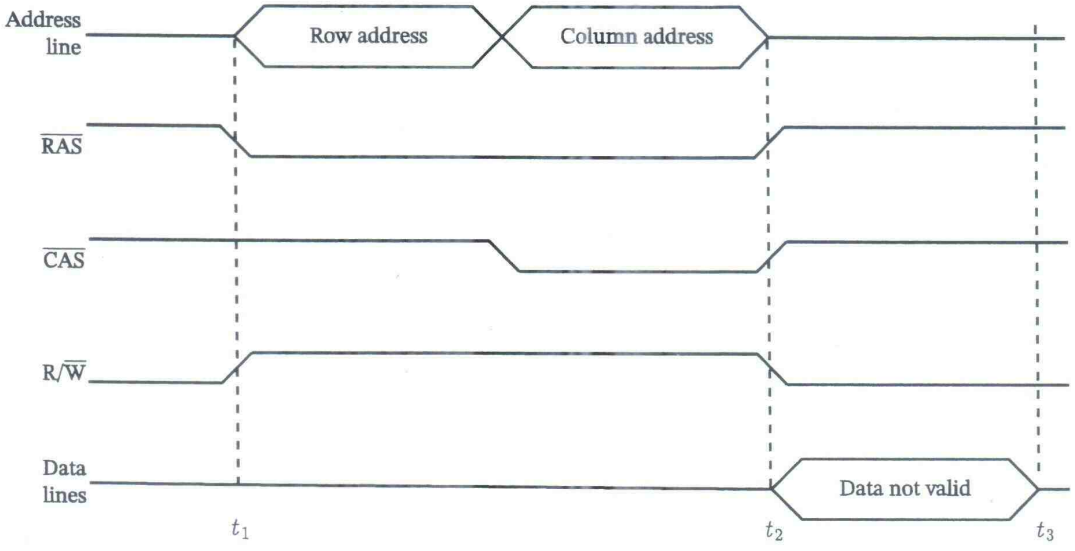


Figure 1: Timing Diagram of a DRAM read operation for Question 1

a) Explain the key steps of DRAM read operation based on the timing diagram represented in Figure 1. Draw another timing diagram for the DRAM write operation showing all key steps. 5 (CO1) (PO1)

b) Explain the total access time (T_1) required to respond to a read or write request based on the timing diagram given in Figure 1. What is the next job of a DRAM chip after performing the read operation? Explain the necessity of this task and its execution. Assume that this task requires T_2 time. 5 (CO1) (PO1)

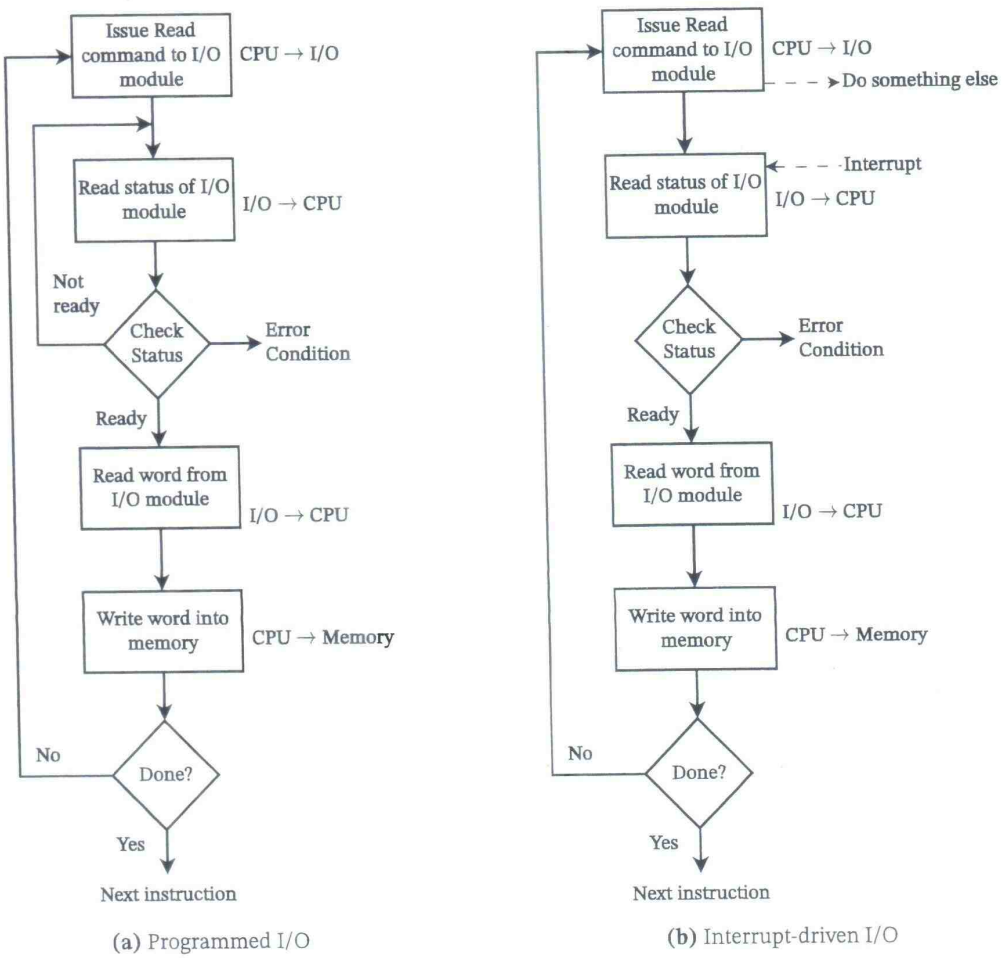
c) Given the information in Question 1.b), what is the memory cycle time if T_1 is $60ns$ and T_2 is $40ns$? What is the maximum data rate supported by this DRAM, presuming a 1-bit output? What data transfer rate can be achieved by implementing a 32-bit wide memory system using these chips? 5 (CO1) (PO1)

d) Draw the memory cell structures of 1-bit DRAM cell and 1-bit SRAM cell. 5 (CO4) (PO1)

2. a) With appropriate examples and/or figures, define the following terms: 2 × 5 (CO4) (PO1)
   i. Instruction Set Architecture
   ii. Cylinder
   iii. Data Channel
   iv. Moore's Law
   v. Victim Cache

   b) To assess a computer system following a SPEC benchmark suit, we have to consider a specific calculation procedure. 4 + 3 + 3 (CO3) (PO2)
   i. Explain the steps of the calculation procedure using a flowchart.
   ii. What kind of Pythagorean mean will be used to calculate the overall metric? Justify your answer.
   iii. How will the pipeline-based system be considered in this assessment process?

   c) The flowchart shown in Figure 2(a) outlines the necessary steps for any data transfer between the CPU and I/O devices. However, interrupt-driven I/O, as shown in Figure 2(b), is often considered to improve the efficiency of any system. Considering both diagrams, explain how interruption could be incorporated into the system. Additionally, apply Amdahl's law to determine the enhancement in performance while using interruption. 5 (CO3) (PO2)



(a) Programmed I/O (b) Interrupt-driven I/O

Figure 2: Flowcharts of data transfer between CPU and I/O for Question 2.c)

3. a) Consider a main memory system with 32-bit byte-level addressing and a cache with 64-byte line size. Assume a four-way set-associative cache with a tag field in the address of 9 bits. 4 + 3 + 3 (CO4) (PO1)

   i. Determine the values of the following parameters:
      - Number of addressable units
      - Number of blocks in main memory
      - Number of lines in set
      - Number of sets in the cache
      - Number of lines in the cache

   ii. What modifications to the memory system configuration can be performed to make it a Direct mapping and fully-associative mapping system, respectively?

   iii. Illustrate the address formats in direct mapping, fully-associative mapping, and four-set associative mapping approaches.

   b) What happens when the Error Correction System finds an error with a check bit instead of a data bit according to its syndrome word? How many check bits are needed if the Hamming error correction code is used to fix single-bit and detect double-bit errors in a 1024-bit data word? Justify your answer. 8 (CO3) (PO1)

   c) Consider a single-platter disk with the following parameters: 6 × 2 (CO2) (PO1)
      - Rotation speed: 7200 rpm
      - Number of tracks on one side of the platter: 30,000
      - Number of sectors per track: 600
      - Sector size: 1kB
      - Seek time: 1ms for every hundred tracks traversed

   Assume that the disk head starts at track 0. Let the disk receive a request to access a random sector on a random track. Now, calculate the following parameters:

   i. Average seek time
   ii. Average rotation latency
   iii. Transfer time for a sector
   iv. Total average time to satisfy a request
   v. Size of a cylinder for a double-sided four-platter disk
   vi. Disk capacity for a double-sided eight-platter disk