ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION
DURATION: 3 HOURS

WINTER SEMESTER, 2022-2023
FULL MARKS: 150

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.
Answer **all 6 (six)** questions. Figures in the right margin indicate full marks of questions whereas corresponding CO and PO are written within parentheses.

1. a) Suppose, you have a memory system where the cache size is 8 bytes and each block holds 1 byte of data. A program of 7 instructions is loaded into the main memory for execution and the sequence of reference to the memory addresses are `0x52A` → `0xB53` → `0x619` → `0xAB3` → `0x52A` → `0xB53` → `0x619`

Table 1: Cache table for Question 1.a)

Index	Valid bit	Tag	Data	Hit/Miss
	0			
	0			
:	:	:	:	:
:	:	:	:	:
	0			

i. For each memory reference, show the index, valid bit, tag, and whether it was a hit or a miss. Draw the final table after the execution of all instructions. 15 (CO3) (PO2)

ii. Calculate the hit ratio and miss ratio from the given scenario. 4 (CO3) (PO1)

b) How do caches take advantage of spatial locality? Explain with an example. 6 (CO1) (PO1)

2. Registers x10, x11, x12, x13, x14, and x15 contain values 20, 8, 5, 6, 3, and 19, respectively. The machine code of an instruction `0x00C5F7B3` is stored at memory address 450. The current value of the Program Counter (PC) is also 450.

Table 2: Data for Question 2.

0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rsl	100	rd	0110011	XOR
0000000	rs2	rs1	111	rd	0110011	AND
0000000	rs2	rsl	110	rd	0110011	OR
0000000	rs2	rsl	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA

a) Convert the machine code into its corresponding RISC-V assembly code. 6 (CO3) (PO1)

b) Considering the given instruction (`0x00C5F7B3`), answer the following questions: 3

i. Identify all the datapath elements required to execute this instruction. 7 + 4 (CO3) (PO2)

ii. Write down all the inputs and outputs of the datapath elements for this instruction.

iii. How many multiplexers will be needed for this instruction? What are the input options for these multiplexers and which of these inputs will be chosen for this instruction?

3. a) Registers x6, x7, x8, x9, and x10 contain the values 13, 9, 5, 7, and 3, respectively. The CPU architecture is shown in Figure 1

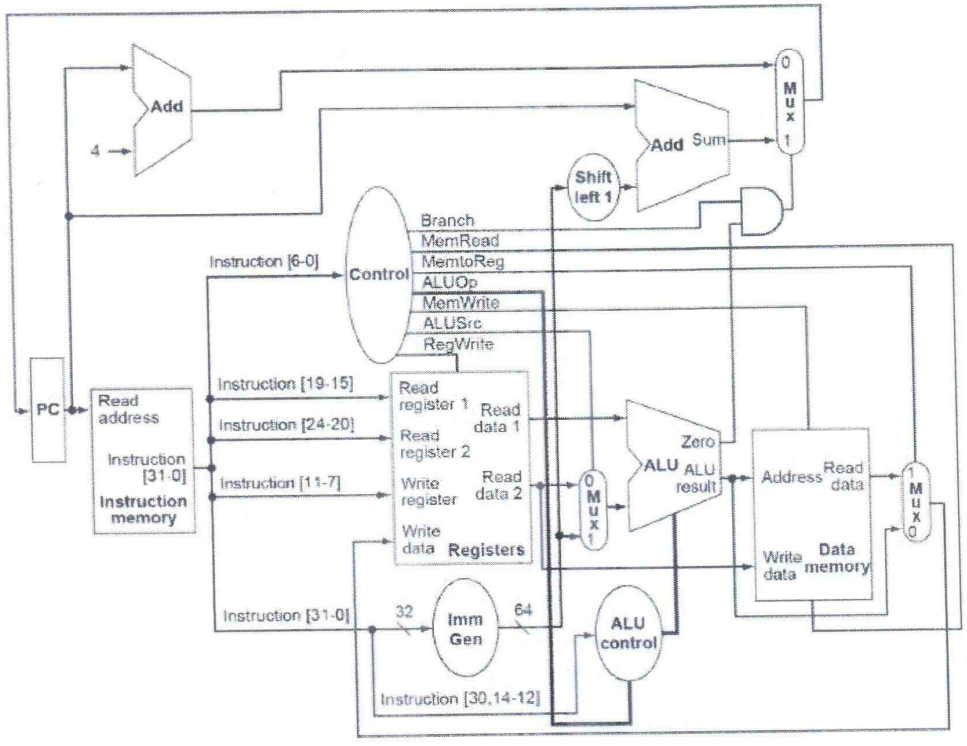

Figure 1: CPU architecture for Question 3.a)

i. Design the datapath that will be active only for the execution of the particular instruction **`"beq x8, x10, 0x3C"`**. 10 (CO4) (PO3)

ii. Show all the bit values of the control lines including the zero output. 6 (CO3) (PO2)

Table 3: Data for Question 3.b)

ALUOP		Funct7 field							Funct3 field			Operation
ALUOp1	ALUOp0	I[31]	I[30]	I[29]	I[28]	I[27]	I[26]	I[25]	I[14]	I[13]	I[12]	
0	0	0	0	0	0	0	0	0	0	1	0	ld
0	1	0	0	0	0	0	0	0	0	0	0	beq
1	0	0	1	0	0	0	0	0	0	0	0	sub
1	0	0	0	0	0	0	0	0	1	1	1	and
1	0	0	0	0	0	0	0	0	1	1	0	or

b) i. What do you understand by don't care terms? 2 (CO1) (PO1)

ii. With an explanation, identify the don't care terms from Table 3. 7 (CO3) (PO2)

4. a) A company has 2 computers to perform the required operations. Computer X has a processor that has a simple single-cycle implementation where as computer Y has a pipelining technique implemented.

Table 4: Stage time for Question 4.a)

IF	ID	EX	MEM	WB
180ps	75ps	300ps	210ps	75ps

i. Assume that the two computers use RISC-V architecture. The time taken for the 5 stages of the pipelined system in computer Y are given in Table 4. If a program with 135,000 instructions is executed on both computers, how much faster will be computer Y than computer X? — 12 (CO2) (PO1)

ii. What are the advantages of computer Y over computer X in terms of their processor implementation? — 5 (CO1) (PO1)

b) How are the control bits passed along for each instruction in a pipelined system? Draw figures to show the implementation. Explain the reason for such an implementation. — 8 (CO2) (PO2)

5. a) Can we connect the I/O devices directly to the system bus? Justify your answer. — 8 (CO1) (PO1)

b) Suppose your program has to take 5 inputs from the user for an array. Which method of data transfer will be the most suitable to achieve the best performance? Justify your answer. — 12 (CO2) (PO2)

c) Write a short note on the SRAM technology. — 5 (CO1) (PO1)

d) What is the purpose of adding the control unit to the processor? — 5 (CO1) (PO1)

6. The instructions shown in Code Snippet 1 are executed sequentially on a RISC-V system with a 5-stage pipeline.

```
1 ld x1, 8(x3)
2 add x9, x10, x12
3 sub x9, x9, x5
4 add x20, x9, x1
5 ld x8, 16(x3)
6 add x15, x8, x7
7 and x24, x26, x27
```

Code Snippet 1: Instruction set for Question 6.

Data hazard detection units are added to the system.

a) Identify the hazard(s) that will occur while executing the first 5 instructions and write the respective conditions to detect the hazard(s). — 12 (CO1) (PO1)

b) Complete Table 5 to show how these instructions will be executed in the pipelined processor. Show the stalls if occur and draw arrows to show data forwarding where necessary. 13 (CO3) (PO2)

Table 5: Partial table for Question 6.b)

	CC1	CC2	CC3	CC4	CC5	....
ld	IF	ID	EX	MEM	WB	...
add		IF	ID			...
sub			IF			...
:	:	:	:	:	:	:
:	:	:	:	:	:	:
and						...