ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION   **WINTER SEMESTER, 2022-2023**
DURATION: 3 HOURS   **FULL MARKS: 150**

CSE 4503: Microprocessors and Assembly Language

Programmable calculators are not allowed. Do not write anything on the question paper.
Answer all **6 (six)** questions. Figures in the right margin indicate full marks of questions whereas corresponding CO and PO are written within parentheses.

1. a)	What is addressing mode? Write a short note on I/O addressing with BIOS and DOS routine.	2 + 8 (CO1) (PO1)
b)	How does 8086 get the address of a particular Interrupt Service Routine (ISR)? Explain the concept using Interrupt Type#31.	5 + 3 (CO1) (PO1)
c)	To perform MUL and DIV operation, write assembly codes each for MUL and DIV using: i. 8086 Register Addressing Modes ii. 8086 Bit Manipulation Instructions	7 (CO4) (PO1)
2. a)	Write short differentiations the following 8086 signals/instructions: i. ALE and BHE ii. LEA and OFFSET iii. NOT and NEG iv. AND and TEST	10 (CO4) (PO1)
b)	Based on the pin specifications (pin no. 24 to 31) of 8086 microprocessor, differentiate between the Minimum mode and Maximum mode operations.	8 (CO1) (PO1)
c)	Write an assembly language program structure to clearly state the operational differentiation between LABEL and LOOP? In your program, you need to allocate exactly 64 Kbytes of memory for Data Segment, 1024 Bytes for Stack Segment and also consider that the size for Code Segment must exceed 64 Kbytes.	7 (CO4) (PO2)
3. a)	Draw the details of READ Bus timing diagram showing all the necessary signals of 8086 microprocessor. You should consider that the read operation is to be made from an input device with port address of 10000H. Consider that there are three WAIT states, interrupt flag is SET and DS register is in use for data accessing.	10 (CO2) (PO2)
b)	Putting multiple processing element/core in a single IC is an intelligent solution. Explain with a suitable example how this process is achieved and motivation of this action.	8 (CO3) (PO1)
c)	Which processor does include the parity-bit at memory segment for error-control and how? Draw and differentiate between the memory banks for 8085, 8086, 80386, and Pentium microprocessors.	2 + 5 (CO3) (PO1)
4. a)	What is VM8086 Mode? Differentiate between the flag registers of 8085, 8086, 80286 and 80386 microprocessors.	2 + 8 (CO3) (PO1)

b) What is Duty Cycle? Find out the relation among Clock State, Bus/Machine Cycle, and Instruction Cycle.

2 + 6
(CO2)
(PO1)

c) With appropriate examples differentiate between the calling operations PROCEDURE and MACRO with respect to use of memory location.

7
(CO4)
(PO1)

5. a) What is multi-segment memory model? How can a Code Segment, three Data Segments, and a Stack Segment be defined in a multi-segment model?

4 + 6
(CO3)
(PO1)

b) What is Linear Address? Explain the concept of 5-stage U-pipeline or V-pipeline of Pentium microprocessor.

2 + 6
(CO3)
(PO1)

c) *Global Descript Table (GDT) occupies 64KB of physical memory*-Justify the statement explaining how this process is performed.

7
(CO3)
(PO1)

6. Write short notes on the followings using appropriate example/figure:

5 × 5
(CO1)
(PO1)

i. Memory Segment Overlapping in EMU8086 Emulator

ii. List out of Co-processors for 80x86 Series

iii. Machine Status Word (MSW)

iv. Floating Point Unit (FPU)

v. Paging