ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination
Course No.: EEE 4307
Course Title: Digital Electronics

Winter Semester, A. Y. 2022-2023
Time: 3 Hours
Full Marks: 150

There are 6 (**six**) questions. Answer all 6 (**six**) questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets.

1. a) Using r's complement, ('r' represents the base) perform the subtraction operations: 12
   (i) $(46894)_{10} - (1883)_{10}$ (ii) $(01100101)_2 - (11101000)_2$. (CO2, PO2)

   b) Prove the identity of each of the following Boolean equations, using algebraic 13
   manipulation: (CO2, PO2)
   (i) $AB\bar{C} + B\bar{C}\bar{D} + BC + \bar{C}D = B + \bar{C}D$
   (ii) $\overline{A}(A+B) + (B+A)(A+\overline{B}) = A+B$

2. a) Design a Full-Adder using two-level NAND gates. 8 (CO2, PO2)

   b) Design an adder that is capable to add four following 4-bit binary numbers 10
   $A = A_3A_2A_1A_0$, $B = B_3B_2B_1B_0$, $C = C_3C_2C_1C_0$ and $D = D_3D_2D_1D_0$. (CO3, PO2)
   Hint: You may use the Full-Adder Block that you have designed in question 2(a).

   c) Deduce the simplified expression of the following Boolean function using 7
   Karnaugh-Map in SOP form: (CO2, PO2)
   $F = (B+C+D).(A+B+\overline{C}+D).(\overline{A}+B+C+\overline{D}).(A+\overline{B}+C+D).(\overline{A}+\overline{B}+C+D)$.

3. a) Determine the state table and the state diagram of the sequential circuit shown in 13
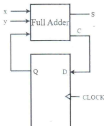   Figure 3.a. (CO2, PO1)

Figure 3.a

b) Suppose you are given a supply of a 25 KHz square wave signal. Design a circuit that will take the mentioned square wave signal as input and give **12.5 KHz signal with 25% duty cycle** as output .

12
(CO3,
PO2)

4. a) Show the logic diagram of a single bit memory cell using J-K flip flop.

8
(CO1,
PO1)

b) The following memory units are specified by the number of words times the number of bits per word. Calculate the number of address lines and input-output data lines that are needed in each case:

   i. 2 K × 16
   ii. 64 K × 8
   iii. 16 M × 32
   iv. 96 K × 12

12
(CO2,
PO2)

c) Calculate the number of 128K × 16 RAM chips needed to provide a memory capacity of 2MB. Show necessary calculations.

5
(CO2,
PO2)

5. a) Design a sequence detector that has a form shown in figure 5.a. The output Z should be 1 if the input sequence ends in either 1000 or 0011 and Z should be 0 otherwise.
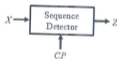
12
(CO3,
PO2)

Figure 5.a

b) Show the implementation of the following logic expression using CMOS.
$F = A.B.C + B.(A + C)$

13
(CO2,
PO2)

6. a) Construct a J-K flip-flop with 'Preset' and 'Clear' inputs. Show the characteristic table.

   10
   (CO1, PO1)

   b) For the J-K flip-flops with inputs as shown in the Figure 6.b, sketch the time-line diagram for the Q_0 and Q_1 output relative to the clock pulse (CP).
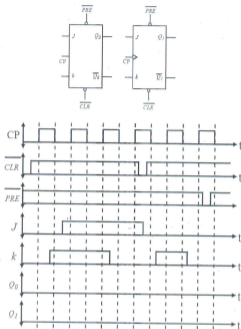
   15
   (CO2, PO2)

Figure 6.b