# ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT) ORGANISATION OF ISLAMIC COOPERATION (OIC) DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING 

Semester Final Examination
Course No.: EEE 4705
Course Title: Microcontroller Based System Design

Winter Semester, A. Y. 2022-2023
Time: 3 Hours
Full Marks: 150

There are 6 (six) questions. Answer all 6 (six) questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets.

1. a) Assume your desired output is saved in the label "MSG_1" and following is the subroutine for displaying the output on a LCD. However, the code is incomplete and shows "?" marks in the missing places. Complete the code and show the

15 connection between AT89C51 and LM016L based on the given subroutine. [Note: Write the complete subroutine on your answer seript.]

| 1 | ORG 90H | 29 |  | LCALL DELAY |
| :---: | :---: | :---: | :---: | :---: |
| 2 | LCD DISPLAY: | 30 |  | CLR ? |
| 3 | MOV SP, \#70H | 31 |  | RET |
| 4 | MOV PSW, \#00 H | 32 | DISPLAY: | LCALL READY |
| 5 | RS EQUP2.0 | 33 |  | MOV P1, A |
| 6 | RW EQUP2.1 | 34 |  | SETB ? |
| 7 | ENBL EQU P2.2 | 35 |  | CLR ? |
| 8 | MOV A, $\ddagger 38 \mathrm{H}$ | 36 |  | SETB ? |
| 9 | LCALL COMMAND | 37 |  | LCALL DELAY |
| 10 | LCALL DELAY | 38 |  | CLR ? |
| 11 | MOV A. \#OEH | 39 |  | RET |
| 12 | LCALL COMMAND | 40 | READY: | SETB ? |
| 13 | LCALL DELAY | 41 |  | CLR ? |
| 14 | ACALL DELAY | 42 |  | SETB ? |
| 15 | MOV DPTR, \#MSG_1 | 43 | WAIT: | CLR ? |
| 16 | LOOP_1: CLR A | 44 |  | ACALL DELAY |
| 17 | MOVC A,@A+DPTR | 45 |  | SETB ? |
| 18 | JZ FINISH_2 | 46 |  | JB ?, WAIT |
| 19 | LCALL DISPLAY | 47 |  | RET |
| 20 | LCALL DELAY | 48 | DELAY: | MOV R3, \#50 |
| 21 | INC DPTR | 49 | AGAIN_2: | MOV R4, \#255 |
| 22 | LTMP LOOP_1 | 50 | AGAIN: | DINZ R4, AGAIN |
| 23 | FINISH_2: SJMP \& | 51 |  | DJNZ R3, AGAIN_2 |
| 24 | COMMAND: LCALL READY | 52 |  | RET |
| 25 | MOV Pl, A | 53 | MSG_1: | DB "Output is ",0 |
| 26 | CLR ? | 54 |  | RET |
| 27 | CLR ? | 55 |  | END |
| 28 | SETB ? |  |  |  |

b) Find the MAX1112 control byte for CH3, single-ended, unipolar, internal clock and fully operational modes.
2. a) Design a binary-ASCII converter.

Use assembly language to convert an 8 bit binary (hex equivalent) data to corresponding ASCII and save them following the Little-Endian convention (low digit in the lower address location and high digit in the higher address location), Assume that the binary data is available through port P1 of AT89C51. Break down your code into two subroutines, one that conyerts binary to decimal, and two, that converts the corresponding decimal to ASCII.
b) Explain the following:
i. Erasable programmable ROM.
ii. Electrically crasable programmable ROM.
iii. Static RAM.
iv. Non-volatile RAM.
3. a) Write a program to generate the following wave pulses simultaneously on the corresponding ports as shown in the Fig. 3. Given XTAL $=11.0592 \mathrm{MHz}$. Justify 15 (CO2, your code.


Fig. 3
b) State the significance of IP register.
4. a) Design a counter for counting the pulses of an input signal. The pulses to be counted are fed to pin P3.4 of an AT89C51. Given XTAL $=22 \mathrm{MHz}$. Justify your design.

15
(CO2,
b) Justify your preference between polling and interrupts.
5. a) Assume there are 2 doors in a room. You have placed ADC0804 in the first door and ADC 0848 in the second door. The ADCs are equipped with necessary sensors in order to count the number of people entering/leaving through the doors. Both the ADCs are connected to your AT89C51 in such a way that both the ADCs are active simultancously.
Sketch the complete connection diagram to design such a system.
[Note: Read Question 5(b) before you sketch your connection.]
b) Create a complete assembly code for executing the design stated in Question 5(a). Initiate the conversion process for both the ADCs and continuously monitor the status of P0.7. Serve each of the ADCs whenever the conversion is finished and reinitiate for the next cycle. If at any moment you get a bit in P0.7, you should terminate your program. Call the sub-routines for data conversion and data display from Question 2(a) and 1 (a) respectively.
6. a) Connect two external memory devices with your AT89C51; one Program ROM and one Data ROM. While giving the connection address the following:
-(CO3,
i. Justify your chosen size for each of the memory devices.
ii. Based on the chosen size, justify how many address lines are required for accessing the memory devices.
iii. Design your own decoder and connect the remaining pins with your decoder.
iv. Use 74LS373 for address/data demultiplexing.
b) Based on your connection in Question 6(a), determine the address range for cach of the connected external memory devices.
c) Assume there are 10 bytes of data stored in the external Program ROM which needs to be transferred to the external Data ROM. However, only the lower nibble of all these data is useful and the rest are redundant. Create an assembly code to transfer the useful data to the Data ROM from the Program ROM. [Note: The data in Program ROM is saved in locations of your choice and the transferred data should also be saved in locations of your choice in the Data ROM. However, these locations should agree with the address range you mentioned in Question 6(b).]



ADC0848 Chip


LM016L


