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ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination
Course No.: EEE 4761
Course Title: VLSI Circuits-I

Winter Semester, A. Y. 2022-2023
Time: 180 Minutes
Full Marks: 150

There are **6 (six)** questions. Answer all **6 (six)** questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets.

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1. a) Explain symbols, different colors, and lines used to draw stick diagram. **10 (CO2, PO2)**

   b) Sketch the transistor-level circuit, and corresponding stick diagram of a given function of static CMOS: $F = \overline{A \cdot B + C \cdot D}$. **15 (CO2, PO2)**

2. a) For the given function, $F = \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}C$, determine the truth table, and if each of the gate is implemented as CMOS gate, determine the number of transistors needed to build this logic. **10 (CO3, PO4)**

   b) Discuss raising and falling time assymetry in complex combinational logic. From the below 3-input NAND logic circuit (Figure 1), determine the origin of such assymetry and the ways to control using progressive sizing technique. **15 (CO3, PO5)**

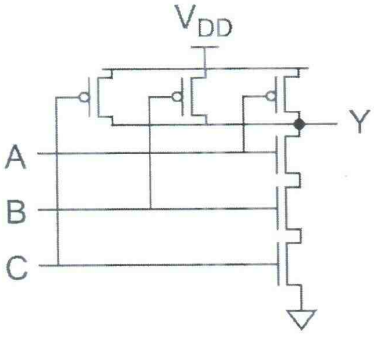

Figure 1: NAND logic circuit with three inputs.

3. a) Explain what shift register (SR) is and two basic operations. Explain the synchronous and asynchronous data loading in shift register. **10 (CO4, PO3)**

   b) Design a 4-bits parallel in serial out (PISO) shift register (SR) as shown in Figure 2 using synchronous data loading. (Hint) Use AND/OR logic combination for data loading in SR. **15 (CO4, PO5)**

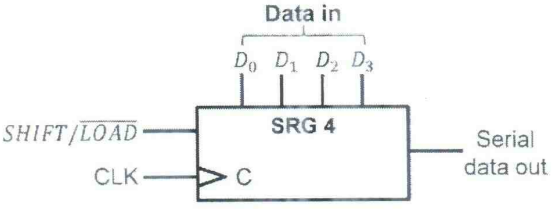

Figure 2: Logic symbol for 4-bits PISO SR.

4. a) Illustrate FPGA logic and explain how it differs from CPLD. Discuss two main categories of FPGA in terms of fabrication. Discuss a simplified building block of FPGA and one representative lookup table. **10 (CO5, PO3)**

b) The PLA circuit shown below (Figure 3) is used to implement read only memory. Write the truth table and logic equations of F1, F2, F3, F4, and F5. **15 (CO5, PO5)**

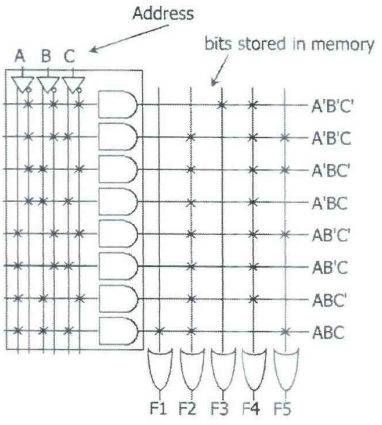

Figure 3: Programmable logical array (PLA) circuit.

5. a) Discuss content addressable memory (CAM) and explain the differences with random access memory (RAM) technology. **10 (CO6, PO3)**

b) Sketch a 3-input 4-output read only memory (ROM) (8x4 ROM) circuit that implements the following Boolean functions: **15 (CO6, PO5)**

$$A(x, y, z) = \Sigma (0, 1, 4, 7)$$
$$B(x, y, z) = \Sigma (1, 3, 6, 7)$$
$$C(x, y, z) = \Sigma (2, 5)$$
$$D(x, y, z) = \Sigma (0, 1, 2, 4, 5, 7)$$

6. a) Discuss the key differences between BiCMOS and CMOS technology in brief. Explain the operation of a BiCMOS two input NAND gate with the help of a circuit diagram. **10 (CO7, PO4)**

b) The VTC curve of BiCMOS inverter in Figure 4 shows smaller V_{OUT} at low input (V_{IN}), and comparatively higher (non-zero) V_{OUT} at higher V_{IN} signal as compared to conventional CMOS technology. Explain the origin of such behavior. **15 (CO7, PO5)**

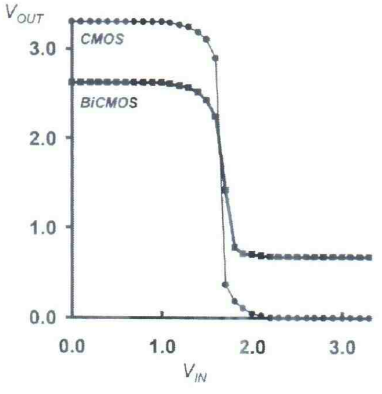

Figure 4: Comparison of VTC characteristics of CMOS and BiCMOS circuit.