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M.Sc. TE. (2 yr), 1st Sem. Date: December 15, 2023 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination — Winter Semester, A.Y. 2022-2023
Course No.: EEE 6199 — Time: 3 Hours
Course Title: Solid State Devices — Full Marks: 150

There are **8 (eight)** questions. Answer **any 6 (six)** questions. All questions carry equal marks. Marks in the margin indicate full marks. The symbols carry their usual meanings. Do not write on this question paper.

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1. a) Write short notes on Zener diode. 05

   b) What are the equivalent models available for *p-n* junction diode? Draw the equivalent circuit and sketch the forward characteristics for each model. 10

   c) With proper diagrams discuss the Evaporation method and Sputtering method for thin film deposition. 10

2. a) How can you categorize semiconductor photodevices? What are the different categories? 05

   b) With neat diagrams, describe the working principle of *p-n* junction photodiode. Also draw its *I-V* characteristics graph for different photogeneration rate. 10

   c) In solid-state device fabrication, what is the purpose of the diffusion and ion implantation process? With neat diagrams, describe the diffusion process. Write the advantages of ion implantation process over diffusion? 10

3. a) Describe the operation of enhancement type pMOSFET in all regions of operation. Also draw the IV characteristic curve of a typical pMOSFET clearly showing all regions of operation. 13

   b) With neat diagrams discuss the working principle of a light emitting diode (LED). Draw the cross-sectional sketch of the standard LED package and briefly discuss the structure of the LED package. 12

4. a) With neat diagrams, describe nMOSFET fabrication process in details. 15

   b) With figure, explain the body bias effect in a nMOSFET. 10

5. a) With diagram(s), derive the expressions of drain currents of an nMOSFET in linear and saturation regions of operation. 15

   b) For an enhancement type nMOSFET, consider the aspect ratio to be equal to 2, the threshold voltage to be equal to 1V and $\frac{\varepsilon\mu}{D}$ to be $30\mu A/V^2$. If the applied gate to source voltage is 5V and the drain to source voltage is 3V, then describe in which region the nMOSFET is going to operate and determine the value of the corresponding current. 10

6. a) Consider an nMOS inverter with depletion type load. Supply voltage, V_D = 5V. Threshold voltages of load and driver are V_{td} = -4V and V_{te} = 1V, respectively. Required low level output voltage is less than 30% of V_{te}. Let, $\frac{\varepsilon\mu}{D}$ for load and driver be 25μA/V^2 and 30μA/V^2, respectively. What will be the high-level output voltage? Calculate inverter ratio ignoring body effect of load. Choose suitable values of aspect ratios of load and driver network. 13

b) Derive the equation of edge times of nMOS inverter with depletion type load. Follow the same transistor and circuit parameters as mentioned in Question 4(a). 12

7. a) For a CMOS inverter, consider the supply voltage to be 5V. The threshold voltages of the load and driver are -1V and 1V, respectively. Let, $\frac{\varepsilon\mu}{D}$ for load and driver be 15μA/V^2 and 30μA/V^2, respectively. Consider the aspect ratios of the load and driver to be 2 and 1, respectively. For the following range of input voltage (V_{in}) given in Table 1, draw the transfer characteristics of the CMOS inverter. Show the necessary calculations and the relevant plots to obtain the transfer characteristics. 20

Table 1

V_{in}	0V	1V	2V	3V	4V	5V

b) For a CMOS inverter circuit, describe the significance of inversion voltage. 05

8. a) Write some of the disadvantages of nMOS inverter with resistive load. 05

b) Draw the nMOS circuit design and CMOS circuit design for 3 input NOR gate. 08

c) Draw the circuit diagram to implement the following Boolean expression using CMOS logic, 12

$$F = (A + B)' C + D$$