ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination — Winter Semester, A. Y. 2022-2023
Course No.: EEE 6237 — Time: 180 Minutes
Course Title: IC Processing and Fabrication Technology — Full Marks: 150

There are 8 **(eight)** questions. Answer any 6 **(six)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write anything on the question paper. The symbols have their usual meanings.

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1. a) Discuss the key differences between BiCMOS and CMOS technology in brief. Explain the operation of a BiCMOS two input NAND gate with the help of a circuit diagram. **10**

   b) The VTC curve of BiCMOS inverter in Figure 1 shows smaller V_{OUT} at low input (V_{IN}), and comparatively higher (non-zero) V_{OUT} at higher V_{IN} signal as compared to conventional CMOS technology. Explain the origin of such behavior. **15**

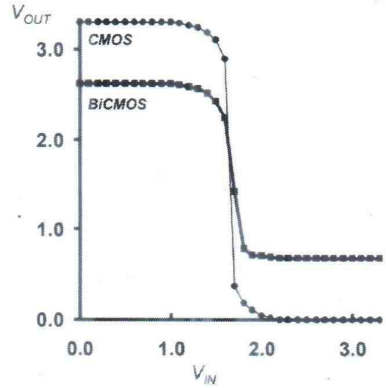

Figure 1: Comparison of VTC characteristics of CMOS and BiCMOS circuit.

2. a) Evaluate the key differences between QFP SMT and "hole-through" IC packaging technologies. **10**

   b) Explain any of the packaging technology as shown in Figure 2 along with advantages, limitations, and applications. **15**

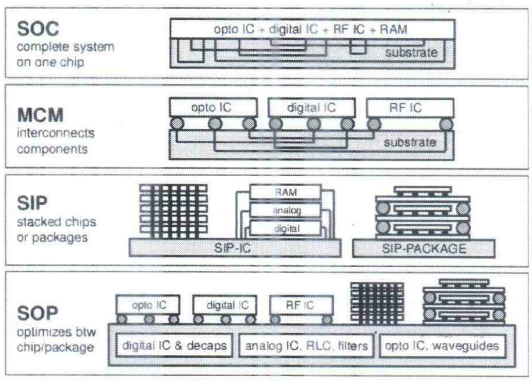

Figure 2: Comparison of IC processing technologies.

3. List down the dissimilarities (at least five) between MOSFET and TFT technology. State the poly-Si crystallization process from a-Si and its application to poly-Si TFT. **25**

4. a) Discuss how semiconductor chip is deferred from integrated circuit (IC). Illustrate the IC fabrication life cycle. **10**

b) Why interconnections engineering are so important to achieve optimal electrical behavior of an electronic circuit? Please discuss MOSFET contact resistance, interconnect Cu wire dishing issue, and interconnect wire capacitance impact as shown in Figure 3 on electrical performance. **15**

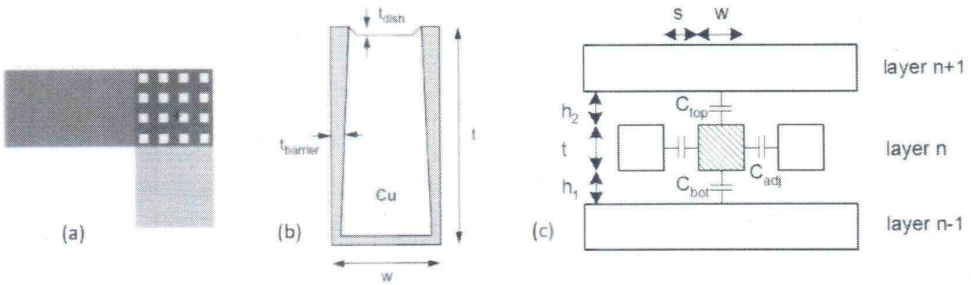

Figure 3: IC Process issues: (a) contact resistance, (b) Cu wire dishing, and (c) wire capacitance.

5 a) Discuss the following issues related to contact metallization and interconnections in IC fabrication: **10**

i) Local Stress
ii) Metal Uniformity over length and area
iii) Reflectivity of Metal

b) Among CVD, thermal evaporation. E-beam evaporation, and sputtering metal deposition techniques as shown in Figure 4, discuss any two and distinguish the differences among them. **15**

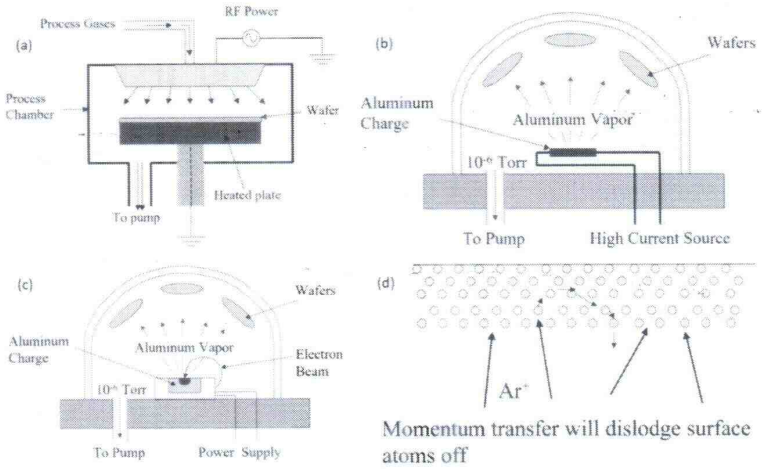

Figure 4: Metal deposition techniques: (a) CVD, (b) Thermal evaporation, and (c) E-beam evaporation, and (d) sputtering.

6 a) Compare the diffusion and ion implantation processes in MOSFET fabrication with brief schematic figure. **10**

b) Compare vacancy, interstitial, and intersticiality diffusion model in silicon. **15**

7. a) Compare the positive and negative photoresists (PR) material and processes in IC fabrication with the brief schematic figure. **10**

b) Explain what is meant to photomask and state the reasons of photomask degradation. Discuss the mask to wafer alignment process for IC fabrication as shown in Figure 5. **15**

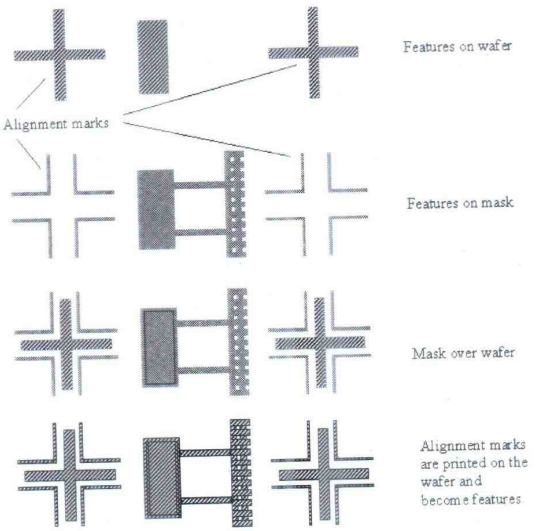

Figure 5. Mask to wafer alignment process in IC fabrication technology.

8. a) State various process steps to achieve silicon wafer from Silicon Ingot for MOSFET fabrication. Discuss several aspects of your preference of using either glass substrate or silicon wafer for semiconductor fabrication. **10**

b) From Figure 6, discuss the advantages of ionic amorphous oxide semiconductors (IOAS) for the TFT process (controlling mobility, stability, etc.): **15**

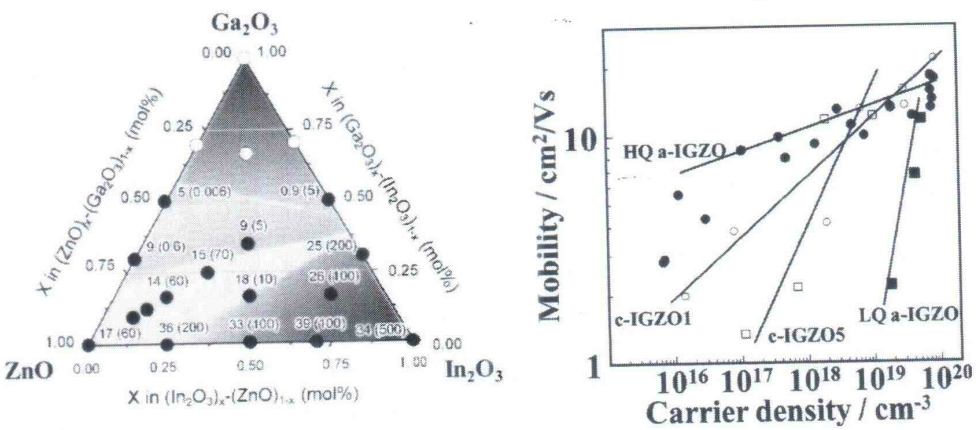

Figure 6: Ionic Oxide Semiconductor composition impact on mobility.