ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION SUMMER SEMESTER, 2022-2023

DURATION: 3 HOURS FULL MARKS: 150

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

Answer **all 6 (six)** questions. Figures in the right margin indicate full marks of questions with corresponding COs and POs in parentheses.

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1. a) Is it possible to increase the number to inputs to a NAND gate or a NOR gate to more than two, similar to AND, OR, or XOR gates? Justify your answer with proper explanation. 5 (CO1) (PO1)

   b) Consider the following Boolean function: 5 + 5 (CO1) (PO1)

   $$F(a, b, c, d) = \sum(1, 3, 4, 11, 12, 13, 15)$$

   i. Implement it using a 4:1 Multiplexer following proper steps.

   ii. Redraw the logic circuit of Question 1.b)i replacing the multiplexer with tri-state buffers.

   c) Design a combinational circuit using logic gates to implement a 4-bit magnitude comparator for binary numbers A and B. Determine the logic expressions for the following outputs: 10

   - A > B (A is greater than B)
   - A < B (A is less than B)
   - A = B (A is equal to B)

2. a) Explain *Race Around* condition in a sequential circuit with an appropriate timing diagram. Describe possible solutions to overcome this problem with proper justifications. 10 (CO1) (PO1)

   b) Design a sequential circuit using JK flip-flop which will have an external input (x), an external output (Z), and produce output, $Z = 1$ if the input sequence encounters the pattern "0110" or "101". 15 (CO2) (PO2)

3. a) Sequential circuits, with their memory, can be visualized using state diagrams. These diagrams come in various forms to best represent the circuit's behavior.

   i. Compare and contrast between Moore and Mealy Finite State Machine (FSM). 5

   ii. Convert the Finite State Diagram (FSD) in Figure 1 into the state diagram of the opposite type. 5

   iii. Verify if the converted FSD from Question 3.a)ii is further reducible or not with proper steps and justifications. 5 (CO3) (PO2)

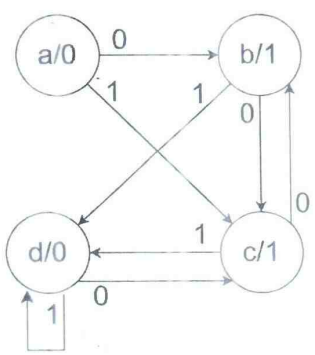

Figure 1: An FSD for Question 3.a

b) Draw a logic diagram of a 5-bit Universal register using JK flip-flop. The register must perform the following operations as the given sequence. 10 (CO3) (PO2)

i. Memory State
ii. Complement of the Current State
iii. Set State
iv. Reset State
v. Load parallel data

4. a) A switch-tail ring counter is a type of binary counter that cycles through a specific sequence of states instead of counting up or down through all binary combinations.

i. Draw a logic diagram of a 5-bit switch-tail ring counter using SR flip-flop. 5

ii. List all unused states of this counter and determine their corresponding next-state for each unused state. Show that, if the circuit finds itself in an invalid or unused state, it does not return to a valid or used state. 7 (CO2) (PO2)

iii. Modify the logic circuit drawn in Question 4.a)i so that the circuit can reach a valid state from any one of the unused states. 8 (CO3) (PO2)

b) Prove that $(x + y) \oplus (x + z) = x'(y \oplus z)$ 5 (CO1) (PO1)

5. a) Design a synchronous counter using JK flip-flop that has the following sequence: 0010, 0110, 1000, 1001, 1100, 1101, and repeat. 15 (CO4) (PO3)
Constraint: From the undesired states the counter must always go to 0010 on the next clock pulse.

b) What are the drawbacks of traditional encoders, and how can we address them to create more robust encoding methods? 10 (CO1) (PO1)

6. a) Programmable Logic Devices (PLD) are a versatile category of digital circuits that offer significant advantages in logic design. PLDs excel at implementing custom logic functions through user-configurable connections. This programmability makes them ideal for a wide range of applications where flexibility and adaptability are crucial.

i. Use an 8×4 Read-Only Memory (ROM) to create a circuit that takes a 3-bit binary number as input and outputs another binary number that represents the square of the input number. 10 (CO3) (PO2)

ii. Implement the following Boolean functions using a 3×4×2 Programmable Logic Array (PLA): 10 (CO3) (PO2)

$$F_1(a, b, c) = \sum(3, 5, 6, 7)$$

$$F_2(a, b, c) = \sum(0, 2, 4, 7)$$

b) Differentiate the following terms with proper example/figure: 5 (CO1) (PO1)

i. Synchronous and asynchronous counter
ii. Preset and clear input