ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)

ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION — SUMMER SEMESTER, 2022-2023

DURATION: 3 HOURS — FULL MARKS: 150

CSE 4621: Microprocessor and Interfacing

Programmable calculators are not allowed. Do not write anything on the question paper.

Answer **all 6 (six)** questions. Figures in the right margin indicate full marks of questions with corresponding COs and POs in parentheses.

---

1. The gaming industry is constantly evolving, demanding more powerful hardware from laptops. Being a hardware engineer at Intel, your job is to design a new high-performance laptop processor for gaming. The laptop must have the necessities - an LED display, integrated keyboard, touch-pad, webcam, built-in speakers, etc. and should be well-equipped with ports like USB ports for data transfer and an Ethernet port for network connectivity. To evaluate the performance of the laptop, you suggested calculating the frames per second (fps) in modern video game titles to be used as benchmarks.

   a) For the scenario, discuss the advantages and disadvantages of using a hybrid core architecture instead of a traditional multi-core architecture. — 8 (CO1) (PO1)

   b) Design the block diagram of the I/O system in the scenario. — 15 (CO3) (PO2)

   c) Assuming that your designed laptop gained around 20% increase in fps on most modern video game titles. What conclusions can be drawn from the statement? — 6 (CO3) (PO2)

   d) Recommend at least three advanced hardware techniques that can be utilized to further boost the performance of the designed laptop. — 6 (CO1) (PO1)

2. a) Differentiate Programmed I/O, Interrupt-driven I/O, and Direct Memory Access (DMA). — 10 (CO1) (PO1)

   b) Suppose you are sending ASCII characters from a microprocessor to an output display device. For asynchronous communication, you opted to use 1 start bit, 1 stop bit, and 1 parity bit for each character. On the other hand, synchronous communication would require an additional ASCII *synch* character to be sent after each 3 characters. Justify which serial transmission model would be more efficient in the given scenario for every 100 output characters transferred. — 10 (CO2) (PO2)

3. a) How does the architecture of Graphics Processing Units (GPUs) vary from Multi-core Microprocessors? — 8 (CO1) (PO1)

   b) Let, `stdID4` represent the last 4 digits of your student ID in hexadecimal. E.g. if your ID is `123456` then `stdID4` is `3456H`. — 3 + 9 (CO2) (PO1)

      i. Perform the following assembly instruction in binary:
      `ADD stdID4, stdID4'` where `stdID4'` is the 2's complement of `stdID4`.

      ii. Based on operation in question 3.b)i, show and explain the updated `Overflow, Sign, Zero, Auxillary Carry, Parity, and Carry` flag resister values.

4. a) Evaluate the statement: An n-core, n-thread CPU will always be outperformed by an n-core, $(n + 1)$ thread CPU, provided that the rest of the CPU specifications are the same. 5 (CO1) (PO1)

b) Two separate sets of registers i.e. segment and offset registers are required for addressing in Intel 8086 as the size of the 20-bit address bus exceeds that of the 16-bit data bus. The addressing scheme involves aggregating the two 16-bit register values into a single physical address. Propose a similar addressing scheme if the size of the address bus is increased from 20-bit to 24-bit while the size of the data bus remains the same. 15 (CO3) (PO2)

5. a) Let, `stdID2` represent the last 2 digits of your student ID in hexadecimal. E.g. if your ID is `123456` then `stdID2` is `56H`. Construct and explain the machine code for the following instructions: 7×2 (CO2) (PO1)

i. `MOV SS:stdID2 [BX], AH`

ii. `MOV CX, stdID2`

b) Decode and explain the following machine code to the corresponding assembly language instructions: 7×2 (CO2) (PO1)

i. `1110 0101; 1101 1100; 0000 0001`

ii. `0010 0110; 1000 1011; 1000 1010; 0000 0000; 1111 1011`

6. You are running a program X on your microprocessor that takes user input using an interrupt and then displays the output using another interrupt. On the other hand, you have a separate program Y that will invoke the program Y_1 using an interrupt. Y_1 will be responsible for taking user inputs using an interrupt.

a) Highlighting the user program and interrupt handler, visually compare the interrupt schemes of program X and Y. 10 (CO3) (PO2)

b) What are the limitations of the aforementioned interrupt schemes in transferring larger volumes of data? What will you use to solve the issues? $5 + 2$ (CO3) (PO2)

c) The program X is serially located in the `segment:offset` memory address from `2345:3456` to `2389:3412`. How many memory locations are occupied by program X? 10 (CO2) (PO1)

Appendix

Table 1: MOV Instruction Coding: REG Field

REG	W=0	W=1
000	Al	AX
001	CL	CX
010	DL	DX
011	BL	BX
100	AH	SP
101	CH	BP
110	DH	SI
111	BH	DI

Table 2: MOV Instruction Coding: MOD and R/M Field

RM/MOD	00	01	10	11	
				W=0	W=1
000	[BX] + [SI]	[BX] + [SI] + d8	[BX] + [SI] + d16	AL	AX
001	[BX] + [DI]	[BX] + [DI] + d8	[BX] + [DI] + d16	CL	CX
010	[BP] + [SI]	[BP] + [SI] + d8	[BP] + [SI] + d16	DL	DX
011	[BP] + [DI]	[BP] + [DI] + d8	[BP] + [DI] + d16	BL	BX
100	[SI]	[SI] + d8	[SI] + d16	AH	SP
101	[DI]	[DI] + d8	[DI] + d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX] + d8	[BX] + d16	BH	DI

Table 3: OP Codes for Various Instructions

Instruction Name	Opcode
IN	1110010
MOV (Reg, Memory)	100010
MOV (Immediate)	1011
Segment Override Prefix	001xx110