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B.Sc. in EEE, 2nd Semester May 16, 2024 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination
Course No.: EEE 4203
Course Title: Electronics I

Summer Semester, A. Y. 2022-2023
Time: 3 Hours
Full Marks: 150

There are 6 **(six)** questions. Answer all 6 **(six)** questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets.

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1. a) A designer has a supply of diodes for which a current of 2 mA flows at 0.7 V. Using a 1-mA current source, the designer wishes to create a reference voltage of 1.25 V. Suggest a combination of series and parallel diodes that will effectively achieve the desired outcome. Find how many diodes are needed. Determine the voltage that is actually achieved. **10 (CO1, PO1)**

   b) Explain the significance of small signal or incremental resistance of a diode. Discuss with an example how this resistance affects the voltage regulation across a diode for small change in supply voltage or current through the diode. **06 (CO1, PO1)**

   c) Design the circuit of the Fig. 1(c) so that V_o = 3 V when I_L= 0, and V_o changes by 20 mV per 1 mA of load current. **09 (CO2, PO2)**
      i. Use the small-signal model of the diode to find the value of R.
      ii. Find the value of I_S of each of the diodes.
      iii. For this design, use the diode exponential model to determine the actual change in V_o when a current I_L = 1 mA is drawn from the regulator.

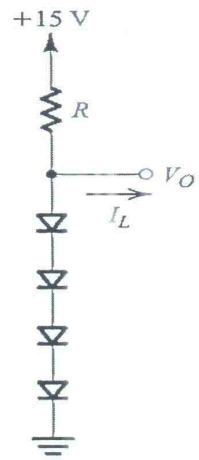

Fig. 1(c)

2. a) Deduce the large signal pi model (with voltage controlled current source) of an NPN BJT considering the fact that EBJ is forward biased and CBJ is reverse biased for active mode of operation. Extend this equivalent circuit model for the same BJT for saturation mode of operation. Find the expressions of collector current and base current. **08 (CO1, PO1)**

   b) Based on question 2(a), sketch the curve for i_c versus v_{CB} and justify i_c decreases to zero when you will move the BJT from active to deepest saturation. Formulate value of v_{CB} at the edge of saturation. **07 (CO1, PO1)**

c) For the Fig. 2(c), find the value of the voltage V_{BB} in the transistor operating in deep saturation with $\beta_{forced} = 8$. Take $V_{BE} = 0.7$ and $\beta_{min} = 30$. **10 (CO2, PO2)**

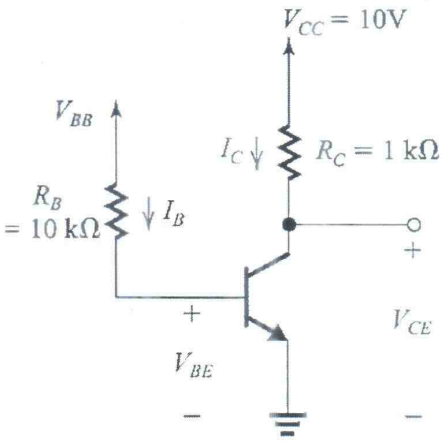

Fig. 2(c)

3. a) Analyse the following circuit given in Fig. 3(a) to determine the voltages at all nodes and the currents through all branches. Assume that the transistor β is specified to be at least 50. **12 (CO2, PO2)**

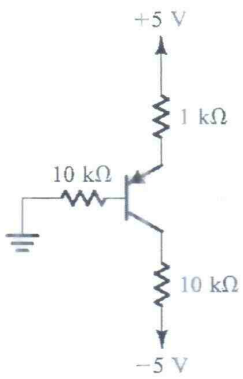

Fig. 3(a)

b) Evaluate the voltages at all nodes and the currents through all branches in the circuit shown in Fig. 3(b) with the voltage feeding the bases to +10 V. Assume that $\beta_{min} = 30$, and find V_E, V_B, I_{C1} and I_{C2}. **13 (CO2, PO2)**

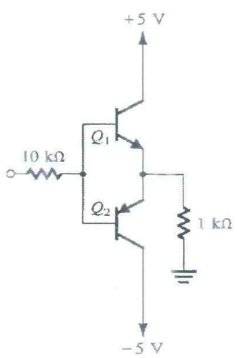

Fig. 3(b)

4. a) Sketch an n-channel enhancement-type MOSFET with the proper biasing applied (V_{DS}> 0V, V_{GS}>V_T) and indicate the channel, the direction of electron flow, and the resulting depletion region. Briefly describe the basic operation of an enhancement type MOSFET. **13 (CO1, PO1)**

b) Using the data provided in Table 4(b) and an average threshold voltage of $V_{GS(TH)}$ = 3V, **12 (CO2, PO2)**

i. Determine the resulting value of k for the N-channel enhancement type MOSFET.

ii. Sketch the transfer characteristics curve. (Show necessary calculation)

Characteristics	Symbol	Min	Max	Unit
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	$V_{GS(TH)}$	1.0	5.0	V_{dc}
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10 V)	$V_{DS(on)}$	-	1.0	V
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	-	mAdc

Table 4(b)

5. a) Show that the transconductance of the BJT is directly proportional to the collector bias current. **05 (CO1, PO1)**

b) Analyze the transistor amplifier circuit using hybrid-π model shown in Fig. 5(b) and find the following parameters. Assume β = 100 and neglect Early effect. **20 (CO2, PO2)**

i. Determine I_B, I_C, I_E and V_C.

ii. Determine the small signal model parameters, r_π, r_e, g_m.

iii. Find voltage gain A_V.

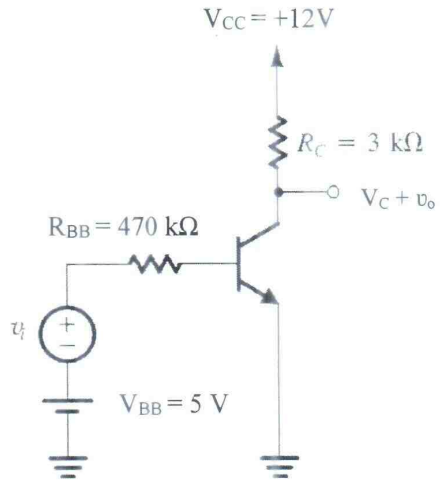

Fig 5 (b)

6. a) Show that the open circuit voltage gain of the emitter follower is unity. **10 (CO1, PO1)**

b) For the self-bias configuration of JFET shown in Fig. 6(b), **15 (CO2, PO2)**

i. Sketch the transfer curve for the device.
ii. Superimpose the network equation on the same graph.
iii. Determine I_{D_Q} and V_{GS_Q}.
iv. Calculate V_{DS}, V_D, V_G and V_S.

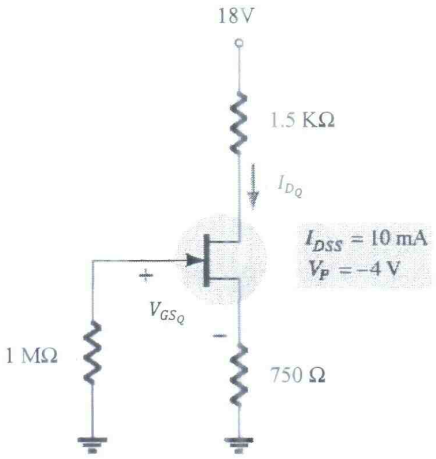

Fig. 6(b)