B.Sc. in CSE, 4th Semester May 29, 2024

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination — Summer Semester, A. Y. 2022-2023
Course No.: EEE 4483 — Time: 3 Hours
Course Title: Digital Electronics and Pulse Techniques — Full Marks: 150

There are **6 (six)** questions. Answer all **6 (six)** questions. The symbols have their usual meanings. Programmable calculators are not allowed. Marks of each question and corresponding COs and POs are written in the brackets. Assume reasonable values for any data that seems to be missing.

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1. a) Sketch the circuit diagram of a monostable multivibrator using OPAMP to generate a pulse wave where the lower voltage level is the stable state, and the upper voltage level is the unstable state. Discuss the operation of this circuit with proper wave shapes and derive an expression for the monostable timing period. If the value of the capacitor in the RC timing circuit is 4.7μF, choose the values of the resistances such that the monostable timing period is 2.5ms. (Consider 0.7V to be the voltage drop across the diode and the saturation voltage to be 15V) **16 (CO2, PO2)**

   b) For the circuit shown in Fig. 1, derive the expression of the time period of the output signal. Determine the value of the capacitor (C) to make the time period equal to 2.5ms. Determine the duty cycle of the output signal. Sketch the wave shapes of the output voltage and the voltage across the capacitor with proper scaling and labelling. **14 (CO2, PO2)**

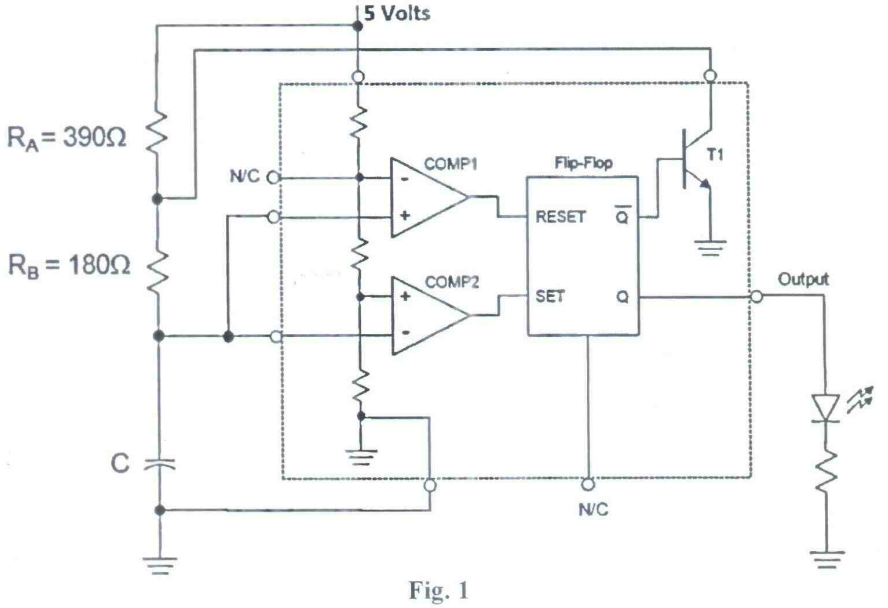

Fig. 1

2. a) Sketch the block diagram of a 5-bit successive approximation A/D converter. For this 5-bit successive approximation A/D converter; assume that the reference voltage applied to the D/A converter circuit is V_{REF} = 10V. For a particular instant of time; if an analog input voltage has the magnitude of V_{IN} = 6V, determine what will be the corresponding output bit pattern of the A/D converter after completing the conversion process? (Show the changes in the output bit pattern after each cycle of the conversion process) **15 (CO2, PO2)**

b) With proper circuit diagram, derive the expression of total conversion time of a dual slope A/D converter. Consider that a 1 MHz clock generator and a 5-bit counter are used in a dual slope A/D converter. The reference voltage is set to, V_{REF} = 7.75 V. Determine what will be the number of clock pulses counted by the counter and the binary form of the digital output, when the analog input voltage is V_{IN} = - 3.15 V, and when it is - 1.25 V? **15 (CO2, PO2)**

3. a) With suitable diagrams discuss the *Read*, *Write* and *Refresh* operation of a one transistor DRAM memory cell. **12 (CO1, PO1)**

b) Sketch the MOS-based OR ROM memory cell array to store the data given in Table 1 along the bit lines. **10 (CO2, PO2)**

Table 1

BL[0]	BL[1]	BL[2]	BL[3]	BL[4]	BL[5]
1	0	0	1	0	0
1	0	0	1	1	1
0	1	0	0	0	1
1	1	1	0	1	1
1	0	0	0	1	0
0	0	1	0	0	1

4. a) With suitable diagram briefly discuss the operation of 6T SRAM. **10 (CO1, PO1)**

b) Sketch the circuit diagram of programmable logic array corresponding to the following Boolean functions. **8 (CO2, PO2)**

$$f1 = AB + ABC'$$
$$f2 = B'C + A'BC'$$
$$f3 = A + A'B + ABC'$$

5. a) Describe which type of logic circuit is presented in Fig. 2. For this circuit, sketch the input-output characteristics curve, determine the different input & output voltage levels and noise margins. [Here, β = 50, σ = 0.85, V_{BE}(Cut-in) = 0.65V, V_{BE}(Sat) = 0.7V, V_{CE}(Sat) = 0.2V] **13 (CO2, PO2)**

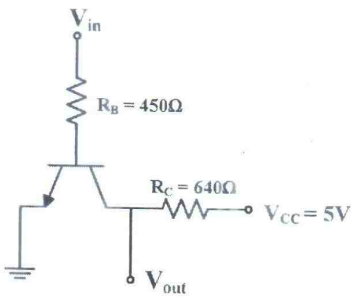

Fig. 2

b) Sketch the circuit diagram of 3 input OR gate using Diode Logic and describe it's working principle. **7 (CO1, PO1)**

c) Sketch the circuit diagram of 2 input XOR gate using CMOS logic. **5 (CO2, PO2)**

6. a) Sketch the circuit diagram of 3-input NAND gate using Diode Transistor Logic (DTL) and describe the operation of the circuit for two possible cases: **12 (CO1, PO1)**

   (i) when all the inputs are at logical '1' state

   (ii) when any one of the inputs is at logical '0' state

   (Assume reasonable values of different components for the analysis)

   b) With proper reasoning, describe how TTL gates overcome the speed limitation of DTL gates. **10 (CO1, PO1)**

   c) Describe the difference between depletion type MOSFET and enhancement type MOSFET. **3 (CO1, PO1)**