



Proposition of a new model for memristive window function through comparative analysis

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Abstract

This work presents a set of mathematical tools for the analysis and modelling of memristor devices. The mathematical framework takes advantage of the compliance of the memristor's output dynamics with the family of Bernoulli differential equations which can always be linearised under an appropriate transformation. Based on this property, a set of conditionally solvable general solutions are defined for obtaining analytically the output for all possible types of ideal memristors. To demonstrate its usefulness, the framework is applied on HP's memristor model for obtaining analytical expressions describing its output for a set of different input signals. It is shown that the output expressions can lead to the identification of a parameter which represents the collective effect of all the model's parameters on the nonlinearity of the memristor's response. The corresponding conclusions are presented for series and parallel networks of memristors as well. The analytic output expressions enable also the study of several device properties of memristors. In particular, the hysteresis of the current-voltage response and the harmonic distortion introduced by the device are investigated and both interlinked with the nonlinearity of the system. Moreover, the reciprocity principle, a property from classical circuit theory, is shown to hold for ideal memristors under specific conditions.

Based on the insights gained through the analysis of the ideal element, this work takes a step further into the modelling of memristive devices in an effort to improve some of the macroscopic models currently used. In particular, a method is proposed for extracting the window function directly from experimentally acquired input-output measurements. The method is based on a simple mathematical transformation which relates window to sigmoidal functions and a set of assumptions which allow the mapping of the sigmoidal to current-voltage measurements. The equivalence between the two representations is demonstrated through a new generalised window function and several existing sigmoidals and windows. The proposed method is applied on three sets of experimental measurements which demonstrate the usefulness of the window modelling approach and the newly proposed window function. Based on this method the extracted windows are tailored to the device under investigation. The analysis also reveals a set of non-idealities which lead to the introduction of a new model for memristive devices whose response cannot be captured by the window-based approach.

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Symbols and Abbreviations

ANN	Artificial Neural Network
CNN	Cellular Neural Network
CMOS	Complementary Metal-Oxide-Semiconductor
CMOL	CMOS/nanowire/MOLecular hybrid circuit
BDE	Bernoulli Differential Equation
LDE	Linear Differential Equation
ODE	Ordinary Differential Equation
FPGA	Field-Programmable Gate Array
mFPGA	Memristor-FPGA hybrid circuit
nFPGA	Nano-FPGA hybrid circuit
FPNI	Field-Programmable Nanowire Interconnect
HP	Hewlett-Packard
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
PLA	Programmable Logic Array
nanoPLA	Nano-Programmable Logic Array
STDP	Spike-Timing-Dependent Plasticity
THD	Total Harmonic Distortion
VLSI	Very-Large-Scale Integration
$P(t), Q(t)$	Time dependent coefficients of Bernoulli's differential equation
$I(t)$	Integrating factor for Bernoulli's differential equation
$\zeta = y^{1-n}$	Change of variable linearising Bernoulli's differential equation
$\inf_{\mathbb{R}} S$	Infimum; greatest lower bound of S in \mathbb{R}
$\sup_{\mathbb{R}} S$	Supremum; least upper bound of S in \mathbb{R}
B	Incremental capacitance; constant capacitance in the linear case

$f_C(v, q) = 0$	Constitutive relation for the nonlinear capacitor
q	Charge (temporal integral of current)
i	Current
d	Euclidean distance; used to measure model's accuracy
ϕ	Flux-linkage (temporal integral of voltage); referred also as flux
γ_m	Formula for evaluating the amplitude of harmonics; $m = 0, 1, 2, 3, \dots$
a_0, a_n, b_n	Coefficients of the Trigonometric Fourier Series; $n = 1, 2, 3, \dots$
C_0, C_n	Magnitude of n -th harmonic component; $n = 1, 2, 3, \dots$
f_j	Frequency; $j = 0, 1, 2, 3, \dots$
L	Incremental inductance; constant inductance in the linear case
$f_L(\phi, i) = 0$	Constitutive relation for the nonlinear inductor
u	Input signal
y	Integrated input
$K(k), F(\varphi, k)$	Complete and incomplete elliptic integral of the first kind
$E(k), E(\varphi, k)$	Complete and incomplete elliptic integral of the second kind
φ	Argument of elliptic integral
k	Modulus of Jacobian elliptic functions and integrals
W	Incremental memductance; constant conductance in the linear case
F	Generalised memristance of memristive system
M	Incremental memristance; constant resistance in the linear case
M	Instantaneous memristance
$f_M(\phi, q) = 0$	Constitutive relation for the nonlinear memristor
μ_v	Mobility of charge carriers
α, α_j	Model's parameter(s) of appropriate dimensions; $j = 1, 2, 3, \dots$
β	Dimensionless parameter controlling the nonlinearity of memristor
$\tilde{\beta}$	Parameter β rescaled such that $\tilde{\beta} \in (0, 1)$
$\kappa, \kappa_1, \kappa_2$	Constant of proportionality; κ_1 in dW/dt , κ_2 in dM/dt
ϑ	Binary parameter determining the state of hybrid model; $\vartheta \in \{0, 1\}$
Z	Set of natural numbers $0, \pm 1, \pm 2, \pm 3, \dots$
Z^+	Set of positive natural numbers $1, 2, 3, \dots$
Z_0^+	Set of positive natural numbers $0, 1, 2, 3, \dots$
N	Set of integer numbers $0, 1, 2, 3, \dots$
N^+	Set of integer numbers $1, 2, 3, \dots$
R	Set of real numbers
R^+	Set of positive real numbers excluding zero
y	Output signal

$\rho(t)$	Instantaneous electric power
R	Incremental resistance; constant resistance in the linear case
R_0	Initial memristance at $t = 0$
R_{OFF}	The maximum resistance value of a memristor
R_{ON}	The minimum resistance value of a memristor
$f_R(v, i) = 0$	Constitutive relation for the nonlinear resistor
S	Sigmoidal curve
L	Lower asymptote of a sigmoidal curve

y_σ	Point of inflexion of a sigmoidal curve
G	State function of memristive system
h	Function of the input signal; constituent part of state equation
z	Internal state variable/vector
z_{\max}	Value of internal state variable at which the window is maximised
w	Thickness of memristor's doped region
D	Total thickness of memristor's oxide layer
w_0	Initial thickness of doped region at $t = 0$
t	Time
x	Normalised time
v	Voltage
$H_\lambda(t)$	Bipolar piecewise linear waveform
λ	Determines rise and fall time of Bipolar piecewise linear waveform
A	Amplitude of a periodic waveform
T_0	Period of a waveform; $T_0 = 1/f_0$
$\sigma(t)$	Sinusoidal waveform
$\Lambda(t)$	Triangular waveform
f	Window function
\hat{f}	Modified window function
δ	Controls the shift of the roots in the modified window
f_{\max}	Maximum value of the window function at $z = z_{\max}$
η	Window parameter; scales the maximum of window
p	Window parameter; controls the flatness around the maximum
r	Window parameter; controls the skewness
\bar{f}	Reciprocal of a window function; $1/f(z)$
$F(z)$	Integrated reciprocal of a window function
W	Electric work

Chapter 1

Introduction

Without entering into any technical details and formal definitions this chapter will introduce the field of memristors and memristive systems, the motivation and the contributions of this project. Starting with a brief history of the memristor, the chapter introduces the concept of memristors and memristive systems in order to initiate the reader. This is followed by a short overview of the field of memristors and its applications in an effort to justify the significance of the field. From this overview two areas of the existing literature in memristors which lack behind will be identified as the motivation of this work. These two areas are: the incomplete circuit theory for the analysis of ideal memristors and the inadequate modelling of devices which fails to describe non-linearities of the device. Finally, with the aim of improving these two areas, we define a window function which will address the problem mentioned above.

1.1 What is a memristor and how it was defined

Leon Chua, a professor at Berkeley university, with his seminal 1971 paper challenged the well established perception of classical electronics that the three fundamental 2-terminal passive circuit elements are only the resistor, the inductor and the capacitor [1].

Based on simple symmetry arguments he claimed that a fourth fundamental 2-terminal passive circuit element is necessary to complement the other three. More specifically, Chua realised that out of the six possible pairwise combinations between the four fundamental circuit variables [2], namely, the current, voltage, charge, and flux-linkage, only five had been identified. He therefore postulated mathematically the *memristor* as the element relating the charge and the flux-linkage in order to establish the missing link (see Figure 2.1).

As its name indicates, the memristor (from memory-resistor) behaves similarly to a nonlinear resistor in the sense that, its current-voltage characteristic is nonlinear. In fact, instantaneously the memristor can be viewed as a resistor, however, unlike the conventional ohmic element, it is a dynamic element with memory [1]. Its memory property stems from the fact that its memristance (or simply instantaneous resistance) is determined by the entire past history of the input (time integral of the voltage or current) driving the element [3,4]. In other words, its memristance, which is measured in Ohms, encodes how much charge (for current driven), or flux-linkage (for voltage driven) has passed through the device over time. Therefore, an ideal memristor will keep changing its memristance as long as an input is applied on the component. Once the driving signal is removed, the ideal device will maintain its state indefinitely or, until the driving signal is applied again. Its intrinsic non-volatile memory property and its multiplicative transfer function give also rise to one of the qualitative characteristics of memristors, namely, the hysteretic current-voltage responses crossing the origin. An indicative example of a hysteretic current-voltage characteristic of an ideal memristor is illustrated in Figure 2.2b. This distinctive behaviour of the memristor cannot be reproduced by any combination of ideal passive resistors, inductors and capacitors. It is in this sense that Chua considers the memristor a rightful candidate for the fourth fundamental 2-terminal passive circuit element [5–7].

It is interesting to remark that the memristor is not the only proposed resistive element exhibiting non-volatile memory. For example, a decade earlier than Chua, Bernard Windrow introduced the *memistor*, a three-terminal passive transistor-like element in which one of its terminals (the control electrode) is used to adjust the resistance between the remaining two electrodes. Although the memistor is passive and exhibits non-volatile history-dependent resistance as well, it is a three-terminal element and should not be confused with the memristor, which is a 2-terminal element [8,9]. In fact, it has been recently suggested that a memistor can be built from two memristors [10].

Soon after the introduction of the memristor, Chua and his student Kang observed that systems or devices may exist which exhibit characteristics (e.g. non-volatile memory, hysteresis, zero-crossing) similar to those of memristors. However, the definition of the ideal memristor is inadequate to capture their behaviour. They therefore introduced the notion of *memristive systems* to enable the modelling of a broader class of nonlinear dynamical systems whose behaviour resembles that of memristors [6,11]. Unlike the memristor, the definition of the new generalised system allows the memristance state to depend on one or more variables which are not restricted to the charge (or flux-linkage). Thus, these systems are not limited to electronic devices since their input/output waveforms need not be current and voltage and the memristance may not have units of Ohms. This renders the memristor a special case of memristive systems which is electrically driven and its state variable, determining the memristance, is exclusively the charge or the flux-linkage.

The introduction of memristors and memristive systems suggested a new taxonomy in nonlinear circuit theory in which classical nonlinear resistors, inductors and capacitors are not sufficient for accurately modelling the behaviour of complex nonlinear circuits [6,7]. Chua and Kang demonstrated the usefulness of these new family of ideal elements by showing that a variety of different systems, such as discharge tubes, the thermistor, Josephson junctions and the Hodgkin-Huxley circuit model of the neuron, can be modelled as memristive systems [6,11,12]. Nevertheless, for almost 40 years extremely few researchers explored further the new ideas presented by Chua and Kang.

The theoretical prediction of the memristor remained unverified for several decades because its existence was suggested during a period when researchers were still experimenting with devices at the micrometre-scale. However, it is evident from the several experimental devices identified as memristive [13–18] that this behaviour is exposed on the nanometre-scale [19,20]. Although some examples of solid state devices appeared in the literature whose behaviour pointed to that of a memristor, researchers failed to identify them as such (see References [15,21–23] for several examples). The first nanoscale solid-state device recognised as a memristor was fabricated very recently, in 2008, by Hewlett-Packard (HP) Labs [13,24,25]. In an attempt to understand the source of the behaviour of their device, HP has provided a simple heuristic model which, although an extreme idealisation, has become a point of reference in the literature of memristors [13].

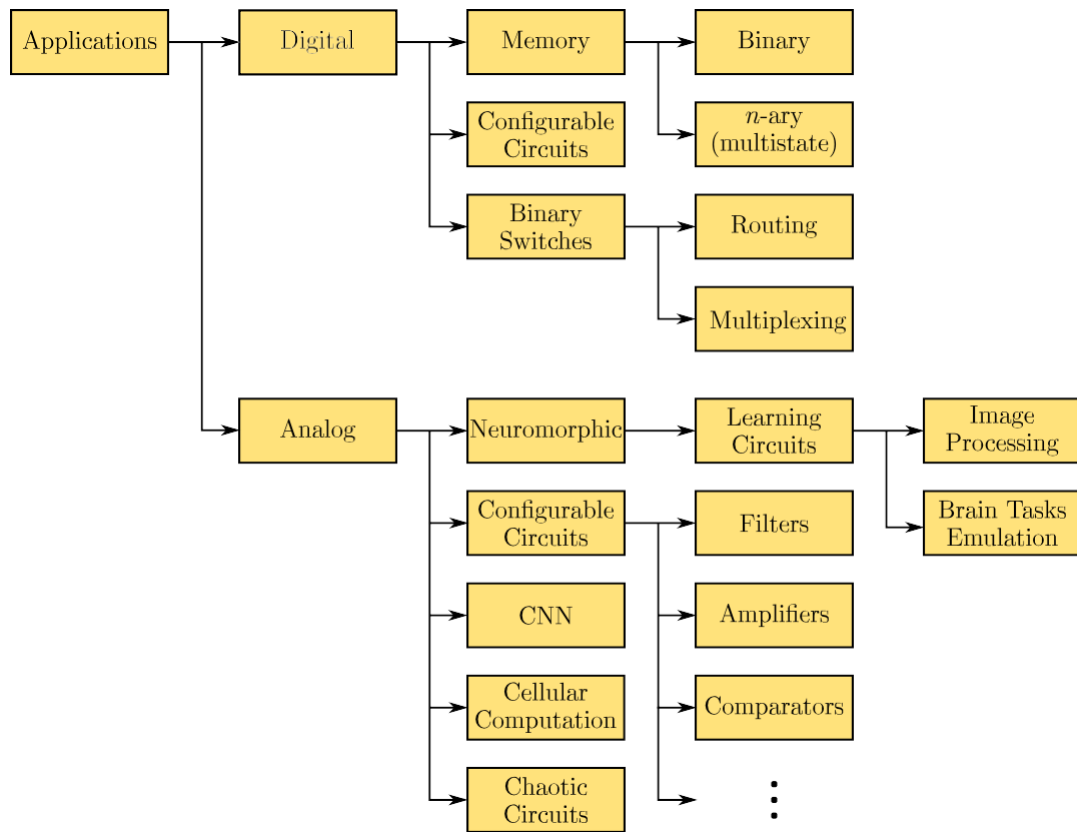


Figure 1.1: Classification of memristor’s applications: The classification is performed based on how the memristance is utilised. In digital applications, only a pre-specified number of discrete resistance levels is utilised. In analog applications, a continuous range between a minimum and a maximum resistance level is exploited.

1.2 Why is the memristor interesting: Applications

The report of the experimental realisation of the memristor by HP reignited the interest of both the scientific community and the electronics industry [21].¹ The large interest for this new element emerges from its many attractive properties (small size [15], low-power consumption [27–29], high-speed [29–31], non-volatile binary [17,32], or multistate [30,33,34], or continuous [17] resistance switching memory and synapse-like behaviour [35]) which make the memristor ideal candidate for improving the performance of already existing applications (e.g. digital memories, digital reconfigurable

logic circuits) and opening up the way for applications previously impossible to materialise (e.g. neuromorphic circuits, learning/adaptive circuits, reconfigurable analog circuits) [36,37]. Figure 1.1 presents a classification of memristors' applications based on how their memristance is utilised. The applications are explained in more detail in the following sections.

An equally important role in the large interest in memristors has played the search of the VLSI community for alternative technologies to extend the lifetime of the well established and extensively used CMOS technology. It has become clear that further scaling of CMOS transistors' gate length is becoming increasingly difficult [37–40]. One proposed solution which may prolong the use of the CMOS technology without requiring further scaling is the combination of CMOS circuits with molecular switches. Such hybrid circuits divide the functionality so that the merits of both worlds are exploited: the rich functionality offered by CMOS circuits and the nanoscale size and low-power consumption of molecular switches. In this scenario the memristor will be the element acting as the molecular switch [37,39,41,42]. In addition, the fabrication process of such nano-devices is simpler (only one critical dimension needs to be controlled) [37], cheaper [36,37] and in many cases compatible with the CMOS fabrication processes currently used in the industry [32,43,44], however, at the expense of an increased proportion of defective devices [45,46]. Nevertheless, the benefits outperform the obstacles of this approach and were not enough to hold back groups which managed to demonstrate hybrid CMOS-memristor circuits with high yield of molecular switches [30,47] and techniques to work around any remaining defects [42,48,49].

A plethora of applications taking advantage of all these unique properties of memristors have been proposed and are actively explored. Their application space can be divided into *digital* and *analog*, depending on how the range of memristance levels of the device is utilised. For digital applications, only a finite number (two for binary or 2^n for 2^n -ary, with $n = 2, 3, \dots$) of discrete resistance levels are used. On the other hand, for analog applications the continuous range of resistances between a minimum and a maximum is used, enabling true analog computation.

1.2.1 Digital Applications

The most important digital applications proposed until now may be further separated into three major categories: 1) digital memories (binary or 2^n -ary), 2) configurable/-

programmable digital logic circuits and 3) bistable switches for routing, multiplexing/-demultiplexing. All these applications are based on the same principle: a single programmable memristor acting as a switch which can be configured to two (for binary) resistance levels by applying an appropriate input pulse. If each of the two resistance levels is assigned to one of the two logical values (Logic '0' and Logic '1'), then every device becomes a binary memory cell able to store 1-bit or, a binary switch which can represent one of the two possible outcomes of a Boolean function or, simply a switch which allows or blocks the propagation of a signal [32,37,43,44,50]. Similarly, a 2^n -ary memristor can be switched to 2^n resistance levels, hence, it is able to store a n -bit value.² Therefore, what changes from one application to the other is how the discrete states are interpreted.

The area of most intensive research is digital memories and in particular binary memories. The choice of the memristor as the fundamental memory cell is motivated by its nanoscale dimensions, allowing extremely dense memories, the potential for low-energy consumption during switching and by the zero power consumption for retaining its state when idle due to its intrinsic non-volatility. More importantly the use of memristors has the potential to revolutionise the computer industry by enabling a new paradigm in which computers can be instantly switched on or off with practically zero booting times [24,51]. Many memristive devices have been reported which demonstrate the required non-volatile bistability and have been used for building small-scale binary memories [17,30,32,43,44,47,52,53], however, large-scale commercial memories have not been developed yet. Nevertheless, these early prototypes indicate the feasibility and the potential of memristor-based memories as a technology that can compete or even overpass the currently used ones. This is also backed by the recommended focus areas of the latest International Technology Roadmap for Semiconductors (ITRS 2011) [54] and the joint announcement by HP and Hynix of their plans to release into the market memristor-based memories in 2014 [55,56]. The possibility to increase even further the density of such memories is also explored by following strategies for stacking multiple layers of memristors on top of each other [53,57] with each layer containing fundamental memory cells configurable to two or more resistance levels [58]. Although progress is slow compared to binary memories, devices have been studied which are suitable for multilevel memories [30,33,34,58,59] and circuits for writing to and reading from memristor-based multilevel memories have been proposed [60].

Digital reconfigurable logic circuits is another field for which the use of memristors is investigated and promoted [19,37,43,44]. These are FPGA-like circuits consisting of a large number of general purpose computational and memory blocks. The various blocks can be wired to each other through a reconfigurable network of interconnections in order to synthesise almost any type of Boolean function to perform massively parallel application-specific computation [41,42]. To benefit from the potentially higher densities and lower power footprint, memristor-based memories can replace the currently used memory blocks. Additionally, memristors can serve as the switches at the programmable interconnections of the signal routing network between the blocks [37]. Finally, memristors can perform some of the computation provided by the functional blocks, however, fundamentally different (to conventional transistor-based logic) approaches are required to implement Boolean functions in this case [61]. The most important of the the approaches proposed are: *wired-AND logic* [43,62], *threshold logic* [63,64] and *implication logic* [61,65,66]. Implication logic is the only computationally complete³ method amongst the three. Additionally, it enables *stateful* logic where the memristors can take part in both, the computation and storage of the final outcome making this approach the most attractive [61].

In order to best utilise the advantages offered by using memristors and also overcome the challenges presented by the fact that this is 2-terminal *passive* element, fundamentally different circuit architectures need to be adopted as well [67]. The majority of architectures proposed for the digital and analog applications are based on the idea of a nano-crossbar array. Such an array consists of two stacked layers of parallel electrodes (nanowires) positioned perpendicular to each other, thus, forming a two-dimensional grid. At each point of intersection, in between the two nanowires, a thin layer of resistance switching material is placed so that each junction operates as a memristor. The two electrodes of each crosspoint serve as the two terminals of the memristor. By applying an appropriate pulse to a crosspoint device, its conductance can be independently configured or sampled [41,42,49,62,68].

Unfortunately, an integrated circuit consisting only of memristors has very limited functionality, especially when used for computation. Being passive, memristors cannot supply energy to drive subsequent parts of the circuit, they cannot offer signal amplification or restoration and other essential operations offered by the active transistors [37,68].

The dominating solution proposed to overcome this bottleneck is to augment the memristive crossbar array with a CMOS circuit layer. With this approach circuit designers can benefit from the advantages offered from both technologies: the functional flexibility and high fabrication yield of CMOS circuits and the high density, low-power consumption and non-volatile memory and programmability of memristors [37,50,68]. Many variants of this hybrid-CMOS/nanocrossbar architecture have been suggested and explored by researchers (CMOL [41,48,49,68,69], FPNI [42,44], nanoPLA [69,70], mFPGA [71] and 3D nFPGA [53,57,72–74]). Each variation results from different compromises between the design specifications and how the functionality is divided between the two layers [42].

1.2.2 Analog Applications

The digital applications for which the use of memristors is proposed is nothing extremely innovative or radically new. Most of them are well established applications for which the memristor can potentially offer a big boost in their performance hence extending their lifetime for a few more years. A far more interesting domain of applications are the analog applications which exploit the continuous range of resistances of the device [51].

The memristor compact in the dimensions of a nanoscale device useful properties and functionality (e.g. multiplicative transfer function, non-volatile and configurable resistance-memory, continuous resistance range, low-power consumption) [45]. These features enable the hardware implementation of systems whose realisation is extremely difficult using currently available technologies. The difficulties arise not because current technologies are incapable of replicating the necessary functionality, but because they cannot do so efficiently in terms of chip area and power consumption [20]. This causes problems in any attempt of scaling up the system in order to perform any useful and realistic task [75]. Initial memristor realisations have demonstrated promising results which indicate that such devices can help in overcoming these severe obstacles (for some indicative examples see References [17,25,30–32,34,35,43,44,76,77] which demonstrate all the aforementioned properties).

One of the most fascinating analog applications, which has attracted most of the attention along with digital memories, is *bioinspired* circuits and in particular *neuromorphic*. These systems employ an *artificial neural network* (ANN) which mimics a particular functionality of a biological neural network inspired from the human or other animal's

neural system to perform a certain task or computation. The ANN consists of the neurons (nodes of the network) and the synapses (edges of the network) which connected together form the neural network. The neuron applies a nonlinear function on the incoming signal and according to the result of this operation transmits signals to other subsequent neurons connected to it through the synapses. The synapse multiplies the incoming signal by its weight and, if the network is *adaptive* [76], at the same time readjusts its weight according to a nonlinear function which depends on the history of the input signal. This diverse and complex functionality of the synapse which combines non-volatile plasticity, memory and a multiplicative transfer function can be replicated by a single memristor [45]. In a realistic neural network able to perform a useful task, each neuron is connected to approximately 10^3 - 10^4 synapses. Assuming a target density of 10^6 neurons per cm^2 , it is not possible to maintain the high ratio of synapses per neuron using only conventional transistor technology due to both space and power limitations. However, using transistors to implement the relatively sparse neurons and memristors to implement the synapse, such systems may become feasible [75].

The potential of memristors enabling large-scale neuromorphic circuits has led many researchers to experiment with such systems through simulations or by fabricating actual devices. Some of the most important examples are *adaptive* or *learning* circuits [19,20,35,45,46,75,76,78–81]. These circuits implement a neural network whose synaptic weights are updated according to a learning algorithm (e.g. Hebbian [78], STDP [35,75]) which takes into account external stimulus and feedback from other interconnected neurons [19,20,45,76]. The use of memristor-based neuromorphic circuits was also demonstrated for *image's features extraction* [82]. For example, in two different studies a sequence of images was used to train a memristor-based neural network employing STDP learning to recognise the orientation of edges in a similar way to the V1 visual cortex layer of the human brain [45,75]. Another subcategory of bioinspired systems (not necessarily neuromorphic) which can benefit from memristors is *cellular computation*. Such hardware systems emulate the behaviour of biological cells. For example, the adaptive behaviour of a type of amoeba cell to environmental changes was simulated with a passive network incorporating a memristor [83]. Finally, a regular grid of memristors was used to determine the solution to a maze problem in an effort to show massively parallel computation using memristors [84].

The analog applications do not stop only at the more exotic neuromorphic circuits. Conventional analog circuits can benefit by including memristors in their setup. In such circuits the memristor can act as a configurable resistor which is operated normally at

low voltages/currents (below a threshold) and programmed using high voltage/current pulses (above a threshold) [85]. As a result, circuits become partially configurable and thus able to adapt to a range of different requirements or conditions. In this way the need of rebuilding the whole circuit for a range of different specifications is eliminated [86]. Analog programmable circuits have already been explored theoretically, mostly through simulations. Some representative examples are: analog filters [23], gain amplifiers [85–87], threshold comparators [85], switching thresholds Schmitt triggers [85] and frequency relaxation oscillators [85]. In all these examples, features of the circuit such as, their bandwidth, gain, threshold and oscillation frequency, were configured, within a certain range, by adjusting the resistance of the memristor(s) accordingly. Other circuits have been also reported which make use of the memristor as an analog memory cell (e.g. signal correlator [88,89]) or simply take advantage of its nonlinearity to improve some performance factors (e.g. extending the linear range of a differential amplifier [90]).

Finally, two other major fields of analog electronics which explore the use of memristors are *chaotic oscillators* and *cellular neural networks* (CNN). Several studies exploit the dynamical and nonlinear behaviour of the memristor in circuits for generating chaotic behaviour [91–96], with an important proportion of them being based on Chua’s modified circuit [94–96].⁴ Such circuits can be potentially used in cryptography and communications [93,97]. Similarly, the community of CNNs is trying to benefit by using memristors to implement the template weights, memory and logic used in these networks [21,98–100]. However, in both areas the work presented until now is theoretical and limited to software simulations (with the exception of Reference [93] which uses hardware emulation). Thus the feasibility of these attempts is yet to be proven in practise.

1.3 Motivations and Contributions

The potential for the commercialisation of many of the aforementioned applications has led to numerous attempts to fabricate memristor devices based on different material combinations. Depending on the application targeted, each experimental attempt was aiming at optimising some performance specification such as read/write speed [29–31], endurance, retention time, ON/OFF resistance ratio [30,32,47], number of discrete

resistance levels [30,33,34], a continuous range of resistance levels [17], power consumption [27–29] and compatibility with standard fabrication processes [32,43,44]. These efforts have resulted to the identification of a wide range of resistance switching devices demonstrating memristive behaviour. In all cases the resistance change, from the high to the low resistance level and vice-versa, is electrically induced (i.e. by applying an appropriate voltage/current pulse). However, the detailed underlying physical mechanisms responsible for these permanent changes vary significantly and are still the subject of active research since they are not well understood [14–16,101]. Indicative examples, out of the several published, range from oxide-based [13,25,27,28,31,33,34,77,102–105], phase-transition [106], single-component nanowires [107], amorphous materials [17,30,35], spintronic [108–111] and nanoparticle assemblies [112]. A few of these studies go a step further, beyond just fabrication, to investigate [25,47,102,113–115] and model [13,77,116–120] the underlying physical mechanisms that give rise to the observed behaviour. The extremely small dimensions and the diverse physical phenomena make this process difficult. As a result, the physical models presented until now have limited applicability and are only relevant to the specific device under consideration. Thus, until a standardised memristor technology is established and well modelled [75,85,121], researchers have turned to the use of macroscopic models which approximately capture the input-output dynamics without looking at the microscopic detail [7,25,67,80,100,121–126].

Despite the remarkable activity and progress in the field of memristors, it should be clear from the above discussion that research is mainly focused on the fabrication of memristors and their use in applications. A very limited amount of efforts is dedicated to the analysis and understanding of the properties and behaviour of the ideal element. This approach has generated a large gap on the theoretical front of memristors. Unlike other conventional elements, there is no well established circuit theory for studying memristors as individual elements or, as part of a larger network of memristors which may include other conventional circuit elements. The theory on memristors is limited to the original papers [1,6,11]. As a result, a big challenge in the effort to understand, and hence optimally design, memristors still remains the development of a general mathematical framework for their analysis that goes beyond mere computational simulations.

Motivated by this lack of tools for the analysis of memristors, a mathematical framework has been introduced which can provide analytic solutions for their input-output dynamics and facilitate the study of their properties. The framework is based on the compliance of the ideal memristor's dynamics with *Jacob Bernoulli's* differential equa-

tion, a classic nonlinear equation which is always linearisable, under an appropriate transformation [127]. Based on this property, a set of conditionally solvable general solutions have been defined for obtaining analytically the output as an explicit function of the input for all possible types of ideal memristors. This formulation provides a powerful and systematic methodology for the analysis, characterisation and design of devices governed by Bernoulli dynamics that does not rely on computationally expensive sweeping of parameters.

The usefulness of this formalism was demonstrated using HP's ideal memristor model as an example. In particular, by applying the mathematical framework analytic expressions were obtained for the model's output as an explicit function of the input for a set of widely used input waveforms, namely, the sinusoidal, triangular and bipolar piecewise linear. The analytic output expressions have revealed that the model's parameters of diverse origin (material, fabrication, input) can be combined into a single quantity which collectively determines the nonlinearity of the memristor's dynamics and hence its device properties. These results have been extended further for series and parallel networks of memristors. More specifically, analytic expressions were obtained describing the output of a series or parallel network of memristors characterised by HP's model. These expressions were also used to study the effect of series parasitic resistance.

The analysis of the output expressions has also provided useful insights into important properties of the memristor such as the hysteresis of the current-voltage characteristic curves and the harmonic distortion introduced at the output by the device. Both of these properties were related to the nonlinearity of the memristor through the identified parameter which governs its behaviour. Moreover, based on HP's memristor, two general memristive models were defined. Their output response is evaluated analytically using the framework and it is discussed under which conditions they give rise to a memristor. The discussion reveals a family of functional forms which will lead to a memristor. The study of the ideal memristor's properties concludes by looking at its compliance with the *reciprocity principle* [128,129]. It is shown that ideal memristors behave as reciprocal elements if certain requirements are satisfied. The property is demonstrated using the analytical output expressions obtained for HP's model and it is also extended to series and parallel networks of memristors.

Another issue which was implied by the previous discussion, is the lack of universal models for describing the behaviour of fabricated devices. Such models are difficult to obtain because of the diverse phenomena, between different devices, that give rise

to memristive behaviour and also because a standard memristor technology has not been established yet in the market. As a result research groups studying memristors, especially the ones with no access to a real device, resort to macroscopic models which attempt to approximately capture the device dynamics. The most common approach followed when defining such macroscopic models is the use of a *window function* [7,13, 121–123]. These are empirical functions which attempt to model the nonlinear dynamics of the internal state variable of the memristor. The problem is that in most cases these functions have been arbitrarily defined without any relevance to experimental input-output measurements.

With the aim of improving the window functions currently used, and consequently the macroscopic models, an alternative way of using experimental current-voltage measurements has been suggested which can help in acquiring an improved and more suitable window function for the device under consideration. The method applies to a certain class of memristors whose resistance state follows a *sigmoidal curve* with respect to the charge or flux (integrated current or voltage). It is shown that such sigmoidal curves can be easily obtained from experimental measurements and converted to a corresponding unique window function by applying a simple mathematical transformation. Based on these observations, an experimental procedure was suggested through which a more appropriate window function can be obtained.

The proposed procedure for extracting the window is tested using experimentally obtained measurements from real devices reported in the literature as memristors [17,34, 107]. For some of the datasets, the analysis revealed an underlying sigmoidal, verifying the relevance of the window-sigmoidal modelling approach. For some other datasets, it was shown that, although an underlying sigmoidal was not identified, it was still possible to approximate their response using simpler models such as HP's. For these models the analysis has identified additional factors which must be taken into account during the modelling of such devices. These factors have led to the introduction of a new memristive model which describes the observed responses more accurately. Finally, the ideality of these devices was discussed, concluding that many fabricated devices are mistakenly referred to as memristors rather than memristive systems. Nevertheless, it is suggested that the theory for ideal memristors can still be applied to such devices, verifying the significance of studying the ideal component. The understanding developed for the behaviour and properties of the ideal memristor was crucial during the analysis of the fabricated devices.

Chapter 2

Background Theory

Chapter 1 introduced informally the reader to the concept of memristors and memristive systems and presented an overview of the field highlighting two major gaps in the literature which have constituted the motivation behind this project. This chapter presents more formally the two notions and the background theory which will form the basis for understanding the results discussed in the subsequent chapters. The chapter begins by explaining the symmetry arguments on which the memristor was originally postulated. This is followed by the formal definitions of memristors and memristive systems and a discussion of some of their fundamental properties and characteristics. Then, a detailed description is given of HP's ideal memristor model which will be used extensively in Chapter 4 as the example model to demonstrate the mathematical framework introduced in Chapter 3. Following HP's model, the window function modelling approach is introduced, together with some of its most important examples, as one of the major methods used to model the nonlinear dynamics of the internal state variables of memristive systems. In Chapter 5, a new generalised window function will be proposed combining all the features of the examples presented here and introducing additional flexibility. Finally, the chapter concludes by discussing some practical issues which arise when window functions are used in practice and the preferred approach for avoiding them is presented.

2.1 Memristors and Memristive Systems

2.1.1 How the memristor was defined

Consider the four fundamental circuit variables which according to elementary circuit theory are the: voltage v , current i , charge q , and flux-linkage ϕ [5]. There are six distinct relations linking these variables pairwise (see Figure 2.1). Two of these relations correspond to the definitions of charge and flux-linkage as time-integrated variables:

$$q(t) = \int_{-\infty}^t i(t) dt \quad (2.1)$$

$$\phi(t) = \int_{-\infty}^t v(t) dt \quad (2.2)$$

with q_0 and ϕ_0 the initial charge and flux at $t = 0$. Three other links are given by the implicit equations that define the constitutive laws of the generalised nonlinear fundamental circuit elements:

$$f_R(v, i) = 0 \quad \text{for the resistor } R, \quad (2.3)$$

$$f_C(v, q) = 0 \quad \text{for the capacitor } C, \quad (2.4)$$

$$f_L(\phi, i) = 0 \quad \text{for the inductor } L. \quad (2.5)$$

In order to complete the symmetry of the system-theoretic structure, Chua's insight was to postulate that the remaining link between q and ϕ should be completed by another constitutive relation:

$$f_M(\phi, q) = 0, \quad (2.6)$$

which would correspond to a missing element: the *memristor*. In this sense, the memristor complements the other three fundamental circuit elements as the fourth ideal passive two-terminal component [1,3,6].

2.1.2 The memristor

A memristor, by definition, is a 2-terminal electronic element characterised by the constitutive relation $f_M(\phi, q) = 0$ relating the charge q and the flux ϕ , where q and ϕ are given by (2.1) and (2.2) respectively [1]. Stating this more simply, the memristor is an element whose input-output response is uniquely determined by a charge-flux ($q - \phi$)

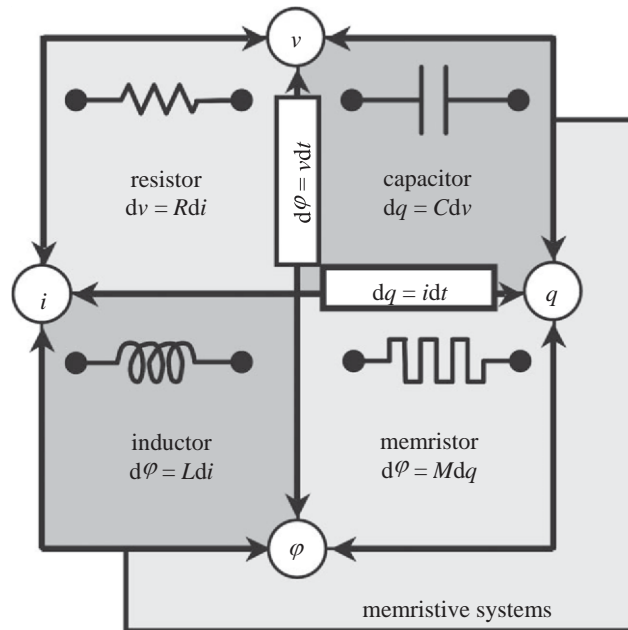


Figure 2.1: The symmetry arguments based on which the memristor was defined. The diagram shows the six possible binary relations between the four fundamental circuit variables (current i , voltage v , charge q and flux ϕ). The two first relations are given by the definition of q and ϕ as the time integral over i and v respectively. The remaining four relations give rise to the four fundamental 2-terminal passive circuit elements: the resistor \mathbf{R} (relates v and i), the capacitor \mathbf{C} (relates q and v), the inductor \mathbf{L} (relates ϕ and i) and the memristor \mathbf{M} (relates q and ϕ). The last relation between the q and ϕ is the one identified by Chua [1]. The symbol of each circuit element is also presented. To highlight that these are the generalised nonlinear components, their symbol is enclosed in a rectangle with its negative terminal indicated by a thicker edge. Adapted from Reference [13].

curve. The memristor is classified as *ideal* and *passive* if its $q - \phi$ curve satisfies the following properties [1,2,130]:¹

2-1.1 unique

2-1.2 nonlinear

2-1.3 continuously differentiable

2-1.4 strictly monotonically increasing.

Figure 2.2a shows a $q - \phi$ curve satisfying the criteria listed above and therefore representing an ideal passive memristor. Its corresponding current-voltage ($i - v$) response is shown in Figure 2.2b when the device is driven by a sinewave input.

The memristor is referred to as *charge-controlled*, or *flux-controlled* if its constitutive relation (2.6) can be re-expressed as an explicit function of q or ϕ respectively:

$$\phi = \hat{\phi}(q) \quad \text{for the charge-controlled,} \quad (2.7)$$

$$q = \hat{q}(\phi) \quad \text{for the flux-controlled.} \quad (2.8)$$

By assuming ideal memristors, (2.7) and (2.8) satisfy the properties (2-1.1)-(2-1.4) hence it can be shown that they are the inverse of each other:

$$\hat{q}^{-1}(q) = \hat{\phi}(q) \quad \Leftrightarrow \quad \hat{\phi}^{-1}(\phi) = \hat{q}(\phi). \quad (2.9)$$

Differentiating (2.7) and (2.8) with respect to time t , results in:

$$\frac{d\phi}{dt} = \frac{d\phi}{dq} \frac{dq}{dt} \quad \text{for the charge-controlled,} \quad (2.10)$$

From (2.1) and (2.2), $dq/dt = i$ and $d\phi/dt = v$ respectively. Replacing these into (2.10) and (2.11) results in the representation of the memristor on the $i - v$ plane. For the charge-controlled case it is given by:

$$v = \mathbf{M}(q)i(t), \quad (2.11)$$

where $\mathbf{M}(q) = d\hat{\phi}(q)/dq$ is the *incremental memristance*² measured in Ohms (Ω) and corresponds to the gradient of the $q - \phi$ curve at an operating point (OP) $Q(q_a, \phi_a)$ as illustrated in Figure 2.2. Similarly, for the flux-controlled case, the $i - v$ representation is given by:

$$i = \mathbf{W}(\phi)v(t), \quad (2.12)$$

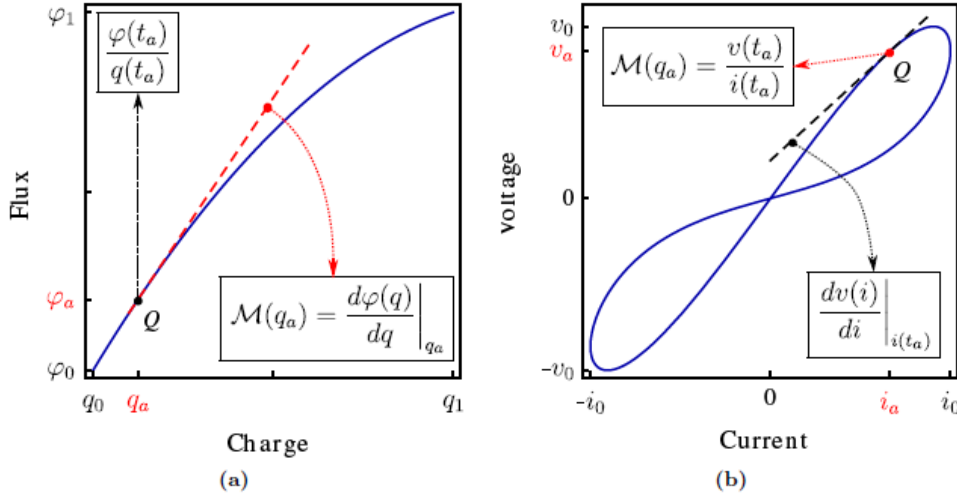


Figure 2.2: (a) An ideal $q-\phi$ curve satisfying the criteria (2-1.1-2-1.4) and (b) its $i-v$ response under a sinusoidal excitation. In both figures the same operating point (OP) $Q(q_a, \phi_a)$ is shown. At Q in (a) the instantaneous memristance $\phi(t)/q(t)$ and the incremental memristance $\mathbf{M}(q) = d\phi(q)/dq$ are shown. For the same OP (b) shows the instantaneous resistance $v(t)/i(t) = \mathbf{M}(q)$ and the incremental resistance $dv(i)/di$. The incremental memristance is equal to the instantaneous resistance when evaluated at the same OP. However, all four quantities will be equal with each other only if the $q-\phi$ curve becomes linear. In this case the memristor is indistinguishable from a linear resistor.

Moreover, restricting the memristors to ideal allows the substitution of (2.9) in (2.12):

$$\mathbf{M}(q) = \mathcal{LW}(\hat{q}^{-1}(q)) \quad \Leftrightarrow \quad \mathbf{M}(\hat{\phi}^{-1}(\phi)) = \mathcal{LW}(\phi). \quad (2.13)$$

Hence, for an ideal memristor the distinction between charge- and flux-controlled is just a mathematical formality. In practise, such an element should have a unique description (i.e. $q-\phi$ curve) irrespective of whether it is driven by a voltage or current input [19].

Equations (2.12) and (2.13) provide a more convenient route for accessing the memristance of a device especially in an experimental setup where the current and voltage are easier to measure. It is important to have in mind though that, the $i-v$ response changes when the memristor is driven by a different input signal. Therefore, the $i-v$ curves, such as the one shown in Figure 2.2b, cannot be used to predict the output of the device. The memristor's response is uniquely defined by its characteristic $q-\phi$ curve for any type of excitation.

Limiting Linear Characteristics: *A passive memristor driven by a periodic waveform degenerates to a linear resistor as the excitation frequency increases towards infinity.*

This property is illustrated in Figure 2.3 which shows that the area enclosed by the hysteretic loops decreases as the frequency increases until the $i - v$ response collapses to a straight line representing the limiting linear resistor [11,21]. On the other hand, an ideal memristor under a dc-bias should eventually settle to one of its two limiting memristances (R_{ON} or R_{OFF}). The final settling value of the memristance depends on the polarity of the bias [11,19].

Closure Theorem: *A one-port⁴ containing only memristors is equivalent to a single memristor [1,6].*

Existence and Uniqueness Theorem: *Any network containing only strictly passive memristors has one, and only one, solution [1,2].*

The combination of these two theorems shows that a network of strictly passive memristors is equivalent to a single and unique memristor. This will form the basis which will enable in Chapter 4 the expression of the output of a network of memristors as an explicit function of its input.

Based on the insights presented in the above discussion it is now easier to justify the conditions (2-1.1-2-1.4) imposed on the $q - \phi$ curve for an ideal memristor [1,2,130,131]:

- *unique:* This is necessary so that the memristor responds in exactly the same way irrespective of the type of waveform applied on the device. Assuming the same initial conditions (q_0, ϕ_0), it ensures that a certain amount of charge (or flux) flowing through the element causes always the same change in the memristance.
- *nonlinear:* The nonlinearity of the $q - \phi$ differentiates the memristor from a linear resistor. From (2.10) (or (2.11)) the memristance is equal to the slope of the $q - \phi$

curve. Therefore, a linear $q - \phi$ would correspond to a device with a constant memristance which, from (2.16), will be indistinguishable from a constant linear resistor.

- *continuously differentiable*: This property ensures that the gradient, which represents the memristance, is uniquely defined at every point along the $q - \phi$ curve and it is finite ($\mathbf{M}(q) < +\infty, \forall q$).
- *strictly monotonically increasing*: The strict monotonicity is imposed so that the $q - \phi$ curve always has a unique inverse such that (2.9) holds with the implications already explained above. Additionally, it makes sure that the memristance is positive and non-zero in order to guarantee strict passivity. A direct consequence of these restrictions is that the $q - \phi$ curve of an ideal memristor must be a one- to-one function. It is important to remark that, the *uniqueness* requirement is implied from this condition. Nevertheless, *uniqueness* was separately stated to highlight its importance. Similarly, the strict sense of this condition, even if not explicitly imposed, it is implied from *continuously differentiable*.

Finally, all the conditions together ensure that the constitutive relation (2.6) can be re-expressed both as an explicit function of q and ϕ as in (2.7) and (2.8) respectively.⁵

2.2 HP's ideal memristor model

The successful fabrication of HP's memristor is an important milestone in the timeline of memristors. The publication reporting its fabrication reignited the interest of the scientific community on the subject and also provided a simple but elegant ideal memristor model which has become a point of reference in the field [13]. Although this model describes an idealised memristor without detailed consideration for the underlying physical mechanisms, it can still reproduce the fundamental constitutive characteristics of a memristor's behaviour over a range of conditions. Indeed, both experimental $i - v$

measurements [35] and theoretical predictions from more detailed models [116] show close resemblance to the responses of the HP model. Therefore, the HP model provides a simple, yet useful approximation, which is valid over given regimes or when a detailed description is unwarranted. The modelling ability of HP's memristor will be investigated further in Chapter 5 using experimental measurements from fabricated devices.

Because of its simplicity and its widespread use, this model will be extensively studied and analysed in Chapter 4 by applying the mathematical framework developed in Chapter 3. It is therefore, introduced here together with a simple description of the underlying operation of the device. Additionally, based on the theory presented in the previous sections, it is shown why this model can be classified as an ideal passive memristor.

Having as an illustration Figure 2.4, the actual device consists of a thin-film semiconductor of TiO_2 (Titanium dioxide) with thickness D placed between two metal contacts made of Pt (Platinum) to form a metal/oxide/metal structure. The oxide film is divided into two regions: a doped region of thickness w with low resistance R_{ON} due to the high concentration of dopants (positive oxygen ions) and an undoped region with thickness $(D - w)$ and high resistance R_{OFF} . The total resistance of the film is modelled by the weighted sum of two variable resistors in series with the first one (R_{ON}) representing the doped region and the second (R_{OFF}) the undoped. The ratio between the two is controlled by the position of the boundary between the doped and undoped regions which determines the value of w . Because of the extremely small dimensions of the device, when a voltage is applied a very strong electric field develops. This causes the oxygen vacancies to move towards (Figure 2.4c) or away from (Figure 2.4b) the doped region effectively changing the position of the boundary between the two regions and hence the total resistance of the device [13].

Assuming ohmic electronic conductance and linear ionic drift with average vacancy mobility μ_v , the device is modelled by the following pair of equations [13]:

$$\dot{w} = i(t) \frac{\mu_v R_{ON}}{D} \quad (2.14)$$

Integrating (2.25a) with respect to t yields:

$$w = \mu_v \frac{R_{ON}}{D} q(t), \quad (2.15)$$

which reveals one of the basic assumptions of the model, namely, that the width of the doped region is proportional to the amount of charge that passes through the device. Models, like HP's, in which the rate of change of the internal state variable is a linear function of the input (i.e. $\dot{z} = \kappa u(t)$), will be referred to as *linear models*.

A comparison of HP's model with (2.20) shows that it actually complies with the definition of the current-driven memristive system with w acting as the internal state variable. However, inserting (2.26) in (2.25b) eliminates the internal state variable w and brings (2.25b) in a form complying with the current-driven charge-controlled memristor:

$$v = M(q)i(t) = \left[R_{off} + (R_{on} - R_{off}) \frac{\mu_v R_{on} q}{D^2} \right] i(t) \quad (2.16)$$

This is an example of a 'hidden memristor' case as described in the previous section. Reducing (2.25) in the canonical form of a memristor is not conclusive as to whether the model represents an ideal memristor or not. Because memristors are uniquely defined on the $q - \phi$ plane, one needs to evaluate the $q - \phi$ representation of (2.27) first, by applying (2.24) and then verify whether the conditions (2-1.1)-(2-1.4) are satisfied. Applying (2.24) on (2.27) gives the charge-controlled representation of the model:

$$q(\phi) = \left[R_o + \frac{\mu_v R_{on}}{D^2} (R_{on} - R_{off}) \frac{q^2}{2} \right] \quad (2.17)$$

Evaluating its inverse gives the flux-controlled representation:

$$q(\phi) = \frac{-R_{on} D^2 \pm D \sqrt{R_o^2 D^2 + 2\mu_v R_{on} (R_{on} - R_{off}) \phi}}{\mu_v R_{on} (R_{on} - R_{off})} \quad (2.18)$$

As shown in Figure 2.5a, equation (2.28) satisfies all the conditions for an ideal passive memristor except monotonicity, hence, its inverse (2.29) which is shown in Figure 2.5b is not uniquely defined. However, if the operation of the model is restricted within the strictly increasing region of $\phi(q)$, as indicated by the solid line sections of the curves in

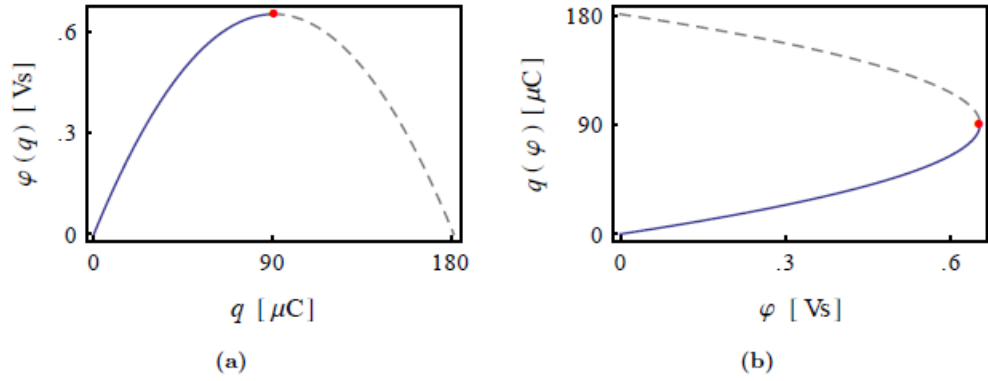


Figure 2.5: (a) A plot of the flux with respect to the charge, $\varphi(q)$, as given by (2.28) and (b) its inverse, $q(\varphi)$, as given by (2.29). It is clear from (a) that (2.28) violates the requirement (2-1.4) for monotonicity, hence its inverse cannot be uniquely defined. In fact, it is a double valued function of φ . Therefore, $\varphi(q)$ will represent an ideal passive memristor only if the operation of HP's model is limited within its strictly increasing region as indicated by the solid line in (a). This results to a unique inverse, indicated by the solid line in (b). Parameters used: $i = i_0 \sin(\omega_0 t)$ with $i_0 = 100 \mu\text{A}$ and $\omega_0 = \pi$, $\mathcal{R}_{ON} = 100 \Omega$, $\mathcal{R}_{OFF} = 16 \text{k}\Omega$, $\mu_v = 10^{-14} \text{ms}^{-1} \text{V}^{-1}$, $D = 10 \text{nm}$ and $w_0/D = 0.1$.

Figure 2.3, represents an ideal passive memristor. For the parameters reported by HP for their device [13], and by limiting operation such that $0 \leq w \leq D$ and $\mathcal{R}_{ON} \leq \mathbf{M}(q) \leq \mathcal{R}_{OFF}$, the model satisfies all the criteria for an ideal passive memristor. Therefore, the flux-controlled representation (2.29) can be uniquely defined and will be given by the solution with the positive branch of the square root.

Chapter 3

Different models of window function

3.1 Unsuitable window functions

The memristor model introduced by HP and discussed in the previous section assumes that the memristance in (2.25b) varies linearly with the internal state variable w which represents the width of the doped region (see Figure 2.4). This assumption is not very restrictive since any nonlinearities can still be accounted for by the dynamics of the internal state variable in (2.25a). However, from (2.25a), the original model assumes linear ionic drift, namely, that the position of the boundary changes linearly with the input. In general, the second assumption does not reflect reality. There is clear evidence that the vacancy drift is highly nonlinear especially close to the two boundaries of the device [13,25,77,116,117,124]. This renders the model unsuitable for detailed

modelling of most practical devices.

As discussed in Chapter 1, due to the diversity of resistance switching devices found and their extremely small dimensions which make them difficult to study, a universal detailed physical model based on the underlying physical mechanisms is difficult to obtain, especially with no standardised memristor technology in place [75,121,125]. To avoid this problem, the group at HP introduced the so called *window function* approach in which an empirical macroscopic function is used with the aim of modelling the nonlinear ionic drift observed at the boundaries of their fabricated device [13]. The simplicity of this approach motivated several groups to follow the same trend by introducing other window functions offering different and improved properties [7,121–123]. Because the majority of groups working on memristors and their applications have no access to a real device, the window approach provides a convenient alternative description for use in their modelling [121,125,133].

The window functions discussed next comply with the following general properties:⁷

3-1.1 $f : [0, 1] \rightarrow [0, 1]$,

3-1.2 $f(0) = f(1) = 0$,

3-1.3 single maximum $f(z_{\max}) = 1$.

These properties essentially describe a strictly concave [134] function for $z \in [0, 1]$ which is increasing from its first root at $z = 0$ until the maximum at $z = z_{\max}$ and then decreasing until the second root at $z = 1$. In practice a window function satisfying these specifications results to z being maximised at $z = z_{\max}$ and minimised as $z \rightarrow 0$ or $z \rightarrow 1$.

The models also assume that the memristance, $M(z)$, is equal to the weighted sum of two resistances, the maximum (R_{OFF}) and the minimum (R_{ON}) resistance values to which the device can be configured. The ratio between the two resistances is determined by the value of the internal state variable z . Therefore, the effective resistance of the device is a linear function of z and is described by:

$$M(z) = zR_{\text{ON}} + (1 - z)R_{\text{OFF}}, \quad (3.1)$$

in exactly the same way as it was defined for HP's ideal memristor in (2.15) [13]. By modelling the memristance as in (2.12) the memristive character of the system will be reflected in the dynamics (2.13a) of the state variable z .

The first window function was introduced by the group at HP and it has the following form [13]:

$$f(z) = z(1 - z), \quad (3.2)$$

with $z = w/D$ as in (2.25). This was incorporated as a factor in the state equation of the original model (2.25a), resulting to the modulated dynamics of w :

Equation (2.33) was subsequently generalised by Joglekar and Wolf to [7]:

$$f(z; p) = 1 - (2z - 1)^{2p}, \quad (3.3)$$

where $p \in \mathbb{Z}^+$. Unlike Strukov's *et al* window in (2.33) which assumes nonlinear drift everywhere in the range of $z \in [0, 1]$, (2.35) is able to model both the linear drift around the midrange of z and the nonlinear drift close to the boundaries using the control parameter p . This parameter changes the flatness of the curve around its maximum, which occurs at $z_{\max} = 1/2$. Figure 2.6 illustrates the behaviour of (2.35) for some representative values of p . It is clear that as p increases, $f(z; p) \approx 1$ for a larger range of z which corresponds to linear drift. In terms of the model's response, a higher p value

represents a device which requires a smaller amount of charge (or flux) to be injected in order to reach saturation

Prodromakis *et al* suggested a revised version of (2.13) with similar properties [122]:

$$f(x) = 1 - ((x - 0.5)^2 + 0.75)^{2p} \quad (3.4)$$

The difference of this window function is that it allows the maximum f_{\max} to take any value between 0 and 1. The value of the maximum, which again occurs at $z_{\max} = 1/2$, as well as the flatness around it, are controlled by the parameter $p \in \mathbb{R}^+$. The parameter $\eta \in \mathbb{R}^+$ is a scaling factor used to compensate for the situations where $f_{\max}(z_{\max}) \neq 1$. The behaviour of this window function is illustrated in Figure 2.7.

It is important to note here that the resulting $q - \phi$ curves for both window functions, (2.35) and (2.36), satisfy the requirements for an ideal passive memristor (2-1.1-2-1.4). The $q - \phi$ curves of the two windows are shown in Figure 2.6 and Figure 2.7 respectively. As an example, Appendix B presents the detailed steps for obtaining the voltage output and its $\phi(q)$ function for HP's model using the window in (2.33). This procedure will be discussed in more detail in Chapter 5 through sigmoidal functions.

Finally, the parameters used for generating Figures 2.6, 2.7 and 2.8 are the following:

$i = i_0 \sin(\omega_0 t)$ with $i_0 = 0.3 \text{ mA}$ and $\omega_0 = \pi/4$, $h(i) = \alpha i(t)$ where $\alpha = \mu_v R_{ON} / D^2$, $\mu_v = 10^{-14} \text{ ms}^{-1} \text{ V}^{-1}$, $D = 10 \text{ nm}$, $R_{ON} = 50 \Omega$ and $R_{OFF} = 2.5 \text{ k}\Omega$.

3.2 Practical implementation issues

The models resulting by incorporating the above window functions will suffer from two major issues, namely, the *terminal state problem* and the *accumulation* of charge (or flux). The first one arises specifically when using the type of window functions presented here, while the second issue is more general and may appear in any model. Any practical implementation of such models needs to have a strategy for overcoming both of these obstacles [22, 121, 125, 126, 133].

The *terminal state problem* stems directly from the specifications (2-2.1)-(2-2.3) imposed on the window functions and in particular (2-2.2). Due to this property, if the initial condition is chosen to be $z(0) = z_0 = 0$ or 1, then the model will remain at z_0 indefinitely irrespective of any subsequent input applied [22, 121]. The consequence of this limitation is that the model cannot have as initial resistance state any of the two

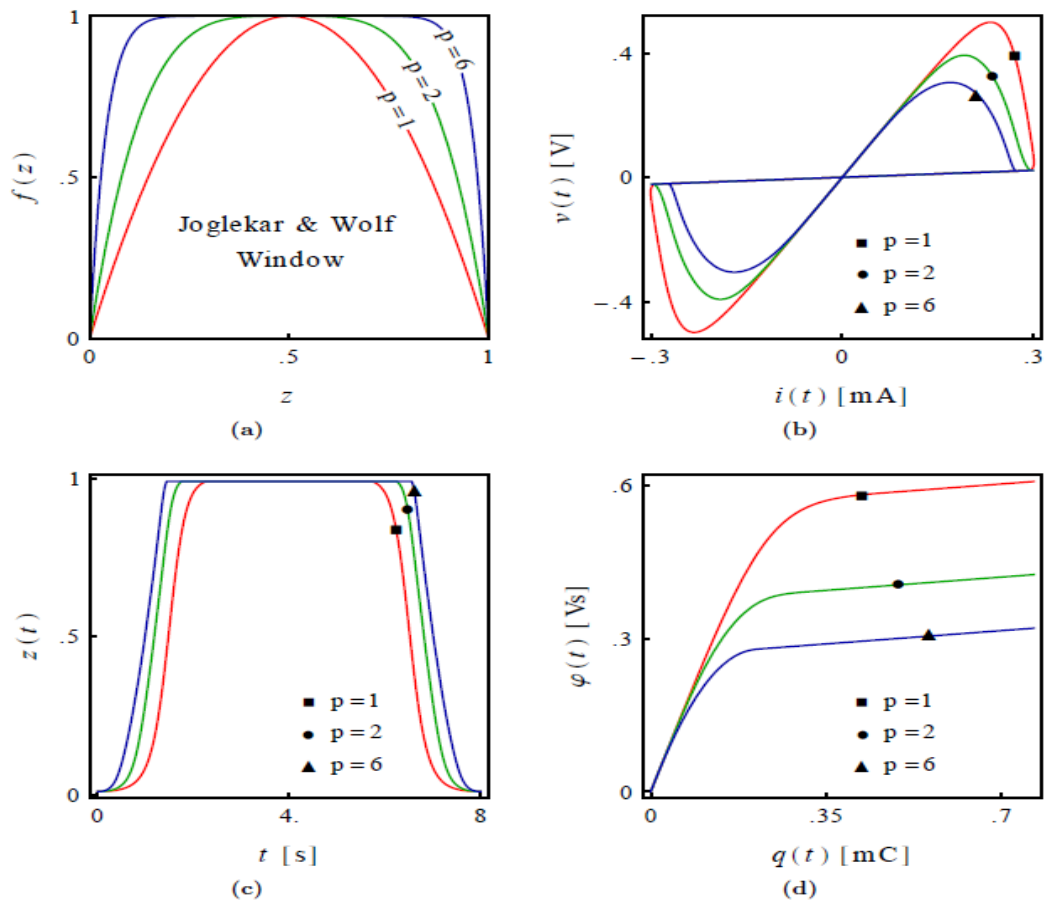


Figure 3.1: The behaviour of Joglekar et al window function) under a sinusoidal input current for different values of its control parameter p . In particular, the figure shows the effect of p on (a) the form of the window $f(z)$, (b) its i - v response, (c) the dynamics of the internal state variable z and (d) the resulting form of the ' q ' curve. From (a) it is clear that as the value of p increases, $f(z)$ becomes more at around its maximum which occurs at $z_{\max} = 0.5$ and eventually tends to a constant. As shown in (c), assuming the same input, a wider region for which $f(z) = 1$ causes the device to saturate faster, or equivalently as shown in (d), for a smaller amount of charge. The saturation region is also evident in (b) and corresponds to the linear part of the i - v response.

limiting resistances, R_{ON} or R_{OFF} . The model fails because when solving (2.31a) for obtaining z the solution involves an integration over the reciprocal of $f(z)$: $\int 1/f(z)dz$. The function $1/f(z)$ is asymptotic at $z = 0$ or $z = 1$ rendering the above integral divergent at the two boundaries and hence undefined at these two initial conditions (see Figure 2.9b).

Regardless of whether a window function is used or not, an additional issue which needs to be taken into account during the development of a model is the *accumulation* of charge (or flux). The resistance of such devices varies only within a limited range of resistance values bounded by a minimum (R_{ON}) and a maximum (R_{OFF}) resistance value. When the device reaches any of the two boundary values it switches from the memristive regime to that of a linear resistor until the polarity of the input is reversed. While in saturation, the input signal has no effect on the memristance, hence, the system loses its memristive character and all the properties that come with it (e.g. memory). Therefore, a mechanism must be incorporated in the model which will temporarily 'freeze' the integration over the input until the device returns back to the memristive regime. This mechanism will account for the fact that the device loses its ability to remember the amount of input applied while in saturation [86,87,125].

The window functions presented until now impose a restriction on the range of z such that $0 < z < 1$. However, due to the terminal state problem, this restriction is not effective on limiting the charge (or flux) as well. As a result of this 'half measure', when the system is in saturation the memristance changes only by an infinitesimal amount but the model keeps accumulating charge (or flux) [22,121]. In other words, the integral over the input signal does not stop during saturation because z is never exactly equal to 0 or 1 when starting from any initial condition $0 < z_0 < 1$. The excess charge (or flux) accumulated after saturation needs to be cancelled when the polarity of the input is reversed although it did not contribute to any change in the memristance. This introduces an unrealistic delay in the response of the system.

To deal with both of these problems Bialek *et al* dropped the compliance with property (2-2.2) and introduced the following piecewise window whose form depends on the polarity of the input [121]:

$$f(z, i; p) = 1 - (z - \text{stp}(-i))^{2p}, \quad (3.5)$$

where $\text{stp}(i) = 1$ for $i \geq 0$ and 0 otherwise. Its control parameter, p , is used to adjust the flatness of the window around the maximum in a similar way to (2.15).

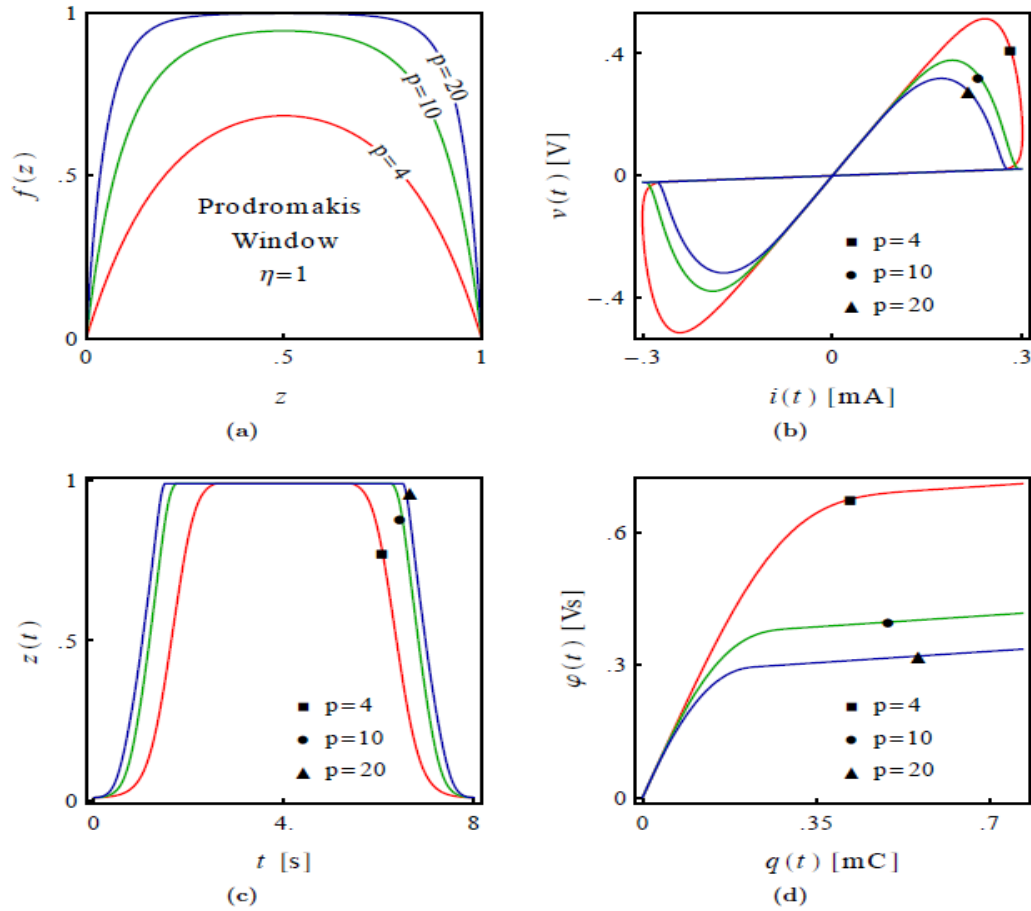


Figure 3.2: The behaviour of Prodromakis *et al* window function (2.36) under a sinusoidal input current for different values of its control parameter p and with $\eta = 1$. In particular, the figure shows the effect of p on **(a)** the form of the window $f(z)$, **(b)** its $i-v$ response, **(c)** the dynamics of the internal state variable z and **(d)** the resulting form of the $\phi(q)$ curve. The behaviour of this window is very similar to (2.35) which is illustrated in Figure 2.6. The difference here is that p can take a continuous range of values and it also controls the value of the maximum $f(z_{\max})$ at $z_{\max} = 0.5$.

illustrates the behaviour of (2.37) for several values of p .

The window function in (2.37) is a step in the correct direction for solving both of the practical implementation issues described above. However, unlike (2.35) and (2.36), for each value of p Biolek's *et al* window has two possible forms depending on the polarity of the input. As shown in Figure 2.8d, this results to a double-valued $q - \phi$ curve which implies that the system behaves in a completely different manner when the input reverses polarity. As a result, its $i - v$ response, shown in Figure 2.8bis asymmetric despite the system being driven by a periodic symmetric input. Additionally, for each value of q ,

$\phi(q)$ has a different slope when not in saturation. This translates to discontinuities in the memristance of the model when switching from one branch to the other [22]. The discontinuities become more apparent when the model is not allowed to saturate. Therefore, devices described by (2.14) cannot be classified as ideal memristors.

An alternative approach for solving the terminal state problem, suggested by Jha *et al*, is defining a *modified window function*, $\hat{f}(x)$, according to [125]:

$$f(x) = j \left(1 - [0.25(x - \text{stp}(-i))^2 + 0.75] \right)^p \quad (3.6)$$

The boundary lock and the scalability is guaranteed by the proposed window function. Here j is a scaling parameter. For any particular p , the value of $f(x)$, as in Fig. 4, can be scaled upward-downward by suitable j . By choosing different j , our window function could be adjusted for various applications

The characteristics of the proposed model are verified by means of typical numerical analysis. In the

following simulation some parameters are set as $R_{on} = 100 \Omega$, $R_{off} = 16 \text{ k}\Omega$, $R_{init} = 0.5 \text{ k}\Omega$, $D = 10 \text{ nm}$

and $\mu\nu = 10^{-14} \text{ m}^2 \text{ s}^{-1} \text{ V}^{-1}$, where R_{init} is the initial resistance of the memristive device. Our window function is implemented with $p = 10$ to impose the nonlinear drift across the whole bilayer. For $j = 1$ or 2 , pinched hysteresis loop driven by a sinusoidal input is asymmetrical as illustrated in Fig. 5, and the model is highly nonlinear when the boundary approaches one of the ends of the

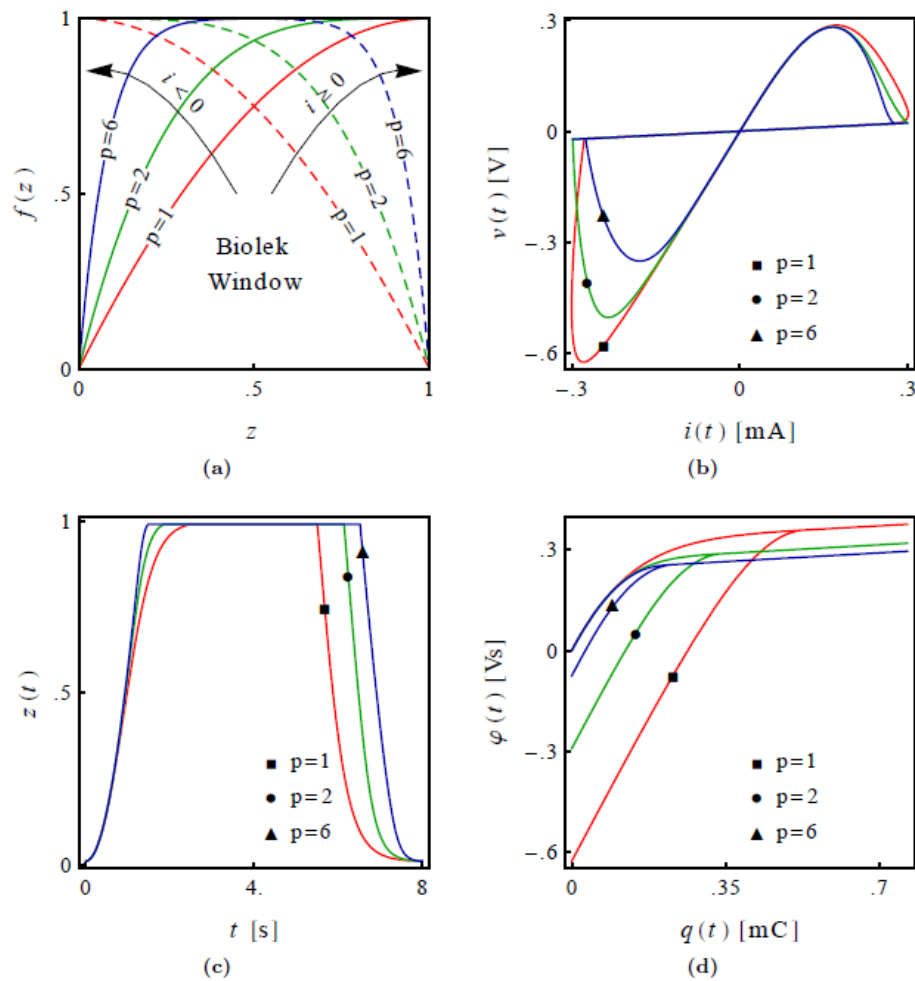
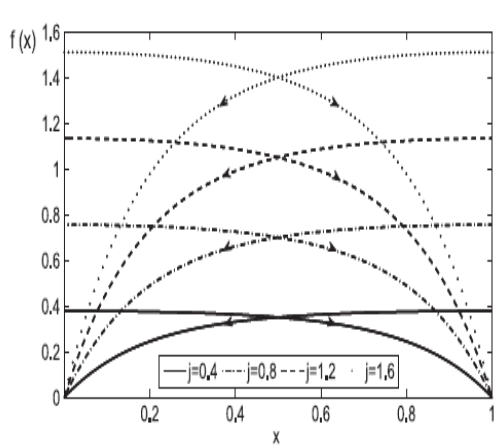
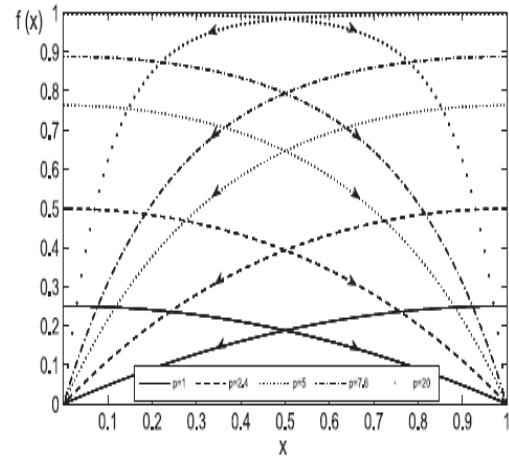


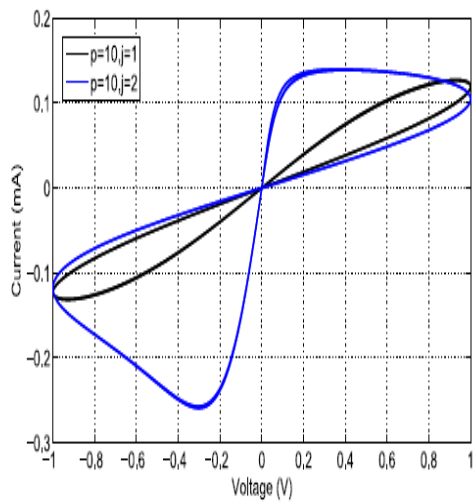
Figure 3.3: The behaviour of Biolek et al window function under a sinusoidal input current for different values of its control parameter p . In particular, the figure shows the effect of p on (a) the form of the window $f(z)$, (b) its i - v response, (c) the dynamics of the internal state variable z and (d) the resulting form of the $\varphi(q)$ curve. The parameter p controls the flatness of $f(z)$ around its maximum similarly to the other two windows (2.35) and (2.36). The difference of this model is that the form of $f(z)$ depends on the polarity of the input signal as shown in (a). As shown in (d), this results to a double-valued $\varphi(q)$ which translates to an asymmetric i - v response, shown in (b), and asymmetric dynamics for z , demonstrated in (c). Moreover, this model introduces discontinuities in the memristance since the slope of $\varphi(q)$ is double-valued as well when not in saturation.



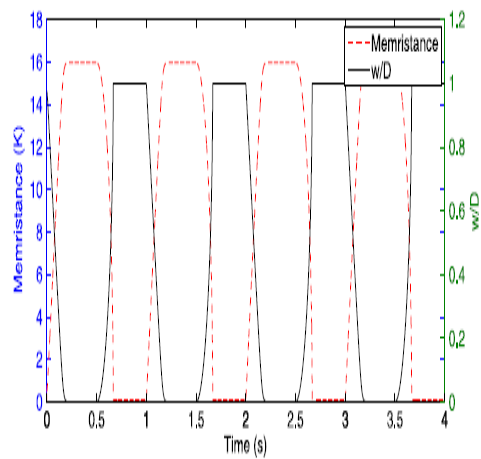
(a)



(b)



(c)



(d)

Fig 3.4: (a) The figure shows variation of window function for different for different values of j (b) The figure shows variation of window function for different p (c) The figures shows the I-V characteristics of memristor for Jha's window function model (d) The figure shows the transient response of the device

Chapter 4

Proposed window function

Window function expresses the speed of change of boundary state at different states.

A sensible window function should have these characteristics :

- It should be able to represent linear dopant drift when not in boundary
- It should be able to represent nonlinear dopant drift when at boundary because of high electric fields at the boundary regions
- It should address boundary lock problem. Boundary lock problem means that no external stimulus can drive the memristive device when the boundary state between the doped and undoped layers reaches either end of the device.
- A window function should have adjustable parameter, which will make the memristor model acquiring more control in scalability (in the range of $f(x) \leq 1$) meaning the region of linear dopant drift and non linear dopant drift can be adjusted by it.
- A window function should have another adjustable parameter, which will make the memristor model acquiring more control in flexibility meaning the range of f_{max} can be adjusted by it
- It should be continuously differentiable so that it can avoid errors while running simulations

Now starting with Strukov's model we can see that it is a simple model, which only considers the linear drift over the entire memristive device . It is thus generally called a linear ionic drift model. The down side of the model is that it doesn't represent non linear drift dopant at boundaries and also doesn't address boundary lock problem. Moreover, it doesn't have any adjustable parameters for flexibility or scalability

Now, looking at it shows linearity when x is not boundary .It shows nonlinearity dopant drift at either of the boundaries and also has adjustable parameter p by

which window function's linear and nonlinear regions can be controlled. So, it provides control of scaling the function. Moreover, it is continuously differentiable. But it doesn't address boundary lock problem.

Coming back to Biolek's model, we see that it shows linear dopant drift as well as nonlinear dopant drift model. It resolves the problem of boundary lock by showing its boundary state changing with direction of current. Moreover, it provides us with the control of scalability. The let downs of the model are that it doesn't fall to zero at either of the boundaries and it is not continuously differentiable.

Then at Prodromakis's model the linear dopant drift and nonlinear dopant drift model is represented quite nicely. It is continuously differentiable and also offers scalability through parameter p. But it doesn't address boundary lock problem as it doesn't show any relation of state change with change of current direction.

Jha's model represents linear dopant drift and nonlinear dopant drift model. It resolves the problem of boundary lock by showing its boundary state change with direction of current. Also, it offers control of scalability through parameter p. adding with a parameter j which provides control of flexibility. But the fact that it doesn't fall to zero at the boundaries. It is not continuously differentiable.

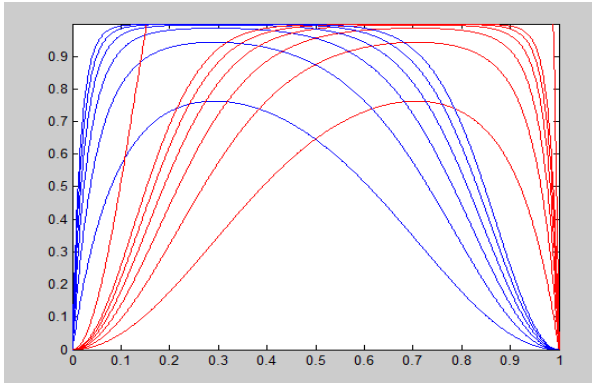
So there is not a window function yet which addresses all the characteristics of a proper window function correctly. So we proposed a novel window function with an aim to overcome the aforementioned issues of different window functions.

Our proposed window function is ,

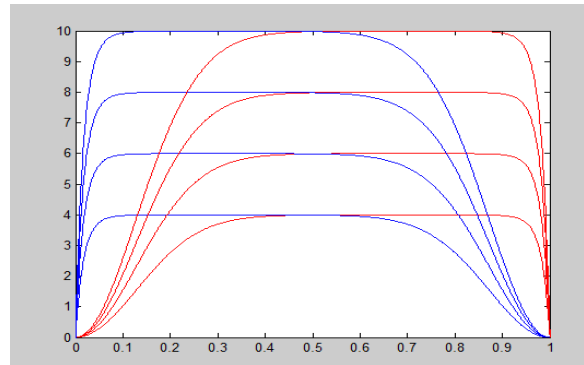
$$f(x) = j(1 - [(x - stp(-i))^2 - 0.5]^2 + 0.75)]^p \quad (4.1)$$

where j and p are any positive integers.

Our window function represents linear dopant drift and nonlinear dopant drift model without giving in to the boundary lock problem. From the equation it is vivid that its boundary state changes with direction of current. Moreover, it offers control of scalability through parameter p. It offers control of flexibility through parameter j. Adding to those it also falls to zero when it reaches either of the boundaries. It is also continuously differentiable.



(a)



(b)

Figure 4.1 : (a) It shows the change in $f(x)$ with change in parameter p . Here $f(x)$ maximum is constant that is 1. But the width of window increase as increase of p . (b) It shows the change in window function maximum value with change of parameter j .

Chapter 5

Conclusion

This chapter summarises the achievements reported in this work and compares them against the initial objectives set in Chapter 1. The potential impact of these results in the field of memristive devices is also discussed and their possible limitations are identified. Finally, the chapter concludes by presenting future research directions in the field which can follow from this research.

5.1 Summary of contributions

The research results reported in this work were driven by the two central objectives detailed in Section 1.3 of the introductory chapter. The two main objectives focused on different but strongly interlinked aspects of memristive devices, with the first one focusing on the theoretical understanding of ideal memristors and the second, on improving the currently used models for memristive devices. The results and contributions obtained while pursuing these goals are critically reviewed in this section.

The first goal of the project was the development of a set of mathematical tools which can be used for expanding the limited understanding of the behaviour and properties of ideal memristors. Expanding our understanding of the ideal element is vital for the progress of the field. Such studies can reveal new properties of the device which have the potential to open the way for new applications. Additionally, they can help in the identification and modelling of devices behaving as memristors or memristive systems in general. However, as already discussed in Chapter 1, only a small number of studies

dealing with these theoretical aspects of the ideal element have been published until now and are mostly limited to Chua's and Kang's original papers. Because of the potential economic impact of their applications, the research community and industry have skipped this step and dedicated their efforts mainly on fabricating devices without being able to fully appreciate and comprehend the observed behaviour of the devices.

The results presented in Chapter 3 and Chapter 4 were dedicated to reducing the existing gap in the theoretical understanding of ideal memristors. More specifically, Chapter 3 has presented different mathematical models of memristers and their properties. Chapter 4 has presented the comparison among the models and finally a model is proposed which is more sensible and acceptable. Here is a table showing comparison analysis among the existing models and our proposed model.

Different F(x)	Strukov	Joglekar	Biolek	Prodromakis	Zha	Our f(x)
Linear dopant drift	Yes	Yes	Yes	Yes	Yes	Yes
Nonlinear dopant drift	No	Yes	Yes	Yes	Yes	Yes
Scalability	No	Yes	Limited	Yes	Yes	Yes
Resolve boundary lock	No	No	Yes	No	Yes	Yes
Differentiability	Yes	Yes	No	Yes	No	Yes
Fall to 0 at boundaries	No	Yes	No	Yes	No	Yes
flexibility	No	No	No	No	Yes	Yes

Table 5.1 Comparison of our window function with other functions

From the table, it is clear that our window function fulfills all the characteristics for it to be suitable for proper modeling of the device and simulations.

5.2 Future work

This work sets the foundations on the theoretical understanding of memristors but at the same time opens up a whole new spectrum of interesting questions that need to be answered in the future:

- The framework is limited to ideal memristors only. The value of studying ideal memristors has already been discussed above. Nevertheless, since most practical devices are memristive systems, an interesting direction of future work is to broaden the framework in order to cover memristive systems as well. Moreover, the benefits of the framework have only been demonstrated through the analysis of models having the specific characteristic that their state equation is a linear

function of their input raised to an integer power. It is therefore unclear whether the benefits, compared to other approaches, will be achieved by using the framework for the analysis of more complex models which do not necessarily satisfy the linearity property. To conclude on this matter a survey using a broader spectrum of ideal memristor models should be carried out in the future.

- Chapter 5 has demonstrated the applicability of the window-based modelling approach by identifying one device whose response can be described using this model. Additionally, in the same chapter a new model was proposed which is able to describe the response of other two memristive devices. Nevertheless, in order to conclude on the generality of these models a survey using a larger number of memristive devices should be executed. Such a study will clarify whether these models are limited to the example device studied here or not. Moreover, additional unaccounted dependencies may be revealed which can potentially improve further the accuracy of the models by incorporating them in the systems' description. Finally, the two macroscopic models can be used, for the respective devices they can describe, as a starting point for understanding the underlying physical mechanisms which give rise to the observed memristive behaviour.
- The noise analysis of memristors is another interesting direction of future work which will continue from the findings of the harmonic analysis. From an application perspective it is important to investigate and determine the behaviour of memristors in a noisy environment. In any realistic application noise is expected to deteriorate the performance of the memristor in terms of speed, power dissipation and reliability [163]. Additionally, its behaviour under noise may determine whether the memristor is suitable for certain applications. For example, if the memristor behaves in an unpredictable manner under the influence of noise, it may not be suitable for memory applications since unexpected switching of the state of the device will result to the loss of data. As a nonlinear element, the noise analysis of the memristor is a non-trivial task, especially when the element is viewed as part of a larger network. Nevertheless, by investigating aspects of its output spectrum, such as the signal-to-noise ratio and the dynamic range it may be possible to reveal a dependency to the nonlinearity of the device similar to that demonstrated for the hysteresis and the harmonic distortion [164]. It is expected that the nonlinearity of the device will result to intermodulation of the input signal with the noise and any possible interference and also, to a variable noise floor which will depend on the excitation applied at the input. A

useful outcome from such an analysis would be the evaluation of a relation analogous to the power spectral density modelling the thermal noise in linear resistors ($S = 4kT R\Delta f$) [163].

- Any application incorporating memristors will make use of this component in combination with other known circuit elements such as the resistor, inductor, capacitor and possibly many others. It is therefore important to extend the findings reported for networks of only memristors, to networks combining memristors with other elements. Starting from simple combinations and extending to more complex configurations it is expected that such a study will reveal unique properties which can be exploited in fields such as filter design. An interesting example, which falls into the category of networks, is the use of the memristor as a more area efficient integrator compared to the bulky capacitor-based integrators. The memristor, by definition is an intrinsic integrator of its input. However, the integral of the input appears at the output nonlinearly transformed. Depending on the network used to cancel the nonlinearity, any area benefits may be eventually lost. By developing further our understanding of networks of memristors combined with other elements, such questions should be easier to answer.

5.3 Final thoughts

The field of memristors is still at its very early stages. Like other new unconventional ideas (e.g. the transistor), it is confronted with a lot of scepticism [165]. It is difficult to predict how the field will grow and whether memristors will find wide use in circuit design or other applications. This will possibly depend on whether they are able to outperform fast enough other competing technologies [166]. Despite the significant efforts of research groups to fabricate memristors, it is expected that the first commercially available devices will be released from companies such as HP [55,56]. Most likely such devices will be optimised for digital applications and in particular digital memories. It will be therefore difficult for the academic community to outperform the industry in terms of the digital applications of memristors. Nevertheless, there is plenty of space for innovative applications outside the boundaries of the digital domain. As discussed in the introductory chapter, such applications will treat the memristor as an analog component by exploiting the continuous range of its memristance. Several analog applications have been proposed in theory (see Section 1.2.2) taking advantage of the unique

properties of memristors but are yet to be proven in practice. The release of a memristor device into the market will give the opportunity to the researchers to test the viability of their theoretically proposed applications. The potential success of these tests will reinforce the efforts of groups working on memristors and give an even stronger push to the field by convincing even the more sceptics.

Irrespective of their commercial success, memristors offer a unique opportunity to rethink the scope of classical electronics. This new element challenges the well established perception that the three fundamental circuit elements are limited to the resistor, capacitor and inductor. The identification of the memristor demonstrates that not only circuit theory is not bounded to these three elements but more importantly it can potentially be extended by introducing additional components. For example, one can theorise new elements by considering the pairwise combinations of higher order derivatives and integrals of the voltage and current. In this manner an infinite amount of 2-terminal dynamical elements can be defined. In fact, this has already been proposed by Leon Chua a decade after the memristor was suggested [6]. After the rediscovery of the memristor by HP, this idea has resurfaced and already resulted to the introduction of two other mem-elements, the memcapacitor (memory capacitor) and the meminductor (memory inductor) by Di Ventra *et al* [167], and it is actively explored by other groups [168]. The introduction of these higher order elements may be useful in the modelling of new complex systems. For example, the memcapacitor and the meminductor have already been used for the modelling of systems which exhibit memory dependent capacitance/-inductance due to input induced non-volatile geometrical variations or changes in their permittivity/permeability [19].

The analysis and results presented in this work constitute a small step in extending our understanding of ideal memristors and in improving the models currently used to capture the response of fabricated memristive devices. It should be clear from the preceding discussion that there are still several non-trivial aspects of the memristor which remain unexplored. A lot of effort is still required until we understand and fully appreciate its potential. We will be able to provide an answer to the questions that remain open only if research in the field of memristors continues.

Bibliography

- [1] Leon O. Chua. Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory*, 18(5):507–519, Sep 1971.
- [2] Leon O. Chua, Charles Desoer, and Ernest Kuh. *Linear and Non Linear Circuits*. McGraw-Hill Education, 1987.
- [3] George F. Oster and D. M. Auslander. The memristor: A new bond graph element. *Journal of Dynamic Systems, Measurement, and Control*, 94(3):249–252, Sep 1972.
- [4] George F. Oster. A note on memristors. *IEEE Transactions on Circuits and Systems*, 21(1):152–152, Jan 1974.
- [5] Leon O. Chua. *Introduction to Nonlinear Network Theory*. Series in Electronic Systems. McGraw-Hill, 1967.
- [6] Leon O. Chua. Device modeling via basic nonlinear circuit elements. *IEEE Transactions on Circuits and Systems*, 27(11):1014–1044, Nov 1980.
- [7] Yogesh N Joglekar and Stephen J Wolf. The elusive memristor: properties of basic electrical circuits. *European Journal of Physics*, 30(4):661, Jul 2009.
- [8] Bernard Widrow. An adaptive 'adaline' neuron using chemical 'memistors'. Technical Report 1553-2, Stanford Electronics Laboratories, Oct 1960.
- [9] Bernard Widrow, W. Pierce, and J. Angell. Birth, life and death in microelectronic systems. Technical Report 1552-2/1851-1, Stanford Electronics Laboratories, May 1961. Also in IRE Transactions of the Professional Group on Military Electronics, pp.191-201, Jul 1961.

- [10] Qiangfei Xia, Matthew D. Pickett, J. Joshua Yang, Xuema Li, Wei Wu, Gilberto Medeiros-Ribeiro, and R. Stanley Williams. Two- and three-terminal resistive switches: Nanometer-scale memristors and memistors. *Advanced Functional Materials*, 21(14):2660–2665, 2011.
- [11] Leon O. Chua and Sung Mo Kang. Memristive devices and systems. *Proceedings of the IEEE*, 64(2):209–223, Feb 1976.
- [12] Leon Chua, Valery Sbitnev, and Hyongsuk Kim. Hodgkin-huxley axon is made of memristors. *International Journal of Bifurcation and Chaos*, 22(03):1230011, 2012.
- [13] Dmitri B. Strukov, Gregory S. Snider, Duncan R. Stewart, and Williams R. Stanley. The missing memristor found. *Nature*, 453(7191):80–83, May 2008.
- [14] Akihito and Sawa. Resistive switching in transition metal oxides. *Materials Today*, 11(6):28 – 36, 2008.
- [15] Rainer Waser, Regina Dittmann, Georgi Staikov, and Kristof Szot. Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges. *Advanced Materials*, 21(25-26):2632–2663, 2009.
- [16] Rainer Waser. Resistive non-volatile memory devices. *Microelectronic Engineering*, 86(7-9):1925–1928, 2009.
- [17] Sung Hyun Jo, Kuk-Hwan Kim, Ting Chang, S. Gaba, and Wei Lu. Si memristive devices applied to memory and neuromorphic circuits. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 13–16, Jun 2010.
- [18] Kyung Min Kim, Doo Seok Jeong, and Cheol Seong Hwang. Nanofilamentary resistive switching in binary oxide system: a review on the present status and outlook. *Nanotechnology*, 22(25):254002, 2011.
- [19] Yuriy V. Pershin and Massimiliano Di Ventra. Memory effects in complex materials and nanoscale systems. *Advances in Physics*, 60(2):145–227, 2011.
- [20] M. Di Ventra and Y. V. Pershin. Biologically-inspired electronics with memory circuit elements. *ArXiv e-prints*, Dec 2011.
- [21] Chagaan Baatar, Wolfgang Porod, and Tamas Roska. *Cellular Nanoscale Sensory Wave Computing*. Springer Publishing Company, Incorporated, 1st edition, 2009.

- [22] Omid Kavehei, A. Iqbal, Y. S. Kim, Kamran Eshraghian, Said Al-Sarawi, and Derek Abbott. The fourth element: Characteristics, modeling and electromagnetic theory of the memristor. *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Science*, 2010.
- [23] T. Driscoll, J. Quinn, S. Klein, H. T. Kim, B. J. Kim, Yu. V. Pershin, M. Di Ventra, and D. N. Basov. Memristive adaptive filters. *Applied Physics Letters*, 97(9):093502, 2010.
- [24] Williams R. Stanley. How we found the missing memristor. *IEEE Spectrum*, 45(12):28–35, Dec 2008.
- [25] J. Joshua Yang, Matthew D. Pickett, Xuema Li, Douglas A. A. Ohlberg, Duncan R. Stewart, and Williams R. Stanley. Memristive switching mechanism for metal/oxide/metal nanodevices. *Nature Nanotechnology*, 3(7):429–433, Jul 2008.
- [26] Web of knowledge. <http://apps.webofknowledge.com>.
- [27] C. Schindler, M. Weides, M. N. Kozicki, and R. Waser. Low current resistive switching in Cu-SiO₂ cells. *Applied Physics Letters*, 92(12):122910, 2008.
- [28] C. Schindler, G. Staikov, and R. Waser. Electrode kinetics of Cu-SiO₂-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories. *Applied Physics Letters*, 94(7):072109, 2009.
- [29] J. Joshua Yang, John Paul Strachan, Qiangfei Xia, Douglas A. A. Ohlberg, Philip J. Kuekes, Ronald D. Kelley, William F. Stickle, Duncan R. Stewart, Gilberto Medeiros-Ribeiro, and Williams R. Stanley. Diffusion of adhesion layer metals controls nanoscale memristive switching. *Advanced Materials*, 22(36):4034–4038, 2010.
- [30] Sung Hyun Jo and Wei Lu. CMOS compatible nanoscale nonvolatile resistance switching memory. *Nano Letters*, 8(2):392–397, 2008.
- [31] Antonio C Torrezan, John Paul Strachan, Gilberto Medeiros-Ribeiro, and R Stanley Williams. Sub-nanosecond switching of a tantalum oxide memristor. *Nanotechnology*, 22(48):485203, 2011.
- [32] Sung Hyun Jo, Kuk-Hwan Kim, and Wei Lu. High-density crossbar arrays based on a Si memristive system. *Nano Letters*, 9(2):870–874, 2009.

- [33] Sheng-Yu Wang, Chin-Wen Huang, Dai-Ying Lee, Tseung-Yuen Tseng, and Ting-Chang Chang. Multilevel resistive switching in Ti-Cu_xO-Pt memory devices. *Journal of Applied Physics*, 108(11):114110, 2010.
- [34] Fabien Alibart, Ligang Gao, Brian D Hoskins, and Dmitri B Strukov. High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm. *Nanotechnology*, 23(7):075201, 2012.
- [35] Sung Hyun Jo, Ting Chang, Idongesit Ebong, Bhavitavya B. Bhadviya, Pinaki Mazumder, and Wei Lu. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Letters*, 10(4):1297–1301, 2010.
- [36] Omid Kavehei, Y. S. Kim, A. Iqbal, Kamran Eshraghian, Said Al-Sarawi, and Derek Abbott. The fourth element: Insights into the memristor. In *International Conference on Communications, Circuits and Systems, 2009*, pages 921–927, Jul 2009.
- [37] Dmitri B. Strukov, Duncan R. Stewart, Julien L. Borghetti, X. Li, Matthew D. Pickett, G.M. Ribeiro, Warren Robinett, Gregory S. Snider, John Paul Strachan, W. Wu, Qiangfei Xia, J. Joshua Yang, and Williams R. Stanley. Hybrid CMOS/memristor circuits. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1967–1970, Jun 2010.
- [38] George I. Bourianoff, Paolo A. Gargini, and Dmitri E. Nikonov. Research directions in beyond CMOS computing. *Solid-State Electronics*, 51(11-12):1426 – 1431, 2007.
- [39] Konstantin Likharev. Electronics below 10 nm. In *Nano and Giga Challenges in Microelectronics*, pages 27–68. Elsevier Science B.V., Amsterdam, 2003.
- [40] D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, and Hon-Sum Philip Wong. Device scaling limits of Si MOSFETs and their application dependencies. *Proceedings of the IEEE*, 89(3):259–288, Mar 2001.
- [41] Dmitri B. Strukov and Konstantin K Likharev. CMOL FPGA: a reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices. *Nanotechnology*, 16(6):888, 2005.
- [42] Gregory S. Snider and Williams R. Stanley. Nano/CMOS architectures using a field-programmable nanowire interconnect. *Nanotechnology*, 18(3):035204, 2007.

- [43] Julien L. Borghetti, Zhiyong Li, Joseph Straznicky, Xuema Li, Douglas A. A. Ohlberg, Wei Wu, Duncan R. Stewart, and Williams R. Stanley. A hybrid nanomemristor/transistor logic circuit capable of self-programming. *Proceedings of the National Academy of Sciences*, 106(6):1699–1703, 2009.
- [44] Qiangfei Xia, Warren Robinett, Michael W. Cumbie, Neel Banerjee, Thomas J. Cardinali, J. Joshua Yang, Wei Wu, Xuema Li, William M. Tong, Dmitri B. Strukov, Gregory S. Snider, Gilberto Medeiros-Ribeiro, and Williams R. Stanley. Memristor-CMOS hybrid integrated circuits for reconfigurable logic. *Nano Letters*, 9(10):3640–3645, Oct 2009.
- [45] Gregory S. Snider. Self-organized computation with unreliable, memristive nanodevices. *Nanotechnology*, 18(36):365202, 2007.
- [46] Gregory S. Snider. Spike-timing-dependent learning in memristive nanodevices. In *IEEE International Symposium on Nanoscale Architectures, 2008*, pages 85–92, Jun 2008.
- [47] Sung Hyun Jo, Kuk-Hwan Kim, and Wei Lu. Programmable resistance switching in nanoscale two-terminal devices. *Nano Letters*, 9(1):496–500, 2009.
- [48] Dmitri B. Strukov and Konstantin K. Likharev. A reconfigurable architecture for hybrid CMOS/nanodevice circuits. In *Proceedings of the 2006 ACM/SIGDA 14th international symposium on Field programmable gate arrays*, pages 131–140, 2006.
- [49] Dmitri B. Strukov and Konstantin K. Likharev. Defect-tolerant architectures for nanoelectronic crossbar memories. *Journal of Nanoscience and Nanotechnology*, 7(1):151–167, 2007.
- [50] Konstantin Likharev and Dmitri B. Strukov. Prospects for the development of digital CMOL circuits. In *IEEE International Symposium on Nanoscale Architectures*, pages 109–116, Oct 2007.
- [51] Massimiliano Di Ventra, Yuriy V. Pershin, and Leon O. Chua. Putting memory into circuit elements: Memristors, memcapacitors, and meminductors. *Proceedings of the IEEE*, 97(8):1371–1372, Aug 2009.
- [52] Philip J. Kuekes, Duncan R. Stewart, and Williams R. Stanley. The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits. 97(3):034301, 2005.

- [53] C. Kugeler, M. Meier, R. Rosezin, S. Gilles, and R. Waser. High density 3D memory architecture based on the resistive switching effect. *Solid-State Electronics*, 53(12):1287–1292, 2009.
- [54] International technology roadmap for semiconductors. <http://www.itrs.net/Links/2011ITRS/Home2011.htm>, 2011.
- [55] HP Newsroom. HP collaborates with Hynix to bring the memristor to market in next-generation memory. <http://www.hp.com/hpinfo/newsroom/press/2010/100831c.html>, Aug 2010.
- [56] EE Times. HP, Hynix delay memristor debut. <http://www.eetimes.com/electronics-news/4397188/HP-Hynix-memristor-debut-pushed-back>, Sept 2012.
- [57] Dmitri B. Strukov and Williams R. Stanley. Four-dimensional address topology for circuits with stacked multilayer crossbar arrays. *Proceedings of the National Academy of Sciences*, 106(48):20155–20158, 2009.
- [58] Yao-Feng Chang, Ting-Chang Chang, and Chun-Yen Chang. Investigation statistics of bipolar multilevel memristive mechanism and characterizations in a thin FeO_x transition layer of TiN-SiO₂-FeO_x-Fe structure. *Journal of Applied Physics*, 110(5):053703, 2011.
- [59] A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel, and D. Widmer. Reproducible switching effect in thin oxide films for memory applications. *Applied Physics Letters*, 77(1):139–141, 2000.
- [60] Hyongsuk Kim, Maheshwar Pd. Sah, Changju Yang, and Leon O. Chua. Memristor-based multilevel memory. In *12th International Workshop on Cellular Nanoscale Networks and Their Applications*, pages 1–6, Feb 2010.
- [61] Julien L. Borghetti, Gregory S. Snider, Philip J. Kuekes, J. Joshua Yang, Duncan R. Stewart, and Williams R. Stanley. 'Memristive' switches enable 'stateful' logic operations via material implication. *Nature*, 464(7290):873–876, May 2010.
- [62] Gregory S. Snider. Computing with hysteretic resistor crossbars. *Applied Physics A: Materials Science & Processing*, 80:1165–1172, 2005. 10.1007/s00339-004-3149-1.

- [63] Garrett S. Rose and Mircea R. Stan. A programmable majority logic array using molecular scale electronics. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(11):2380–2390, Nov 2007.
- [64] Jeyavijayan Rajendran, Harika Manem, and Garrett S. Rose. NDR based threshold logic fabric with memristive synapses. In *9th IEEE Conference on Nanotechnology*, pages 725–728, Jul 2009.
- [65] Eero Lehtonen and Mika Laiho. Stateful implication logic with memristors. In *IEEE/ACM International Symposium on Nanoscale Architectures*, pages 33–36, Jul 2009.
- [66] Eero Lehtonen, J.H. Poikonen, and Mika Laiho. Two memristors suffice to compute all boolean functions. *Electronics Letters*, 46(3):239–240, 4 2010.
- [67] Pascal O. Vontobel, Warren Robinett, Philip J. Kuekes, Duncan R. Stewart, Joseph Straznicky, and Williams R. Stanley. Writing to and reading from a nanoscale crossbar memory based on memristors. *Nanotechnology*, 20(42), Oct 2009.
- [68] Konstantin Likharev and Dmitri B. Strukov. CMOL: Devices, circuits, and architectures. In *Introducing Molecular Electronics*, volume 680 of *Lecture Notes in Physics*, pages 447–477. Springer Berlin / Heidelberg, 2005.
- [69] Andre DeHon and Konstantin K. Likharev. Hybrid CMOS/nanoelectronic digital circuits: devices, architectures, and design automation. In *IEEE/ACM International Conference on Computer-Aided Design*, pages 375–382, Nov 2005.
- [70] Andre DeHon. Nanowire-based programmable architectures. *J. Emerg. Technol. Comput. Syst.*, 1:109–162, Jul 2005.
- [71] Wei Wang, Tom T. Jing, and Brian Butcher. FPGA based on integration of memristors and CMOS devices. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pages 1963–1966, Jun 2010.
- [72] Chen Dong, Deming Chen, S. Haruehanroengra, and Wei Wang. 3D nFPGA: A reconfigurable architecture for 3D CMOS/nanomaterial hybrid digital circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(11):2489–2501, Nov 2007.

- [73] D. Tu, M. Liu, Wei Wang, and S. Haruehanroengra. Three-dimensional CMOL: Three-dimensional integration of CMOS/nanomaterial hybrid digital circuits. *IET Micro Nano Letters*, 2(2):40–45, Jun 2007.
- [74] Dmitri B. Strukov and A. Mishchenko. Monolithically stackable hybrid FPGA. In *Design, Automation Test in Europe Conference Exhibition*, pages 661–666, Mar 2010.
- [75] Bernabe Linares-Barranco, Teresa Serrano-Gotarredona, Luis A. Camunas-Mesa, Jose A. Perez-Carrasco, Carlos Zamarreno-Ramos, and Timothee Masquelier. On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex. *Frontiers in Neuroscience*, 5(0), 2011.
- [76] Hyejung Choi, Heesoo Jung, Joonmyoung Lee, Jaesik Yoon, Jubong Park, Dong jun Seong, Wootae Lee, Musarrat Hasan, Gun-Young Jung, and Hyunsang Hwang. An electrically modifiable synapse array of resistive switching memory. *Nanotechnology*, 20(34):345201, 2009.
- [77] Ting Chang, Sung-Hyun Jo, Kuk-Hwan Kim, Patrick Sheridan, Siddharth Gaba, and Wei Lu. Synaptic behaviors and modeling of a metal oxide memristive device. *Applied Physics A: Materials Science & Processing*, 102:857–863, 2011. 10.1007/s00339-011-6296-1.
- [78] Yuriy V. Pershin and Massimiliano Di Ventra. Experimental demonstration of associative memory with memristive neural networks. *Neural Networks*, 23(7):881–886, 2010.
- [79] Bernabe Linares-Barranco and Teresa Serrano-Gotarredona. Exploiting memristance in adaptive asynchronous spiking neuromorphic nanotechnology systems. In *9th IEEE Conference on Nanotechnology*, pages 601–604, Jul 2009.
- [80] Bernabe Linares-Barranco and Teresa Serrano-Gotarredona. Memristance can explain spike-time-dependent-plasticity in neural synapses. *Nature Precedings*, Mar 2009.
- [81] Jose A. Perez-Carrasco, Carlos Zamarreno-Ramos, Teresa Serrano-Gotarredona, and Bernabe Linares-Barranco. On neuromorphic spiking architectures for asynchronous STDP memristive systems. In *Proceedings of IEEE International Symposium on Circuits and Systems*, pages 1659–1662, May 2010.

- [82]I.E. Ebong and P. Mazumder. CMOS and memristor-based neural network design for position detection. *Proceedings of the IEEE*, 100(6):2050–2060, Jun 2012.
- [83] Yuriy V. Pershin, Steven La Fontaine, and Massimiliano Di Ventra. Memristive model of amoeba learning. *Physical Review E*, 80(2):021926, Aug 2009.
- [84] Yuriy Pershin and Massimiliano Di Ventra. Solving mazes with memristors: a massively-parallel approach. 2011.
- [85] Yuriy V. Pershin and Massimiliano Di Ventra. Practical approach to programmable analog circuits with memristors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 57(8):1857–1864, Aug 2010.
- [86] Sangho Shin, Kyungmin Kim, and Sung-Mo Kang. Memristor applications for programmable analog ICs. *IEEE Transactions on Nanotechnology*, 10(2):266–274, Mar 2011.
- [87] Sangho Shin, Kyungmin Kim, and Sung-Mo Kang. Memristor-based fine resolution programmable resistance and its applications. In *International Conference on Communications, Circuits and Systems*, pages 948–951, Jul 2009.
- [88]K. Witrisal. A memristor-based multicarrier UWB receiver. In *IEEE International Conference on Ultra-Wideband*, pages 679–683, Sep 2009.
- [89]K. Witrisal. Memristor-based stored-reference receiver - the UWB solution? *Electronics Letters*, 45(14):713–714, 2 2009.
- [90]Gaurav Gandhi David Varghese. Memristor based high linear range differential pair. In *International Conference on Communications, Circuits and Systems*, pages 935–938, Jul 2009.
- [91]Eero Lehtonen, Mika Laiho, and J.H. Poikonen. A chaotic memristor circuit. In *12th International Workshop on Cellular Nanoscale Networks and Their Applications*, pages 1–3, Feb 2010.
- [92]F. Corinto, A. Ascoli, and Marco Gilli. Nonlinear dynamics of memristor oscillators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(6):1323–1336, Jun 2011.
- [93]T. Driscoll, Y. Pershin, D. Basov, and M. Di Ventra. Chaotic memristor. *Applied Physics A: Materials Science & Processing*, 102:885–889, 2011.

- [94] Makoto Itoh and Leon O. Chua. Memristor oscillators. *International Journal of Bifurcation and Chaos*, 18(11):3183–3206, 2008.
- [95] Bharathwaj Muthuswamy and Pracheta. Kokate. Memristor-based chaotic circuits. *IETE Technical Review*, 26(6):417–429, 2009.
- [96] B.C. Bao, Z. Liu, and J.P. Xu. Steady periodic memristor oscillator with transient chaotic behaviours. *Electronics Letters*, 46(3):237–238, 4 2010.
- [97] Zhao hui Lin and Hong xia Wang. Image encryption based on chaos with PWL memristor in chua’s circuit. In *International Conference on Communications, Circuits and Systems*, Jul 2009.
- [98] Makoto Itoh and Leon O. Chua. Memristor cellular automata and memristor discrete-time cellular neural networks. *International Journal of Bifurcation and Chaos*, 19(11):3605–3656, Nov 2009.
- [99] Mika Laiho and Eero Lehtonen. Cellular nanoscale network cell with memristors for local implication logic and synapses. In *Proceedings of IEEE International Symposium on Circuits and Systems*, pages 2051–2054, Jun 2010.
- [100] Eero Lehtonen and Mika Laiho. CNN using memristors for neighborhood connections. In *12th International Workshop on Cellular Nanoscale Networks and Their Applications*, pages 1–4, Feb 2010.
- [101] Ilia Valov, Rainer Waser, John R Jameson, and Michael N Kozicki. Electrochemical metallization memories-fundamentals, applications, prospects. *Nanotechnology*, 22(25):254003, 2011.
- [102] John Paul Strachan, Dmitri B. Strukov, Julien L. Borghetti, J. Joshua Yang, Gilberto Medeiros-Ribeiro, and Williams R. Stanley. The switching location of a bipolar memristor: chemical, thermal and structural mapping. *Nanotechnology*, 22(25):254015, 2011.
- [103] Jubong Park, Seungjae Jung, Joonmyoung Lee, Wootae Lee, Seonghyun Kim, Jungho Shin, and Hyunsang Hwang. Resistive switching characteristics of ultra-thin TiO_x. *Microelectronic Engineering*, 88(7):1136–1139, 2011.
- [104] Myoung-Jae Lee, Chang B. Lee, Dongsoo Lee, Seung R. Lee, Man Chang, Ji H. Hur, Young-Bae Kim, Chang-Jung Kim, David H. Seo, Sunae Seo, U-In Chung, In-Kyeong Yoo, and Kinam Kim. A fast, high-endurance and scalable non-volatile

memory device made from asymmetric $\text{Ta}_2\text{O}_{5-x}/\text{TaO}_{2-x}$ bilayer structures. *Nature Materials*, 10:625–630, Jul 2011.

- [105] Adnan Mehonic, Sebastien Cueff, Maciej Wojdak, Stephen Hudziak, Olivier Jambois, Christophe Labbe, Blas Garrido, Richard Rizk, and Anthony J. Kenyon. Resistive switching in silicon suboxide films. *Journal of Applied Physics*, 111(7):074507, 2012.
- [106] T. Driscoll, H.-T. Kim, B.-G. Chae, Massimiliano Di Ventra, and D. N. Basov. Phase-transition driven memristive system. 95(4):043503, 2009.
- [107] S L Johnson, A Sundararajan, D P Hunley, and D R Strachan. Memristive switching of single-component metallic nanowires. *Nanotechnology*, 21(12):125204, 2010.
- [108] Yiran Chen, Hai Li, and Xiaobin Wang. Spintronic devices: From memory to memristor. In *International Conference on Communications, Circuits and Systems*, pages 811–816, Jul 2010.
- [109] Xiaobin Wang and Yiran Chen. Spintronic memristor devices and application. In *Design, Automation Test in Europe Conference Exhibition (DATE), 2010*, pages 667–672, Mar 2010.
- [110] Xiaobin Wang, Yiran Chen, Haiwen Xi, Hai Li, and D. Dimitrov. Spintronic memristor through spin-torque-induced magnetization motion. *Electron Device Letters, IEEE*, 30(3):294–297, march 2009.
- [111] Yuriy V. Pershin and Massimiliano Di Ventra. Spin memristive systems: Spin memory effects in semiconductor spintronics. *Phys. Rev. B*, 78:113309, Sep 2008.
- [112] Tae Hee Kim, Eun Young Jang, Nyun Jong Lee, Deung Jang Choi, Kyung-Jin Lee, Jung tak Jang, Jin sil Choi, Seung Ho Moon, and Jinwoo Cheon. Nanoparticle assemblies as memristors. *Nano Letters*, 9(6):2229–2233, 2009.
- [113] John Paul Strachan, J. Joshua Yang, Ruth Munstermann, Andreas Scholl, Gilberto Medeiros-Ribeiro, Duncan R. Stewart, and Williams R. Stanley. Structural and chemical characterization of TiO_2 memristive devices by spatially-resolved NEXAFS. *Nanotechnology*, 20(48):485701, 2009.

- [114] Deok-Hwang Kwon, Kyung Min Kim, Jae Hyuck Jang, Jong Myeong Jeon, Min Hwan Lee, Gun Hwan Kim, Xiang-Shu Li, Gyeong-Su Park, Bora Lee, Seungwu Han, Miyoung Kim, and Cheol Seong Hwang. Atomic structure of conducting nanofilaments in TiO₂ resistive switching memory. *Nat Nano*, 5:148–153, 2010.
- [115] John Paul Strachan, Matthew D. Pickett, J. Joshua Yang, Shaul Aloni, A. L. David Kilcoyne, Gilberto Medeiros-Ribeiro, and Williams R. Stanley. Direct identification of the conducting channels in a functioning memristive device. *Advanced Materials*, 22(32):3573–3577, 2010.
- [116] Dmitri B. Strukov, Julien L. Borghetti, and Williams R. Stanley. Coupled ionic and electronic transport model of thin-film semiconductor memristive behavior. *Small*, 5(9):1058–1063, May 2009.
- [117] Dmitri B. Strukov and Williams R. Stanley. Exponential ionic drift: fast switching and low volatility of thin-film memristors. *Applied Physics A: Materials Science & Processing*, 94(3):515–519, Mar 2009.
- [118] Shimeng Yu, Jiale Liang, Yi Wu, and H-S Philip Wong. Read-write schemes analysis for novel complementary resistive switches in passive crossbar memory arrays. *Nanotechnology*, 21(46):465202, 2010.
- [119] Shimeng Yu and H.-S.P. Wong. Modeling the switching dynamics of programmable-metallization-cell (PMC) memory and its application as synapse device for a neuromorphic computation system. In *IEEE International Electron Devices Meeting*, pages 22.1.1–22.1.4, Dec 2010.
- [120] Omid Kavehei, Said Al-Sarawi, Kyoung-Rok Cho, Kamran Eshraghian, and Derek Abbott. An analytical approach for memristive nanoarchitectures. *ArXiv e-prints*, Jun 2011.
- [121] Zdenek Biolek, Dalibor Biolek, and Viera Biolkova. SPICE model of memristor with nonlinear dopant drift. *Radioengineering*, 18(2):210–214, Jun 2009.
- [122] Themis Prodromakis, Boon Pin Peh, Christos Papavassiliou, and Chris Toumazou. A versatile memristor model with nonlinear dopant kinetics. *IEEE Transactions on Electron Devices*, 58(9):3099–3105, Sep 2011.
- [123] S. Benderli and T.A. Wey. On SPICE macromodelling of TiO₂ memristors. *Electronics Letters*, 45(7):377–379, 2009.

- [124] Matthew D. Pickett, Dmitri B. Strukov, Julien L. Borghetti, J. Joshua Yang, Gregory S. Snider, Duncan R. Stewart, and Williams R. Stanley. Switching dynamics in titanium dioxide memristive devices. *Journal of Applied Physics*, 106(7), Oct 2009.
- [125] Sangho Shin, Kyungmin Kim, and Sung-Mo Kang. Compact models for memristors based on charge-flux constitutive relationships. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 29(4):590–598, Apr 2010.
- [126] K. Eshraghian, O. Kavehei, Kyoung-Rok Cho, J.M. Chappell, A. Iqbal, S.F. Al-Sarawi, and D. Abbott. Memristive device fundamentals and modeling: Applications to circuits and systems simulation. *Proceedings of the IEEE*, 100(6):1991–2007, Jun 2012.
- [127] Andrei D. Polyanin and Valentin F. Zaitsev. *Handbook of exact solutions for ordinary differential equations*. Chapman & Hall/CRC, 2nd edition, 2003.
- [128] Robert Spence. *Linear active networks*. Wiley-Interscience, 1970.
- [129] Wai-Kai Chen and Run-Sheng Liang. A general n-port network reciprocity theorem. *IEEE Transactions on Education*, 33(4):360–362, Nov 1990.
- [130] Leon O. Chua. Resistance switching memories are memristors. *Applied Physics A: Materials Science & Processing*, 102:765–783, 2011.
- [131] Tom M. Apostol. *Mathematical analysis*. Addison-Wesley Series in Mathematics. Addison-Wesley Pub. Co., 1st edition, 1957.
- [132] Themistoklis Prodromakis, Christofer Toumazou, and Leon O. Chua. Two centuries of memristors. *Nature Materials*, 11(6):478–481, Jun 2012.
- [133] Kamran Eshraghian, Kyoung-Rok Cho, Omid Kavehei, Soon-Ku Kang, Derek Abbott, and Sung-Mo Steve Kang. Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines. *IEEE Transactions on Very Large Scale Integration Systems*, 19(8):1407–1417, Aug 2011.
- [134] Singiresu S. Rao. *Engineering Optimization: Theory and Practice*. John Wiley and Sons, 2009.

- [135] Leon O. Chua and Charles A. Desoer. *Linear and Non Linear Circuits*. McGraw-Hill Education, 1987.
- [136] Emmanuel M. Drakakis. The bernoulli cell: A transistor-level approach for log-domain filters. *PhD Thesis, Imperial College London*, Feb 2000.
- [137] Emmanuel M. Drakakis, S.N. Yaliraki, and M. Barahona. Memristors and bernoulli dynamics. In *Proceedings of the IEEE 12th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, pages 1–6, feb. 2010.
- [138] Paul F Byrd and Morris D Friedman. *Handbook of Elliptic Integrals for Engineers and Scientists*. Springer-Verlag, 2nd edition, 1971.
- [139] I.S. Gradshteyn and I.M. Ryzhik. *Table of Integrals, Series, and Products*. Elsevier Academic Press, 7th edition, 2007.
- [140] Raymond A. DeCarlo and Pen-Min Lin. *Linear Circuit Analysis: Time Domain, Phasor, and Laplace Transform Approaches*. The Oxford Series in Electrical and Computer Engineering Series. Oxford University Press, 2001.
- [141] A.V. Oppenheim, A.S. Willsky, and S.H. Nawab. *Signals and systems*. Prentice-Hall signal processing series. Prentice Hall, 1997.
- [142] B.P. Lathi and Zhi Ding. *Modern digital and analog communication systems*. The Oxford series in electrical and computer engineering. Oxford University Press, 1998.
- [143] Francisco C. De La Rosa. *Harmonics and power systems*. The Electric Power Engineering Series. CRC/Taylor & Francis, 2006.
- [144] P.R. Gray. *Analysis and Design of Analog Integrated Circuits*. Analysis and Design of Analog Integrated Circuits. John Wiley & Sons, 2009.
- [145] Paul Penfield, Robert Spence, and Simon Duinker. *Tellegen's theorem and electrical networks*. M.I.T. Press research monographs. MIT Press, 1970.
- [146] Paul Penfield, Robert Spence, and Simon Duinker. A generalized form of Tellegen's theorem. *IEEE Transactions on Circuit Theory*, 17(3):302–305, Aug 1970.
- [147] Marianela Carrillo and Jose M Gonzalez. A new approach to modelling sigmoidal curves. *Technological Forecasting and Social Change*, 69(3):233 – 241, 2002.

- [148] Perrin Meyer and Jesse H. Ausubel. Carrying capacity: A model with logistically varying limits. *Technological Forecasting and Social Change*, 61(3):209–214, 1999.
- [149] Subhash C. Bhargava, Raj K. Bhargava, and Ashok Jain. Requirement of dimensional consistency in model equations: Diffusion models incorporating price and their applications. *Technological Forecasting and Social Change*, 41(2):177–188, 1992.
- [150] Dipak C. Jain and Ram C. Rao. Effect of price on the demand for durables: Modeling, estimation, and findings. *Journal of Business and Economic Statistics*, 8(2):163–170, 1990.
- [151] E. Miranda, D. Jimenez, and J. Sune. Progressive breakdown dynamics and entropy production in ultrathin SiO₂ gate oxides. *Applied Physics Letters*, 98(25):253504, 2011.
- [152] John A. Drakopoulos. Sigmoidal theory. *Fuzzy Sets and Systems*, 76(3):349–363, 1995.
- [153] Miljenko Marusic. Mathematical models of tumor growth. 1996.
- [154] D.A. Ratkowsky. *Nonlinear Regression Modeling: A Unified Practical Approach*. Statistics, textbooks and monographs. Marcel Dekker, 1986.
- [155] Jr. Turner, Malcolm E., Edwin L. Bradley, Katherine A. Kirk, and Kenneth M. Pruitt. A theory of growth. *Mathematical Biosciences*, 29(3-4):367–373, 1976.
- [156] Boris Zeide. Analysis of growth equations. *Forest Science*, 39(3):594–616, 1993.
- [157] Desta Fekedulegn, Mairitin P. Mac Siurtain, and Jim J. Colbert. Parameter estimation of nonlinear growth models in forestry. *Silva Fennica*, 4(33):327–336, Nov 1999.
- [158] A. Tsoularis and J. Wallace. Analysis of logistic growth models. *Mathematical Biosciences*, 179(1):21–55, 2002.
- [159] Roger Buis. On the generalization of the logistic law of growth. *Acta Biotheoretica*, 39:185–195, 1991.
- [160] M. Abramowitz and I.A. Stegun. *Handbook of Mathematical Functions: With Formulas, Graphs, and Mathematical Tables*. Applied mathematics series. Dover Publications, 1964.

- [161]W. Cai, F. Ellinger, R. Tetzlaff, and T. Schmidt. Abel dynamics of titanium dioxide memristor based on nonlinear ionic drift model. *arXiv*, May 2011.
- [162] Patryk Krzysteczko, Gunter Reiss, and Andy Thomas. Memristive switching of MgO based magnetic tunnel junctions. 95(11):112508, 2009.
- [163] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill series in electrical and computer engineering. McGraw-Hill Education, 2000.
- [164] Jan Mulder. *Static and Dynamic Translinear Circuits*. Delft University Press, 1998.
- [165]S. Vongehr. The missing memristor: Novel nanotechnology or rather new case study for the philosophy and sociology of science? *ArXiv e-prints*, Feb 2012.
- [166]G. I. Meijer. Who wins the nonvolatile memory race? *Science*, 319(5870):1625–1626, 2008.
- [167] Massimiliano Di Ventra, Yuriy V. Pershin, and Leon O. Chua. Circuit elements with memory: Memristors, memcapacitors, and meminductors. *Proceedings of the IEEE*, 97(10):1717–1724, Oct 2009.
- [168] Ricardo Riaza. First order devices, hybrid memristors, and the frontiers of non-linear circuit theory. *ArXiv e-prints*, Oct 2010.

