

Design and Analysis of a Single Switch DC-DC Boost Converter Based on Voltage Lift Technique

By

Shabir Ahmad

MASTER OF SCIENCE

IN

ELECTRICAL AND ELECTRONIC ENGINEERING



Department of Electrical and Electronic Engineering

Islamic University of Technology (IUT)

Board Bazar, Gazipur-1704, Bangladesh.

August 2020

CERTIFICATE OF APPROVAL

The thesis entitled “**Design and Analysis of a Single Switch DC-DC Boost Converter Based on Voltage Lift Technique**” submitted by Shabir Ahmad, Student No. 1710021016 of the Academic year 2019-20 has been found as satisfactory and accepted as partial fulfillment of the requirement for the Degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on August 28, 2020.

BOARD OF EXAMINERS:

1. _____ Chairman
Dr. Golam sarowar (Supervisor)
Professor
Department of Electrical and Electronic Engineering
Islamic University of Technology (IUT) Board Bazar, Gazipur-1704, Bangladesh.

2. _____ Member
Dr. Md. Ruhul Amin (Ex-Officio)
Professor & Head
Department of Electrical and Electronic Engineering
Islamic University of Technology (IUT) Board Bazar, Gazipur-1704, Bangladesh.

3. _____ Member
Dr. Ashik Ahmed
Professor
Department of Electrical and Electronic Engineering
Islamic University of Technology (IUT) Board Bazar, Gazipur-1704, Bangladesh.

4. _____ Member(External)
Dr. Md. Raju Ahmed
Professor
Department of Electrical and Electronic Engineering
Dhaka University of Engineering and Technology (DUET)
Gazipur-1707, Bangladesh.

DECLARATION OF CANDIDATE

It is hereby declared that this thesis report or any part of it has not been submitted elsewhere for the award of any Degree or Diploma.

Dr. Golam Sarowar
Professor
Department of Electrical and Electronic Engineering
Islamic University of Technology (IUT)
Date: August 28, 2020

Shabir Ahmad
Student No. 1710021016
Academic Year: 2019, 2020
Date: August 28, 2020

Table of Contents

Contents

CERTIFICATE OF APPROVAL.....	i
DECLARATION OF CANDIDATE.....	ii
List of Tables.....	iii
List of Figures.....	iv
Nomenclature.....	viii
Acknowledgments.....	ix
ABSTRACT.....	x
CHAPTER 1 INTRODUCTION AND BACKGROUND	1
1.1 Introduction:.....	1
1.2 Scope of the research work	2
1.3 Categories of step-up DC-DC converters	2
1.3.1 Nonisolated / Isolated	2
1.3.2 Unidirectional/Bidirectional	3
1.3.3 Voltage-Fed/Current-Fed.....	4
1.3.4 Hard Switched/Soft Switched.....	5
1.3.5 NMP/Minimum Phase	6
1.4 Statement of problem.....	6
1.5 Thesis Objective.....	7
1.6 Thesis Organization	8
CHAPTER 2 PERFORMANCE PARAMETERS OF DC-DC CONVERTER.....	9
2.1 Percentage ripple.....	9
2.2 Effect of parasitics	9
2.3 Converter parameter design	9
CHAPTER 3 PROPOSED CONVERTER AND OPERATING PRINCIPLE.....	14
3 The proposed converter structure.....	15
3.1 Operation of the proposed high step-up converter in CCM.....	16
3.1.1 Voltage and current equations of the inductor $L1$:.....	18
3.1.2 Voltage and current equations of the inductor $L2$:.....	18

3.1.3	Voltage and current equations of the inductor $L3$:	20
3.1.4	Voltage equations of the Diodes	21
3.2	Operation of the proposed high step-up converter in DCM	23
3.3	Calculation of critical inductance, rms and efficiency	29
3.3.1.	Current equations of the capacitor $C4$ are as follow:	29
3.3.2.	Current equations of Capacitor $C1$, during T_{on} and T_{off} are given as follow:	30
3.3.3.	Current equations of Capacitor $C2$, are given as follow:	31
3.4.	RMS calculation:	31
3.5.	Efficiency analysis:	34
CHAPTER 4 RESULT AND DISCUSSION		34
4.1	Comparison analysis with recent converters	36
4.2	Simulation and experimental results	38
4.3	Simulation and experimental results for CCM	39
4.4	Simulation and experimental results for DCM	47
4.5	Summary of the comparison results	49
CHAPTER 5 CONCLUSION AND FUTURE WORK		52
5.	Conclusion	53
5.1	Summary	53
5.2	Research contribution	50
5.3	Recommendation for future work	541
References:		55

List of Tables

Table 4.1	Comparison summary between the proposed converter and other high gain converters37
Table 4.2.	Switch current comparison between the proposed converter and other high gain converters37
Table 4.3	Specifications of the proposed converter in CCM39
Table 4.4	Comparison of simulation and experimental results of the proposed converter in CCM42
Table 4.5	Specifications of the proposed converter with parasitic elements42
Table 4.6	Power loss in conveter components and efficiency46
Table 4.7	Specifications of the proposed converter in DCM47
Table 4.8	Comparison of simulation and experimental results of the proposed converter in DCM.47

List of Figures

Figure 1.1	Categorization of step-up dc-dc converters 2
Figure 1.2	Isolated and nonisolated dc-dc converter structures; (a) Single-stage (b) floated output and (c) common grounded nonisolated dc-dc converters3
Figure 1.3	Unidirectional and bidirectional dc-dc converter structures. (a) Nonisolated Buck and (b) bidirectional boost dc-dc converter, (c) isolated full bridge, and (d) bidirectional DAB dc-dc converter 4
Figure 1.4	Current- and voltage-fed converter structures. (a) Current-fed full-bridge structure. (b) Voltage-fed full-bridge structure 5
Figure 1.5	Various soft switching cells with auxiliary circuits 5
Figure 1.6	Different structures of minimum-phase boost converters. (a) Boost converter with single switch, (b) Boost converter with two active switches. (c) Boost converter with magnetic coupling 6
Figure 2.1	Output voltage ripple 9
Figure 2.2	Effect of the parasitic elements on conversion ratio 10
Figure 2.3	Conventional boost with inclusion of winding resistance 10
Figure 2.4	Effect of RL on voltage gain 11
Figure 2.5	Efficiency vs. duty cycle, Conventional boost12
Figure 3.1	Structure of the proposed converter16
Figure 3.2	Proposed converter structure; (a) During on-switching; (c) During Off- switching16
Figure 3.3	The current and voltage waveforms in CCM for; Capacitor C1, C2, C3 and C4.17
Figure 3.4	The current and voltage waveforms in CCM for; Capacitor C1, C2, C3 and C421
Figure 3.5	The current and voltage waveforms in CCM for; Diode D1, D2, D3 and D422
Figure 3.6	Proposed converter during discontinuous current time (t_2 , t_3)24
Figure 3.7	The current and voltage waveforms in DCM for; inductors L1, L2 and L3.25
Figure 3.8	The current and voltage waveforms in DCM for; (a) Capacitors C1, C2; (b) Capacitors C3 and C425
Figure 3.9	The current and voltage waveforms in DCM for ;(a) Diodes D1 and D2 ; (b) Diodes D3 and D4.27
Figure 4.1	Comparison between the proposed converter and other converters in terms of (a) Current stress and (b) Voltage gain38
Figure 4.2	Proposed converter Power circuit40
Figure 4.3	Voltage waveforms in CCM (simulation) for; (a) inductors; (b) capacitors; (c) switch and output 40
Figure 4.4	Current waveforms in CCM (simulation) for; (a) inductors;(b) Switch current41
Figure 4.5	Simulation waveforms in CCM for; (a) Diode voltages; (b) Diode currents41
Figure 4.6	Efficiency variation with Duty cycle43
Figure 4.7	Efficiency variation of the proposed and other recent converters43

	with duty	
Figure 4.8	Experimental waveforms in CCM for; (a) Output Voltage; (b) inductor L1 Current43
Figure 4.9	Experimental waveforms in CCM for; (a) inductor L2 Voltage; (b) inductor L3 Voltage44
Figure 4.10	Experimental waveforms in CCM for; (a) Capacitor C1 Voltage (b) Capacitor C2 Voltage; (c) Capacitor C3 Voltage (d) Diode D1 Voltage.45
Figure 4.11	Voltage waveforms (Experimental) in CCM for; (a) Diode D2; (b) Diode D3; (c) Diode D4; (d) Switch46
Figure 4.12	Current and voltage waveforms (simulation) in DCM for; (a) inductors L1, L2 and L3; (b) capacitor C1, C2, C3 and C447
Figure 4.13	Current and voltage waveforms (simulation) in DCM for Diodes (D1-D4)48
Figure 4.14	Voltage waveforms (Experimental) in DCM for; (a) inductor L1; (b) inductor L248
Figure 4.15	Voltage waveforms (Experimental) in DCM for; (a) capacitor C1; (b) inductor L349
Figure 4.16	Voltage waveforms (Experimental) in DCM for; (a) capacitor C2; (b) capacitor C349
Figure 4.17	Voltage waveforms (Experimental) in DCM for; (a) Diode D1; (b) Diode D250
Figure 4.18	Voltage waveforms (Experimental) in DCM for; (a) Diode D3; (b) Diode D4; (c) Capacitor C451
Figure 4.19	Voltage gain vs duty cycle (DCM operation)51

Nomenclature

$v_{L1,1}, v_{L2,1}, v_{L3,1}$	Inductors voltage at time interval T_{on}
$v_{L1,2}, v_{L2,2}, v_{L3,2}$	Inductors voltage at time interval T_{off}
$v_{C1,1}, v_{C2,1}, v_{C3,1}$	Capacitors voltage at time interval T_{on}
$v_{C1,2}, v_{C2,2}, v_{C3,2}$	Capacitors voltage at time interval T_{off}
$v_{D1}, v_{D2}, v_{D3}, v_{D4}$	Diodes voltages at time interval T_{off}
$v_{CV1}, v_{CV2}, v_{CV3}, v_{CV4},$	Capacitors discharge voltages
$v_{CP1}, v_{CP2}, v_{CP3}, v_{CP4},$	Capacitors peak-charge voltages
$i_{L1,1}, i_{L2,1}, i_{L3,1}$	Inductors current at time interval T_{on}
$i_{L1,2}, i_{L2,2}, i_{L3,2}$	Inductors current at time interval T_{off}
$i_{LV1}, i_{LV2}, i_{LV3}$	Inductors discharge current
$i_{LP1}, i_{LP2}, i_{LP3}$	Peak inductors current
$i_{C1,1}, i_{C2,1}, i_{C3,1}, i_{C4,1}$	Capacitors current at time interval T_{on}
$i_{C1,2}, i_{C2,2}, i_{C3,2}, i_{C4,2}$	Capacitors current at time interval T_{off}
$\Delta i_{L1}, \Delta i_{L2}, \Delta i_{L3}$	Inductors ripple current
 I_o, V_o, I_i, V_i	 The load (o) and source (i) average parameters
$C_{OSS}, Q_{rr}, r_s, t_r, t_f$	Switch parameters (Output capacitance, reverse recovery charge, series resistance, rise time and fall time).
 r_D, V_F	 Diode parameters (Diode series resistance and forward voltage drop).

Acknowledgments

First and foremost, I offer gratitude to the Almighty Allah (SWT) for giving me the capability to do this work with good health.

I want to express my sincere gratitude to my supervisor, Prof. Dr. Golam Sarowar, Department of Electrical and Electronic Engineering (EEE), Islamic university of technology (IUT), for his support and encouragement throughout this work. The valuable discussions with him gave me many vital impulses that contributed considerably to both my scientific and personal development. I am also indebted to all the faculty and staff members of the EEE department, IUT. My sincere thanks to all those who assisted me in connection with this work.

Finally, I am grateful to my family members, particularly my beloved Father, for his continuous support and inspiration.

ABSTRACT

Renewable energy systems (solar, fuel cells, batteries) are one of the trending research topics due to its ease of availability, sustainability, and environmental friendliness. DC-DC converters impart a crucial role in these renewable energy systems while boosting up the voltages to higher levels. In this thesis, a novel structure of DC-DC boost converter based on voltage lift technique is presented. The extensive analysis is performed for the proposed converter in continuous current mode (CCM) and discontinuous current mode (DCM) along with the voltage and current relations of converter elements and semiconductor devices. Moreover, critical values of inductors are determined to investigate the boundary conditions between CCM and DCM. It was firmly concluded that while considering the lesser number of elements and semiconductor devices for the same input voltage the proposed converter can yield comparatively high voltage gain than the conventional boost dc-dc converters. Root mean square (RMS) values of the voltages and currents for the elements and semiconductors are also calculated along with the converter's efficiency at various duty cycles. Simulation results of the proposed converter are provided in CCM and DCM using PSIM software. Finally, to avail the desired validation of acquired simulation results a laboratory prototype of the proposed converter is tested and comparisons were made with the theoretical analysis.

CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Introduction:

Advances in technology and sharp elevation in human living standards have caused significant augmentation in world energy demand over the last decade. To meet this growing energy demand employing the conventional power generation methods (using fossil fuels) induces adverse environmental effects, such as greenhouse effect, air pollution due to emission of SO₂ and Nitrogen oxides, etc. [1]. For years, researchers have demonstrated a substantial inclination towards the boundless other alternate energy sources such as fuel cells, wind energy, photovoltaic (PV) systems, and batteries that feature cleanliness and sustainability. However, energy resources such as principally photovoltaic cells and fuel cells yield significantly lower voltage levels (up to 50V). Therefore, step-up converters are greatly encouraged to boost up this low level voltage for various applications [2, 3]. Conventional non-isolated step-up PWM converters such as boost, buck-boost, and SEPIC, etc., possess noticeable features in regards to its simplicity and cost-effectivity. Unfortunately, the gain of these converters is limited due to circuit parameters and operation at high duty cycles to attain high voltage gains, which in results reduces the converter efficiency to a paramount extent. Various voltage-boosting techniques have been elucidated in the literature to achieve augmented gain while operating at low duty ratios and improved efficiency [4, 5, 6].

Major voltage-boosting techniques that can be found in the literature are segregated into five categories, i.e., switched inductor, voltage multiplier, voltage lift (VL), switched capacitor (SC), magnetic coupling, and multistage/-level converters. New power converter topologies with the inclusion of the above voltage-boosting techniques are continuously being proposed and developed to meet the rising demand for power conversion applications [7]. Switched-capacitor can achieve high-voltage conversion gain [8-9]. However, these converters require a number of switches, which increases the complexity of the control strategies and associated driving circuitry. This converter topology also suffers from poor regulation, which results in pulsating input current. A number of voltage multiplier circuits are presented in the literature for high boost applications as they can be implemented easily in any circuit [10, 11]. However, a number of cells required for high gains also multiplies, which results in enhanced power loss, cost, and circuit size. The magnetic coupling-based boosting technique for isolated and non-isolated converters is consistently proposed [12, 13]. Even though, these converters have dominant boost ability; however, they suffer from obvious drawbacks. For instance, leakage inductance must be recycled to avoid large voltage spikes. Furthermore, with the increment of turns ratio converter size also tends to rise. Multilevel DC-DC converters are suitable for high-power high-voltage applications [14, 15]. Despite various noticeable advantages such as high-power density, modularity structure, and reliability, these converters also require a large number of components, high-priced and deteriorated efficiency, due to a higher number of stages.

Eventually, among the aforementioned voltage-boosting techniques, voltage lift (VL) technique is a prestigious, relatively simple and amenable in many converters. This technique has been widely employed in the literature introduced by Luo (VL Luo converters) [16, 17]. VL

technique utilizes fundamental energy storage elements i.e; inductors and capacitors in combination with power semiconductor switches and diodes to boost the input voltage level to higher voltage levels. The energy storage elements transfer the low input energy (in steps) to the output capacitor with a much higher level because of its storage capabilities. High power density, greater efficiency, plain structure and cost-effectiveness, and small output voltage ripple as compared to the other techniques are the crucial features of this technique. Furthermore, absence of additional switches which complicates the control scheme of the converter is a prominent outcome of this technique.

1.2 Scope of the research work

In this thesis, a modified non-isolated structure of a conventional boost converter using a single switch is proposed to achieve a high voltage gain. The proposed converter possesses the capability of achieving high voltage gain at a reasonable duty cycle condition, which makes it more suitable for medium and high voltage applications for instance in DC microgrids, they can be used to interface various low power voltage sources like batteries, photovoltaic (PV) panels and fuel cells into a common DC bus (380V). This common bus is further coupled to the AC grid through a centralized DC/AC inverter. The extensive operation of the proposed converter is also analyzed in both CCM and DCM while the current and voltage equations of each converter element are extracted. In order to determine the operation mode of the converter, critical values of inductors are extracted to distinguish between CCM and DCM. The efficiency of the proposed converter is calculated, and a detailed comparison of efficiency change with the duty cycle is illustrated.

1.3 Types of step-up dc-dc converters

A broad classification of step-up dc-dc converters is illustrated in Figure 1.1. The main features and respective major circuits of each class are explained in the following sections.

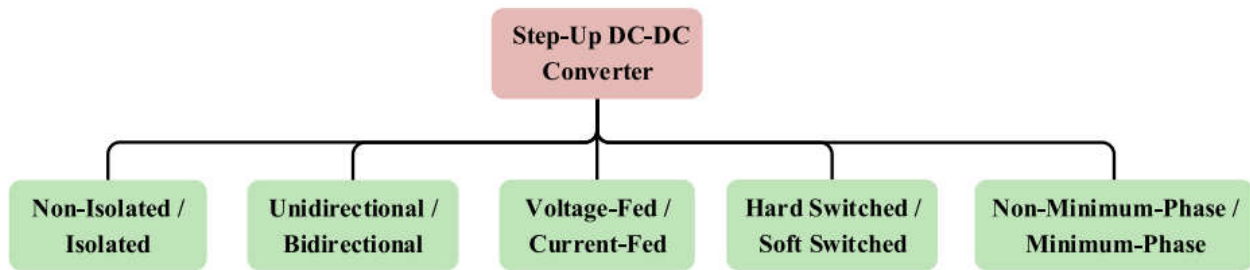


Figure 1.1 Categorization of step-up dc-dc converters

1.3.1 Nonisolated / Isolated

Non-isolated DC-DC converters usually make use of inductors and there is no dielectric separation between the input and the output. Figure. 1.2 (a) illustrates a basic nonisolated PWM boost dc-dc converter which is comprised of three components i.e; a diode, a switch, and an inductor. Figure 1.2(b) shows a general three-level boost converter with floated output. Due to their relatively smaller size, low cost, and lower switching losses and elevated efficiency, significant research has been conducted on the study of nonisolated dc-dc converters. Moreover, nonisolated dc-dc converters does not necessarily require magnetic coupling to be built.

Nonisolated structures with magnetic coupling are used when high voltage gain and efficiency is a major concern.

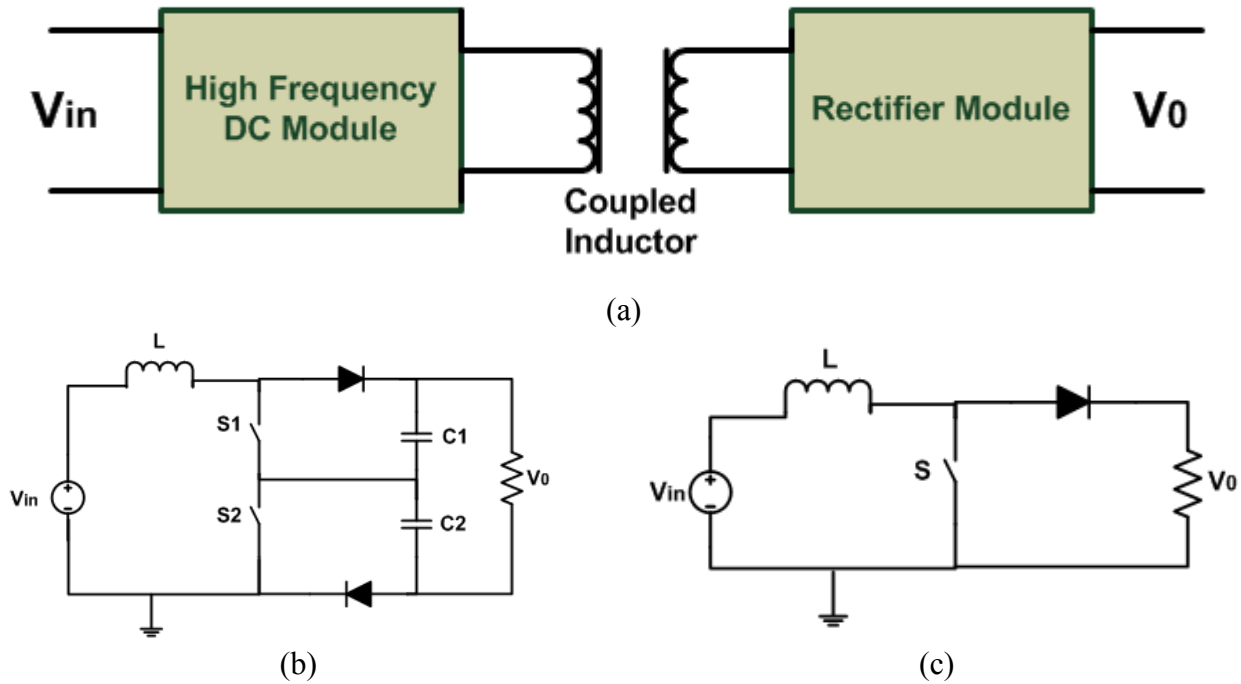


Figure 1.2. Various isolated and nonisolated converter circuits; (a) isolated single-stage (b) nonisolated three-level boost converter and (c) nonisolated DC-DC boost converter.

Transformer or coupled inductor is used to achieve electrical isolation between the input and output. Electrical isolation is typically essential for loads which are prone to noise and faults and when security is a major concern. For example in medical, avionics and military applications. Figure. 1.2(c) illustrates the diagram of an isolated coupled inductor based dc-dc converter.

1.3.2 Unidirectional/Bidirectional

Such converters utilize unidirectional semiconductors for example diodes and power MOSFETs, which take into account unidirectional power flow. Examples of some unidirectional dc-dc converters are demonstrated in Figure. 1.3(a). These converters utilizes single-quadrant switches and hence current can not flow in the reverse direction.

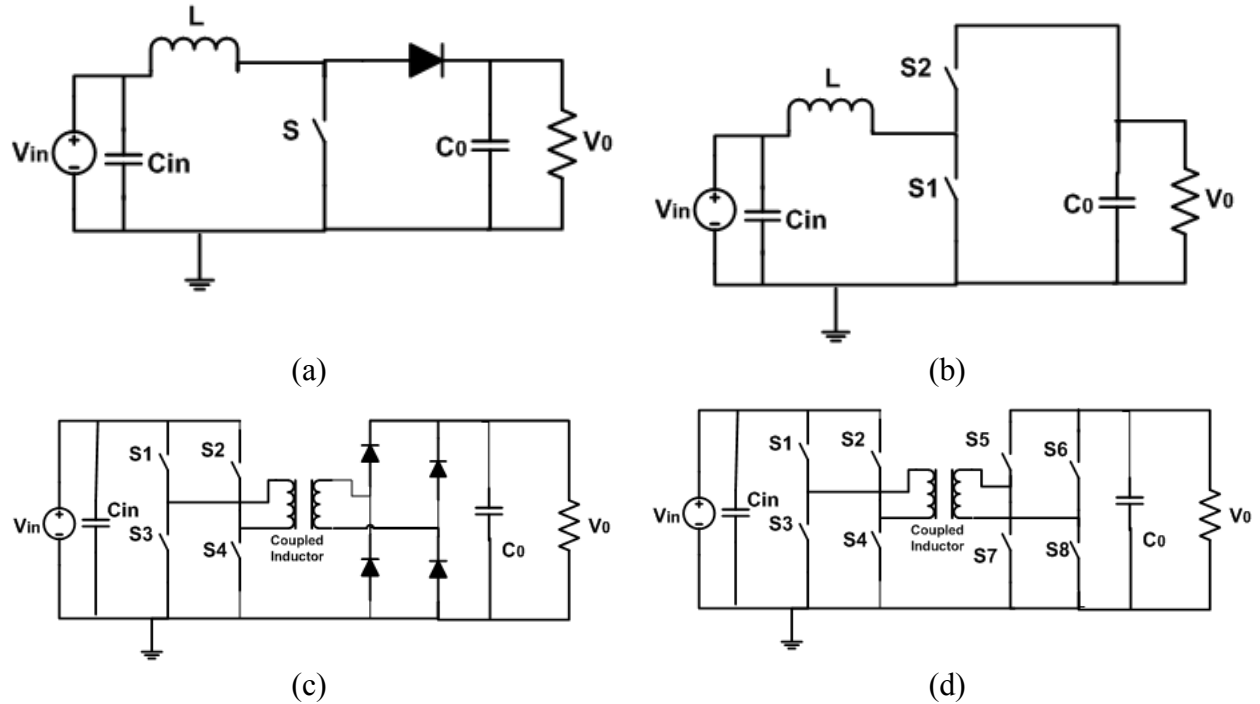


Figure 1.3. Unidirectional and bidirectional DC-DC converter structures. (a) Nonisolated Boost and (b) bidirectional boost DC-DC converter, (c) isolated full bridge, and (d) bidirectional DAB DC-DC converter.

Figure. 1.3(b) demonstrates the bi-directional arrangement of a nonisolated dc-dc converter. In these converters two-quadrant switches are employed which allows for bidirectional current flow.

Unidirectional step up converters are appropriate for applications where high output voltage is required and losses due to diodes do not affect the circuit's efficiency. Conversely, bidirectional dc-dc converters are suitable for applications where low output voltage is expected and diodes losses become dominant. Figure. 1.3(c) illustrates diagram of an isolated unidirectional dc-dc converter. The converter consist of inverter stage and then high-frequency transformer next to rectification stage.

The increased demand for applications with bidirectional energy transfer has led to the enlarged usage of bidirectional dc-dc converters. Converters with bidirectional capability are used in railway transportation, renewable energy systems, automotive transportation, aerospace applications, uninterruptable power supplies, elevators and escalators, supercapacitors, batteries, smart grid applications etc. Figure. 1.3(d) demonstrates schematic diagram of an isolated bidirectional dual active bridge (DAB) converter, which is a popular type of isolated bidirectional dc-dc converter.

1.3.3 Voltage-Fed/Current-Fed

Based on the input circuitry, DC-DC converters are classified into voltage-fed and current-fed converters. The voltage-fed converter consist of an input filter capacitor (C_{in}) and generally

convert the input voltage to a lower output. Voltage-fed full-bridge converter can be utilized for high-power applications. The schematic diagram is demonstrated in Figure. 1.4(a). On the other hand, current-fed DC-DC converters comprises an input inductor and capable to convert the input voltage to a higher output voltage.

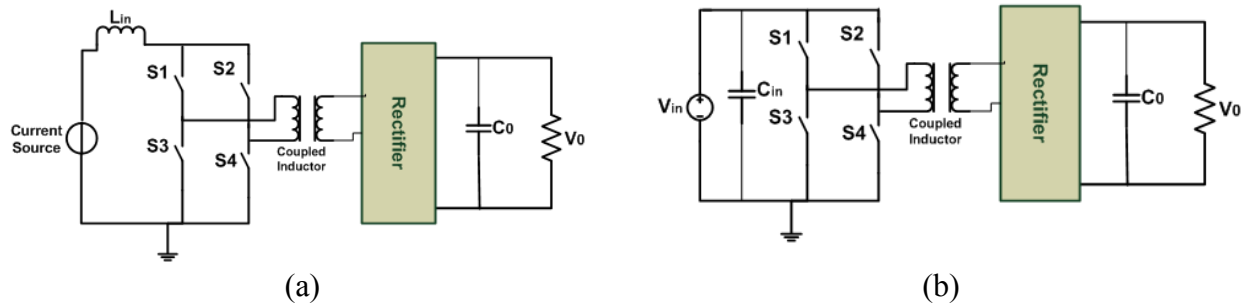


Figure 1.4. Current- and voltage-fed converter structures. (a) Current-fed full-bridge structure. (b) Voltage-fed full-bridge structure.

Current-fed converters are suitable for low voltage applications for instance photovoltaics and fuel cells. The input inductor supplies continuous input current, particularly with small ripple.

1.3.4 Hard Switched/Soft Switched

Hard-switched converters suffer from EMI issues due to high dv/dt and di/dt at switching transition. High switching frequency operation is restricted in such converters as switching losses is proportional to frequency. Nevertheless, increasing power density calls for the high-frequency operation of dc-dc converters which lessen the size of the storage components. On the contrary, soft-switched converters can trim down the above drawbacks by utilizing stray inductance and capacitance to attain zero-voltage switching or zero-current switching. During switching transitions voltage and current are zero and hence the converter can operate at relatively high switching frequency, which reduces size and weight of the converter. Figure. 1.5 illustrates a universal switch cell type dc-dc converter.

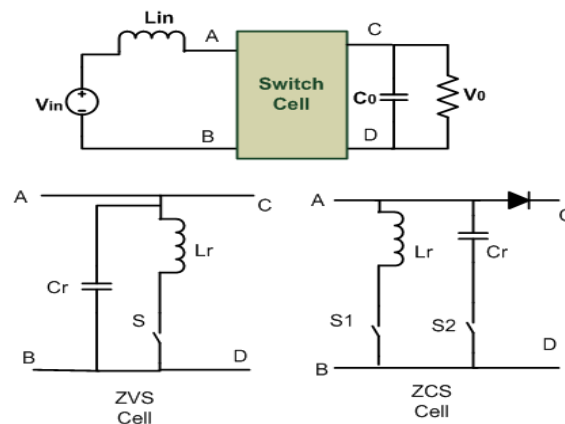


Figure 1.5. Different soft-switching cells (ZVS and ZCS).

1.3.5 Non-minimum phase (NMP)/Minimum Phase (MP)

NMP converters contains a right half plane (RHP) zero in their transfer function. Designing a Controller for such converters is somehow complex because of the fact that the closed-loop poles are liable to move towards right half plane as the gain increases in conventional controllers which causes destabilization of the system. Therefore, conventional controllers will not serve the purpose of achieving high converter gain . Different techniques can be used to minimize the effect of the RHP zero in step-up converters..

Tristate boost converters eradicate the RHP zero and are used in applications where fast-response boost action is required. A tristate boost converter is illustrated in Figure. 1.6(a).The RHP zero can be entirely removed at the preferred operating point by applying a proper control technique on the converter. Another circuit with no RHP zero is demonstrated in Figure. 1.6(b). Another way to eradicate RHP zero is to use magnetic coupling as shown in Figure. 1.6(c).

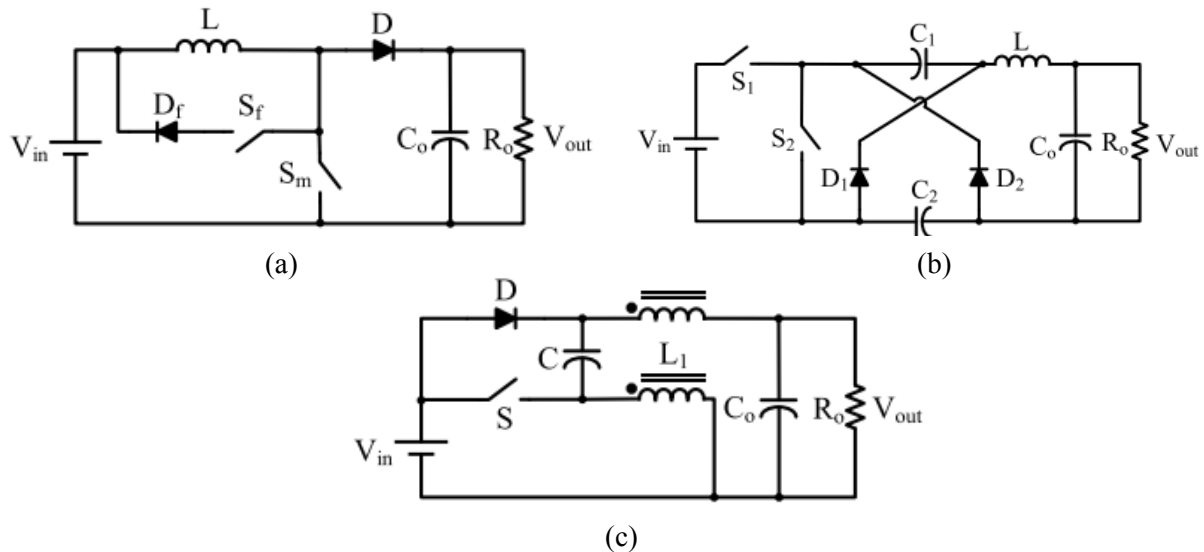


Figure 1.6. Different structures of minimum-phase boost converters. (a) Boost converter with single switch, (b) Boost converter with two active switches. (c) Boost converter with magnetic coupling.

1.4 Statement of the Problem

A PWM boost converter is an essential voltage boost circuit with numerous features that make it suitable for a range of applications such as renewable energy systems, fuel cells etc. The extensive applications of high boost converters is due to its low number of elements, simple design implementation, and manufacturing.

A significant research has been conducted in achieving efficient, reliable, small-sized, and light-weight boost converters for diverse power applications. A few of these demands can be merely

accomplished by using second-order, third-order, and fourth-order fundamental converters, e.g., Cuk, boost, SEPIC and Zeta converters. Moreover, basic push-pull, flyback, half-, and full-bridge converters are even prevalent and are used in various applications. However, more complicated recent topologies that employ different voltage-boosting techniques are also presented in the literature for instance interleaved, multilevel, or cascaded topologies, or using voltage multiplier cells (VMC) [18]–[22]. However, for applications with the low input voltage but high output voltage, these conventional converters suffer from increased voltage stress on the semiconductor devices and circuit elements. Furthermore, the converter has to operate at extreme duty cycles, which in result, induce significant power loss. Various circuits (combined switched capacitors (SCs) and/or coupled inductors) and techniques are presented to boost the voltage level while operating at low duty cycles. A new hybrid DC-DC converter is presented in [23], different switched capacitors techniques and coupled inductors are merged with a conventional boost converter to achieve high voltage gain. The advantages of this technique are high voltage, low current and voltage stress on elements, and using a single switch. However, the converter has a large number of components, which results in increased cost, losses, and size of the converter. Converter presented in [24] can achieve high voltage gain at low duty cycles, and the structure can be extended to n stages, which further increases the voltage gain of the converter. The voltage stress on the components compared with output voltage is decreased. However, a number of switches are employed, which complicates the control tactics, and hence the cost as separate driving circuitry is required to drive the switches. A new structure by combining coupled inductor and voltage lift technique is presented in [25]. High voltage gain can be achieved by adjusting the turns ratio of the coupled inductor, and stress on semiconductors is low; however, the voltage gain is proportional to the turns ratio of the coupled inductor, which increases the size and causes EMI issues. A new topology of step-up dc-dc converter using voltage lift technique is proposed in [26]. Capacitor–inductor–capacitor (CLC) cells are developed to increase the voltage gain, and the converter can further be extended to N -lift topology to boost up the voltage gain. The converter employs a single switch and has low switching voltage; however, high voltage gain is achieved at the price of utilizing a large number of elements, which degrades converter efficiency and also increases the cost.

1.5 Thesis Objective

The principal objective of this research work is to design and analyze a novel single-switch DC-DC boost converter, capable of achieving high voltage gain with the minimal number of circuit components. However, more specifically, the goals include:

- a. To design a novel single-switch DC-DC Boost coveter with high voltage gain based on voltage lift technique.
- b. To determine the critical value of inductor of the proposed converter for CCM and DCM operation.

- c. To implement a prototype of the proposed converter in the laboratory and analyze the performance.
- d. To compare the performance of the proposed converter with the existing converters.

1.6 Thesis Organization

The writeup for this research work can be organized as follows:

In chapter two, The performance parameters of DC converters are discussed. The effect of parasitic elements on the converter's voltage gain and efficiency is studied extensively. Graphs of efficiency vs. duty cycle and gain vs. duty cycle in the presence of parasitic elements are demonstrated.

In chapter three, the operation of the proposed structure in CCM and DCM is studied in detail. The fundamental waveforms (current and voltage) of the proposed circuit elements is demonstrated, which is performed in PSIM software. Moreover, numerous critical current and voltage relations are also established along with the voltage gain of the converter in CCM operation. Furthermore, Relations of the critical inductance of the inductors are extracted by applying boundary conditions to determine the mode of operation of the proposed converter. Voltage and current RMS values are calculated, and the efficiency of the converter is analyzed in detail.

In chapter four, The comparison analysis between the proposed converter and other recent converters is studied exhaustively. Current stress and voltage gain of the currently proposed converter is compared with some recently proposed converters while considering the least number of components count for the same input voltage. The significant results obtained from Software simulations performed in PSIM and experimental outcomes (both CCM and DCM operations) from laboratory prototype are provided to acutely acquire their validations. Power loss in each converter element is computed, and the converter's efficiency is analyzed at various duty cycles.

In chapter five, the research work presented in this thesis is summarized, and key results are displayed. The possible modification and control strategy of the proposed converter is to be studied in the future.

CHAPTER 2

PERFORMANCE PARAMETERS OF DC-DC CONVERTER

In this thesis, the analysis of the converter is performed, realizing the inductors current and capacitors voltage ripple to be ignored. The converter components such as a switch, diode, and passive components are considered ideal. Nonidealities or parasitics of practical devices and components may, however, greatly affect some performance parameters of the dc-dc converter such as efficiency, voltage gain, and percentage ripple.

2.1 Percentage Ripple

The actual output voltage consists of a desired dc component voltage, plus a small undesired ac component, as shown in **Figure 2.1**. It is impossible to build a perfect low pass filter that allows the dc component to pass but completely remove the components at the switching frequency and its harmonics. so the low pass filter must allow at least some small amount of high-frequency harmonics generated by the switch to reach the output.

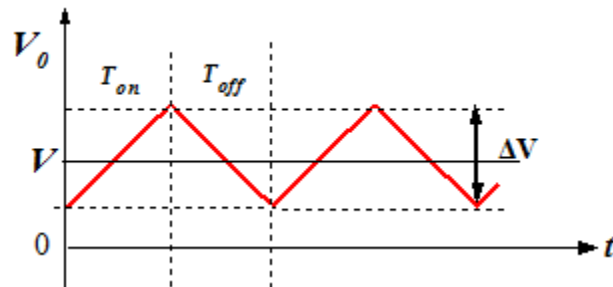


Figure 2.1. Output voltage ripple.

The output voltage switching ripple should be small in any well-designed converter, since the goal is to produce dc output. For example, in a computer power supply having a 3.3 V output, the switching ripple is normally required to be less than a few tens of millivolts, or less than 1% of the dc component. Therefore it is always a good approximation to assume that the magnitude of the switching ripple is much smaller than the dc voltage. This approximation, known as small ripple approximation, greatly simplifies the analysis of the converter and is used in this thesis.

2.2 Effect of Parasitics

The parasitic elements in the proposed converter are due to the losses associated with the inductors, the capacitors, the switch and the diode. **Figure 2.2** qualitatively shows the effect of these parasitics on the voltage transfer ratio. Unlike the ideal characteristics, in practice, V_o / V_i declines as the duty ratio approaches unity. The parasitic elements have been ignored in the the simplified analysis presented in the succeeding sections; however, practically they can not be avoided and their effect is taken into consideration.

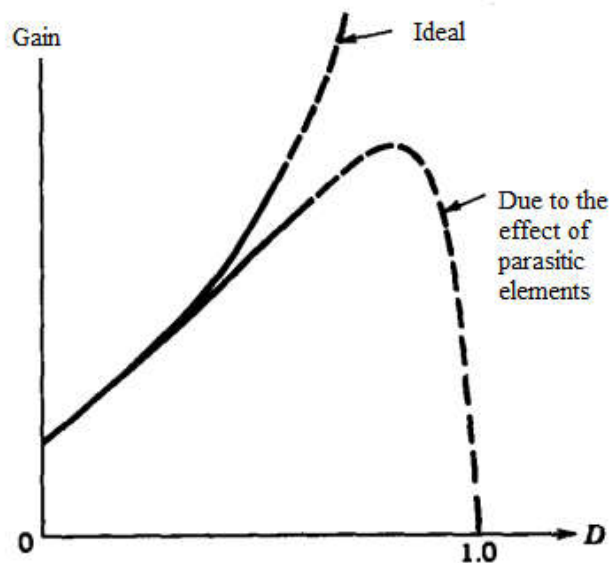


Figure 2.2 Effect of the parasitic elements on conversion ratio.

To elaborately explain the effect of the parasitics, taking the example of a conventional boost converter with the inclusion of induction copper loss (resistance of winding), as shown in **Figure 2.3**.

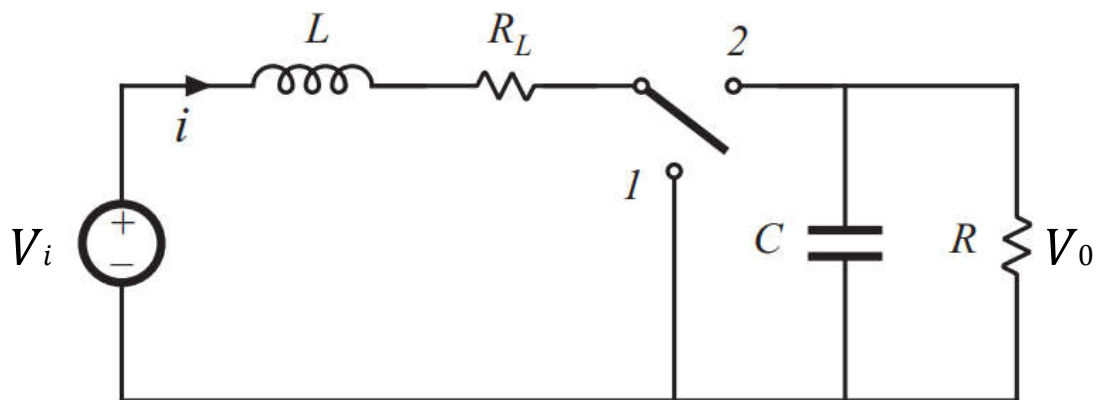


Figure 2.3. Conventional boost with the inclusion of winding resistance.

The final gain equation can be written as follow:

$$\frac{V_0}{V_i} = \frac{1}{D'(1 + R_L / D^2 R)} \quad (2.1)$$

Where D' is the off-switching time.

The plot of voltage gain vs. D for various R_L is shown in **Figure 2.4**. It can be seen that equation (2.1) has two terms. The 1st term $\frac{1}{D'}$ represents ideal conversion ratio excluding R_L . The 2nd term, $\frac{1}{(1 + R_L / D^2 R)}$, represent the effect of the winding resistance. The gain will be approximately equal to ideal conversion ratio $\frac{1}{D'}$ if R_L is much smaller than the product $D^2 R$. If the value of R_L is considerable then the gain $\frac{V_0}{V_i}$ will have reduced value compared with the ideal value.

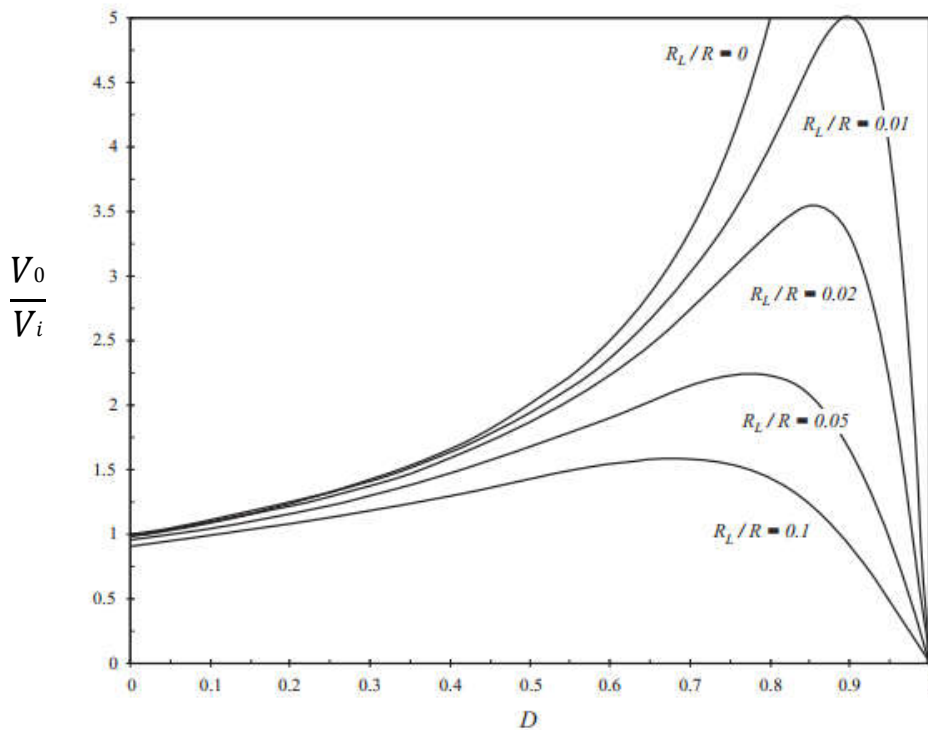


Figure 2.4. Effect of R_L on voltage gain.

When the duty cycle is unity, the inductor series resistance R_L causes significant change in the $\frac{V_0}{V_i}$ vs D graph. The gain should approach infinity as D approaches 1 but actually the curve trim

down to zero. The reason is that when duty cycle is unity, the switch is always in on position. There will be no connection between the inductor and the output, so no energy will be transferred to the output, and the output will become zero. The efficiency relation of the converter is written as follow:

$$\eta = \frac{1}{(1 + R_L / D'^2 R)}$$

The current in the inductor will tends to rise and its value is limited only by the inductor series resistance R_L . A significant power is lost, while no power is transferred to the load; therefore, we can assume that the converter efficiency tends to zero at unity duty cycle, as illustrated in **Figure 2.5**.

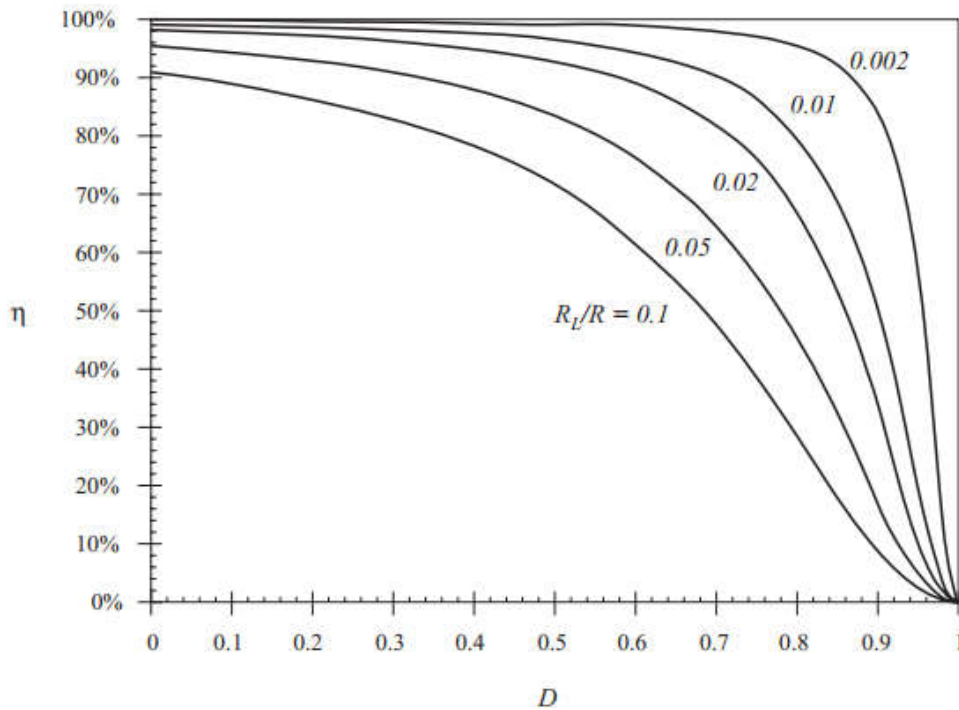


Figure 2.5. Efficiency vs. duty cycle, Conventional boost.

The example discussed here is fairly straightforward, wherein only one loss component is present. Practicable converters are considerably more complicated and contain a large number of loss components.

2.3. Converter parameters Design.

Design of inductors and capacitors is based on the permissible voltage and current fluctuation range. The voltage and current stress on elements is also an important design consideration.

The inductor L_l can be designed based on the fundamental inductor voltage relation:

$$v_{L1,1} = V_i = L_1 \frac{di_{L1,1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{on}}$$

The value of Δi_{L1} is restricted by permissible fluctuation limit i.e. $x\%$ of i_{L1} . Various applications have certain permissible fluctuation range which should not be increased above that range for smooth operation. From above relation Inductor L_1 is calculated as:

$$L_1 = \frac{V_i D}{\%x_{L1} i_{L1} f} = \frac{V_i D (1-D)^2}{\%x I_0 (1+D) f}$$

Similarly the value of inductor L_2 can be calculated as:

$$v_{L2,1} = L_2 \frac{di_{L2,1}}{dt} = L_2 \frac{\Delta i_{L2}}{T_{on}} = v_{C2,1} = \frac{V_i}{(1-D)}$$

$$L_2 = \frac{v_{C2} D}{\%x i_{L2} f} = \frac{V_i D}{\%x I_0 (1+D) f}$$

Also, inductor L_3 is calculated as:

$$v_{L3,2} = L_3 \frac{di_{L3,2}}{dt} = L_3 \frac{\Delta i_{L3}}{T_{off}} = v_{C3,2}$$

$$L_3 = \frac{v_{C3} (1-D)}{\%x i_{L3} f} = \frac{V_0 (1-D)^2 - V_i}{(1-D) \%x I_0 f}$$

By similar arguments, capacitor C_1 can be calculated from the fundamental current relation:

$$i_{C1,1} = C_1 \frac{dv_{C1,1}}{dt} = C_1 \frac{\Delta v_{C1}}{T_{on}}$$

$$C_1 = \frac{i_{C1,1} D}{\%x v_{C1} f} = \frac{I_0 D (1-D)^2}{\%x V_i (2D - D^2) f}$$

Also capacitor C_2 is calculated as:

$$i_{C2,1} = C_2 \frac{dv_{C2,1}}{dt} = C_2 \frac{\Delta v_{C2}}{T_{on}}$$

$$C_2 = \frac{i_{C2,1} D}{\%x v_{C2} f} = \frac{I_0 D (1+D)}{\%x V_i f}$$

Similarly capacitor C_3 is calculated as follow:

$$i_{C3,1} = C_3 \frac{dv_{C3,1}}{dt} = C_3 \frac{\Delta v_{C3}}{T_{on}}$$

$$C_3 = \frac{i_{C3,1} D}{\%xv_{C3} f} = \frac{I_0 D (1-D)^2}{\%x(V_0(1-D)^2 - V_i) f}$$

And capacitor C_4 is calculated as:

$$i_{C4,1} = C_4 \frac{dv_{C4,1}}{dt} = C_4 \frac{\Delta v_{C4}}{T_{on}}$$

$$C_4 = \frac{i_{C4,1} D}{\%xv_{C4} f} = \frac{I_0 D}{\%xV_0 f}$$

CHAPTER 3

PROPOSED CONVERTER AND OPERATING PRINCIPLE

3.0 The proposed Converter structure

The proposed structure elucidated in **Figure 3.1**. Which is encompassed of three inductors, a single switch, four capacitors, and four diodes. The operation of the switch is controlled by a PWM technique with a switching frequency of 25 kHz. To simplify the analysis of the proposed converter, few assumptions are made. i) To eradicate the inconsistent behavior of the converter, the steady-state operation of the converter is considered. ii) The voltage ripple for each capacitor is neglected due to a sufficiently large capacitor value; therefore, the capacitor's voltage in each switching period is identical. iii) The switch and diodes are considered ideal.

The voltage-lift technique has been employed to boost the output voltage. Voltage-lift technique was first introduced by Luo (and the converters are called Luo converters). The voltage-lift technique basically utilizes inductors and capacitors to store the input energy and transfers this energy to the output at higher level. These elements act like electronic charge pump which takes the energy in one step and then releases it in the next step. For instance, in the proposed circuit, inductor L_1 and capacitor C_2 act as primary sources of storing the input energy. This stored energy is then transferred by inductor L_2 and capacitor C_1 and finally the energy is transferred to the output capacitor by the inductor L_3 and capacitor C_3 .

The input voltage is augmented in steps and finally transferred to the output capacitor. During the on-switching period, the input energy is stored in the magnetic field of the inductor L_1 , while inductors L_2 and L_3 are getting the energy from capacitors C_1 and C_2 (energy stored during off-switching). In the next cycle, when the switch is off, inductors L_2 and L_3 transfer the stored energy to the capacitors C_2 and C_4 (output). In this way, the energy is transferred by the storage elements to the output with amplitude greatly enhanced than the input.

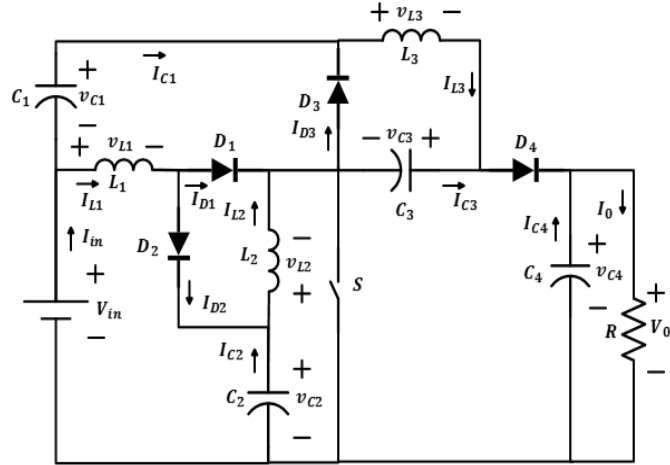


Figure 3.1 Structure of the proposed step-up converter.

3.1. Operation of the proposed high step-up converter in CCM.

In this section, the key focus is given to extensively elaborate the CCM operation of the proposed circuit performed in PSIM software. The overview of the various waveforms is presented for capacitors, diodes, switch, and inductors, which incorporates both on-switching and off-switching states. Moreover, various prominent current and voltage relations are also demonstrated availed theoretically. The proposed converter structure during CCM operation is shown in **Figure 3.2**.

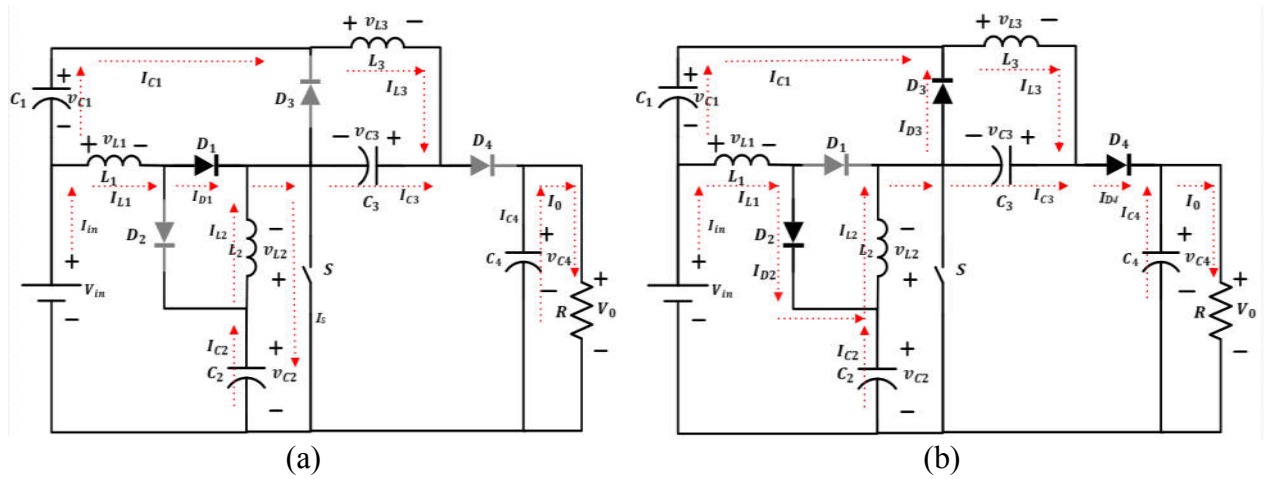


Figure 3.2 Proposed converter structure; (a) During on-switching; (b) During Off-switching

During the on switching period, diodes D_2 , D_3 and D_4 are reverse biased and diode D_1 is forward biased. In this state, supply voltage V_i is providing energy to the inductor L_1 and hence its current value is linearly increased from its minimum value (I_{LV1}) to its peak value (I_{LP1}), as illustrated in

Figure 3.3. In the meanwhile, Capacitor C_2 is discharged through the inductor L_2 by releasing its stored energy. The voltage of the Capacitor C_2 is dropped to the lowest value v_{CV2} and inductor L_2 current is raised from the lowest value I_{LV2} to its highest value I_{LP2} . Also, the capacitor C_1 is discharged through the inductor L_3 and capacitor C_3 . As a result, capacitor C_1 voltage is dropped to the lowest value v_{CV1} and current in the inductor L_3 is augmented from its minimum value I_{LV3} to its maximum value I_{LP3} , while the voltage of the capacitor C_3 is raised from its minimum value v_{CV3} to its maximum value v_{CP3} as shown in **Figure 3.4**. During on-period, the load is isolated from rest of the circuit as D_4 is reverse biased, capacitor C_4 is providing energy to the load and its voltage is dropped from its maximum value v_{CP4} to the lowest value v_{CV4} .

During the off-switching period, diodes D_2, D_3 and D_4 are forward biased and diode D_1 is reverse biased. Inductor L_1 is providing energy to Capacitor C_2 by losing its stored energy and capacitor's C_2 voltage is raised from the lowest value v_{CV2} to maximum value v_{CP2} , while current in the inductor is dropped to a minimum value I_{LV1} . Also inductor L_2 is supplying energy to a capacitor C_1 by liberating its stored energy and voltage of C_2 is raised to a peak value of v_{CP1} thereby the current in the inductor L_2 is dropped to I_{LV2} . Inductor L_3 and capacitor C_3 both are supplying energy to the capacitor C_4 and load. Current in inductor L_3 is reduced to I_{LV3} while the voltage of the capacitor C_3 is dropped to v_{CV3} and voltage of the capacitor C_4 is raised to a peak value of v_{CP4} . Currents and voltages of all the four diodes in CCM are illustrated in **Figure 3.5**.

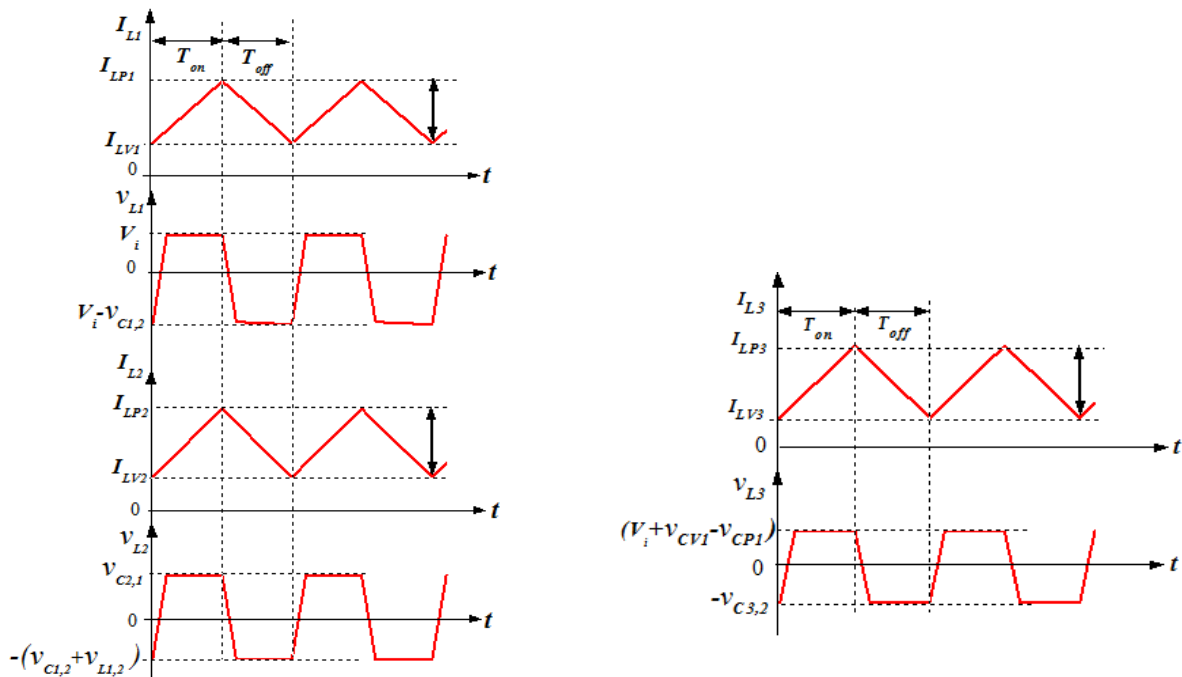


Figure 3.3. The current and voltage waveforms in CCM for; Inductor L_1, L_2 and L_3

3.1.1 Voltage and current equations of the inductor L_1 :

By applying KVL when the switch is on, inductor L_1 voltage is obtained as:

$$v_{L1,1} = V_i = L_1 \frac{di_{L1,1}}{dt} = \frac{\Delta i_{L1,1}}{T_{on}} \quad (1)$$

From Eq. (1), the inductor L_1 current is obtained as:

$$i_{L1,1} = \frac{V_i}{L_1} t + I_{LV1} \quad (2)$$

Inductor current at the end of the on-switching period is given as:

$$i_{L2,1} \Big|_{t=T_{on}} = I_{LP2} \quad (3)$$

By applying KVL when the switch is turned off, inductor L_1 voltage is obtained as:

$$v_{L1,2} = V_i - v_{C2,2} = L_1 \frac{di_{L1,2}}{dt} = -\frac{\Delta i_{L1}}{T_{off}} \quad (4)$$

From Eq. (4), the inductor L_1 current is obtained as:

$$i_{L1,2} = -\frac{(V_i - v_{C2,2})}{L_1} t + I_{LP1} \quad (5)$$

By using inductor volt-sec balance rule for L_1 , Average capacitor C_2 voltage is obtained as:

$$\int_0^{T_{on}} V_i dt + \int_0^{T_{off}} (V_i - v_{C2,2}) dt = 0$$

$$v_{C2,2} = \frac{V_i}{(1-D)} \quad (6)$$

Neglecting small ripple of the capacitor C_2 voltage, its average value is given as:

$$v_{C2,1} = v_{C2,2} = v_{C2} = \frac{V_i}{(1-D)} \quad (7)$$

3.1.2 Voltage and current equations of the inductor L_2 :

By applying KVL during the on-switching period, inductor L_2 voltage is obtained as:

$$v_{L2,1} = L_2 \frac{di_{L2,1}}{dt} = v_{C2,1} = \frac{V_i}{(1-D)} \quad (8)$$

From Eq. (8), the inductor L_2 current is obtained as:

$$i_{L2,1} = \frac{v_{C2,1}}{L_2} t + I_{LV2} \quad (9)$$

Inductor current at the end of the on-switching period is given as:

$$i_{L2,1} \Big|_{t=T_{on}} = I_{LP2} \quad (10)$$

By applying KVL in the time interval of T_{off} , inductor L_2 voltage is obtained as:

$$v_{L2,2} = -(v_{C1,2} + v_{L1,2}) \quad (11)$$

Also,

$$v_{L2,2} = v_{C3,2} + v_{C2,2} - V_0 = L_2 \frac{di_{L2,2}}{dt} \quad (12)$$

From Eq. (12), the inductor L_2 current is obtained as:

$$i_{L2,2} = -\frac{(v_{C3,2} + v_{C2,2} - V_0)}{L_2} t + I_{LP2} \quad (13)$$

By using inductor volt-sec balance rule for L_2 , Average capacitor C_3 voltage can be calculated:

$$\int_0^{T_{on}} v_{C2,1} dt + \int_0^{T_{off}} (v_{C3,2} + v_{C2,2} - V_0) dt = 0$$

$$\frac{V_i}{(1-D)} DT + v_{C3,2} (1-D) + \frac{V_i}{(1-D)} (1-D) T - V_0 (1-D) T = 0$$

$$v_{C3,2} = V_0 - \frac{V_i}{(1-D)^2} \quad (14)$$

Neglecting small ripple of the capacitor C_2 voltage, its average value is given as:

$$v_{C3,1} = v_{C3,2} = v_{C3} = V_0 - \frac{V_i}{(1-D)^2} \quad (15)$$

3.1.3 Voltage and current equations of the inductor L_3 :

By applying KVL in the time interval of T_{on} , inductor L_3 voltage is obtained as:

$$v_{L3,1} = L_3 \frac{di_{L3,1}}{dt} = v_{L1,1} + v_{C1,1} - v_{C3,1} \quad (16)$$

From Eq. (16), the inductor L_2 current is obtained as:

$$i_{L3,1} = \frac{(v_{L1,1} + v_{C1,1} - v_{C3,1})}{L_3} t + I_{LV3} \quad (17)$$

Inductor current at the end of the on-switching period is given as:

$$i_{L3,1} |_{t=T_{on}} = I_{LP3} \quad (18)$$

By applying KVL in the time interval of T_{on} , inductor L_3 voltage is obtained as:

$$v_{L3,2} = L_3 \frac{di_{L3,2}}{dt} = -v_{C3,2} \quad (19)$$

From Eq. (19), the inductor L_3 current is obtained as:

$$i_{L3,2} = \frac{v_{C3,2}}{L_3} t + I_{LP3} \quad (20)$$

Inductor current at the end of the on-switching period is given as:

$$i_{L3,2} |_{t=T_{off}} = I_{LV3} \quad (21)$$

By using inductor volt-sec balance rule for L_3 , Average capacitor C_1 voltage can be calculated:

$$\int_0^{T_{on}} (v_{L1,1} + v_{C1,1} - v_{C3,1}) dt + \int_0^{T_{off}} -(v_{C3,2}) dt = 0$$

$$V_i DT + v_{C1,1} DT - \left[V_0 - \frac{V_i}{(1-D)^2} \right] DT - \left[V_0 - \frac{V_i}{(1-D)^2} \right] (1-D)T = 0$$

$$v_{C1,1} = \frac{V_0 (1-D)^2 - V_i - V_i (1-D)^2}{(1-D)^2} \quad (22)$$

Also, By using the inductor volt-sec balance rule for L_2 We have:

$$\int_0^{T_{on}} v_{C2,1} dt + \int_0^{T_{off}} -(v_{L1,2} + v_{C1,2}) dt = 0$$

Solving for $v_{C1,2}$, the following is obtained:

$$v_{C1,2} = \frac{V_i(2D - D^2)}{(1 - D)^2} \quad (23)$$

Neglecting small ripple of the capacitor C_1 voltage, its average value is given as:

$$v_{C1,1} = v_{C1,2} = v_{C1} = \frac{V_i(2D - D^2)}{(1 - D)^2} \quad (24)$$

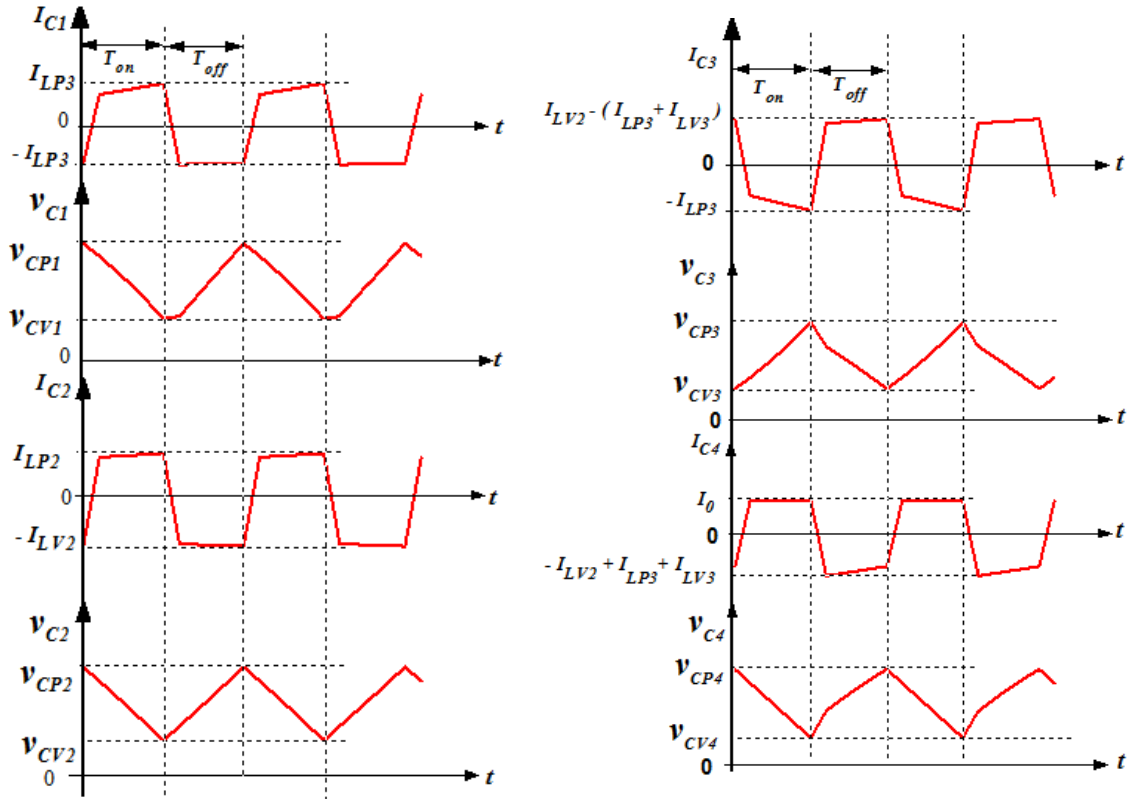


Figure 3.4. The current and voltage waveforms in CCM for; Capacitor C_1 , C_2 , C_3 , and C_4 .

3.1.4 Voltage equations of the Diodes

When the switch is on, diode D_1 is reverse biased, and all other diodes are forward biased. By applying KVL in the time interval of T_{on} , Diode D_1 voltage can be obtained as:

$$V_{D1} + V_{C1} + V_{L1,1} = 0$$

$$V_{D1} = -(V_{C1} + V_{L1,1}) \quad (25)$$

By applying KVL in the time interval of T_{off} , Diode D_2 voltage can be obtained as:

$$V_{in} - V_{L1,1} - V_{D2} - V_{C2} = 0$$

$$V_{D2} = V_{in} - V_{L1,1} - V_{C2} \quad (26)$$

By applying KVL in the time interval of T_{off} , Diode D_3 voltage can be obtained as:

$$V_{D3} + V_{L3,2} + V_{C3} = 0$$

$$V_{D3} = -(V_{L3,2} + V_{C3}) \quad (27)$$

By applying KVL in the time interval of T_{off} , Diode D_4 voltage can be obtained as:

$$V_{D4} + V_{C4} - V_{C3} = 0$$

$$V_{D4} = V_{C3} - V_{C4} \quad (28)$$

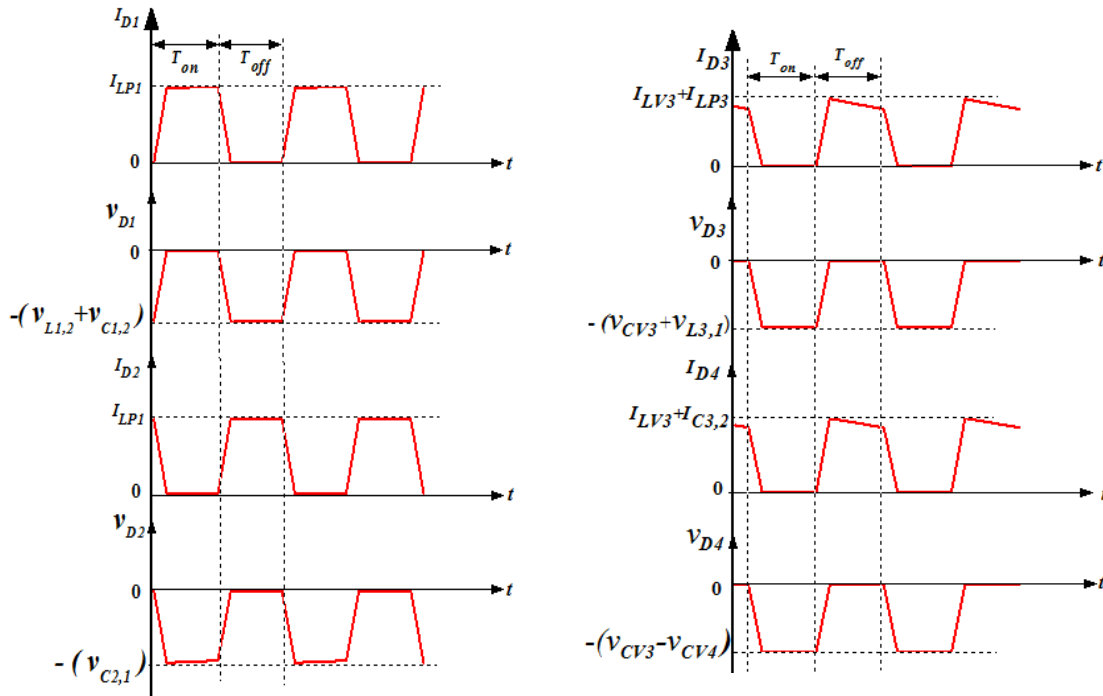


Figure 3.5. The current and voltage waveforms in CCM for; Diode D_1 , D_2 , D_3 , and D_4 .

Voltage gain is calculated by using inductor volt-sec balance rule for L_3 and putting values of $v_{C1,1}$, $v_{C3,1}$ and $v_{C3,2}$, we have:

$$\int_0^{T_{on}} (v_{L1,1} + v_{C1,1} - v_{C3,1}) dt + \int_0^{T_{off}} -(v_{C3,2}) dt = 0$$

$$V_i DT + \frac{V_i(2D - D^2)}{(1-D)^2} DT - \left[V_0 - \frac{V_i}{D^2} \right] DT = 0$$

$$\frac{V_0}{V_i} = \frac{(1+D)}{(1-D)^2} \quad (29)$$

Considering lossless converter, the current ratio is extracted as:

$$\frac{I_0}{I_i} = \frac{(1-D)^2}{(1+D)} \quad (30)$$

3.2. Operation of the proposed high step-up converter in DCM

In this section operation of the proposed converter in DCM is extensively analyzed. Various modes of operation are enlightened, and key waveforms are illustrated in DCM operation. The proposed converter has three modes of operation during DCM. The equivalent circuits during DCM operation are shown in **Figures** 3.2, and 3. The characteristic waveforms during DCM are also demonstrated in **Figures** (3.7-3.9).

Mode I.

When the switch is on, i.e., at the time (t_0, t_1) , diodes D_2, D_3 and D_4 are reverse biased and diode D_1 is forward biased, as shown in Fig 3.2. Input voltage V_i provides energy to the inductor L_1 and its current is increased to the maximum value I_{LP1} (**Figure** 3.7). Also, capacitor C_2 is discharged through the inductor L_2 and its voltage is dropped to the lowest value v_{CV2} (**Figure** 3.8). This energy is stored by the inductor L_2 and its current is raised from the lowest value I_{LV2} to its highest value I_{LP2} . In the meanwhile, capacitor C_1 is supplying energy to the inductor L_3 and capacitor C_3 and current of the inductor L_3 is raised to its maximum value I_{LP3} while the voltage of the capacitor C_3 reaches to the highest value v_{CP3} . During this time interval, the voltage of the capacitor C_1 is dropped to its minimum value v_{CV1} . Since diode D_4 is reverse biased, capacitor C_4 is providing energy to the load and its voltage is dropped to its lowest value v_{CV4} . Currents and voltages of all the four diodes are illustrated in **Figure 3.9**.

Mode II.

During the off-switching period at a time (t_1, t_2) , diode D_1 is reverse biased and diodes D_2, D_3 and D_4 are forward biased. Inductor L_1 is supplying energy to the capacitor C_2 and the current falls to zero at the end of time interval (t_1, t_2) , while the voltage of the capacitor C_2 is increased to its maximum value v_{CP2} . Also, inductor L_2 current falls to zero at the end of time interval (t_1, t_2) , providing energy to the capacitor C_1 thus its voltage is increased to the highest value v_{CP1} . During this time, inductor L_3 and capacitor C_3 both are supplying energy to the capacitor C_4 and load and thus the voltage of the capacitor C_4 is reached to a peak value v_{CP4} . Current in inductor L_3 is reduced to zero while the voltage of the capacitor C_3 is dropped to the lowest value v_{CV3} at the end of the time interval (t_1, t_2) .

Mode III.

At the time (t_2, t_3) , all the four diodes are reverse biased, and current in the three inductors is zero, as shown in **Figure 3.6**. Voltage of capacitors C_1 and C_2 is maintained at peak values v_{CP1} and v_{CP2} respectively as capacitor's C_1 and C_2 current is zero during this time interval. Also the voltage of the capacitor C_3 remains at the lowest value v_{CV3} during the time (t_2, t_3) as a capacitor C_3 current is zero. Capacitor C_4 continues to supply energy to the load by releasing its stored energy. Voltage of capacitor C_4 is reduced to the minimum value v_{CV4} at the end of the time interval (t_2, t_3) .

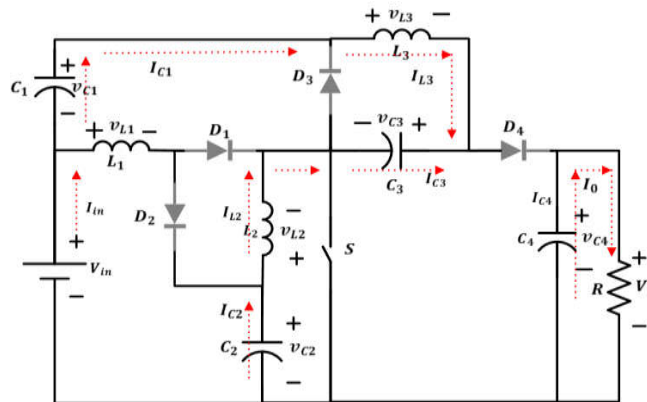


Figure 3.6. Proposed converter during the discontinuous current (t_2, t_3) .

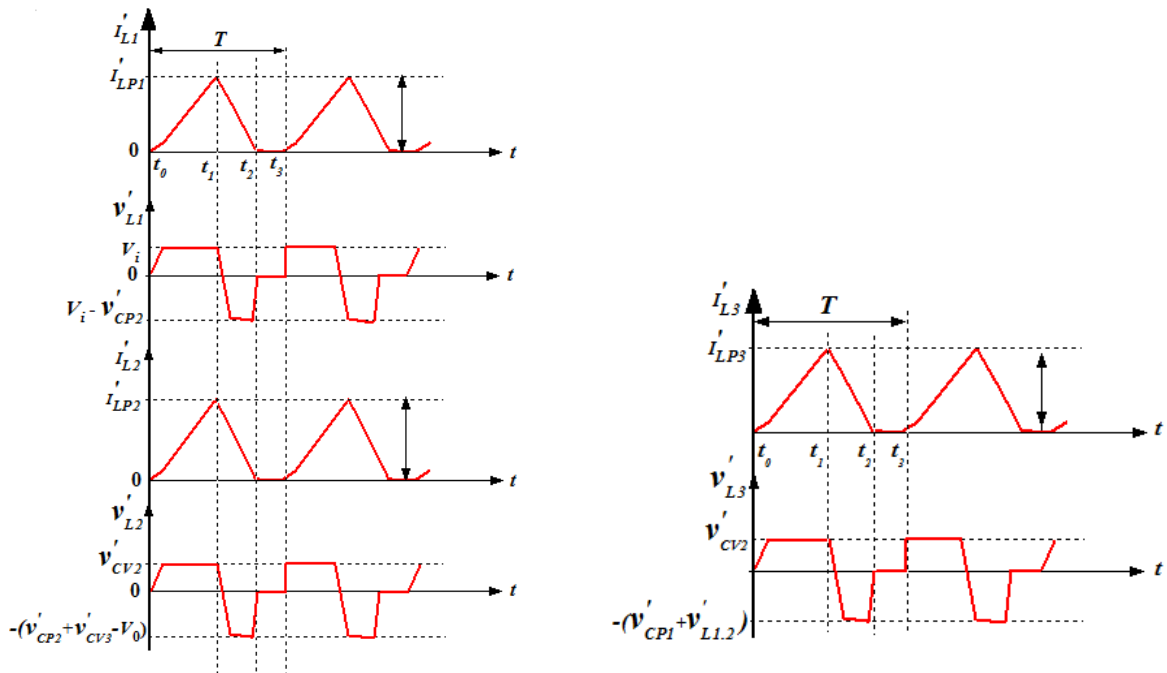


Figure 3.7. The current and voltage waveforms in DCM for; inductors L_1 , L_2 , and L_3 .

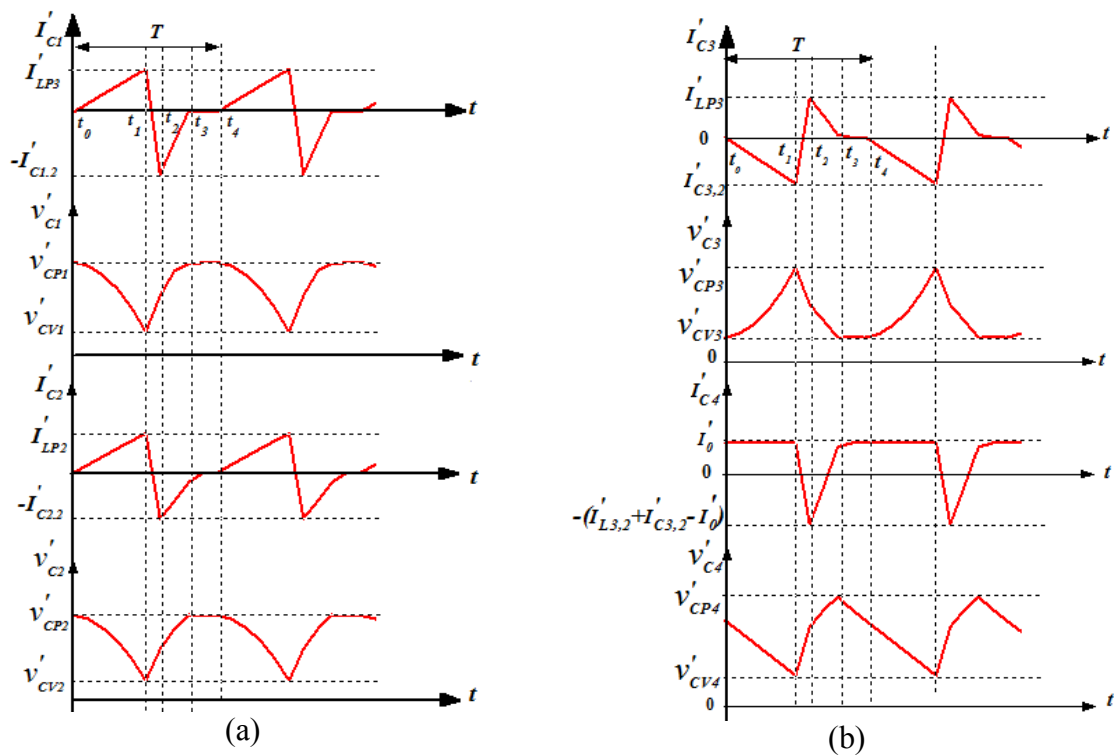


Figure 3.8. The current and voltage waveforms in DCM for; (a) Capacitors C_1 , C_2 ; (b) Capacitors C_3 and C_4 .

At $t = DT$, Inductor L_2 voltage is given as:

$$v'_{L2,1} = v'_{C2,1} = L_2 \frac{di'_{L2,1}}{dt} = L_2 \frac{\Delta i'_{L2}}{\Delta t} \quad (34)$$

At $t = D'T$, Inductor L_2 voltage is given as:

$$v'_{L2,2} = (v'_{C3,2} + v'_{C2,2} - V'_0) = L_2 \frac{di'_{L2,2}}{dt} = -L_2 \frac{\Delta i'_{L2}}{\Delta t} \quad (35)$$

By using inductor volt-sec balance rule for L_2 and solving for average capacitor C_3 voltage, we have:

$$\int_0^{DT} v'_{C2,1} dt + \int_0^{D'T} (v'_{C3,2} + v'_{C2,2} - V'_0) dt = 0$$

$$\frac{V_i(D+D')}{D'} T + \frac{V_i(D+D')}{D'} D'T + v'_{C3,2} D'T - V'_0 D'T = 0$$

$$v'_{C3,2} = V_0 - \frac{V_i(D+D')^2}{(D')^2} \quad (36)$$

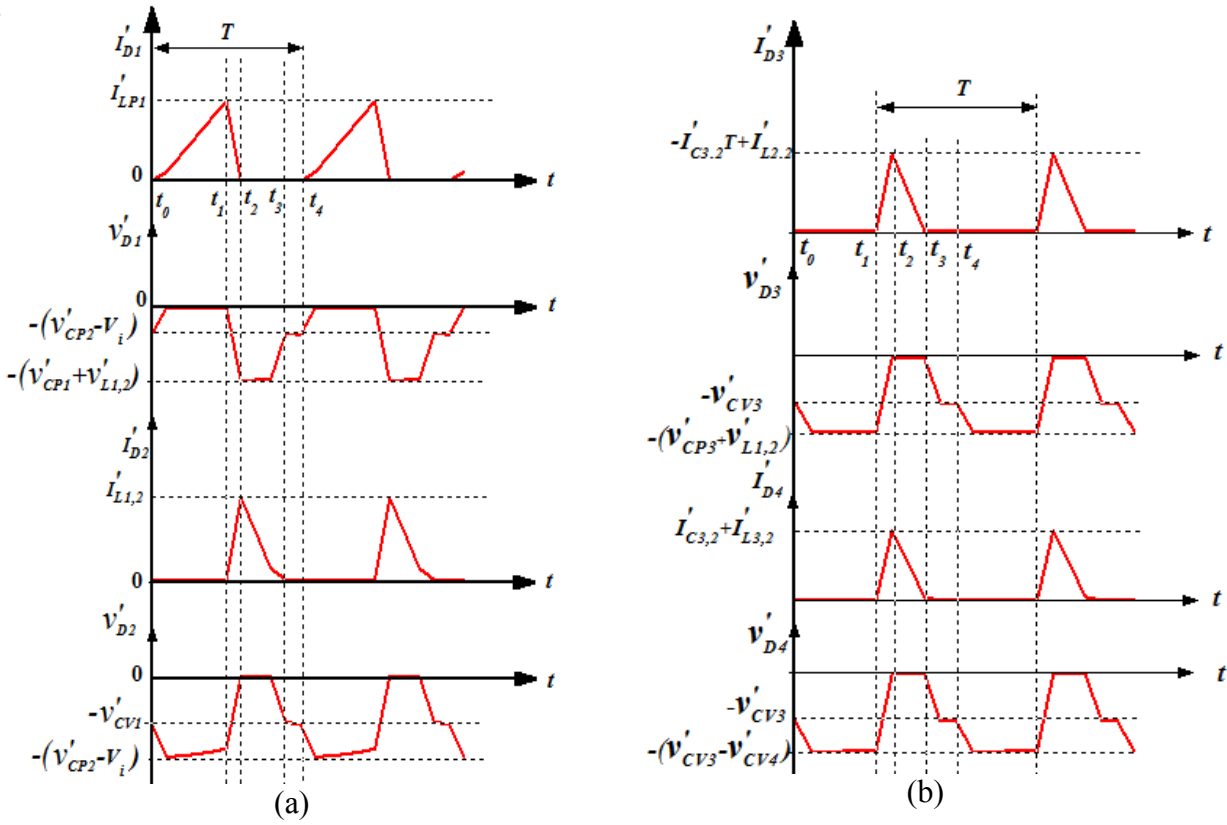


Figure 3.9. The current and voltage waveforms in DCM for ;(a) Diodes D_1 and D_2 ; (b)Diodes D_3 and D_4 .

By using inductor volt-sec balance rule for L_2 and solving for average capacitor C_3 voltage, the following has resulted:

$$\int_0^{DT} v'_{C2,1} dt + \int_0^{D'T} (v'_{C3,2} + v'_{C2,2} - V'_0) dt = 0$$

$$\frac{V_i(D+D')}{D'} T + \frac{V_i(D+D')}{D'} D'T + v'_{C3,2} D'T - V'_0 D'T = 0$$

$$v'_{C3,2} = V'_0 - \frac{V_i(D+D')^2}{(D')^2} \quad (37)$$

At $t = DT$, Inductor L_3 voltage is given as:

$$v'_{L3,1} = v'_{L1,1} + v'_{C1,1} - v'_{C3,1} = L_3 \frac{di'_{L3,1}}{dt} = L_3 \frac{\Delta i'_{L3}}{\Delta t} \quad (38)$$

At $t = D'T$, Inductor L_3 voltage is given as:

$$v'_{L3,2} = -v'_{C3,2} = L_3 \frac{di'_{L3,1}}{dt} = -L_3 \frac{\Delta i'_{L3}}{\Delta t} \quad (39)$$

By using inductor volt-sec balance rule for L_3 and solving for average capacitor C_1 voltage, the following has resulted:

$$\int_0^{DT} v'_{C2,1} dt + \int_0^{D'T} -(v'_{L1,2} + v'_{C1,2}) dt = 0$$

$$v'_{C1,2} = \frac{V_i (D + D') D + DD'}{(D')^2} \quad (40)$$

At $t = D''T$, Voltage of Inductors L_1 , L_2 , and L_3 is zero as the current is zero during $D''T$.

Where the time intervals DT , $D'T$ and $D''T$ are $\frac{t_0 - t_1}{T}$, $\frac{t_1 - t_2}{T} = \frac{t_1 - t_3}{T}$ and $\frac{t_2 - t_3}{T} = \frac{t_3 - t_4}{T}$, respectively.

Voltage gain can be calculated by using inductor volt-sec balance rule for L_3 and by putting values of $v'_{C1,1}$, $v'_{L1,1}$, $v'_{C3,1}$ and $v'_{C3,2}$, we have:

$$\int_0^{DT} (v'_{L1,1} + v'_{C1,1} - v'_{C3,1}) dt + \int_0^{D'T} -(v'_{C3,2}) dt = 0$$

$$V_i DT + \frac{V_i (D + D') D + DD'}{(D')^2} DT - V_0 DT - V_0 D'T + \frac{V_i (D + D')^2}{(D')^2} DT + \frac{V_i (D + D')^2}{(D')^2} D'T = 0$$

$$V_i \left[D + \frac{(D + D')(D)^2 + D'(D)^2}{(D')^2} + \frac{(D + D')^3}{(D')^2} \right] = V_0 (D + D')$$

$$\frac{V_0}{V_i} = \frac{(D + D')^2 + D^2 + DD'}{D'^2} \quad (41)$$

3.3. Calculation of critical inductance, rms of elements current, and efficiency

The critical inductance of inductors is of great importance as it determines the boundary between CCM and DCM. At boundary conditions, the inductors current just reaches zero, and this occurs at a critical value of inductor(s). In the proposed structure, three inductors are used; therefore, three critical values for L_1 (L_{C1}), L_2 (L_{C2}), and L_3 (L_{C3}) will be calculated. In order to find the critical values, the following equation has to be fulfilled.

$$I_{LV1} + I_{LV2} + I_{LV3} = 0 \quad (42)$$

Where I_{LV1} , I_{LV2} , and I_{LV3} are the minimum values of the three inductors.

3.3.1. Current equations of the capacitor C_4 are as follow:

$$I_{C4,1} = -I_0 \quad (43)$$

$$I_{C4,2} = I_{L3,2} + I_{C3,2} - I_0 \quad (44)$$

By using charge balance rule for capacitor C_4 , we have:

$$\begin{aligned} \int_0^{T_{on}} (I_{C4,1}) dt + \int_0^{T_{off}} (I_{C4,2}) dt &= 0 \\ \int_0^{T_{on}} -(I_0) dt + \int_0^{T_{off}} (I_{L3,2}) dt + \int_0^{T_{off}} (I_{C3,2}) dt + \int_0^{T_{off}} -(I_0) dt &= 0 \\ -(I_0)DT + \frac{V_{C3,2}}{2L_3} t^2 \Big|_{t=T_{off}} + I_{LP3} (1-D)T + \int_0^{T_{off}} (I_{C3,2}) dt - I_0 (1-D)T &= 0 \end{aligned} \quad (45)$$

By applying boundary conditions (i.e., $I_{LV3} = 0$) to above Eq. and solving for integral of $I_{C3,2}$, we have:

$$\int_0^{T_{off}} (I_{C3,2}) dt = I_0 T - \frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) - I_{LV3} \quad (46)$$

By using charge balance rule for capacitor C_3 and applying boundary conditions, the value L_3 is calculated as:

$$\int_0^{T_{on}} (I_{C3,1}) dt + \int_0^{T_{off}} (I_{C3,2}) dt = 0$$

$$\begin{aligned}
& -\frac{(v_{L1,1} + v_{C1,1} - v_{C3,1})}{2L_3} D^2 T^2 - I_{LV3} DT + I_0 T - \frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) - I_{LV3} = 0 \\
& -\frac{D^2 T^2}{2L_3} \left[V_i - \frac{V_0 (1-D)^2 - V_i}{(1-D)^2} + \frac{V_i (2D-D^2)}{(1-D)^2} \right] - I_{LV3} DT + I_0 T - \frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) - I_{LV3} = 0 \\
& -\frac{D^2 T^2}{2L_3} \left[\frac{2V_i - V_0 (1-D)^2}{(1-D)^2} \right] - I_{LV3} DT + I_0 T - \frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) - I_{LV3} = 0 \\
& -\frac{T^2}{2L_3} \left[\frac{2V_i - V_0 (1-D)^2}{(1-D)^2} D^2 + (V_0 (1-D)^2 - V_i) \right] - I_{LV3} DT + I_0 T - I_{LV3} = 0 \\
& -\frac{T^2}{2L_3} \left[\frac{V_i (D^2 + 2D - 1) - V_0 (1-D)^2 D^2 + V_0 (1-D)^4}{(1-D)^2} \right] - I_{LV3} DT + I_0 T - I_{LV3} = 0
\end{aligned}$$

$$L_3 = \frac{1}{2I_0 f} \left[\frac{V_i (D^2 + 2D - 1) - V_0 (1-D)^2 D^2 + V_0 (1-D)^4}{(1-D)^2} \right] \quad (47)$$

3.3.2. Current equations of Capacitor C_1 , during on and off states of the switch are given as follow:

$$I_{C1,1} = I_{L3,1} \quad (48)$$

$$I_{C1,2} = I_{L3,2} + I_{C3,2} - I_{L2,2} \quad (49)$$

By using charge balance rule for capacitor C_1 , we have:

$$\int_0^{T_{on}} (I_{L3,1}) dt + \int_0^{T_{off}} (I_{C3,2}) dt + \int_0^{T_{off}} (I_{L3,2}) dt - \int_0^{T_{off}} (I_{L2,2}) dt = 0$$

$$\frac{1}{2L_3} \frac{(v_{L1,1} + v_{C1,1} - v_{C3,1})}{L_3} D^2 T^2 I_{LV3} DT + I_0 T - \frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) - I_{LV3} +$$

$$\frac{T^2}{2L_3} (V_0 (1-D)^2 - V_i) + I_{LP3} (1-D) T + -I_{LP2} (1-D) T = 0$$

$$\frac{D^2 T^2}{2L_3} \left[\frac{2V_i - V_0 (1-D)^2}{(1-D)^2} \right] + I_{LV3} DT + I_0 T + I_{LP3} (1-D) T - I_{LV3} - \frac{T^2 V_i D}{2L_3} - I_{LP2} (1-D) T = 0 \quad (50)$$

By applying boundary conditions to above Eq. and solving for L_2 , yields

$$L_2 = \frac{1}{\left[\frac{D}{V_i L_3} \left\{ \frac{2V_i - V_0 (1-D)^2}{(1-D)^2 D^2} \right\} + \frac{2I_0 f}{D V_i} \right]} \quad (51)$$

3.3.3. Current equations of Capacitor C_2 , are given as follow:

$$I_{C2,1} = I_{L2,1} \quad (52)$$

$$I_{C2,2} = I_{L3,2} - I_{L1,2} \quad (53)$$

By using charge balance rule for capacitor C_2 , we have:

$$\int_0^{T_{on}} (I_{L2,1}) dt + \int_0^{T_{off}} (I_{L2,2}) dt - \int_0^{T_{off}} (I_{L1,2}) dt = 0$$

$$\frac{V_i}{(1-D) 2L_2} D^2 T^2 + I_{LV2} DT + \frac{1}{2L_2} [V_i - v_{C2,2} + v_{C1,2}] (1-D)^2 T^2 + I_{LP2} (1-D) T +$$

$$\frac{1}{2L_1} [V_i - v_{C2,2}] (1-D)^2 T^2 - I_{LP1} (1-D) T = 0$$

$$\frac{V_i}{(1-D) 2L_2} D^2 T^2 + \frac{T^2 V_i D}{2L_2} - \frac{T^2 V_i D}{2L_1} (1-D) + I_{LV2} DT + I_{LP2} (1-D) T - I_{LP1} (1-D) T = 0 \quad (54)$$

By applying boundary conditions to the above equation and solving for L_1 , yields

$$L_1 = L_2 (1-D)^2 \quad (55)$$

Therefore, the converter operates in CCM when $L_1 > L_{C1}$, $L_2 > L_{C2}$, and $L_3 > L_{C3}$ while operates in DCM when $L_1 < L_{C1}$, $L_2 < L_{C2}$ and $L_3 < L_{C3}$. At boundary conditions, i.e., when $L_1 = L_{C1}$, $L_2 = L_{C2}$ and $L_3 = L_{C3}$ the converter operates at the edge of between CCM and DCM.

3.4. RMS calculation:

For RMS calculation, to simplify the analysis inductor's current and capacitor's voltage ripple is ignored. Average inductor L_j current can be calculated as:

$$I_i = I_{L1,1} = I_{L1,2} = I_{L1} = \frac{I_0(1+D)}{(1-D)^2} \quad (56)$$

Average inductor L_2 current can be calculated as:

$$\int_0^{T_{on}} (I_{L2,1}) dt + \int_0^{T_{off}} (I_{L2,2}) dt - \int_0^{T_{off}} (I_{L1,2}) dt = 0$$

$$I_{L2,1}DT + I_{L2,2}(1-D)T - I_{L1,2}(1-D)T = 0$$

$$I_{L2,1} = I_{L2,2} = I_{L2} = I_i(1-D) \quad (57)$$

Average Capacitor C_3 current at $t=T_{off}$ can be calculated as:

$$\int_0^{T_{on}} (I_{L3,1}) dt + \int_0^{T_{off}} (I_{C3,2}) dt + \int_0^{T_{off}} (I_{L3,2}) dt - \int_0^{T_{off}} (I_{L2,2}) dt = 0$$

$$I_{L3,1}DT + \int_0^{T_{off}} (I_{C3,2}) dt + I_{L3,2}(1-D)T - I_{L2,2}(1-D)T = 0$$

$$\int_0^{T_{off}} (I_{C3,2}) dt = I_{L2,2}(1-D)T - I_{L3}T$$

$$\int_0^{T_{off}} (I_{C3,2}) dt = I_i(1-D)^2 T - I_{L3}T \quad (58)$$

$$I_{C3,2} = I_{L2,2} - \frac{I_{L3}}{(1-D)} \quad (59)$$

Capacitor C_3 current at $t=T_{on}$ can be written as:

$$I_{C3,1} = -I_{L3,1} = -I_{L3,2} = -I_{L3} = -I_0 \quad (60)$$

Average inductor L_3 current can be calculated as:

$$\int_0^{T_{on}} -(I_0) dt + \int_0^{T_{off}} (I_{L3,2}) dt + \int_0^{T_{off}} (I_{C3,2}) dt + \int_0^{T_{off}} -(I_0) dt = 0$$

$$I_{L3}(1-D) + I_i(1-D)^2 - I_{L3} = I_0$$

$$I_{L3} = I_0 \quad (61)$$

Capacitor C_1 current at $t=T_{on}$ can be written as:

$$I_{C1,1} = I_{L3,1} = I_{L3,2} = I_{L3} = I_0 \quad (62)$$

Capacitor C_1 current at $t=T_{off}$ can be calculated as:

$$I_{C1,2} = I_{L3,2} + I_{C3,2} - I_{L2,2} \quad (63)$$

$$I_{C1,2} = -\frac{I_0 D}{(1-D)} \quad (64)$$

Capacitor C_4 current at $t=T_{off}$ can be calculated as:

$$\int_0^{T_{on}} (I_{C4,1}) dt + \int_0^{T_{off}} (I_{C4,2}) dt = 0$$

$$I_{C4,2} = \frac{I_0 D}{(1-D)} \quad (65)$$

Capacitor C_2 current at $t=T_{on}$ can be written as:

$$I_{C2,1} = I_{L2} = I_i (1-D) = \frac{I_0 (1+D)}{(1-D)} \quad (66)$$

Capacitor C_2 current at $t=T_{off}$ can be calculated as:

$$I_{C2,2} = I_{L2,2} - I_{L1,2} = I_i (1-D) - I_i$$

$$I_{C2,2} = -\frac{I_0 (1+D) D}{(1-D)^2} \quad (67)$$

Diodes D_1 and D_2 currents are given as:

$$I_{D1} = I_{D2} = I_i = \frac{I_0 (1+D)}{(1-D)^2} \quad (68)$$

Average Diode D_1 current is given as:

$$I_{D1,avg} = I_i = \frac{I_0 (1+D)}{(1-D)^2} D \quad (69)$$

Average Diode D_2 current is given as:

$$I_{D2,avg} = \frac{I_0 (1+D)}{(1-D)^2} (1-D) \quad (70)$$

Diode D_3 and D_4 currents are given as:

$$I_{D3} = I_{L2,2} - I_{C3,2} = \frac{I_0}{(1-D)} \quad (71)$$

$$I_{D4} = I_{L3,2} + I_{C3,2} = \frac{I_0}{(1-D)} \quad (72)$$

Average Diode D_3 and D_4 currents are given as:

$$I_{D3,avg} = I_{D4,avg} = I_0 \quad (73)$$

Diode's RMS values are calculated as:

$$I_{D1,rms} = \sqrt{\frac{1}{T} \int_0^{T_{on}} \left(\frac{I_0(1+D)}{(1-D)^2} \right)^2 dt} = \frac{I_0(1+D)}{(1-D)^2} \sqrt{D} \quad (74)$$

$$I_{D2,rms} = \sqrt{\frac{1}{T} \int_0^{T_{on}} \left(\frac{I_0(1+D)}{(1-D)^2} \right)^2 dt} = \frac{I_0(1+D)}{(1-D)^2} \sqrt{(1-D)} \quad (75)$$

$$I_{D3,rms} = I_{D4,rms} = \sqrt{\frac{1}{T} \int_0^{T_{off}} \left(\frac{I_0}{(1-D)} \right)^2 dt} = \frac{I_0}{\sqrt{(1-D)}} \quad (76)$$

Capacitor's RMS values are calculated as:

$$I_{C1,rms} = \sqrt{\frac{1}{T} \left[\int_0^{T_{on}} (-I_0)^2 dt + \int_0^{T_{off}} \left(\frac{I_0 D}{(1-D)} \right)^2 dt \right]} = I_0 \sqrt{\frac{D}{(1-D)}} \quad (77)$$

$$I_{C2,rms} = \sqrt{\frac{1}{T} \left[\int_0^{T_{on}} \left(\frac{I_0(1+D)D}{(1-D)} \right)^2 dt + \int_0^{T_{off}} \left(\frac{-I_0(1+D)D}{(1-D)^2} \right)^2 dt \right]} = \frac{I_0(1+D)}{(1-D)^2} \sqrt{D(1-D)} \quad (78)$$

$$I_{C3,rms} = \sqrt{\frac{1}{T} \left[\int_0^{T_{on}} (-I_0)^2 dt + \int_0^{T_{off}} \left(\frac{I_0 D}{(1-D)} \right)^2 dt \right]} = I_0 \sqrt{\frac{D}{(1-D)}} \quad (79)$$

$$I_{C4,rms} = \sqrt{\frac{1}{T} \left[\int_0^{T_{on}} (-I_0)^2 dt + \int_0^{T_{off}} \left(\frac{I_0 D}{(1-D)} \right)^2 dt \right]} = I_0 \sqrt{\frac{D}{(1-D)}} \quad (80)$$

3.5. Efficiency analysis:

For efficiency analysis, parasitic resistances of inductors, capacitors, diodes, and switches are taken into consideration. The parasitic on-state resistance of Mosfet is represented by r_s . Parasitic resistances of inductors and capacitors are represented by (r_{L1}, r_{L2}, r_{L3}) and (r_{C1}, r_{C2}, r_{C3}) , respectively. Forward voltage and parasitic resistances of diodes is represented by V_F and $(r_{D1}, r_{D2}, r_{D3}, r_{D4})$, respectively.

Losses due to inductors are calculated as:

$$P_{L,loss} = I_{L1}^2 r_{L1} + I_{L2}^2 r_{L2} + I_{L3}^2 r_{L3} \quad (81)$$

Losses due to capacitors are calculated as:

$$P_{C,loss} = I_{C1,rms}^2 r_{C1} + I_{C2,rms}^2 r_{C3} + I_{C3,rms}^2 r_{C3} + I_{C4,rms}^2 r_{C4} \quad (82)$$

Losses due to diodes are calculated as:

$$P_{D1,loss} = I_{D1,rms}^2 r_{D1} + V_F I_{D1,avg} \quad (83)$$

$$P_{D2,loss} = I_{D2,rms}^2 r_{D2} + V_F I_{D2,avg} \quad (84)$$

$$P_{D3,loss} = I_{D3,rms}^2 r_{D3} + V_F I_{D3,avg} \quad (85)$$

$$P_{D4,loss} = I_{D4,rms}^2 r_{D4} + V_F I_{D4,avg} \quad (86)$$

$$P_{D,loss} = P_{D1,loss} + P_{D2,loss} + P_{D3,loss} + P_{D4,loss} \quad (87)$$

Switch current is obtained as:

$$I_S = I_{L1} + I_{L2} = \frac{I_0(1+D)}{(1-D)^2} + \frac{I_0(1+D)}{(1-D)} = \frac{I_0(1+D)(2-D)}{(1-D)^2} \quad (88)$$

The RMS switch current is given as:

$$I_{S,rms} = \sqrt{\frac{1}{T} \int_0^{T_{on}} \left(\frac{I_0(1+D)}{(1-D)^2} \right)^2 dt} = \frac{I_0(1+D)(2-D)}{(1-D)^2} \sqrt{D} \quad (89)$$

The average switch current is given as:

$$I_{S,avg} = \frac{I_0(1+D)(2-D)}{(1-D)^2} D \quad (90)$$

Switch voltage is obtained as:

$$V_S = v_{L1,2} + v_{C1,2} + v_{C2,2} = V_i - v_{C2,1} + v_{C1,2} + v_{C2,2} \quad (91)$$

$$V_S = V_i + \frac{V_i(2D-D^2)}{(1-D)^2} = \frac{V_i}{(1-D)^2} \quad (92)$$

Switch conduction loss is earned as:

$$P_{S,loss} = I_{S,rms}^2 r_S \quad (93)$$

Switching loss is calculated as:

$$P_{Switch} = \frac{1}{2} \frac{(t_r + t_f)}{T} I_{S,avg} V_S + \frac{1}{2} \frac{C_{oss}}{T} V_S^2 \quad (94)$$

Total power loss is given as:

$$P_{Loss} = P_{L,loss} + P_{C,loss} + P_{D,loss} + P_{S,loss} + P_{Switch} \quad (95)$$

Output power is given as:

$$P_{out} = I_0^2 R \quad (96)$$

$$\eta\% = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100 \quad (97)$$

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Comparison Analysis with recent converters

In this section, comparison results between the proposed converter and other converters mentioned in **Table 4.1** are presented to verify the primacy of the proposed converter. The performance of the proposed converter is compared with other converters stated above in terms of voltage gain, the number of elements, and current stress on the power semiconductor switch(s). The proposed converter has a prominent performance, particularly when the high gain is required. To achieve high voltage gain, the above-mentioned converters have to operate at extreme duty cycles, which degrade system efficiency and increases stress on circuit elements. The comprehensive comparative analysis is scrutinized in Table 4.1 to avow the noteworthy significance of the converter proposed in the study. The voltage gain of the proposed converter at $D \geq 0.6$ is higher in comparison with the converters mentioned above. The curve of voltage gain variation of the proposed converter and other converters with D at CCM operation is shown in Figure 4.1. Converters presented in [18] and [19] have a higher number of elements (13 and 14) with additional switch than the currently proposed converter (12). Moreover, the voltage gain calculated in ref [20] possesses negative value, which coerces to implement an additional circuitry to avail positive voltage. However, the currently proposed converter and previously proposed converters in [21], [22], [23] have the same number of elements. But the authors in [21] have adopted two switches, which in results increase the complexity of the system and reduce the cost-effectivity. The converter presented in [22] can achieve high voltage gain by increasing the turns ratio of the coupled inductor. However, the enhancement in the turns ratio provides an increment in size and cost. The gain of these converters is limited due to the operation at extreme duty cycles when high voltage gain is required. Table 4.2 shows that the current stress on the active switch of the proposed converter is less compared with other converters to achieve the same output voltage (160V) for the same input (12V). **Figure 4.1** demonstrates the comparison of current stress on the main switch between the proposed and other converters. As can be seen in **Figure 4.1(a)** and **Table 4.2**, the proposed converter has low current stress than the others while operating at a reasonable duty cycle. Also, the proposed converter uses a single switch and either less or parallel the number of elements compared with other converters and avoid transformers or coupled inductor to achieve high voltage transfer gain.

Table 4.1. Comparison summary between the proposed converter and other high gain converters.

	Proposed converter	Converter in [27]	Converter in [28]	Converter in [29]	Converter in [30]	Converter in [31]	Converter in [32]
Switches	01	02	02	02	01	01	01
Capacitors	04	03	05	03	05	04	06
Inductors	03	03	02	03	01 (coupled inductor)	02	04
Diodes	04	05	05	04	05	05	03
Total count	12	13	14	12	12	12	14
Voltage gain	$\frac{(1+D)}{(1-D)^2}$	$\frac{n}{D(1-D)}$ $n = 2$ $n = \text{no. of stages}$	$\frac{-5}{(1-D)}$	$\frac{2}{D(1-D)}$	$\frac{2+n(2-D)}{(1-D)}$ $n = 2$ $n = \text{turns ratio}$	$\frac{4}{(1-D)}$	$\frac{3D}{(1-D)}$

Table 4.2. Switch current comparison between the proposed converter and other high gain converters

	Switch(s) RMS Current	Duty	Output voltage	Input voltage	Load resistor (Ω)
Proposed converter	$I_{s,rms} = I_0 \left[\frac{(1+D)}{(1-D)^2} - 1 + \frac{(1+D)}{(1-D)} \right] \sqrt{D}$	0.7	294	12	200
Converter in [28]	$I_{s1,rms} = \frac{2\sqrt{D}I_0}{(1-D)}$ $I_{s2,rms} = \frac{3}{2}I_0 \sqrt{\frac{1}{(1-D)D^2}}$	0.91	294	12	200

Converter in [27]	$I_{s1,rms} = 2I_0 \left[\frac{1}{D(1-D)} + 1 \right] \sqrt{D}$ $I_{s2,rms} = \frac{3}{2D(1-D)}$	0.91	294	12	200
Converter in [32]	$I_{s,rms} = \frac{3I_0 \sqrt{D}}{(1-D)}$	0.83	294	12	200
Converter in [30]	$I_{s,rms} = \sqrt{D} \left[\frac{2+2D(2-D)}{D(1-D)} \right] I_0$	0.89	294	12	200

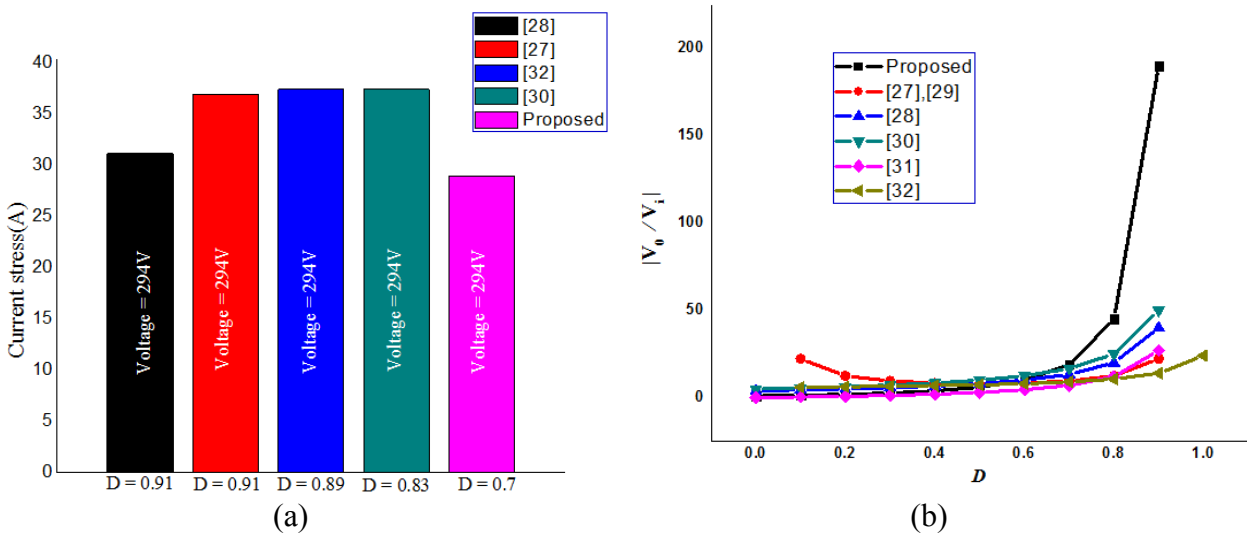


Figure 4.1. Comparison between the proposed converter and other converters in terms of (a) Current stress and (b) Voltage gain.

4.2 Simulation and Experimental Results

In this section, Simulation results in PSIM and experimental results by testing laboratory prototype are provided to verify the theoretical analysis and validate the performance of the proposed DC-DC converter shown in **Figure 3.1**. The converter specification (CCM operation) used in simulation and hardware is given in **Table 4.3**.

Table 4.3. Specifications of the proposed converter in CCM.

Input voltage	12 V
Switching frequency	25 KHz
Inductors L_1, L_2, L_3	8mH, 5mH, 4.5mH
Capacitors C_1, C_2	8 u F
Capacitors C_3, C_4	220 u F
Power switch	IRFP250
Diodes	MUR3060PT
Duty cycle	50%
Load Resistor	200m

4.3 Simulation and Experimental Results for CCM

The waveforms of the converter (simulation) while operating in continuous conduction (CCM) are illustrated in **Figures. (4.3-4.5)**. Considering $L_1=8\text{mH}$, $L_2=5\text{mH}$, and $L_3=4.5\text{mH}$ as provided in **Table 4.3**, the converter operates in CCM. From **Figure.4.3 (a)**, inductor L_1 voltage at $t=t_{on}$ is reached to 12.8 V, which is consistent with theoretical results in (1). At $t=t_{off}$, inductor L_1 voltage is reduced to -11.6 V, which shows the validity of equation (4). Similarly, at the end of the on-switching period, inductor L_2 and inductor L_3 voltages achieved are 21.6 V and 22.3 V, respectively, which shows consistency with theoretical analysis in (8) and (16). At the end of the off-switching period, the voltages attained are -21.6 V and -22.3 V, which is consistent with the results obtained in (12) and (19). As shown in **Figure.4.3 (b)**, capacitors C_1, C_2 and C_3 voltages are approximately 26.2 V, 19.9 V, and 17.8 V respectively, which is confirmed by (24), (6), and (15). The voltages of all the four diodes are -23.8V, -23.8 V, -46.8 V, and -47.8V, respectively, as shown in **Figure 4.5 (a)**, which is in accordance with (25), (26), (27) and (28). From Figure 4.4(b), the switch current at $t=t_{on}$ reaches 3.5 A, which follows equation (88). **Figure 4.4 (a)** shows the variation of inductors currents having peak values 2.2A, 1.14 A, and 0.43 A, respectively, which is in accordance with results obtained in (56), (57), and (61). All the diode currents are shown in **Figure 4.5 (b)**, which is consistent with (68) and (72).

The experimental results are provided at 25 kHz switching frequency with 50% duty cycle to demonstrate the proposed converter operation in CCM. Experimental waveforms of the Inductor's and capacitor's voltages are provided in **Figures. (4.7- 4.10)**. The diode voltages are illustrated in **Figs. 4.9 and 4.10**. The output voltage and MOSFET voltage are given in **Figures. 4.7 (a) and 4.10 (d)**. Summary of comparison results of simulation and experiment is provided in **Table 4.4**. It can be seen that the experimental results reaffirm the simulation results with some small differences due to the effect of parasitic elements. The converter specification with the inclusion of parasitic elements is shown in **Table 4.5**. The losses in each component at $D = 30\%$, 40% , and 50% are listed in **Table 4.6**, which elucidates the major losses occurs in the diodes and inductors. The losses can be minimized by the selection of proper diode with low forward voltage drop and fine quality inductor core. The experimental prototype of the proposed converter is shown in **Figure 4.2**.

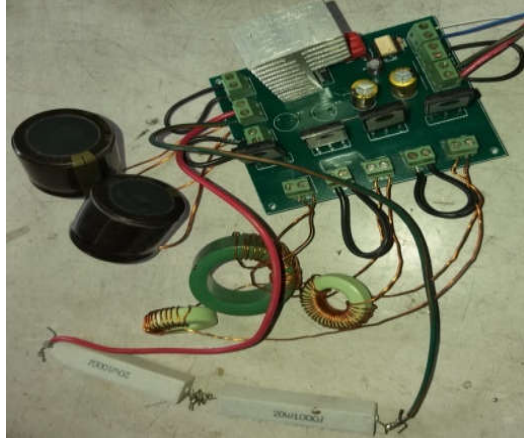


Figure 4.2. Proposed converter Power circuit

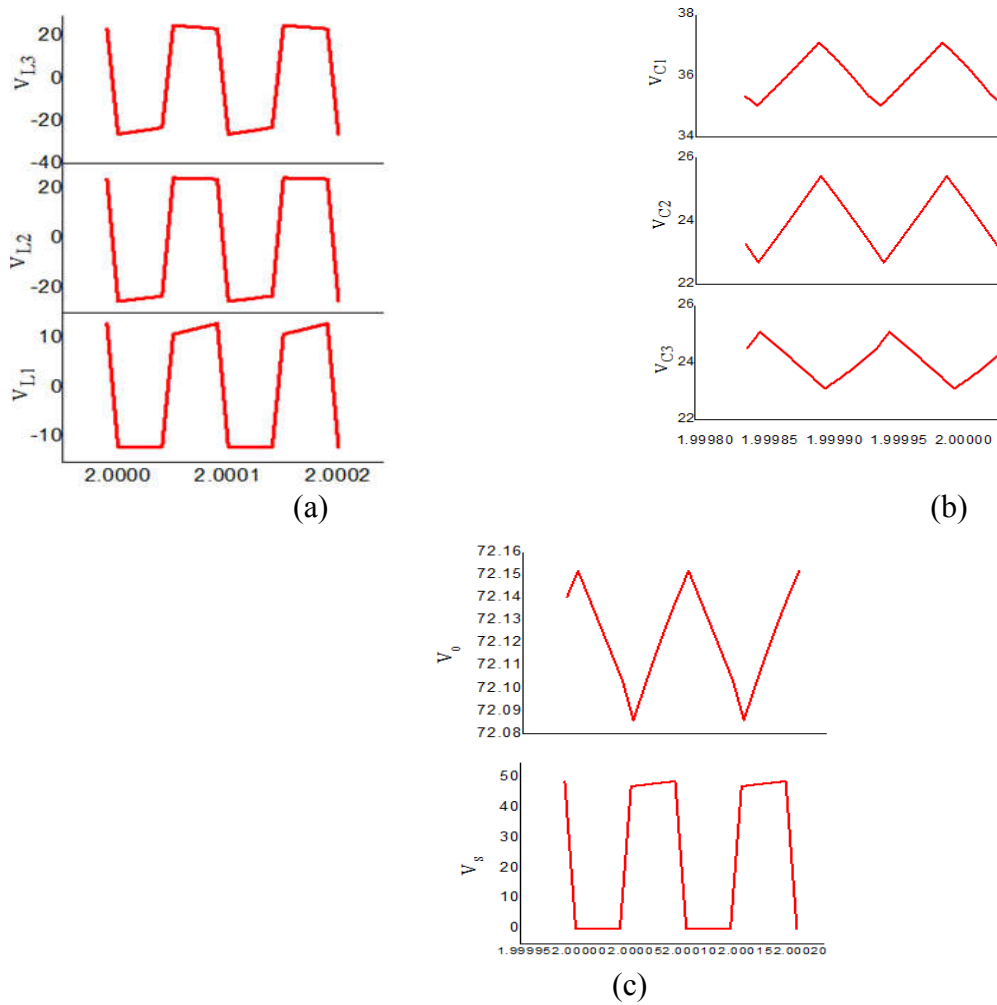


Figure 4.3. Voltage waveforms in CCM (simulation) for; (a) inductors; (b) capacitors; (c) switch and output.

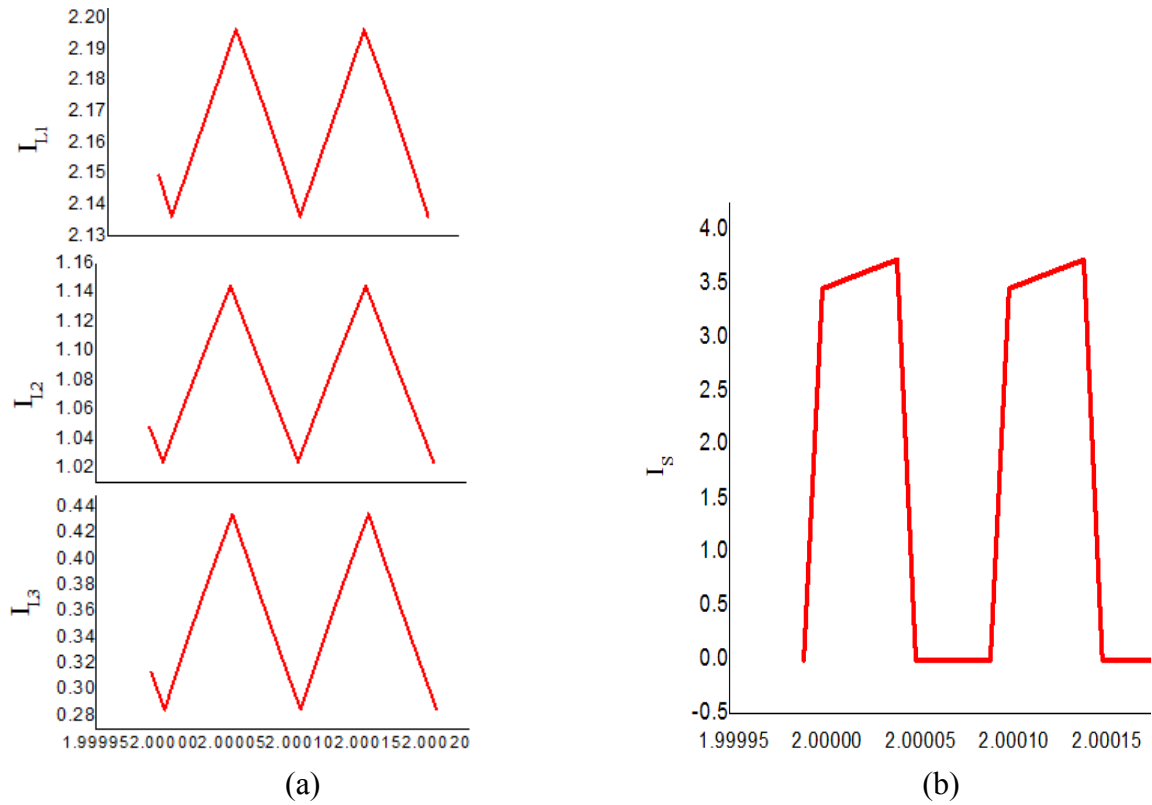


Figure 4.4. Current waveforms in CCM (simulation) for; (a) inductors; (b) Switch current.

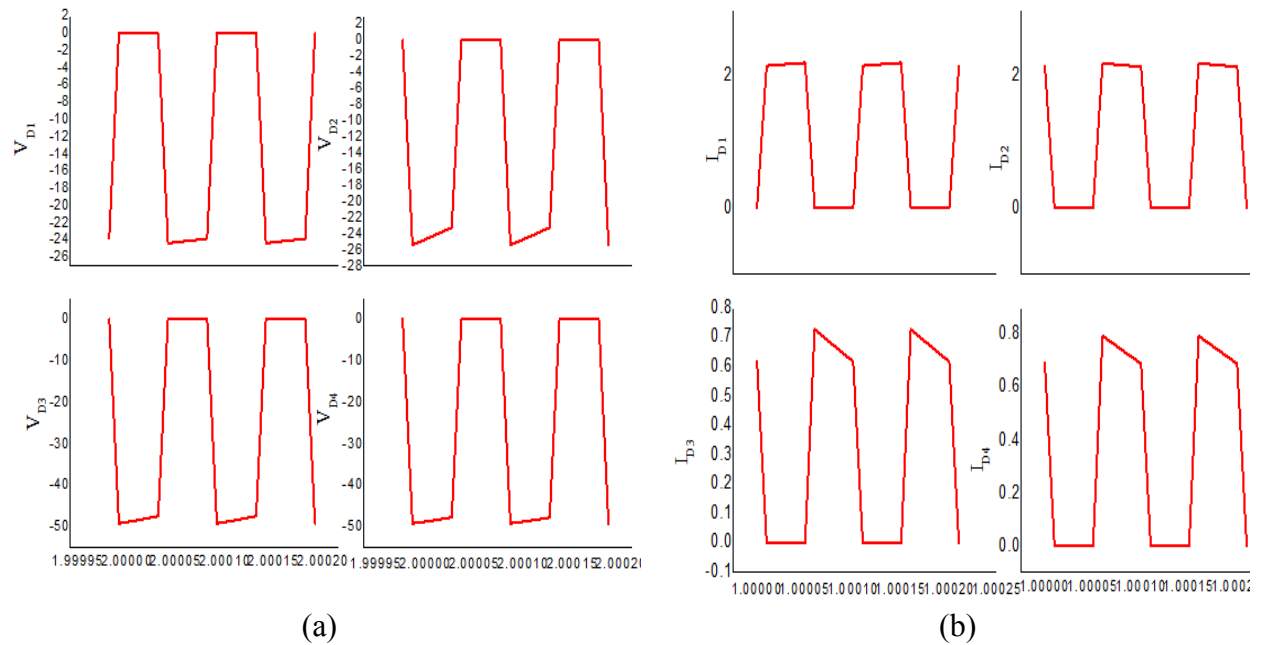


Figure 4.5. Simulation waveforms in CCM for; (a) Diode voltages; (b) Diode currents

Table 4.4. Comparison of simulation and experimental results of the proposed converter in CCM.

	Simulation (D=50% , Vi=12 V)	Experiment (D=50%, Vi=12 V)
V_0	72	58 V
V_{L1}, V_{L2}, V_{L3}	12, 24, 24	12, 21.6, 22.3
V_{C1}, V_{C2}, V_{C3}	35, 23, 23	26.2, 19.9, 17.8
$V_{D1}, V_{D2}, V_{D3}, V_{D4}$	17, 17, 33, 34	13.5, 13.5, 29.2, 29
V_S	33	30
I_{L1}, I_{L2}, I_{L3}	2.2, 1.2, 0.38	2.1, 0.92, 0.30
$I_{D1}, I_{D2}, I_{D3}, I_{D4}$	1.5, 1.5, 0.67, 0.63	1.18, 1.16, 0.39, 0.32
I_S	2.6	2

Table 4.5. Specifications of the proposed converter with parasitic elements.

Input voltage	12 V
Switching frequency	25 KHz
Inductors L_1, L_2, L_3	8mH, 5mH, 4.5mH ($r_{L1}=0.2$ Ohm, $r_{L2}=0.3$ Ohm, $r_{L3} = 0.3$ Ohm)
Capacitors C_1, C_2	8 u F ($r_{C1}=r_{C2}= 0.2$ Ohm)
Capacitors C_3, C_4	220 u F ($r_{C3}=r_{C4}=0..3$ Ohm)
Power switch	IRFP250 ($r_{s-on} = 30$ m Ohm)
Diodes	MUR3060PT ($V_F=0.8$, $r_{s-on} = 10$ m Ohm)
Duty cycle	50%
Load Resistor	200 Ohm

The efficiency analysis of the proposed converter is shown in **Figure 4.6**, which demonstrates the reduction of efficiency with the increase of a duty cycle. It can be explained by a phenomenon that the current value is augmented as D is enhanced, which yields the minute power loss in the circuit elements. Efficiency of the proposed converter is compared with converters presented in [29] and [32]. It can be seen from Figure 4.8 that the efficiency of the proposed converter is high at low duty cycle values (upto 0.6) in comparison with the reference converters. The efficiency of the proposed converter drastically drops as the duty cycle exceeds 0.6. The reason for this sharp decrease in efficiency is due to large parasitic elements values. The efficiency could be greatly increased if elements with low parasitics are utilized in the experimental power circuit.

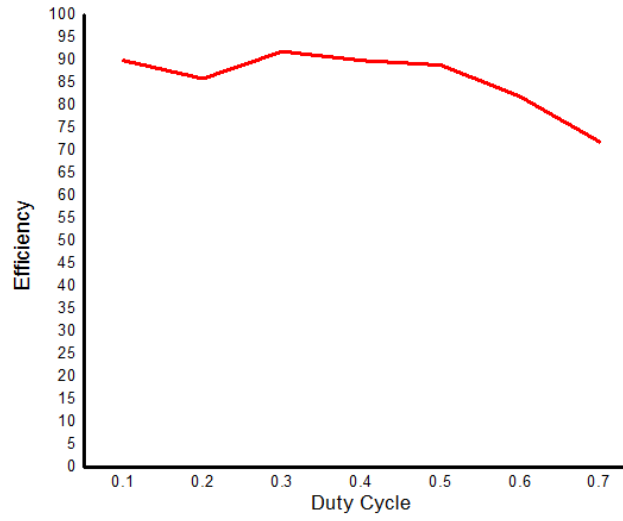


Figure 4.6. Efficiency variation with Duty cycle

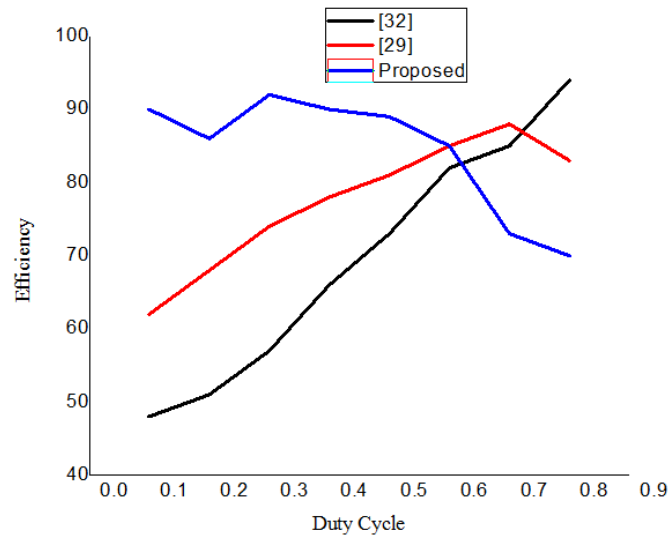
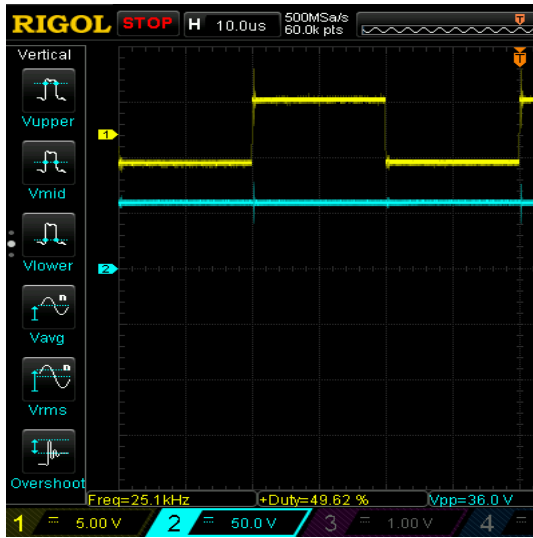
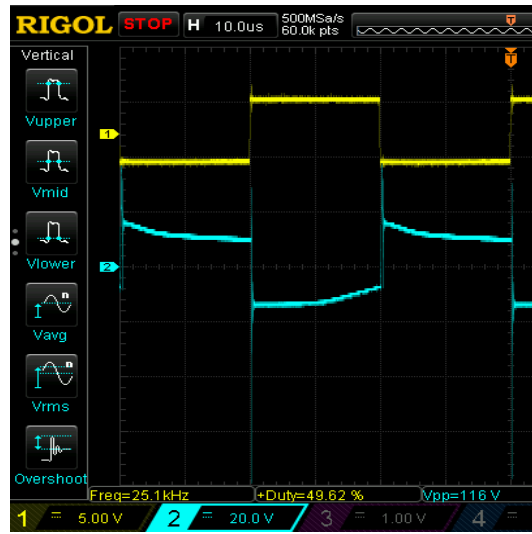


Figure 4.7. Efficiency variation of the proposed and other recent converters with duty cycle.



(a)



(b)

Figure 4.8. Experimental waveforms in CCM for; (a) Output Voltage; (b) inductor L_1 Current.

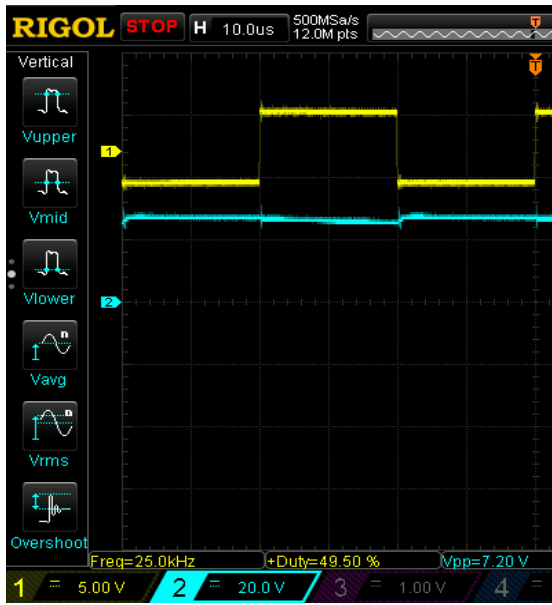


(a)

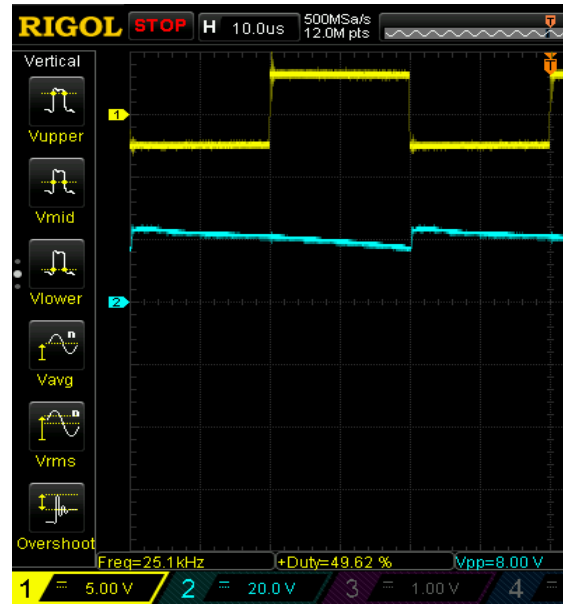


(b)

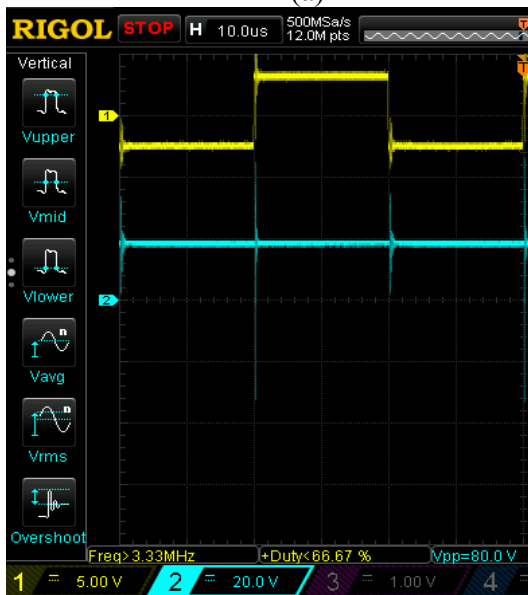
Figure 4.9. Experimental waveforms in CCM for; (a) inductor L_2 Voltage; (b) inductor L_3 Voltage



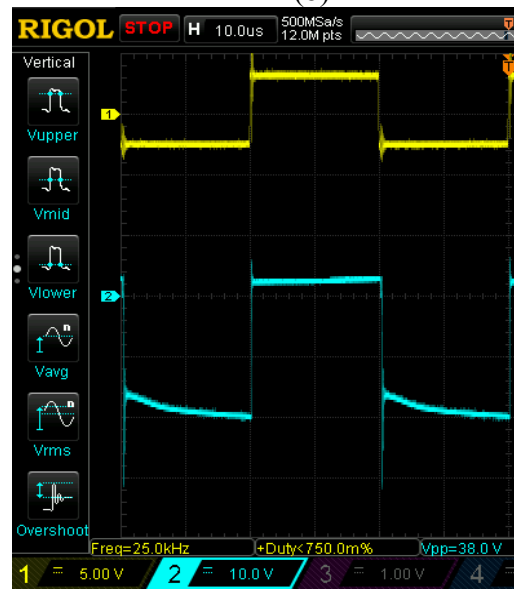
(a)



(b)



(c)



(d)

Figure 4.10. Experimental waveforms in CCM for; (a) Capacitor C_1 Voltage (b) Capacitor C_2 Voltage; (c) Capacitor C_3 Voltage (d) Diode D_1 Voltage

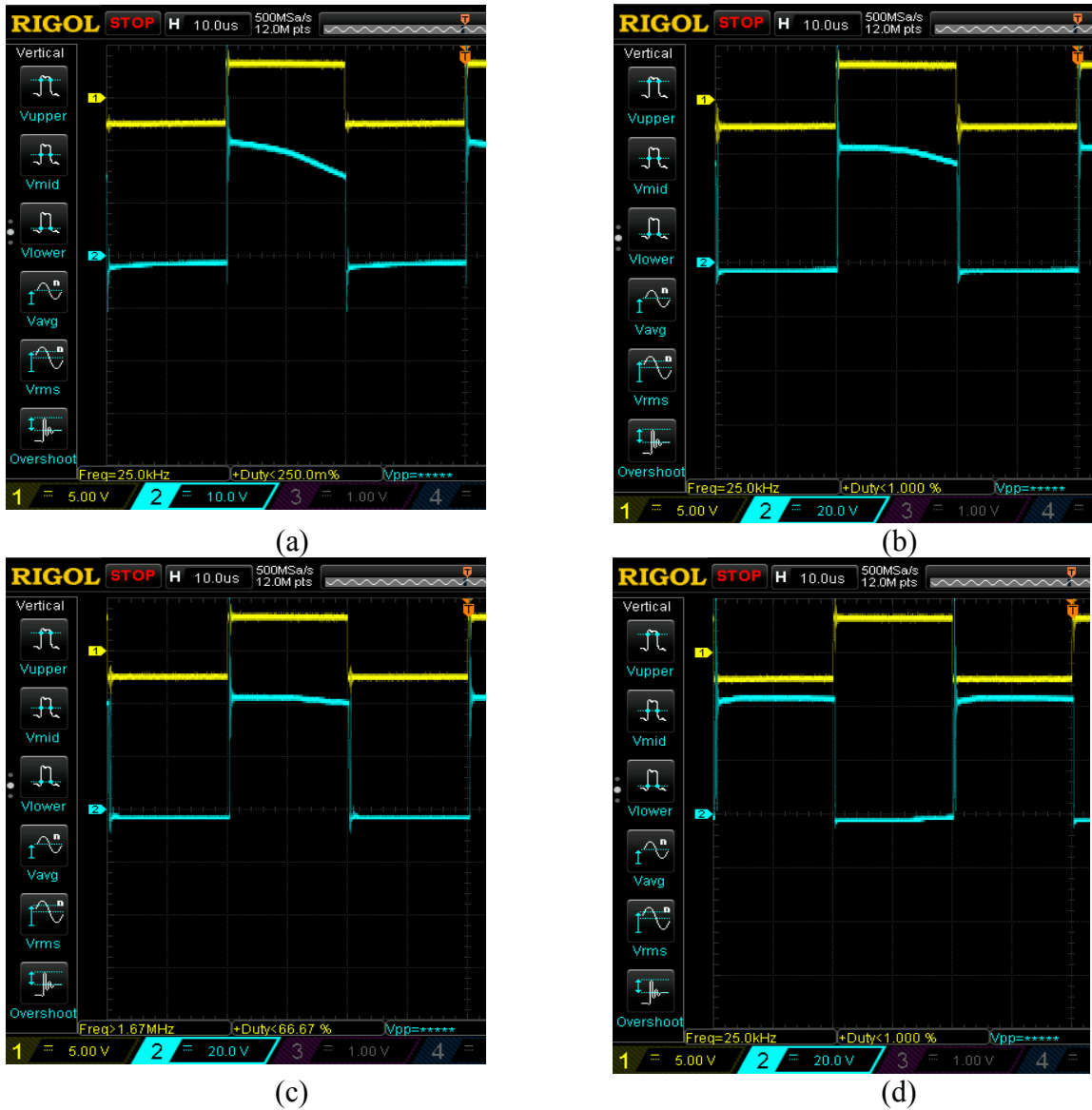


Figure 4.11. Voltage waveforms (Experimental) in CCM for; (a) Diode D_2 ; (b) Diode D_3 ; (c) Diode D_4 ; (d) Switch.

Table 4.6. Power loss in converter components and efficiency

	Switch	Diodes	Inductors	Capacitors	Efficiency (%)	Duty (%)
Loss (W)	17	16	54	3.2	73	70
	1.5	7.5	4	1.4	85	60
	0.9	1.25	1.14	0.15	89	50
	0.11	0.57	0.27	0.03	90	40
	0.03	0.41	0.09	0.014	92	30
	0.0024	0.9	0.016	0.006	86	20
	0.0014	0.2	0.006	0.004	90	10

Table 4.7. Specifications of the proposed converter in DCM.

Input voltage	12 V
Switching frequency	25 KHz
Inductors L_1, L_2, L_3	30u, 60u, 300u
Capacitors C_1, C_2	8 u F
Capacitors C_3, C_4	220 u F
Power switch	IRFP250
Diodes	MUR3060PT
Duty cycle	50%
Load Resistor	200 Ohm

4.4 Simulation and Experimental Results for DCM

The proposed converter operates in DCM by considering the inductance values provided in **Table 4.7**. The key waveforms in DCM are shown in Figures. 4.12 and 4.13. As shown in Figure 4.12(a), the voltage of the three inductors is in accordance with equations (31),(32), (34), (35), (38), and (39). The voltage of the capacitors shown in Figure 4.12 (b) is in accordance with (33), (36), and (40). The voltage and current waveforms of the four diodes shown in Figure 4.13 reaffirm the theoretical analysis, as depicted in Figure 3.9. The experimental results for DCM are provided in Figures. (4.14-4.18).The output voltage at 50% duty ratio is 66.4 Volts. It should be noted that the experimental results reaffirm the simulation results with some differences due to the effect of parasitic elements and also the quality of components used in the laboratory. The comparison of simulation and experimental results is tabulated in Table 4.8. The voltage gain variation with duty cycle in DCM operation is illustrated in Figure 4.19.

Table 4.8. Comparison of simulation and experimental results of the proposed converter in DCM.

	Simulation (D=50% , Vi=12 V)	Experiment (D=50%, Vi=12 V)
V_0	112	66.4
V_{L1}, V_{L2}, V_{L3}	12, 38, 37	10.6, 22.1, 22.3
V_{C1}, V_{C2}, V_{C3}	60, 38, 42	32, 23, 19
$V_{D1}, V_{D2}, V_{D3}, V_{D4}$	25, 17, 36, 36	31.1, 13.5, 31.24, 31.6
V_S	33	30
I_{L1}, I_{L2}, I_{L3}	9, 3.8, 0.75	3.5, 1.2, 0.38
$I_{D1}, I_{D2}, I_{D3}, I_{D4}$	3.8, 3.7, 1.7, 1.3	1.8, 1.7, 0.53, 0.42
I_S	6.2	3.3

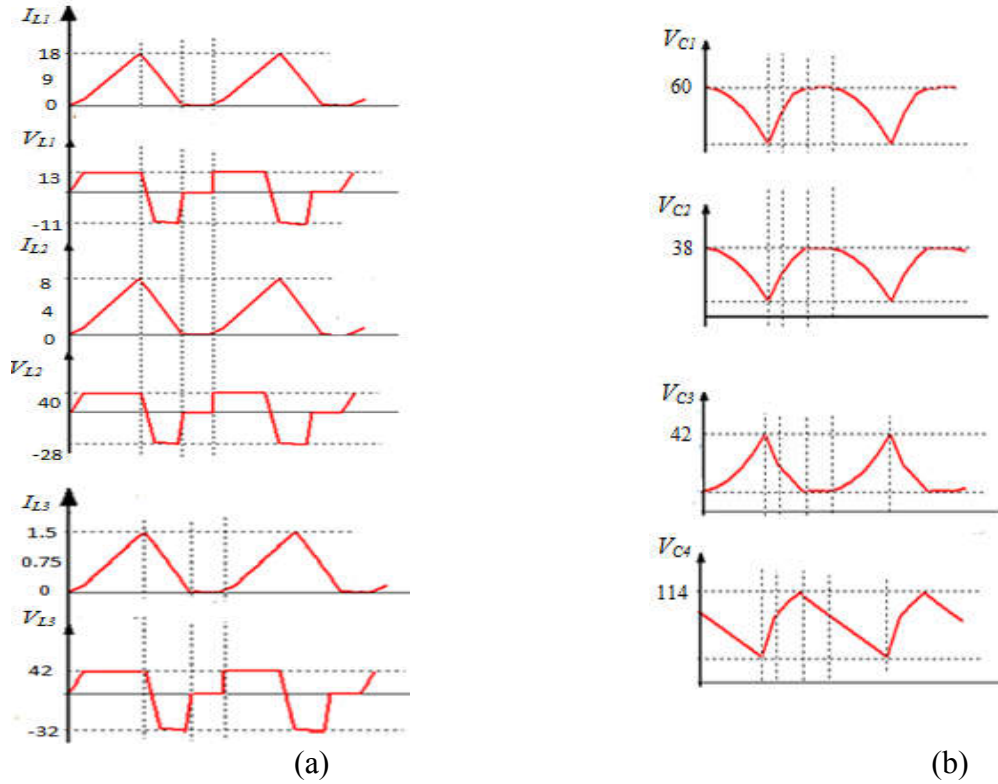


Figure 4.12. Current and voltage waveforms (simulation) in DCM for; (a) inductors L_1 , L_2 and L_3 ; (b) capacitor C_1 , C_2 , C_3 and C_4 .

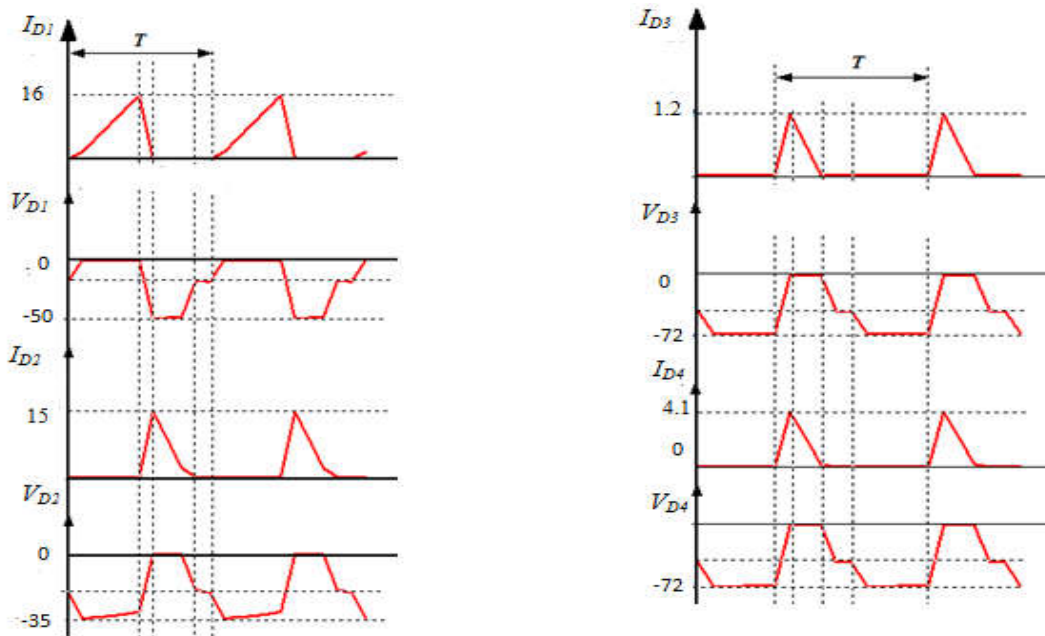
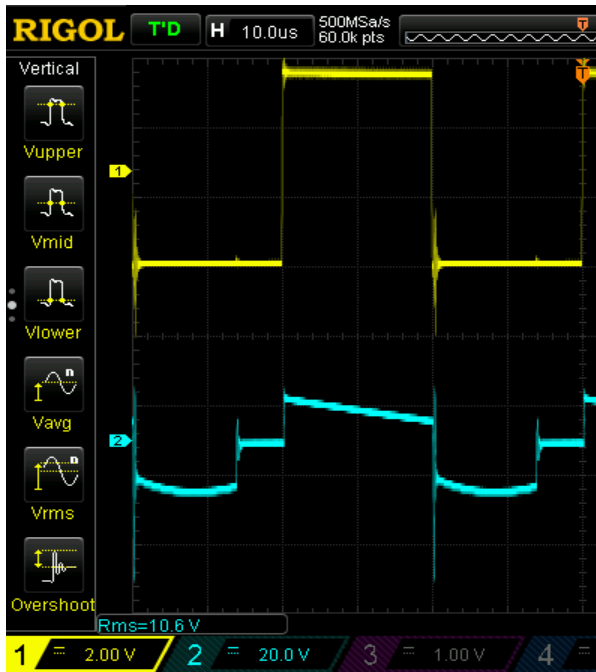
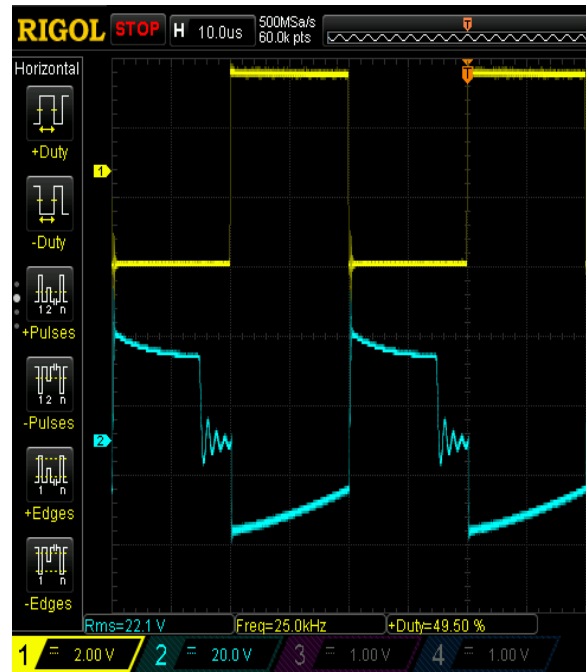


Figure 4.13. Current and voltage waveforms (simulation) in DCM for Diodes (D_1 - D_4).

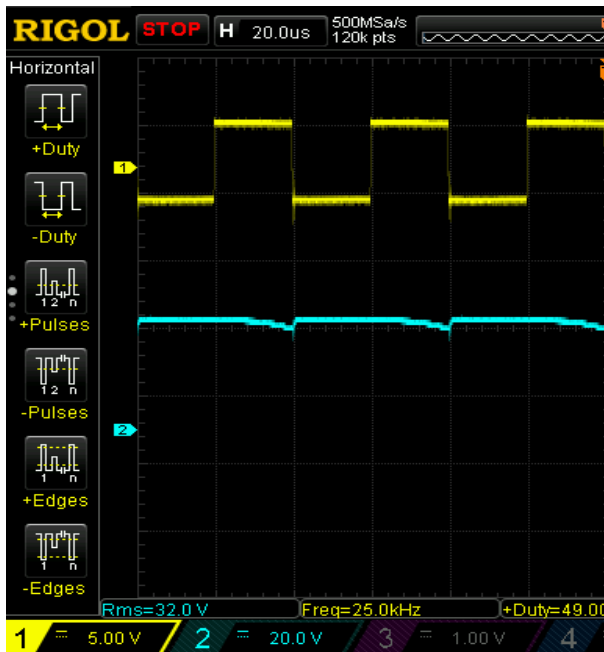


(a)

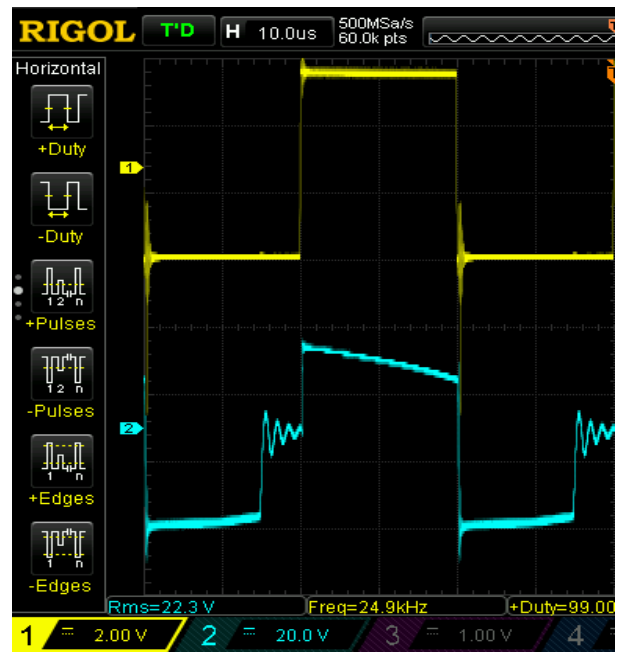


(b)

Figure 4.14. voltage waveforms (Experimental) in DCM for; (a) inductor L_1 ; (b) inductor L_2

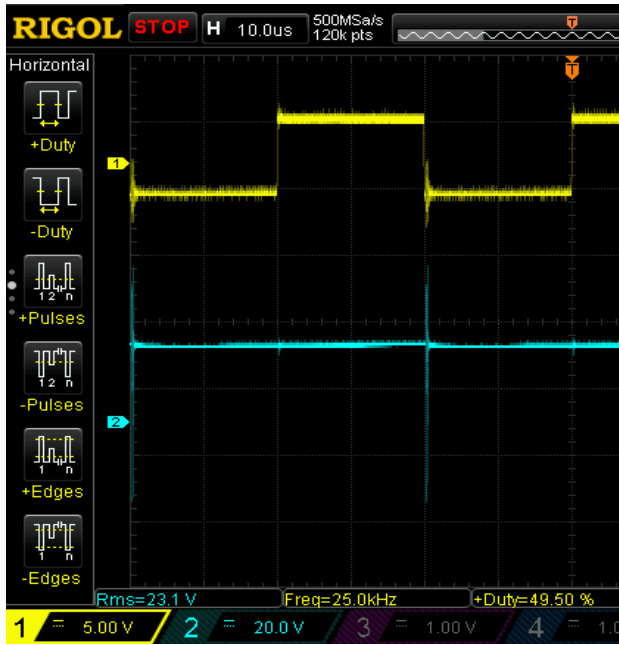


(a)

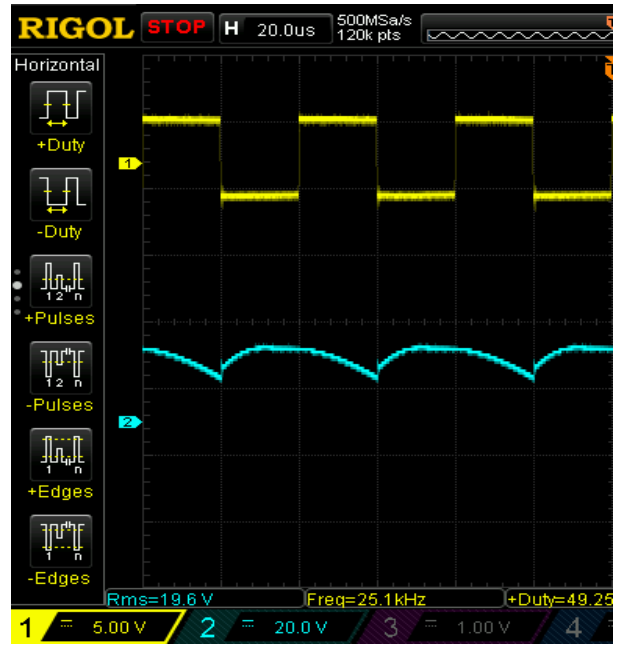


(b)

Figure 4.15. Voltage waveforms (Experimental) in DCM for; (a) capacitor C_1 ; (b) inductor L_3



(a)

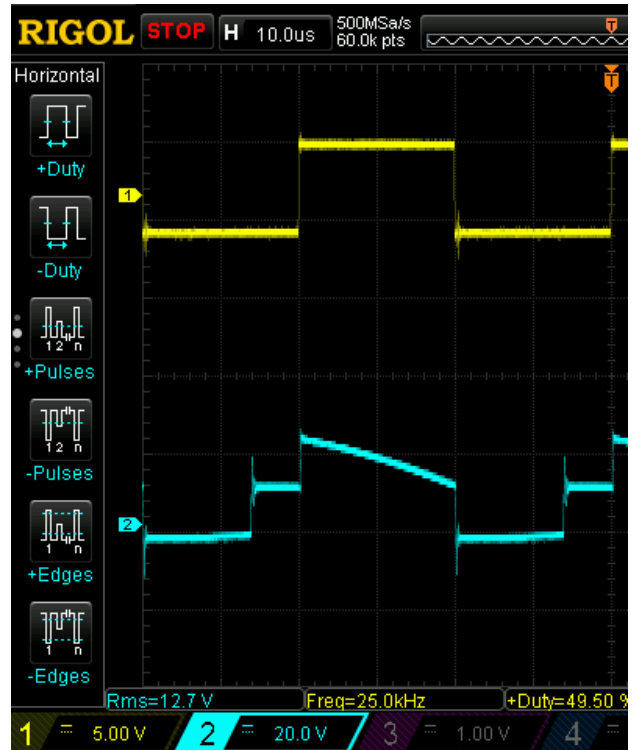


(b)

Figure 4.16. Voltage waveforms (Experimental) in DCM for; (a) capacitor C_2 ; (b) capacitor C_3



(a)



(b)

Figure 4.17. Voltage waveforms (Experimental) in DCM for; (a) Diode D_1 ; (b) Diode D_2

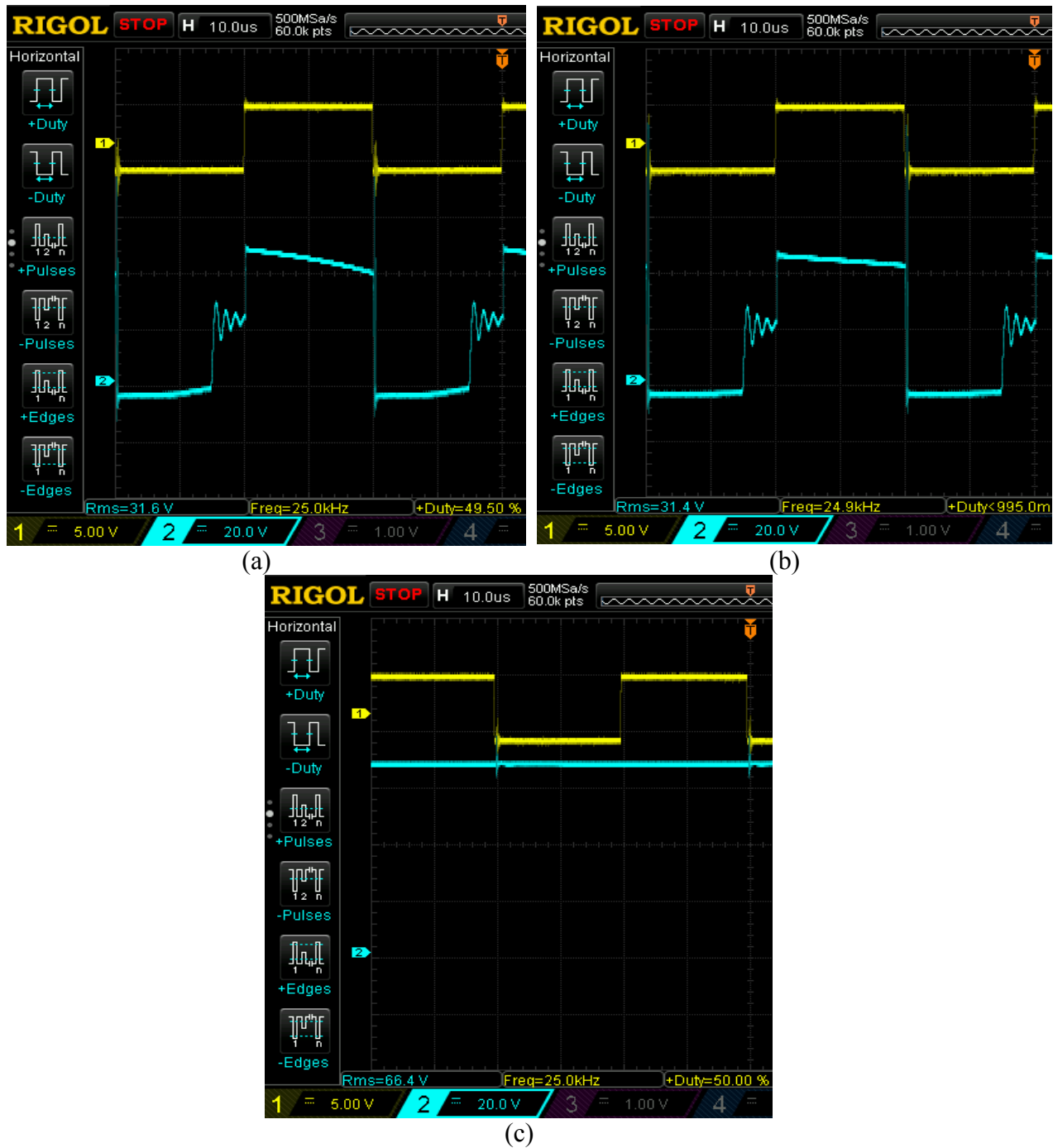


Figure 4.18. Voltage waveforms (Experimental) in DCM for; (a) Diode D_3 ; (b) Diode D_4 ; (c) Capacitor C_4 .

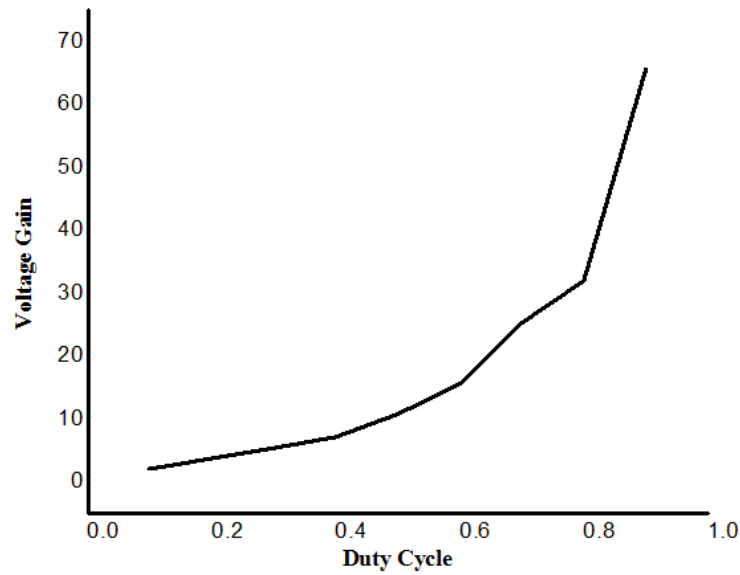


Figure 4.19. Voltage gain vs duty cycle (DCM operation)

4.5 Summary of the comparison results

In this section, the results obtained from theoretical analysis, simulation and experimental prototype will be examined. Also, comparison analysis with the recent converters will be discussed.

It can be observed from the previous discussions that the mathematical concepts are fairly validated by the simulation results. Also, considering **Table 4.4**, it can be seen that the experimental results authenticate the simulation results with some trivial differences. This small deviation is due to the effect of parasitic elements. At low duty cycles, the impact of the parasitics is little since the current values are small. However, at high duty cycles, their effect becomes dominant, which may cause considerable variation from the expected result. In the experimental prototype, components with reasonably large parasitic values are utilized due to the unavailability of the components in the local market. Inductors were designed manually with the available resources. Thus, the efficiency of the converter reduces drastically at high duty cycles. The parasitics' effect can be diminished by using good quality components with low equivalent series resistance (ESR) values and fine quality inductor core. The gain of the proposed converter compared with the recent boost converters is high from 0.6 to 0.9. Even though the converters presented in section 4.1 have comparable or high voltage gain at low duty cycles, but these converters have either a higher number of components and employed more switches. These converters are inappropriate for applications that require high voltage gain, such as interfacing low voltage sources like PV panels to a universal DC bus (380 volts) in DC microgrid.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5. Conclusion

In this section, the research work is summarised, and key outcomes of the proposed converter are presented. Future prospective of the research work is discussed, and possible modifications are proposed.

5.1 Summary

In this thesis, a new structure for the DC-DC boost converter was designed and analyzed. The voltage lift technique was employed using a single switch to boost up the output voltage. The resulting gain equation indicated that the proposed converter could achieve high voltage gain as compared to other conventional converters which makes it more suitable for high step-up applications such as photo-voltaic system, boosting up the low voltage of solar panels to the required dc bus voltage and impart noteworthy role in augmenting the voltage in DC nano-grids. Moreover, current stress on the switch was studied and compared with the other converters. It was concluded that the current stress on the switch is low, which in results enhances the converter's efficiency. Simulation results and theoretical concepts were fairly validated by experimental results. The output voltage obtained in CCM and DCM from experimental setup was 58 V and 66.4V, respectively considering $V_i = 12V$, $f = 25kHz$, $D = 50\%$ and $D' = 50\%$. The switch current at this percentage in CCM and DCM was found to be 2A and 3.3A, respectively. Furthermore, the efficiency variation with a duty cycle (D) was illustrated, and maximum efficiency of 92% was achieved at a 30% duty cycle.

5.2 Reseach Contribution

The main focus of this research work was to design a new structure of DC-DC boost converter which can yield maximum gain at reasonable duty cycle values while utilizing minimum number of elements and semiconductor devices. The idea initiated from already-published research article as presented in [33]. In [33] the circuit has achieved an adequate voltage gain while emplyoying lesser number of circuit components. However, the voltage gain was still limited due to circuit parameters. To improve the voltage gain and reduce the voltage and current stress on circuit components, a new charge pump branch was added to the existing circuit in [33]. As a result, the voltage gain was greatly improved and the voltage and current stress on circuit components was reduced. Efficiency of the proposed converter was compared with some recent converters. The graph indicated high efficiency of the proposed converter at low duty cycle values compared with other converters while efficiency of the proposed converter at high duty cycles showed reduction due to the limitation of the laboratory setup. If components with low ESR values are employed, the efficiency of the proposed converter will be greater even at high duty cycle values.

5.3 Recommendation for future work

For future studies, for further enhancement in the voltage gain and power level, the interleaved concept can be integrated into the existing topology. As power densities continue to rise, interleaved boost designs become a powerful tool to keep currents manageable and increase efficiency. For high-power applications (greater than 1.5 kW), boost converters need to be connected parallel in an interleaved manner to increase the output current and reduce the input current ripple. In the interleaved converter, the current is split into two power paths; conduction losses can be reduced, which in turn increases overall efficiency.

For voltage regulation, Fuzzy logic controller implementation will be studied. As the output of the proposed converter is proportional to the input voltage, any change in the input voltage will cause significant variation in the output voltage. To compensate for the change in input voltage, the duty cycle must be adjusted to maintain the required output voltage.

References:

- [1]. Forouzesh, M., Shen, Y., Yari, K., Siwakoti, Y.P., Blaabjerg, F.: High-efficiency high step-up DC DC converter with dual coupled inductors for grid-connected photovoltaic systems. *IEEE Trans. Power Electron.* Vol.33, no.7, pp. 5967–5982 (2018).
- [2]. Pratt, A., Kumar, P., Aldridge, T.V.: Evaluation of 400 V DC distribution in telco and data centers to improve energy efficiency. In: *Proc. INTELEC*, pp. 32–39 (2007)
- [3]. Velasco-Quesada, G., Guinjoan-Gispert, F., Piqué-López, R., Román-Lumbreras, M., Conesa-Roca, A.: Electrical PV array reconfiguration strategy for energy extraction improvement in grid-connected PV systems. *IEEE Trans. Ind. Electron.* **56**(11), 4319–4331 (2009)
- [4]. Sanjida Moury, John Lam, Vineet Srivastava, Ron Church, “A novel multi-input converter using soft-switched single-switch input modules with integrated power factor correction capability for hybrid renewable energy systems,” in *Proc. IEEE (APEC)*, 2016, pp. 786 – 793.
- [5] F. M. Shahir, E. Babaei, M. Sabahi, and S. Laali, “A new dc-dc converter based on voltage lift technique,” *International Trans. Elect. Energy Syst.*, vol. 26, pp. 1260-1286, June 2016.
- [6] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Leman, “Step-up dc-dc converters: a comprehensive review of voltage-boosting techniques, topologies, and applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.
- [7] W. Qian, D. Cao, J. G. Cintron-Rivera, M. Gebben, D. Wey, and F. Z. Peng, “A switched-capacitor DC-DC converter with high voltage gain and reduced component rating and count,” *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul./Aug. 2012.
- [8] B. Wu, S. Li, K. M. Smedley, and S. Singer, “A family of two-switch boosting switched-capacitor converters,” *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5413–5424, Oct. 2015.
- [9]. Prudente, M., et al., “Voltage multiplier cells applied to non-isolated DC-DC converters,” *IEEE Transactions on Power Electronics* Vol.23, no.2, pp. 871-887, 2008.
- [10]. X. Zhang and T. C. Green, “The modular multilevel converter for high step-up ratio DC-DC conversion,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015.
- [11]. K. C. Tseng, C. C. Huang, and C. A. Cheng, “A high step-up converter with voltage-multiplier modules for sustainable energy applications,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 1100–1108, Dec. 2015.
- [12] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, S. J. Andreasen, and G. E. Town, “Y-source boost DC/DC converter for distributed generation,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1059–1069, Feb. 2015.

- [13] Y. Tang, D. Fu, J. Kan, and T. Wang, "Dual switches DC/DC converter with a three-winding-coupled inductor and charge pump," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 461–469, Jan. 2016.
- [14] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio DC-DC conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015.
- [15] W. Li, X. Xiang, C. Li, W. Li, and X. He, "Interleaved high step-up ZVT converter with built-in transformer voltage doubler cell for generation system," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 300–313, Jan. 2013.
- [16] F. L. Luo, "Luo-converters, voltage lift technique," in *Proc. 29th Annu. IEEE Power Electron. Spec. Conf.*, 1998, vol. 2, pp. 1783–1789.
- [17] F. L. Luo, "Luo-converters, a series of new DC-DC step-up (boost) conversion circuits," in *Proc. 2nd Int. Conf. Power Electron. Drive Syst.*, 1997, vol. 2, pp. 882–888.
- [18] F. Zhang, F. Z. Peng, and Z. Qian, "Study of the multilevel converters in DC-DC applications," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, 2004, pp. 1702–1706.
- [19] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "New magnetically coupled impedance (Z-) source networks," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7419–7435, Nov. 2016.
- [20] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC-DC converter photovoltaic systems: Power optimization issues," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 403–411, Feb. 2011.
- [21] R. Gules, L. L. Pfitscher, and L. C. Franco, "An interleaved boost DC-DC converter with large conversion ratio," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2003, vol. 1, pp. 411–416.
- [22] Y. Berkovich and B. Axelrod, "Switched-coupled inductor cell for DC-DC converters with very large conversion ratio," *IET Power Electron.*, vol. 4, no. 3, pp. 309–315, 2011.
- [23] Andrade, António Manuel Santos Spencer, Luciano Schuch, and Mário Lúcio da Silva Martins. "Analysis and design of high-efficiency hybrid high step-up dc-dc converter for distributed pv generation systems." *IEEE Transactions on Industrial Electronics* 66.5 (2018): 3860-3868.
- [24] Maalandish, Mohammad, Seyed Hossein Hosseini, and Tohid Jalilzadeh. "High step-up dc/dc converter using switch-capacitor techniques and lower losses for renewable energy applications." *IET Power Electronics* 11.10 (2018): 1718-1729.

- [25] Bahrami, Hamid, et al. "Modified step-up boost converter with coupled-inductor and super-lift techniques." *IET power Electronics* 8.6 (2015): 898-905.
- [26] Li, Yiyang, SwamidossSathiakumar, and John Long Soon. "Multiple lift DC–DC boost converter using CLC cell." *Australian Journal of Electrical and Electronics Engineering* 16.1 (2019): 46-55.
- [27].Farzad Mohammadzadeh Shahir, Ebrahim Babaei, Murtaza Farsadi,"Extended Topology for Boost DC-DC Converter," IEEE Trans. Power Electron.,vol. 34, pp.2375 – 2384, March 2019.
- [28] F.M. Shahir, E. Babaei, M. Sabahi, and S. Laali, "A new dc-dc converter based on the voltage lift technique," *International Trans. Elec. Energy Syst. (ETEP)*, vol. 26, pp. 1260-1286, June 2016.
- [29] Ahmad Alzahrani, Poryya Shamsi, and Mehdi Ferdowsi,"An interleaved non-isolated DC-DC boost converter with diode-capacitor cells" in ICRERA, San Diego, CA, USA, Nov 5-8 2017.
- [30] Mohamad Reza Banaei, SajadGhabeliSani,"Analysis and Implementation of a New SEPIC-Based Single-Switch Buck-Boost DC-DC Converter With Continuous Input Current" IEEE Transactions on Power Electronics, Vol. 33, pp. 10317 – 10325, Issue: 12, Dec. 2018.
- [31] Nilanjan Tewari, V.T. Sreedevi, "A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems",solar. Energy Vol. 171, pp. 466 – 477,1 September 2018.
- [32] MahmoodrezaEskandarpourAzizkandi, Farzad Sedaghati, Hossein Shayeghi,"Design and analysis of a high step-up single-switch coupled inductor DC-DC converter with low-voltage stress on components for PV power application",Int J Circ Theor Appl, Vol. 47 ,issue 7, pp. 1121 –1151,12March 2019.
- [33] Shahir, Farzad Mohammadzadeh, Ebrahim Babaei, and Murtaza Farsadi. "Voltage-lift technique based nonisolated boost dc–dc converter: Analysis and design." *IEEE Transactions on Power Electronics* 33.7 (2017): 5917-5926.