Development of Nonlinear Optimization Techniques Based PID Controller for SEPIC Converter

by

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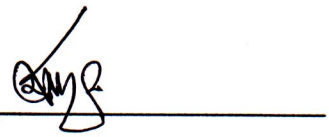

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DEDICATION

I would like to dedicate this thesis to my family who supported me through both good and tough times. They always give me the motivation to move forward in my life.

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ABSTRACT

This thesis presents an investigation on closed loop stability of SEPIC (Single-Ended Primary Inductor Converter) converter by employing an optimized PID controller where the parameters are tuned by Genetic Algorithm (GA) and Simulated Annealing (SA) algorithm. Genetic Algorithm is a stochastic algorithm inspired by natural evolution and is extensively used as an optimization technique in power electronics in recent years. SA refers to an optimization technique, based on the principles of thermodynamics where the analogy of cooling of metal and freezing into a minimum energy level is utilized. Here, State Space Average method is deployed to model and obtain the transfer function of the converter based system. Hence, GA and SA based PID controller is studied and implemented in the system so that the stability of the converter can be evaluated and compared with the conventional PID controller. Different fitness functions (IAE, ITAE, ISE, ITSE) and performance parameters like percentage of overshoot, rise time, settling time and peak amplitude are taken into account to investigate the stability of the system. The step responses of the closed loop system are obtained through rigorous simulation in MATLAB. It is observed that, GA-PID-2 (IAE) is the most optimized controller among the entire GA based PID controllers as the overshoot is the lowest (3.43%) and peak amplitude is 1.03. Moreover, rise time (0.000102s) and settling time (0.00418s) are also in acceptable limit. However, GA-PID-2 (ISE) shows quick rise (0.000102s) and settling time (0.000676s) but the overshoot of ISE is 11.3% which is much greater than IAE of GA-PID-2. Meanwhile, SA-PID-2 (IAE) is the most optimized controller among all other SA based controllers where the value of overshoot is 2.2% and peak amplitude is 1.01. For Rise time and settling time, the values for SA-PID-2 (IAE) are 0.000665s and 0.000104s respectively which are in acceptable limit. Though SA-PID-3 (IAE) shows quick rise time (0.000118s), the overshoot is high (22.2%). Therefore, SA-PID-2 (IAE) is selected as the most optimized and suitable controller for SEPIC converter. For changed value of inductor, the simulation is done for GA-PID-2 (for IAE) and SA-PID-2 (for IAE), it is observed that less overshoot is obtained than conventional PID controller (overshoot 17.3%). For GA-PID-2, the overshoot is 3.36% and for SA-PID-2 the value is 9.12%. So, it is evident that, nonlinear optimization technique based PID controller is providing more optimized result in case of any change in the value of inductor of the circuit than conventional PID controller. However, GA is more suitable option than SA in terms of designing the controller for less overshoot. Therefore, GA-PID-2 (IAE) is the most optimized controller for SEPIC converter in this investigative study.

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LIST OF ACRONYMS

Abbreviated Form	Descrption
LED	Light Emiting Diode
HID	High Intensity Discharge
SEPIC	Single Ended Primary Inductance Converter
GA	Genetic Algorithm
SA	Simulated Annelaing Algorithm
FNN	Fuzzy Neural Network
PSO	Particle Swarm Optimization
FLC	Fuzzy Logic Controller
MPPT	Maximum Power Point Tracking
NLC	Non Linear Carrier
PFC	Power Factor Correction
GMPPT	Global Maximum Power Point Tracking
SPDT	Single Pole Double Throw
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BJT	Bipolar Junction Transistor
IAE	Integral of Absolute Magnitude of Error
ITAE	Integral of Time multiplied by Absolute Error
ISE	Integral of Squared Error
ITSE	Integral of Time multiplied by Squared Error

CHAPTER 1

INTRODUCTION AND BACKGROUND STUDY

Power Electronics is the technology associated with efficient conversion, control and conditioning of electric power by static means from its available input into the desired electrical output form. With rapid advancement and modernization in the field of power electronics, researchers are more aligned in modeling and designing reliable and robust systems to achieve better performance and efficiency. In this regard, DC-DC converters are on the top of the choice because of their widespread applications in battery charger [1], maximum power point tracking [2], LED drivers [3], motor drivers [4], braking system [5], renewable energy system applications, such as photovoltaic, fuel cell and wind turbine, dc micro-grid, telecommunication industries, high intensity discharge (HID) lamp ballast used in automotive headlamps, hybrid vehicles and switching mode regulators such as uninterruptable power supplies (UPS) etc. [6-11]. Hence, the increasing demand of dc-dc step up converters for various household and industrial applications demands further improvement of the performance of conventional dc-dc converters that could convert a fixed dc voltage level into a desired level in the most efficient way.

1.1 Introduction

The DC-DC conversion techniques were established in the 1920s. Some preliminary types of DC-DC converters were used in industrial applications before the Second World War. Research was blocked during the war, but applications of DC-DC converters were recognized. After the war, the communication technology developed very rapidly and required low voltage dc power supplies. This resulted in the rapid development of DC-DC converter techniques.

Different types of converters are maneuvered in various applications in power electronics. Amongst them, Boost converter has high input current ripple and Buck converter gives high output voltage ripple. However, the effects can be minimized if coupled with switched capacitor [12] and switched inductor [13]. Meanwhile, Buck-boost converter suffers from harmonics and to minimize that phenomenon a large capacitor or an LC filter is required [14]. Hence, Cúk converters solve both of these problems by using an

extra capacitor and inductor [15]. However, huge amount of electrical stress on the components result in device failure or overheating. Thus, SEPIC converter manifests better performance in terms of these problems and is brought into play in different sectors of power electronics [16].

Various close loop control techniques like hysteresis current control, PI control and PID control are employed to observe the performance of SEPIC converter [17]. Among these control techniques, PID control is the most common and extensively used method for power converters. It comprises of three terms named as Proportional, Integral and Derivative component which are tuned by empirical methods like Ziegler-Nicholas method, analytical methods and different optimization techniques [18]. By taking into account different tuning methods, these parameters are tuned for close loop system to enhance the performance of the SEPIC converter.

However, it is quite difficult to determine the exact values of these parameters as most of the classical methods demand explicit mathematical modeling of the processing plant and may not provide satisfactory results because of input-output disturbances or nonlinear behavior of the plant. For this reason, nonlinear optimization methods named as Genetic Algorithm (GA), Simulated Annealing Algorithm (SAA), Particle Swarm Optimization (PSO), and Fuzzy Neural Network (FNN) are proven to be powerful tools in control engineering in recent years [19-21].

In this work, some effective nonlinear optimization techniques will be investigated and performances will be evaluated of the proposed system. Techniques like genetic algorithm (GA) and Simulated Annealing Algorithm (SAA) will be used for investigation and overall comparative analysis with the conventional method will be reported in terms of different performance parameters like rise time, settling time, overshoot, steady-state error and voltage stability.

1.2 Literature review

DC-DC converters are considered to be of immense economical importance in today's modern society. The converters are classified into Buck, Boost, Buck-Boost, Cuk and SEPIC converters. Among all the converters, SEPIC converter is the most significant and widely employed as it can both increase and decrease the voltage by changing the duty cycle without reversing the polarity [22]. Moreover, small input ripple current and extension to multiple outputs are two prominent features of this converter [23].

The output voltage of SEPIC converter should be constant and stable. In this regard, feedback control is necessary so that stable output can be achieved. Various control techniques are employed in SEPIC converter to achieve better performance in terms of regulating the output voltage [24]. Among different control methods, Hysteresis Current control, PI control, PID control are the most common and extensively used methods for power converters [25]. Moreover, the usage of this controller ranges from small-scale industries to high technology industries [26], high step up applications [27], refineries and ship buildings.

PID controller comprises of three terms named as Proportional, Integral and Derivative component which are tuned by empirical methods like Ziegler-Nicholas method [28], analytical methods and different optimization techniques. The proportional component utilizes proportion of the system error to control it, the integral component introduces lag in the system which implicates that it evaluates the total past history of error by continuously integrating the area under the error curve and the derivative component responds to the rate of change of error and which can pro-duce a correction before the error approaches to a larger value. By taking into account different tuning methods, these parameters are tuned for different close loop systems to enhance the performance of the system. However, it is quite difficult to determine the exact values of these parameters as most of the classical methods demand explicit mathematical modeling of the processing plant and may not provide satisfactory results because of input-output disturbances or nonlinear behavior of the plant. To encounter the nonlinear behavior of the plant, different nonlinear optimization techniques are employed in order to design optimized PID controller. Genetic Algorithm (GA) , Simulated Annealing (SA) Algorithm, Particle Swarm Optimization (PSO), Fuzzy Neural Network (FNN) are some of the techniques that are widely employed in optimizing the parameters of PID controller with a view to achieving better controller for power converters.

A Rubaai et al [29] employed a fuzzy controller in DC-DC converter where two different fuzzy logic control topologies are developed and implemented using different types of DC-DC converters such as the buck, the boost, the buck-boost, and the SEPIC converters. *A. El Khateb et al.* [30] presents a fuzzy logic controller (FLC)-based single-ended primary-inductor converter (SEPIC) for maximum power point tracking (MPPT) operation of a photovoltaic (PV) system. The fuzzy controller for the SEPIC MPPT scheme shows high precision in current transition and keeps the voltage without any changes, in the variable-load case, represented in small steady-state error and small overshoot.

Wei-Der Chang et al. [31] presented an improved particle swarm optimization algorithm to search for the optimal PID controller gains for a class of nonlinear systems. The proposed algorithm is to modify the velocity formula of the general PSO systems in order for improving the searching efficiency. In the improved PSO-based nonlinear PID control system design, three PID control gains are optimized to obtain stable output from nonlinear system. *W. M. Utomo et al.* [32] proposes a neural network control scheme of a DC-DC buck-boost converter using online learning method. In this technique, a back propagation algorithm is derived. The controller is designed to stabilize the output voltage of the DC-DC converter and to improve performance of the Buck-Boost converter during transient operations.

R. Zane et al [33] proposed a nonlinear-carrier (NLC) control for high-power-factor rectifiers based on fly back, Cuk or SEPIC converters operated in the continuous conduction mode. In the NLC controller, the switch duty ratio is determined by comparing a signal proportional to the integral of the switch current with a periodic nonlinear carrier waveform. *Subbiah Durgadevi et al*. [34] presents the analysis and design of a single phase power factor correction (PFC) scheme using a DC–DC single ended primary inductance converter (SEPIC) with genetic algorithm (GA)-tuned proportional integral (PI) controllers. A systematic off-line design approach using GA for optimizing the parameters of the PI controller is proposed and the performance is compared with the conventional Z–N tuned PI controller. *Stefan Daraban et al*. [35] present a novel MPPT (maximum power point tracking) algorithm, based on a modified GA (genetic algorithm).

When photovoltaic systems are affected by partial shading, a GMPPT (global maximum power point tracking) algorithm is required to increase the energy harvesting capability of the system. *Amin Alqudah* [36] states a new adaptive control method used to adjust the output voltage and current of DC-DC power converter under different sudden changes in load where a PID controller is used. The gains of the PID controller tuned using Simulated Annealing (SA) algorithm which is part of Generic Probabilistic Metaheuristic family. The new control system is expected to have a fast transient response feature, with les undershoot of the output voltage and less over-shoot of the reactor current.

Genetic algorithm, a heuristic search algorithm [37-42] is proven to be the most powerful optimization technique in a large solution space and has received quite a lot of attention in control engineering in recent years. This algorithm is a method for solving both constrained and unconstrained optimization problems that is based on natural selection, the process that drives biological evolution and repeatedly modifies a population of individual solutions. In this case, GA is used to achieve optimum values of the PID controller [43-44] when implemented in close loop analysis of the SEPIC converter to investigate the stability of the system.

Simulated Annealing (SA) algorithm is a probabilistic search algorithm which is widely applied in power electronics [45], stability analysis in different power converters [46], robotics [47], bioinformatics [48] and optimization problems [49]. In order to make really strong metallic objects, slow and controlled cooling is followed which is known as annealing. Hence, the concept is applied in this thesis with an intention of achieving the values of the PID controller (k_P, k_I and k_D) without the requirement of manual tuning.

1.3 Statement of the Problem

SEPIC converter is one of the most widely employed converters in different applications of power electronics. As nonlinearity is associated with the system, obtaining stable and faster response is always a challenge for the control engineers. In case of open loop response of the converter, stable output can be achieved but high overshoot, longer rise time and settling time are noticed which is not desirable in modern power converters. In accordance to that, researchers are more aligned in developing compact, fast and robust power converters where stability can be achieved rapidly. In this regard, closed loop system is needed to achieve stable output with less overshoot, rise time and settling time and steady state error. For this, classical PID controller is employed but rigorous trial and error method is required to tune the parameters of the controller in order to achieve stable output. Hence, nonlinear optimization technique is deployed with a view to achieving optimized values of PID controller and acquiring enhanced performance of the overall system. Among various techniques, genetic algorithm and simulated annealing algorithm are implemented to design and develop optimized PID controller for SEPIC converter.

1.4 Thesis objectives

The main thesis objective is to develop nonlinear optimization technique based PID controller for SEPIC converter. However, more particularly, the objectives include:

- To observe and estimate different performance parameters of power electronic converters specifically DC-DC SEPIC converter.
- To analyze the compatibility of different nonlinear techniques for controller design of power electronic converters.
- To optimize the performance parameters of closed loop SEPIC converter employing nonlinear control techniques. To carry out a comparative analysis between conventional controller and nonlinear optimization technique based controller for SEPIC Converter.

1.5 Thesis organization

This thesis focuses on studying and developing nonlinear optimization technique based PID controller for obtaining better performance of SEPIC converter.

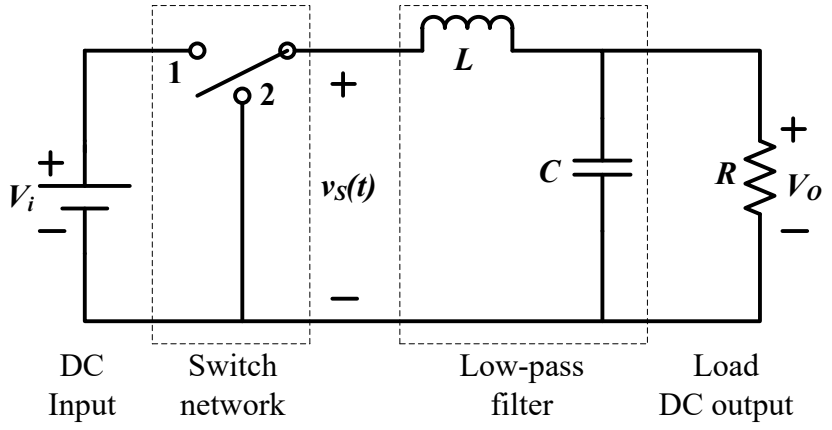
- In **Chapter 2**, different types of existing widely used dc-dc converters are discussed. The methods and analysis dc-dc converters are presented in details.
- In **Chapter 3**, conventional SEPIC converter is studied and State Space Modeling of the converter is illustrated. Then, open loop and closed loop analysis of the converter is carried out.
- In **Chapter 4**, general discussion on different nonlinear optimization techniques are reported. The elaborate discussion on implementation of Genetic Algorithm and Simulated Annealing Algorithm is depicted where overviews, objective function of the algorithm and design of the optimized PID Controller are stated.
- **Chapter 5** includes the simulation results of the nonlinear optimized PID controller for SEPIC converter. The performance parameters are investigated and quantitative analysis is presented.
- **Chapter 6** contains the conclusion of the thesis, where the brief summary of the results is given with some recommendations for future works.

CHAPTER 2

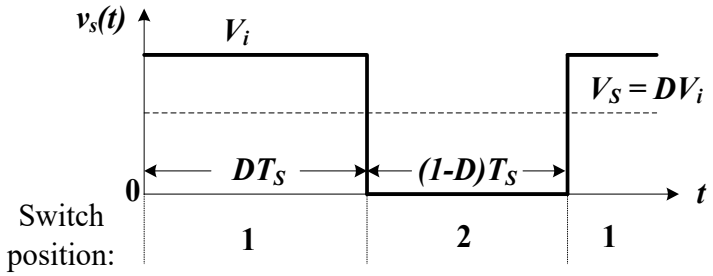
DC-DC CONVERTERS

DC-DC power converters are employed in a variety of applications, including renewable energy systems, power supplies for personal computers, office equipment, spacecraft power systems, laptop computers, and telecommunications equipment, as well as dc motor drives. The input to a dc-dc converter is an unregulated dc voltage, V_i. The converter produces a regulated output voltage, V_O, having a magnitude (and possibly polarity) that differs fromV_i. For example, in a computer off-line power supply, the 120 V or 240 V ac utility voltage is rectified, producing a dc voltage of approximately 170 V or 340 V, respectively.

A dc-dc converter then reduces the voltage to the regulated 5 V or 3.3 V required by the processor ICs. High efficiency is invariably required, since cooling of inefficient power converters is difficult and expensive. The ideal dc-dc converter exhibits 100% efficiency; in practice, efficiencies of 70% to 95% are typically obtained. This is achieved using switched-mode, or chopper, circuits whose elements dissipate negligible power. Pulse-width modulation (PWM) allows control and regulation of the total output voltage. This approach is also employed in applications involving alternating current, including high-efficiency dc-ac power converters (inverters and power amplifiers), ac-ac power converters, and some ac-dc power converters (low harmonic rectifiers).



(a)



(b)

Fig. 2.1 The buck converter consists of a switch network that reduces the dc component of voltage, and a low pass filter that removes the high-frequency switching harmonics: (a) schematic, (b) switch voltage waveform.

2.1 Working principle of a dc-dc converter

A basic dc-dc converter circuit known as the buck converter is illustrated in Fig. 2.1. A single-pole double-throw (SPDT) switch is connected to the dc input voltage V_i as shown. The switch output voltage $v_s(t)$ is equal to V_i when the switch is in position 1, and is equal to zero when the switch is in position 2. The switch position is varies periodically, such that $v_s(t)$ is a rectangular waveform having period T_S and duty cycle D. The duty cycle is equal to the fraction of time that the switch is connected in position 1, and hence $0 \leq D \leq 1$. The switching frequency f_S is equal to $1/T_S$. In practice, the SPDT switch is realized using semiconductor devices such as diodes, power MOSFETs, IGBTs, BJTs, or thyristors. Typical switching frequencies lie in the range of 1 kHz to 1 MHz, depending on the speed of the semiconductor devices.

The switch network changes the dc component of the voltage. By Fourier analysis, the dc component of a waveform is given by its average value. The average value of $v_s(t)$ is given by

$$V_S = \frac{1}{T_S} \int_0^{T_S} v_s(t)\, dt = DV_i \tag{2.1}$$

The integral is equal to the area under the waveform, or the height V_i multiplied by the time DT_S. It can be seen that the switch network reduces the dc component of the voltage by a factor equal to the duty cycle D. Since $0 \leq D \leq 1$, the dc component of v_S is less than or equal to V_i.

The power dissipated by the switch network is ideally equal to zero. When the switch contacts are closed, then the voltage across the contacts is equal to zero and hence the power dissipation is zero. When the switch contacts are open, then there is zero current and the power dissipation is again equal to zero. Therefore, the ideal switch network is able to change the dc component of voltage without dissipation of power.

In addition to the desired dc voltage component V_s, the switch waveform $v_s(t)$ also contains undesired harmonics of the switching frequency. In most applications, these harmonics must be removed, such that the converter output voltage $v_O(t)$ is essentially equal to the dc component $V_O = V_S$. A low-pass filter is employed for this purpose. The converter of Figure 2.1 contains a single-section L-C low-pass filter. The filter has corner frequency f_0 given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.2}$$

The corner frequency f_0 is chosen to be sufficiently less than the switching frequency f_S, so that the filter essentially passes only the dc component of $v_s(t)$. To the extent that the inductor and capacitor are ideal, the filter removes the switching harmonics without dissipation of power. Thus, the converter produces a dc output voltage whose magnitude is controllable via the duty cycle D, using circuit elements that (ideally) do not dissipate power.

The conversion ratio G known as voltage gain is defined as the ratio of the dc output voltage V_O to the dc input voltage V_i under steady-state conditions:

$$G = \frac{V_O}{V_i} \tag{2.3}$$

For buck converter it is given by

$$G = D \tag{2.4}$$

This equation is plotted in Fig. 2.2.

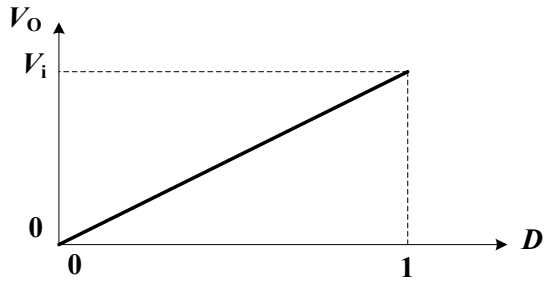


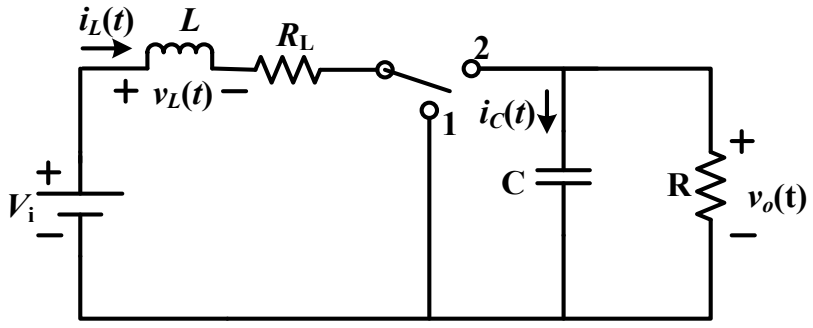
Fig. 2.2 Buck converter dc output voltage V_O vs. duty cycle D

It can be seen that the dc output voltage V_O is controllable between 0 and V_i, by adjustment of the duty cycle D.

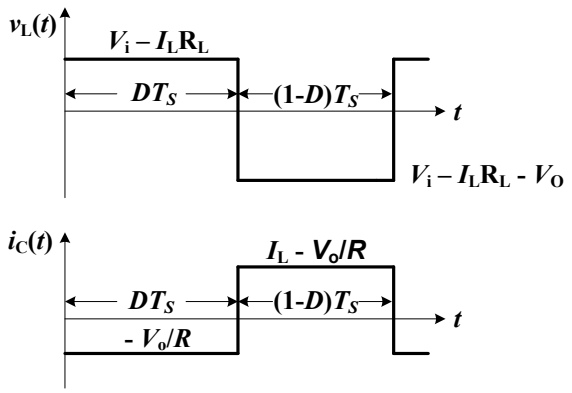
2.2 Analysis of converter waveforms

Under steady-state conditions, the voltage and current waveforms of a dc-dc converter can be found by use of two basic circuit analysis principles. The principle of inductor volt-second balance states that the average value, or dc component, of voltage applied across an ideal inductor winding must be zero. This principle also applies to each winding of a transformer or other multiple winding magnetic devices. Its dual, the principle of capacitor amp second or charge balance, states that the average current that flows through an ideal capacitor must be zero. Hence, to determine the voltages and currents of dc-dc converters operating in periodic steady state, one averages the inductor current and capacitor voltage waveforms over one switching period, and equates the results to zero.

The equations are greatly simplified by use of a third artifice, the small ripple approximation. The inductor currents and capacitor voltages contain dc components, plus switching ripple at the switching frequency and its harmonics. In most well designed converters, the switching ripple is small in magnitude compared to the dc components. For inductor currents, a typical value of switching ripple at maximum load is 10% to 20% of the dc component of current. For an output capacitor voltage, the switching ripple is typically required to be much less than 1% of the dc output voltage. In both cases, the ripple magnitude is small compared with the dc component, and can be ignored.



(a)



(b)

Fig. 2.3 A non-ideal boost converter: (a) schematic, (b) inductor voltage and capacitor current waveforms

As an example, consider the boost converter of Fig. 2.3(a). A resistor R_L is included in series with the inductor, to model the resistance of the inductor winding. It is desired to determine simple expressions for the output voltage V_O, inductor current I_L, and efficiency η. Typical inductor voltage and capacitor current waveforms are sketched in Fig. 2.3(b).

With the switch in position 1, the inductor voltage is equal to $v_L(t) = V_i - i_L(t)R_L$. By use of the small ripple approximation, we can replace $i_L(t)$ with its dc component I_L, and hence obtain $v_L(t) \approx V_i - I_L R_L$. Likewise, the capacitor current is equal to $i_C(t) \approx -v_O(t)/R$, which can be approximated as $i_C(t) = -V_O/R$.

When the switch is in position 2, the inductor is connected between the input and output voltages. The inductor voltage can now be written $v_L(t) = V_i - i_L(t)R_L - v_O(t) \approx V_i - I_L R_L - V_O$. The capacitor current can be expressed as $i_C(t) = i_L(t) - v_O(t)/R \approx I_L - V_O/R$.

When the converter operates in steady state, the average value, or dc component, of the inductor voltage waveform $v_L(t)$ must be equal to zero. Upon equating the average value of the $v_L(t)$ waveform of Figure 2.4(b) to zero, we obtain

$$0 = D(V_i - I_L R_L) + (1 - D)(V_i - I_L R_L - V_O) \tag{2.5}$$

Likewise, application of the principle of capacitor charge balance to the capacitor current waveform of Fig. 2.4(b) leads to

$$0 = D\left(-\frac{V_O}{R}\right) + (1-D)(I_L - \frac{V_O}{R}) \tag{2.6}$$

Equations (2.5) and (2.6) can now be solved for the unknowns V_O and I_L. The result is

$$\frac{V_O}{V_i} = \frac{1}{(1-D)} \frac{1}{(1+\frac{R_L}{(1-D)^2 R})} \tag{2.7}$$

$$I_L = \frac{V_i}{(1-D)^2 R} \frac{1}{(1+\frac{R_L}{(1-D)^2 R})} \tag{2.8}$$

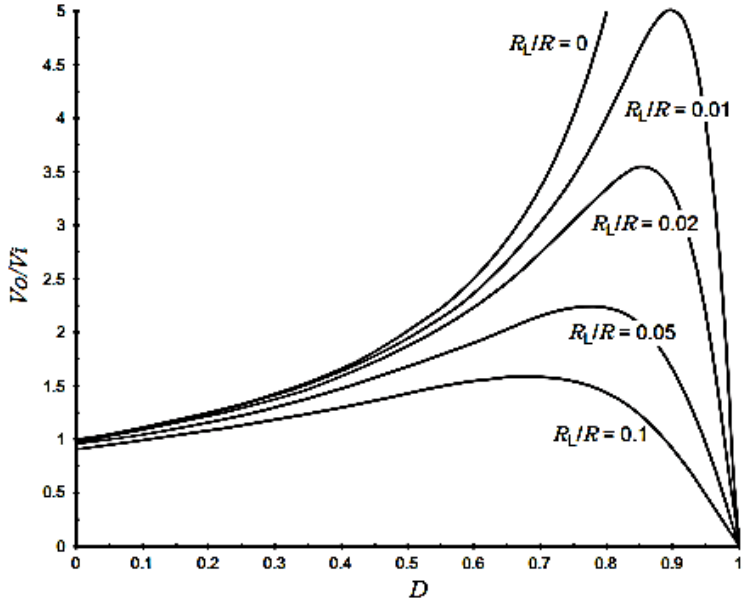


Fig. 2.4 Output voltage vs. duty cycle, for the non-ideal boost converter of Fig. 2.3

Equation (2.7) is plotted in Fig. 2.4, for several values of R_L/R. In the ideal case when R_L = 0, the voltage conversion ratio G is equal to one at $D = 0$, and tends to infinity as D approaches one. In the practical case where some small inductor resistance R_L is present, the output voltage tends to zero at $D = 1$. In addition, it can be seen that the inductor winding resistance R_L (and other loss elements as well) limits the maximum output voltage

that the converter can produce. Obtaining a given large value of V_O/V_i requires that the winding resistance R_L be sufficiently small.

The converter efficiency can also be determined. For this boost converter example, the efficiency is equal to

$$\eta = \frac{P_{out}}{P_{in}} = \frac{{V_O}^2/R}{V_i i_L} \tag{2.9}$$

Substitution of (2.7) and (2.8) into (2.9) leads to

$$\eta = \frac{1}{\left(1+\frac{R_L}{(1-D)^2 R}\right)} \tag{2.10}$$

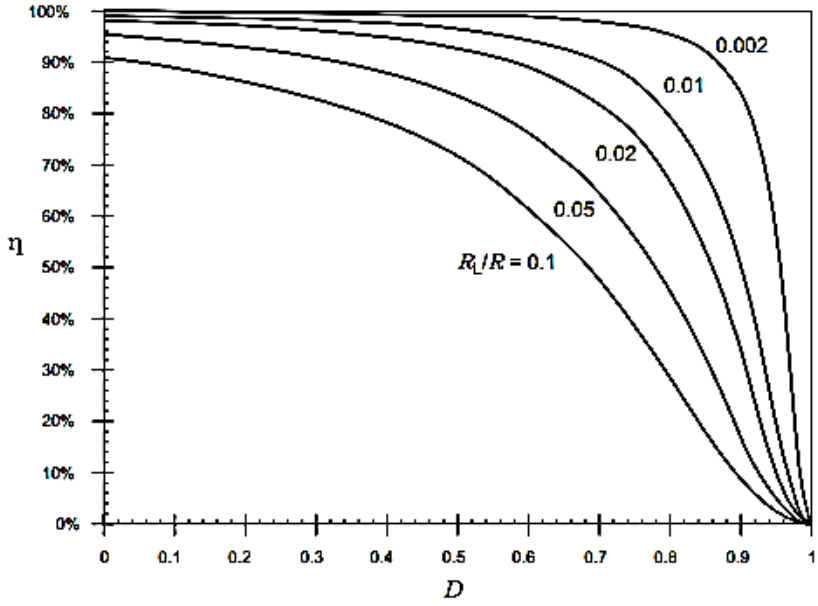


Fig. 2.5 Efficiency vs. duty cycle, for the non-ideal boost converter of Fig. 2.3

This expression is plotted in Fig. 2.5, again for several values of R_L/R. It can be seen that, to obtain high efficiency, the inductor winding resistance R_L should be much smaller than $(1-D)^2R$. This is much easier to accomplish at low duty cycles, where $(1-D)$ is close to unity, that at high duty cycles where $(1-D)$ approaches zero. Consequently, the efficiency is high at low duty cycles, but decreases rapidly to zero near$D = 1$. This behavior is typical of converters having boost or buck-boost characteristics.

2.3 Converter circuit topologies

A large number of dc-dc converter circuits are known that can increase or decrease the magnitude of the dc voltage and/or invert its polarity [50-54]. These are basically divided into two categories- Isolated converters and Non-isolated converters. In this chapter, a discussion on different non-isolated converters is presented.

2.3.1 Non- isolated converters

The commonly used non-isolated converters are:

1. Buck converter
2. Boost converter
3. Buck-boost converter
4. Cuk converter
5. SEPIC converter

In each of the above the converters, the switch is realized using a power MOSFET and diode. However, other semiconductor switches such as IGBTs, BJTs, or thyristors can be substituted if desired.

2.3.1.1 Buck converter

Buck converter shown in Fig. 2.6 reduces the output voltage. When the switch is on, the diode is reverse biased and the inductor is charged by V_i. When the switch is off, the diode is forward biased and the inductor discharges to load. It has a voltage gain of $G = D$ and it is plotted in Fig. 2.7.

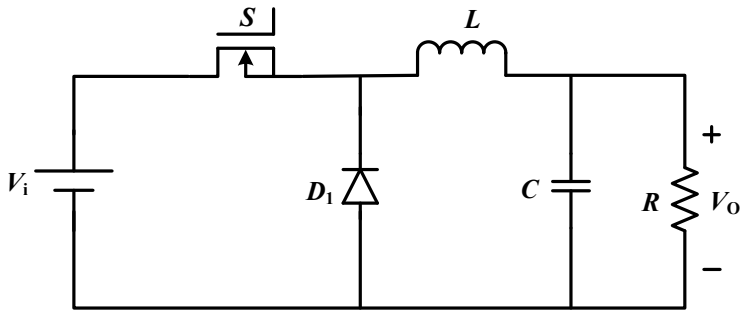


Fig. 2.6 Buck converter

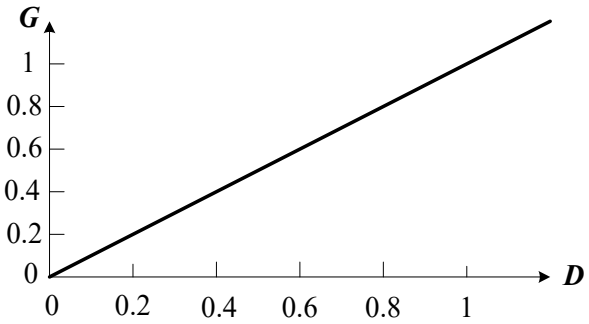


Fig. 2.7 Voltage gain versus duty cycle of buck converter

2.3.1.2 Boost converter

When the positions of switch and inductor are interchanged, the buck converter becomes boost converter shown in Fig. 2.8. It produces the output voltage greater than the input voltage. When the switch is on, the diode is reverse biased and the inductor is energized by V_i. When the switch is off, the diode gets forward biased and the inductor discharges to the load. The voltage gain of this converter is $G = 1/(1 - D)$ and it is depicted in Fig. 2.9.

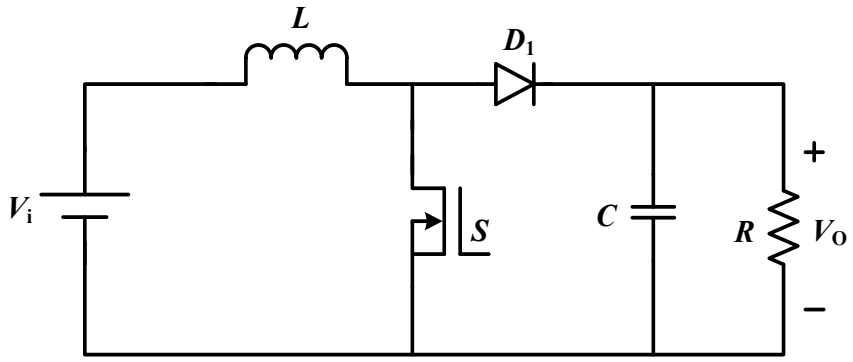


Fig. 2.8 Boost converter

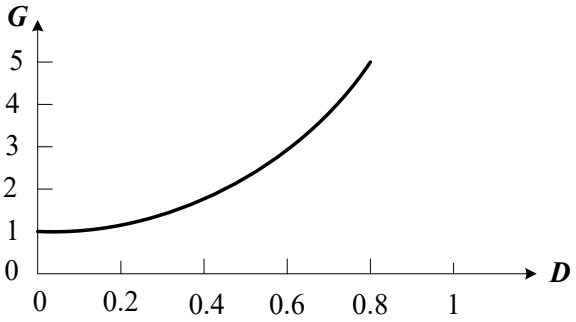


Fig. 2.9 Voltage gain versus duty cycle of boost converter

2.3.1.3 Buck-boost converter

The buck-boost converter is the cascaded form of buck converter and boost converter. In the buck-boost converter shown in Fig. 2.10, the switch alternately connects the inductor across the power input and output voltages. This converter inverts the polarity of the voltage, and can either increase or decrease the voltage magnitude. When the switch is on, the diode is reverse biased and the inductor is charged, and the capacitor delivers power to load. When the switch is off, the diode gets forward biased and the inductor discharges to the capacitor and the load. The voltage gain is $G = -D/(1-D)$ and it is shown in Fig. 2.11. The voltage stress in the switches will be high. It has non pulsating current characteristics [47]-[48].

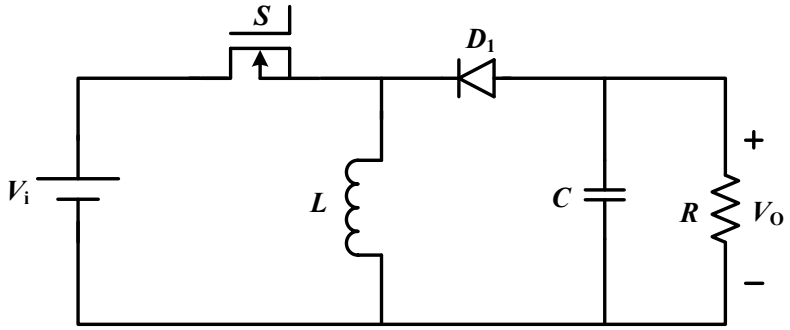


Fig. 2.10 Buck-boost converter

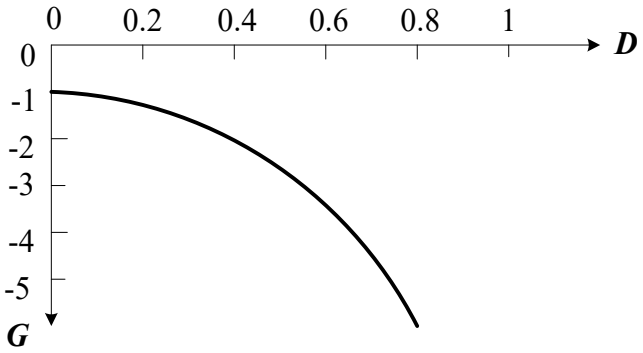


Fig. 2.11 Voltage gain versus duty cycle of buck-boost converter

2.3.1.4 Cuk converter

The Cuk converter contains inductors in series with the converter input and output ports. The switch network alternately connects a capacitor to the input and output inductors. The conversion ratio G is identical to that of the buck-boost converter. Hence, this converter also inverts the voltage polarity, while either increasing or decreasing the voltage magnitude. Fig. 2.12 and Fig. 2.13 show the circuit diagram and the voltage gain with respect to duty cycle respectively.

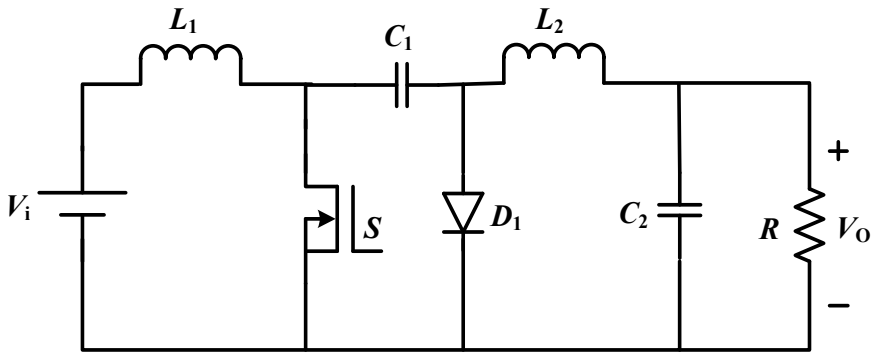


Fig. 2.12 Cuk converter

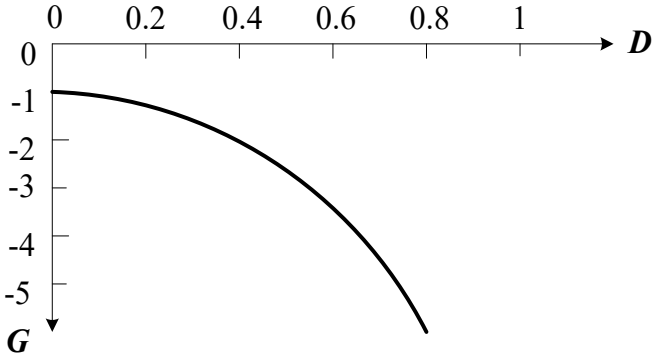


Fig. 2.13 Voltage gain versus duty cycle of cuk converter

The cuk converter has low switching losses and the highest efficiency. It can provide better output current characteristics due to the inductor on the output stage [55]-[57].

2.3.1.6 SEPIC converter

The single-ended primary inductance converter (SEPIC) can also either increase or decrease the voltage magnitude. However, it does not invert the polarity. The conversion ratio is $G = D/(1 - D)$. The circuit diagram and the voltage gain with respect to duty cycle are shown in Fig. 2.14 and Fig. 2.15 respectively.

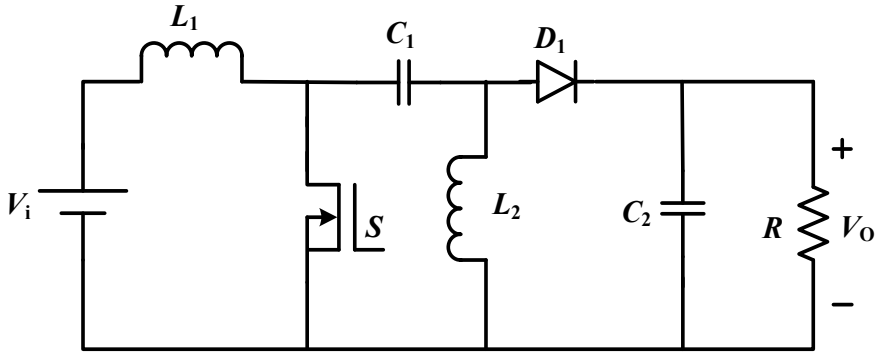


Fig. 2.14 SEPIC converter

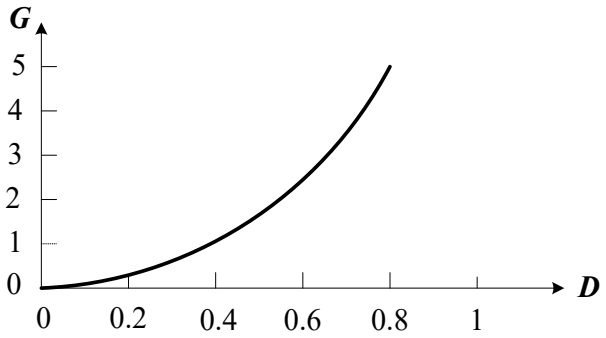


Fig. 2.15 Voltage gain versus duty cycle of SEPIC converter

Among all the converters, SEPIC converter is the most significant and widely employed as it can both step up and step down the voltage by changing the duty cycle without reversing the polarity. Moreover, small input ripple current and extension to multiple outputs are two prominent features of this converter [58]. For this reason, SEPIC converter is chosen as processing plant of this thesis. The mathematical modeling, open loop and closed loop response, implementation of optimized PID controller by nonlinear techniques, simulation results and comparative study are discussed in the forthcoming chapters.

CHAPTER 3

DC-DC SEPIC CONVERTER

Single Ended Primary Inductor converter is a widely used DC-DC converter which is a fourth-order system which makes it difficult to control and makes them only suitable for very slow varying applications. The output of the SEPIC is controlled by changing the duty cycle of the control transistor. *Hren & Slibar et al*. (2015) [59] have discussed that SEPIC is a DC-DC converter possessing high-voltage transfer gain, high power density, high efficiency, reduced ripple voltage and current. *Jaafer et al* (2013) [60] have studied that SEPIC converters are widely used in computer peripheral equipment, industrial applications and switch mode power supplies. *Chen & Sun* (2006) [61] have presented reduced order averaged modeling and analysis of soft switching DC-DC converters employing active clamping techniques which are applied in SEPIC converter.

Hence, it is identified that the SEPIC has high nonlinear behavior in static and dynamic conditions due to the switching nature of the power converter. The design of high performance control for SEPIC is a challenge for both the control engineers and the power electronic engineers. In general, a good control of DC-DC converters always ensures stability in arbitrary operating condition. With different state-space averaging techniques, a small-signal state-space equation of the converter system could be derived. For the purpose of optimizing the stability of SEPIC converter dynamics, while ensuring correct operation in any working condition, PI and PID control is a feasible approach. These control techniques offer several advantages such as stability, even for large line and load variations, reduce the steady error, robustness, good dynamic response and simple implementation. The main advantage of PI control schemes is its insusceptibility to plant/system parameter variations that lead to invariant dynamic and static response in the ideal case.

3.1 Conventional SEPIC Converter

A Single Ended Primary Inductor Converter (SEPIC) is a significant converter in power electronics whose output voltage can be controlled by the duty cycle of the switching device. The SEPIC converter consists of two inductors (L_1 and L_2), two capacitors (C_1 and C_2), a switch (S) with duty cycle (D), a diode (D_1), and a resistive load (R).

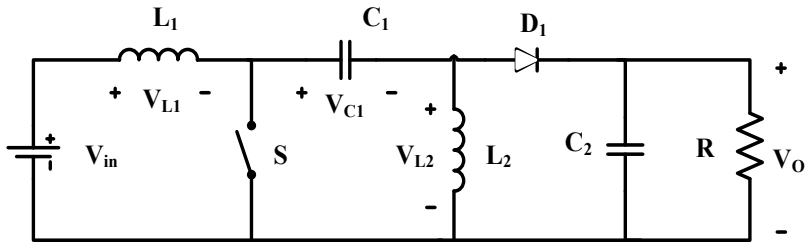


Fig. 3.1 Conventional SEPIC Converter [62]

The circuit diagram of the conventional SEPIC converter is shown in Fig. 3.1 and the equivalent circuits during ON and OFF states are shown in Fig. 3.2 (a & b). In SEPIC converter, at first when the switch is open, by applying KVL, is obtained. When the switch is closed, if KVL is applied in the inner loop is formed. So, capacitor C_2 is providing the load power in this case. The current through inductors L_1 and L_2 are ramping up and the capacitors (C_1 and C_2) are getting discharged. When the switch is open again, the capacitors are getting charged and inductor currents are getting discharged. In this case, KVL shows that $V_{L_1} = -V_o$.The average voltage across L_1 is zero.

So, the equation can be written as,

$$V_{L_1(avg)} = DV_{in} + (1-D)(-V_{out}) = 0$$

$$V_o(1-D) = DV_{in}$$

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{3.1}$$

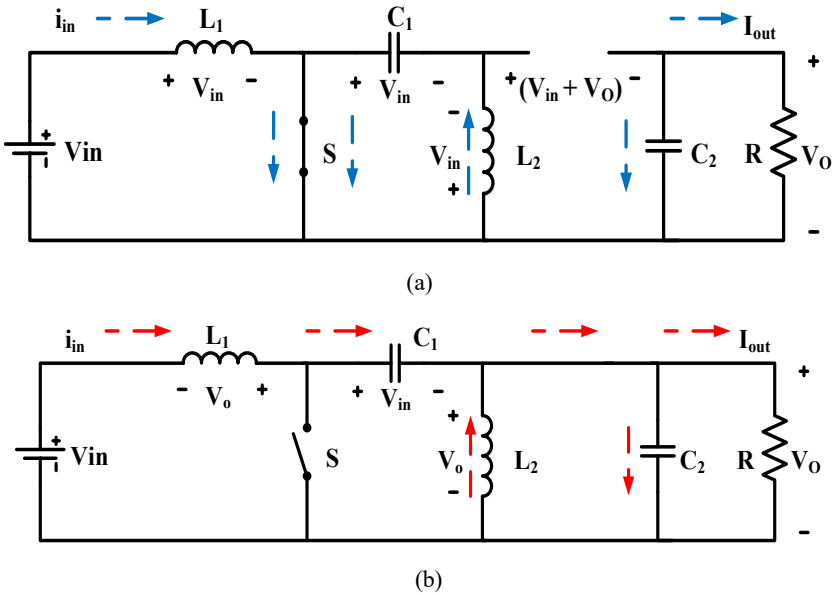


Fig. 3.2. Modes of operation of the conventional SEPIC converter (a) Switch ON and (b) Switch OFF

3.2 State Space Modeling

In order to represent the SEPIC converter by first order differential equation, state space average technique is taken into consideration as this mathematical model is best suited to describe any nonlinear dynamic system into simple form. A set of input, output and state variables are modeled in first order differential form and later the matrix is obtained. Hence, the state space representation provides a convenient and compact way to model and analyze a system with multiple inputs and outputs. Unlike the frequency domain approach, the use of the state space representation is to demonstrate the system with linear components and zero initial conditions which make it a handy tool to model power converters.

With a view to deriving the differential equations for the SEPIC converter, the circuit that is considered is as follows:

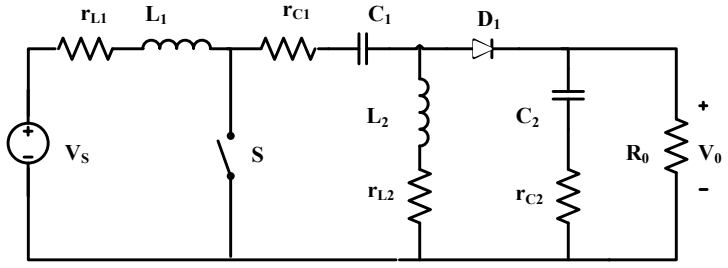


Fig. 3.3 Conventional SEPIC Converter

The state variables of SEPIC are considered as currents and voltages, respectively. When the converter is in continuous conduction mode, the operation can be outlined for two cases:

A. Switch (S) is ON and Diode (D_1) is OFF
B. Switch (S) is OFF and Diode (D_1) is ON

The circuit diagrams for case-A and case-B are given below as shown in Fig. 3.4:

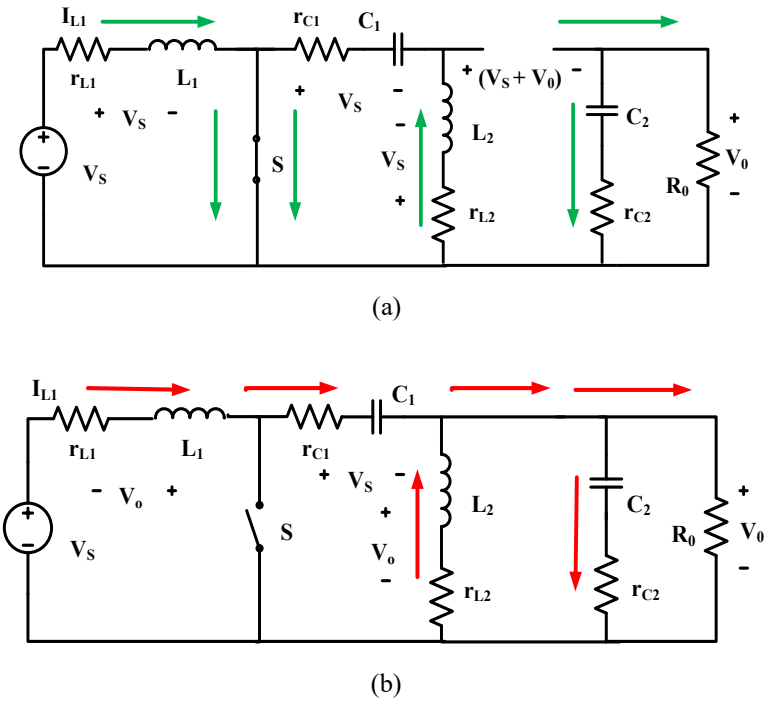


Fig. 3.4 Modes of operation for the SEPIC converter (a) case A and (b) case B

The corresponding equations for the two cases are stated below:

- *Switch (S) is ON and Diode (D_1) is OFF*:

$$\frac{dI_{L1}}{dt} = \frac{1}{L_1}(-r_{L1}I_{L1} + V_s) \tag{3.2}$$

$$\frac{dI_{L2}}{dt} = \frac{1}{L_2}[-(r_{C1} + r_{L2})I_{L2} + V_{C1}] \tag{3.3}$$

$$\frac{dV_{C1}}{dt} = -\frac{1}{C_1}I_{L2} \tag{3.4}$$

$$\frac{dV_{C2}}{dt} = -\frac{1}{C_2}\frac{1}{R_0 + r_{C2}}V_{C2} \tag{3.5}$$

- *Switch (S) is OFF and Diode (D_1) is ON*

$$\frac{dI_{L1}}{dt} = \frac{1}{L_1}[-(r_{C1} + r_{L1} + r_{C2}r_A)I_{L1} - r_{C2}r_A I_{L2} - V_{C1} - r_A V_{C2} + V_s] \quad (3.6)$$

$$\frac{dI_{L2}}{dt} = \frac{1}{L_2}[-r_{C2}r_A I_{L1} - (r_{L2} + r_{C2}r_A)I_{L2} - r_A V_{C2}] \quad (3.7)$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1} I_{L1} \quad (3.8)$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}[r_A I_{L1} + r_A I_{L2} - \frac{1}{R_0 + r_{C2}} V_{C2}] \quad (3.9)$$

where, $r_A = \frac{R_o}{(R_o + r_{C2})}$

For $r_{C1} = r_{C2} = 0$, $r_A = 1$, putting the value in above equations the simplified forms are obtained and they are as follows:

i) *For S ON and D_1 OFF*:

$$\frac{dI_{L1}}{dt} = \frac{1}{L_1}(-r_{L1} I_{L1} + V_s) \quad (3.10)$$

$$\frac{dI_{L2}}{dt} = \frac{1}{L_2}[-r_{L2} I_{L2} + V_{C1}] \quad (3.11)$$

$$\frac{dV_{C1}}{dt} = -\frac{1}{C_1} I_{L2} \quad (3.12)$$

$$\frac{dV_{C2}}{dt} = -\frac{1}{C_2 R_0} V_{C2} \quad (3.13)$$

So in matrix form, the following equation is obtained:

$$\frac{d}{dt}\begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix} = \begin{pmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-r_{L2}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{R_0 C_2} \end{pmatrix} \begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s$$

ii) *For S OFF and D_1 ON*:

$$\frac{dI_{L1}}{dt} = \frac{1}{L_1}[-r_{L1}I_{L1} - V_{C1} - V_{C2} + V_s] \tag{3.14}$$

$$\frac{dI_{L2}}{dt} = \frac{1}{L_2}[-r_{L2}I_{L2} - V_{C2}] \tag{3.15}$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}I_{L1} \tag{3.16}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}[I_{L1} + I_{L2} - \frac{1}{R_0}V_{C2}] \tag{3.17}$$

So, in matrix form, the following equation is achieved:

$$\frac{d}{dt}\begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix} = \begin{pmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & \frac{-r_{L2}}{L_2} & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{R_0C_2} \end{pmatrix} \begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{pmatrix} V_s$$

The state vector for the SEPIC converter is defined as

$$x(t) = \begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix},$$

where I_{L1} and I_{L2} are the currents through L_1 and L_2 respectively, V_{C1} and V_{C2} are the voltages across the capacitors C_1 and C_2 respectively. So, the overall state space representation is stated by the following equation:

$$x(t) = Ax(t) + Bu(t)$$

where,

$$A = A_1D + A_2(1-D)$$
$$B = B_1D + B_2(1-D)$$

Here , A and B are system matrix and control matrix. A_1 and B_1 stand for ON condition; A_2 and B_2 stand for OFF condition. A_1, A_2, B_1, B_2 are as follows:

$$A_1 = \begin{pmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-r_{L2}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{R_0 C_2} \end{pmatrix}, \quad A_2 = \begin{pmatrix} \frac{-r_{L1}}{L_1} & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & \frac{-r_{L2}}{L_2} & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{R_0 C_2} \end{pmatrix}$$

$$B_1 = \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{pmatrix}, \quad B_2 = \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

The output of the system is stated by the following equation:

$$y(t) = Cx(t)$$

$$y(t) = (0 \quad 0 \quad 0 \quad 1) \begin{pmatrix} I_{L_1} \\ I_{L_2} \\ V_{C_1} \\ V_{C_2} \end{pmatrix}$$

C is the output matrix. In this case voltage (V_{C2}) across capacitor C_2 is considered as output variable. y(t) is the output vector. Hence, the transfer function of the DC-DC SEPIC converter is achieved from the following equation:

$$H_4(s) = (sI - A)^{-1}B + C \qquad (3.18)$$

Here, $H_4(s)$ states the forth order transfer function of the system. In order to reduce the computation time and complexity in the controller design, the fourth-order system is converted into the second-order system so that the transient behavior of the reduced order model remains the same as that of the original order model by retaining the dominant poles. Thus, it is inferred that the time domain parameters of the reduced order model are retained as that of the original fourth order model. There are various model order reduction

methods available. Here, the moment matching technique has been applied to reduce the fourth-order system into the second-order system. The technique is essentially the matching of time-moments of full order model's response to those of the reduced order model. The transfer function for third order reduced model is given by the following equation:

$$H_3(s)=\frac{a_{31}+a_{32}s+a_{33}s^3}{1+a_{21}s+a_{22}s^2+a_{23}s^3} \tag{3.19}$$

Here, The values of a_{31} to a_{33} are found by using the coefficients C_0, C_1,C_2, C_3, C_4, C_5 as given in the following equations:

$$\begin{bmatrix} a_{31} \\ a_{32} \\ a_{33} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ C_0 & 0 & 0 \\ C_1 & C_0 & 0 \end{bmatrix} \begin{bmatrix} a_{21} \\ a_{22} \\ a_{23} \end{bmatrix} + \begin{bmatrix} C_0 \\ C_1 \\ C_2 \end{bmatrix} \tag{3.20}$$

$$\begin{bmatrix} a_{21} \\ a_{22} \\ a_{23} \end{bmatrix} = \begin{bmatrix} C_2 & C_1 & C_0 \\ C_3 & C_2 & C_1 \\ C_4 & C_3 & C_2 \end{bmatrix} \begin{bmatrix} -C_3 \\ -C_4 \\ -C_5 \end{bmatrix} \tag{3.21}$$

After that, the general expression for the reduced second-order transfer function is given as:

$$H_2(s)=\frac{a_{21}+a_{22}s}{1+a_{11}s+a_{12}s^2} \tag{3.22}$$

The values of a_{11}, a_{12}, a_{21}, a_{22} are found by using the coefficients C_0, C_1, C_2, C_3 as given below:

$$\begin{bmatrix} a_{11} \\ a_{12} \end{bmatrix} = \begin{bmatrix} C_1 & C_0 \\ C_2 & C_1 \end{bmatrix} \begin{bmatrix} -C_2 \\ -C_3 \end{bmatrix} \tag{3.23}$$

$$\begin{bmatrix} a_{21} \\ a_{22} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ C_0 & 0 \end{bmatrix} \begin{bmatrix} a_{11} \\ a_{12} \end{bmatrix} + \begin{bmatrix} C_0 \\ C_1 \end{bmatrix} \tag{3.24}$$

Thus, the reduced model is obtained so that this transfer function can be utilized to inspect the stability of the DC-DC converter.

3.3 Design of DC-DC SPEIC Converter

DC–DC SEPIC can perform in Buck mode for d<0.5 and in Boost mode for d>0.5. The assumption of a lossless circuit needs that the input power should be equal to output power.

So, $I_o=\frac{(1-D)I_{in}}{D}$. When the switch is OFF, L is discharging, $\Delta I_{L1}=\frac{V_o(1-D)}{L1f_s}$

Here, fs is the switching frequency.

The boundary of continuous condition for L1 is when $I_{L1\min}=0$.

At boundary condition, $2I_{in}=\frac{V_o(1-D)}{L1bf_s}$.

So that, $L1b=\frac{V_o(1-D)}{2I_{in}f_s}=\frac{V_sD}{2I_{in}f_s}$

where L1b is the inductance at the boundary condition.

As d approaches unity, the inductor L1 becomes, $L1>\frac{V_s}{2I_{in}f_s}$

This equation confirms that the continuous conduction can be achieved more easily, when Iin and fs are larger than than I_D.

When the switch S is OFF, L_2 is discharging

So, $\Delta I_{L2}=\frac{-V_o(1-D)}{L2f_s}$

The boundary of continuous conduction for L2 is when $I_{L2\min}=0$.

At this boundary, $2I_o=\frac{V_o(1-D)}{L2bf_s}$

Since the maximum value occurs at d=0, the derived inductor L2 becomes $L2>\frac{V_0}{2I_0f_s}$

The maximum peak to peak ripple voltage ΔV_m occurs as d=1, so $\Delta V_m=\frac{I_o}{C1f_s}$

And $C2=\frac{P_o}{4\pi f_sV_o\Delta V_0}$

Thus the circuit parameters are chosen for SEPIC converter and tabulated in Table 3.1

Table 3.1 Parameters used for SEPIC Converter [91]

Parameter	***Symbol***	***Values***
Input Voltage	V_{in}	10 V
Switching Frequency	f_s	100 KHz
Duty Cycle	d	0.5
Inductor	L_1, L_2	100 µH
Resistance	r_{L1}, r_{L2}	1 mΩ
	r_{C1}	3 mΩ
	r_{C2}	1 mΩ
Capacitor	C_1,C_2	800 µF, 3000 µF
Load Resistance	R_o	1 Ω
Output Voltage	Vo	10 V

3.4 Gain Equation of SEPIC Converter

For ideal converter, when no equivalent series is considered, the output voltage is related to the input voltage by duty cycle.

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{3.25}$$

By varying the duty cycle from 0 to 1, the output voltage can be varied. The equation 3.18 is rearranged to convert into voltage gain (V_o/V_{in}). The graph is taken between voltage gain and duty cycle which is shown in Fig. 3.5. When the duty cycle is 0, the voltage gain is 0. By increasing the duty cycle, the voltage gain increases, and at duty cycle of 0.5, the voltage gain is 1. That means the duty cycle below 0.5, the converter steps down the input voltage. At 0.5, the output voltage is equal to the input voltage. Duty cycle above 0.5, the voltage gain increases above 1 and since the derivation is for ideal converter, when duty cycle is 1, the voltage gain is infinity. The equation 3.18 is not valid for practical converter. That's why the equation is modified by including the internal resistances for inductor and capacitor. In ideal converter, the output voltage does not depend upon the load resistance whereas in practical converter, the output voltage depends on both load resistance and equivalent series resistance.

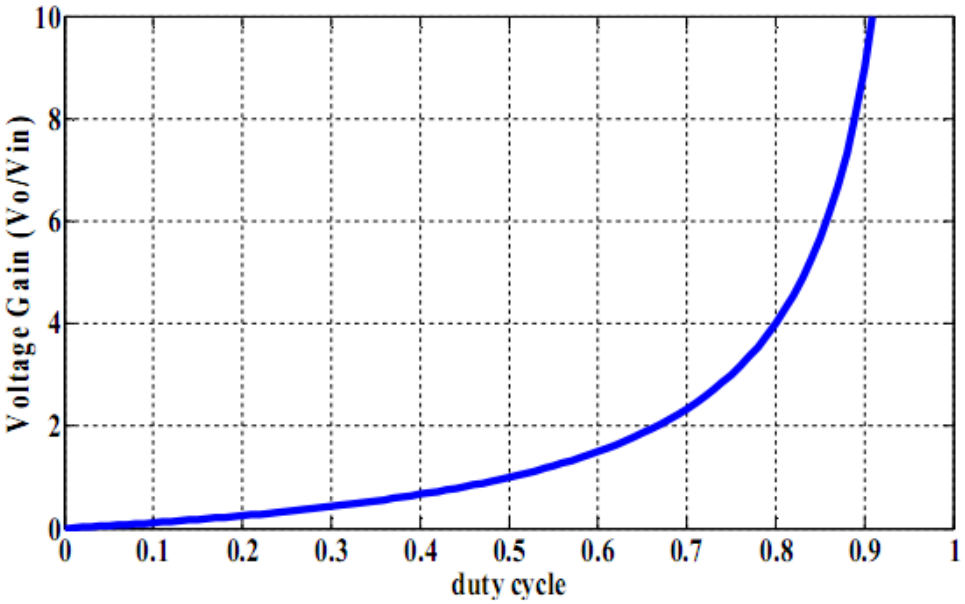


Fig. 3.5 Voltage Gain vs. duty cycle with variable load.

The output voltage for practical converter is

$$V_o = \frac{V_{in}}{\frac{1-D}{D} + \frac{Dr_{L1}}{(1-D)R} - \frac{(1-D)r_{L2}}{DR} + \frac{(2D-1)r_{C1}}{R}} \qquad (3.26)$$

By rearranging the equation, the voltage gain is calculated and it is drawn against the duty cycle. Fig. 3.6 shows the variation of voltage gain with respect to duty cycle for different load. It is shown that when the load resistance increases, the maximum voltage gain is also increases. In this figure, R is varied from 1 to 10 Ω and it is observed that upto duty cycle 0.8, there is no change of voltage gain, but when it is more than 0.8, the voltage gain is different for different value of R which is increasing for increasing of R.

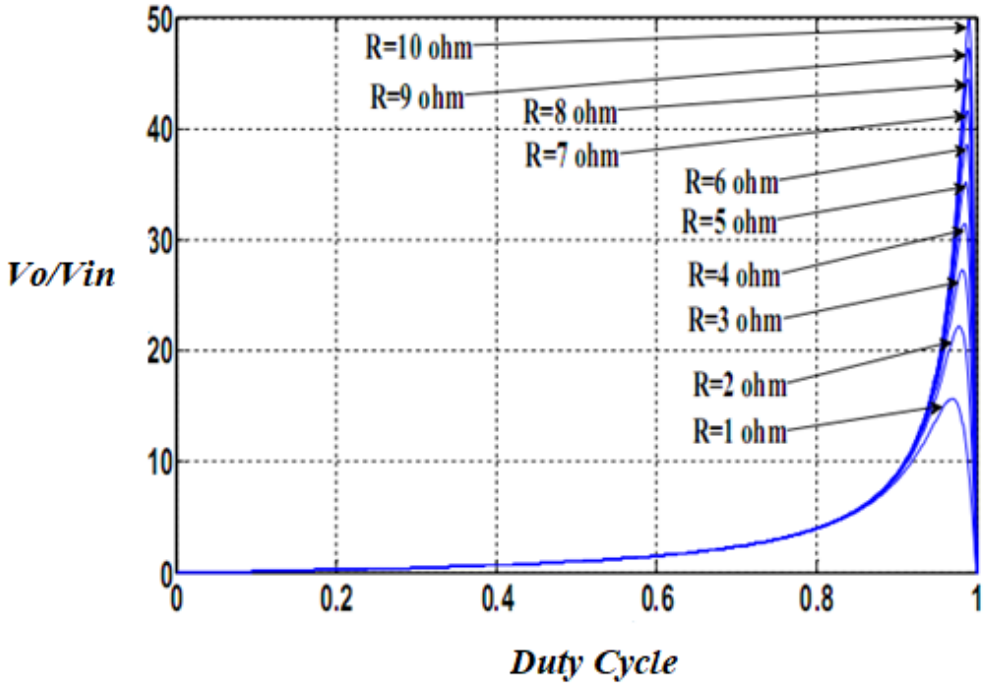


Fig. 3.6 Voltage Gain vs. duty cycle with variable load.

3.5 Response of Average Model

The converter is derived by converting into mathematical equation. The averaging state space model in matrix form is defined in the program and the values of parameters are utilized and with the help of programming language, the state space model is converted into transfer function which is a 4th order function.

$$H_4(s) = \frac{4.995s^3 + 1.655e^6 s^2 + 7.284e^7 s + 1.041e^{13}}{s^4 + 393s^3 + 7.933e^6 s^2 + 2.319e^9 s + 1.045e^{13}} \qquad (3.27)$$

Now the converter is reduced into 2nd order by using model order reduction technique. The 2nd order transfer function is

$$H_2(s) = \frac{3.515s + 1.664e^6}{s^2 + 362.8s + 1.671e^6} \qquad (3.28)$$

The average model is used for steady state analysis. The output voltage waveform is shown in Fig. 3.7 with duty cycle 0.5. It is shown that the steady state is achieved approximately at 0.03 sec.

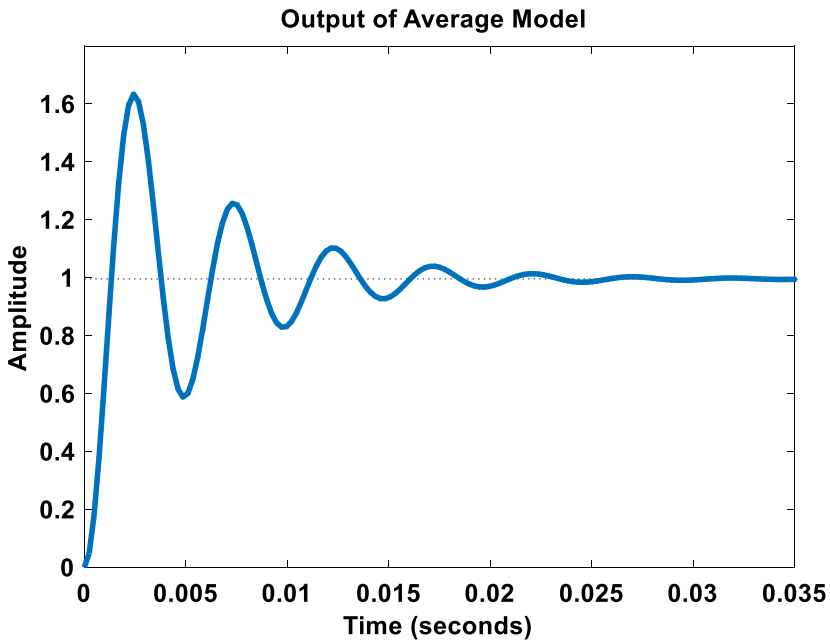


Fig. 3.7 Voltage amplitude Vs. Time for output of average model

The output of the average model is a reflection of the response of the converter in open loop. From the output, it is observed that percentage of overshoot is 64%, peak amplitude is 1.63, rise time is 0.000902s and settling time is 0.0203s. Hence, it is evident that overshoot is really high in terms of open loop response which needs to be reduced as it is a major concern for different application of SEPIC converter.

To enhance the performance of the converter, closed loop techniques are employed by many researchers in different time. Among various methods, PID controller is the most widely employed method and researchers implement this control technique to investigate and improve the performance of power converters.

3.6 Closed Loop Analysis with PID Controller

PID controller comprises of three terms named as Proportional, Integral and Derivative component which are tuned by empirical methods like Ziegler-Nicholas method [63], analytical methods and different optimization techniques. The proportional component utilizes proportion of the system error to control it, the integral component introduces lag in the system which implicates that it evaluates the total past history of error by continuously integrating the area under the error curve and the derivative component responds to the rate of change of error and which can pro-duce a correction before the error approaches to a larger value.

By taking into account different tuning methods, these parameters are tuned for different close loop systems to enhance the performance of the system. However, it is quite difficult to determine the exact values of these parameters as most of the classical methods demand explicit mathematical modeling of the processing plant and may not provide satisfactory results because of input-output disturbances or nonlinear behavior of the plant.

The mathematical representation of PID controller is as follows:

$$U(t) = k_i \int e(t)dt + k_p e(t) + k_d \frac{d}{dt} e(t) \tag{3.29}$$

So, the transfer function of the PID controller is given below:

$$\frac{U(s)}{E(s)} = k_p + \frac{k_i}{s} + sk_d = k_p(1 + \frac{1}{T_i s} + sT_d) \tag{3.30}$$

Typical PID controller structure is depicted in Fig 3.8.

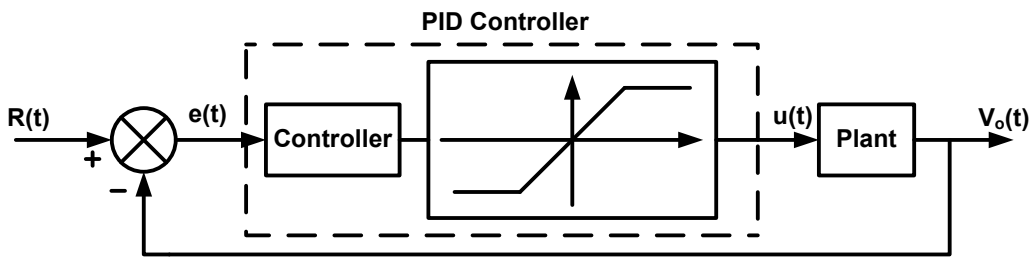


Fig. 3.8 Typical PID controller structure

Here, k_P, k_i and k_d are designated as the proportional, integral and derivative constants of the PID controller respectively. However, the values of the k_P, k_i and k_d need to be tuned to achieve better results. For this reason, the most popular method, Ziegler Nichols tuning is utilized. The parameters of the PID controller are obtained by Ziegler Nichols tuning method [64] in this work.

Rigorous trial and error process is carried out to obtain better values of k_P, k_i and k_d. The overall block diagram of the closed loop system is illustrated in Fig. 3.9.

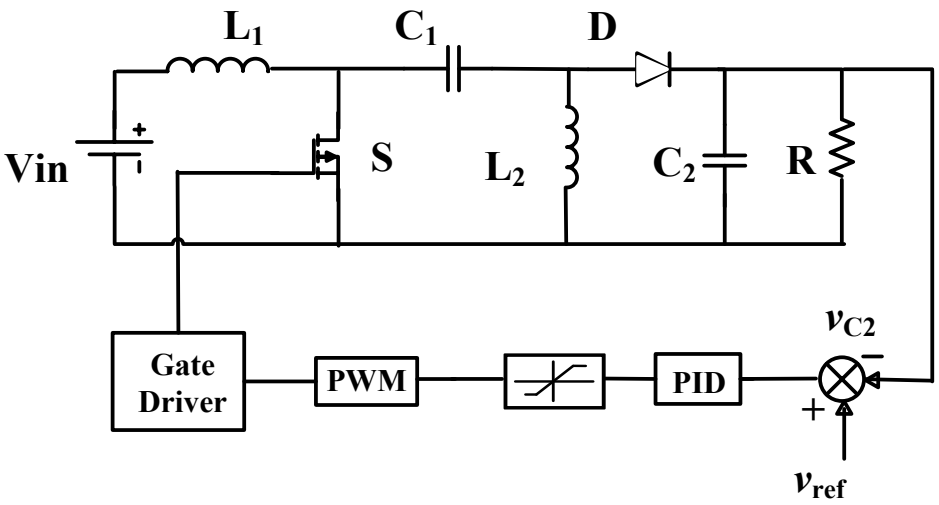


Fig. 3.9 Proposed SEPIC Converter with PID Controller

Typical PID controller with SEPIC converter [65] is implemented with the help of Table 3.2 [66]. The main objective of using PI controller is to eliminate the steady state error, reduce overshoot and obtain quick rise and settling time keeping in mind the following chart shown in Table 3.3 [66].

Table 3.2 Different Response for different controllers

Types of controller	K_p	T_i	T_d
P	$\frac{T}{L}$	∞	0
PI	$\frac{.9T}{L}$	$\frac{L}{0.3}$	0
PID	$\frac{1.2T}{L}$	$2L$	$0.5L$

Table 3.3 Effect of PID controller on SEPIC Converter

Type of controller	*Rise Time*	*Overshoot*	*Settling Time*	*Steady State Error*
Proportional	Decrease	Increase	Small Change	Decrease
Integral	Decrease	Increase	Increase	Eliminate
Derivative	Minor Change	Decrease	Decrease	No effect

At first, conventional PID controller is employed in SEPIC converter and the step response is taken to inspect the stability of the system which is shown in Fig. 3.10.

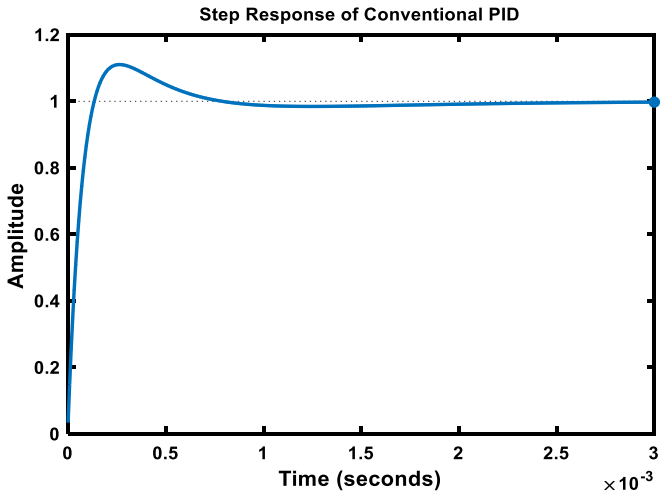


Fig. 3.10 Step Response of Conventional PID Controller for SEPIC converter

In closed loop analysis, it is observed that the overshoot it is 11% which is much less than open loop analysis. Moreover, rise time and settling time have also improved and they are 0.000954s and 0.000639s respectively. In addition, peak amplitude has also decreased and it is 1.11 which leads to leads steady state error. But this approach takes a lot of time as the parameters are obtained through manual tuning. A lot of time is needed to achieve satisfactory performance through trial and error process. Therefore, different nonlinear optimization techniques are implemented by many researchers in PID controller so that the optimized values of parameters can be attained with the help of algorithm development. Thus, better performance will be achieved without manual intervention.

CHAPTER 4

IMPLEMENTATION OF NONLINEAR OPTIMIZATION TECHNIQUE BASED PID CONTROLLER FOR SEPIC CONVERTER

Different nonlinear optimization techniques are implemented in designing optimized PID controller for power converters by many researchers. In this chapter, a brief review of various nonlinear optimization techniques is stated and two techniques, Genetic Algorithm and Simulated Annealing Algorithm are discussed elaborately for investigating the stability of SEPIC Converter.

4.1 Overview of Nonlinear optimization technique

Nonlinear optimization technique plays an important role in enhancing performance of complex nonlinear systems. The initial oscillatory behavior of system is not desirable in power converters. In order to obtain less overshoot, faster rise and settling time, the controller should be designed optimally. For this reason, a lot nonlinear techniques are studied and among them, Genetic Algorithm and Simulated Annealing Algorithm are chosen to investigate the performance of closed loop SEPIC converter and propose the most optimized model which will provide stable output. The reason behind choosing these algorithms, their methodology, different features, comparison with other techniques and design of the optimized PID controller are illustrated in further sections.

4.2 Introduction to Genetic Algorithm

Genetic Algorithms [67] provide an adaptive searching mechanism inspired on Darwin's principle of reproduction and survival of the fittest. The individuals (solutions) in a population are represented by chromosomes; each of them is associated to a fitness value (problem evaluation). The chromosomes are subjected to an evolutionary process which takes several cycles. Basic operations are selection, reproduction, crossover and mutation.

Parent selection gives more reproductive chances to the fittest individuals. During crossover some reproduced individuals cross and exchange their genetic characteristics. Mutations may occur in a small percentage and cause a random change in the genetic material, thus contributing to introduce variety in the population. The evolution process guides the genetic algorithm through more promising regions in the search space.

4.2.1 What is Genetic Algorithm?

Genetic Algorithm (GA) is a stochastic global search method that mimics the process of natural evolution. It is one of the methods used for optimization. John Holland formally introduced this method in the United States in the 1970 at the University of Michigan. The continuing performance improvement of computational systems has made them attractive for some types of optimization. The genetic algorithm starts with no knowledge of the correct solution and depends entirely on responses from its environment and evolution operators such as reproduction, crossover and mutation to arrive at the best solution. By starting at several independent points and searching in parallel, the algorithm avoids local minima and converging to sub optimal solutions [68-69].

In this way, GAs have been shown to be capable of locating high performance areas in complex domains without experiencing the difficulties associated with high dimensionality, as may occur with gradient decent techniques or methods that rely on derivative information [70].

4.2.2 Characteristics of Genetic Algorithm

Genetic Algorithms are search and optimization techniques inspired by two biological principles namely the process of natural selection and the mechanics of natural genetics [71-73]. GA manipulates not just one potential solution to a problem but a collection of potential solutions. This is known as population. The potential solution in the population is called chromosomes. These chromosomes are the encoded representations of all the parameters of the solution. Each chromosomes is compared to other chromosomes in the population and awarded fitness rating that indicates how successful this chromosomes to the latter.

To encode better solutions [74], the GA will use genetic operators or evolution operators such as crossover and mutation for the creation of new chromosomes from the existing ones in the population. This is achieved by either merging the existing ones in the population or by modifying existing chromosomes. The selection mechanism for parent chromosomes takes the fitness of the parent into account. This will ensure that the better

solution will have a higher chance to procreate and donate their beneficial characteristic to their off spring. A genetic algorithm is typically initialized with a random population consisting of between 20-100 individuals. This population or also known as mating pool is usually represented by a real-valued number or a binary string called a chromosome. Each chromosome is a binary string. On the other hand, how well an individual performs a task is measured and assessed by the objective function [73]. The objective function assigns each individual a corresponding number called its fitness. The fitness of each chromosome is assessed and a survival of the fittest strategy is applied. Hence, the magnitude of the error will be used to assess the fitness of each chromosome. There are three main stages of a genetic algorithm these are known as reproduction, crossover and mutation. These concepts have been explained in details in the following sections.

4.2.3 Population Size

Determining the number of population is the one of the important steps in GA. There are many research papers that dwell in the subject. Many theories have been documented and experiments recorded [75]. However the matter of the fact is that more and more theories and experiments are conducted and tested and there is no fast and thumb rule with regards to which is the best method to adopt. For a long time the decision on the population size is based on trial and error [76]. So, it is suggested by researchers that the safe population size is from 20 to 100. In this paper, an initial population of 25, 50 and 75 are taken and simulations are carried out investigate the response of the system.

4.2.4 Reproduction

During the reproduction phase the fitness value of each chromosome is assessed. This value is used in the selection process to provide bias towards fitter individuals. Just like in natural evolution, a fit chromosome has a higher probability of being selected for reproduction. An example of a common selection technique is the Roulette Wheel selection method as shown in Fig. 4.1. Each individual in the population is allocated a section of a roulette wheel. The size of the section is proportional to the fitness of the individual. A pointer is spun and the individual to whom it points is selected. This continues until the selection criterion has been met. The probability of an individual being selected is thus related to its fitness, ensuring that fitter individuals are more likely to leave offspring. Multiple copies of the same string may be selected for reproduction and the fitter strings should begin to dominate. However, for the situation illustrated in Figure 8, it is not implausible for the weakest string (01001) to dominate the selection process.

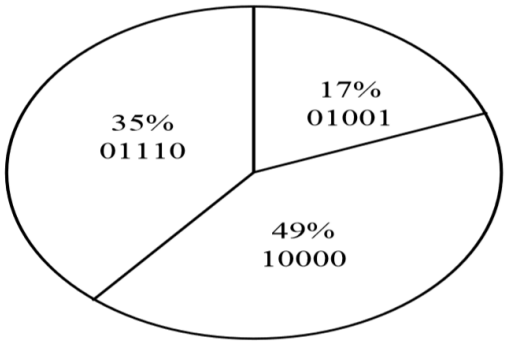


Fig. 4.1 Depiction of roulette wheel selection

There are a number of other selection methods available and it is up to the user to select the appropriate one for each process over conventional PID controller [77]. All selection methods are based on the same principal that is giving fitter chromosomes a larger probability of selection.

Four common methods for selection are:

1. Roulette Wheel selection
2. Stochastic Universal sampling
3. Normalized geometric selection
4. Tournament selection

4.2.5 Crossover

Once the selection process is completed, the crossover algorithm is initiated. The crossover operations swap certain parts of the two selected strings in a bid to capture the good parts of old chromosomes and create better new ones. Genetic operators manipulate the characters of a chromosome directly, using the assumption that certain individuals' gene codes, on average, produce fitter individuals. The crossover probability indicates how often crossover is performed. A probability of 0% means that the offspring will be exact replicas of their parents and a probability of 100% means that each generation will be composed of entirely new offspring.

i. ***Single Point Crossover***:

The simplest crossover technique is the Single Point Crossover. There are two stages involved in single point crossover:

a) Members of the newly reproduced strings in the mating pool are mated (paired) at random.
b) Each pair of strings undergoes a crossover as follows: An integer k is randomly selected between one and the length of the string less one, [1, L-1]. Swapping all the characters between positions k+1 and L inclusively creates two new strings.

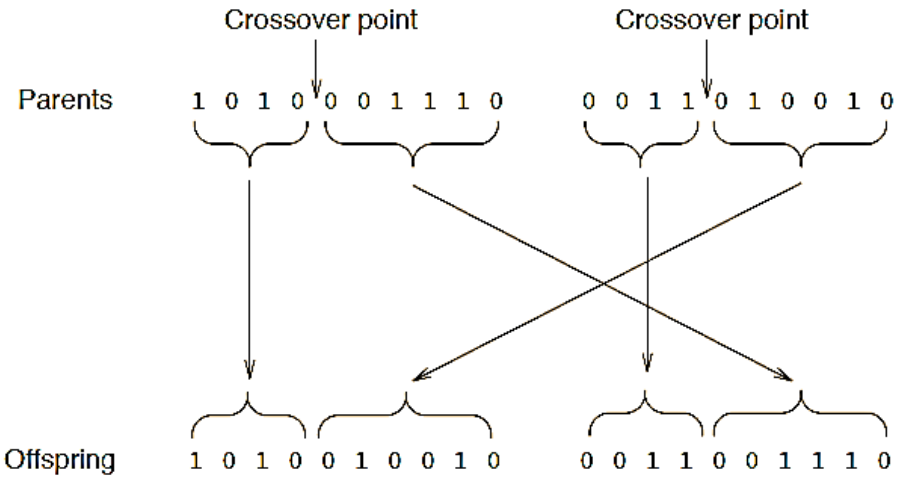


Fig. 4.2 Single Point Crossover

ii. ***Multi Point Crossover:***

More complex crossover techniques exist in the form of Multi-point and Uniform Crossover Algorithms. In Multipoint crossover, it is an extension of the single point crossover algorithm and operates on the principle that the parts of a chromosome that contribute most to its fitness might not be adjacent. There are three main stages involved in a Multi-point crossover.

a) Members of the newly reproduced strings in the mating pool are mated (paired) at random.

b) Multiple positions are selected randomly with no duplicates and sorted into ascending order.
c) The bits between successive crossover points are exchanged to produce new offspring.

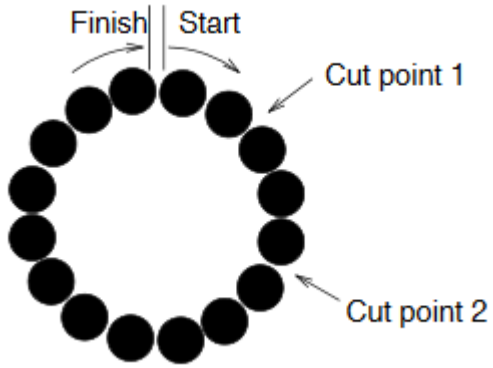


Fig. 4.3 Multi Point Crossover

iii. ***Uniform crossover***:

Uniform crossover is the most disruptive of the crossover algorithms and has the capability to completely dismantle a fit string, rendering it useless in the next generation.

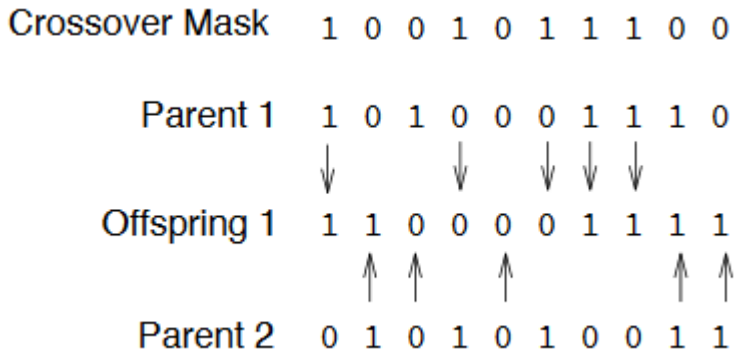


Fig. 4.4 Uniform Crossover

4.2.6 Mutation

Using ‘selection’ and ‘crossover’ on their own will generate a large amount of different strings. However there are two main problems with this:

1. Depending on the initial population chosen, there may not be enough diversity in the initial strings to ensure the Genetic Algorithm searches the entire problem space.
2. The Genetic Algorithm may converge on sub-optimum strings due to a bad choice of initial population

These problems may be overcome by the introduction of a mutation operator into the Genetic Algorithm. Mutation is the occasional random alteration of a value of a string position. It is considered a background operator in the genetic algorithm. The probability of mutation is normally low because a high mutation rate would destroy fit strings and degenerate the genetic algorithm into a random search. Mutation probability values of around 0.1% or 0.01% are common, these values 55 represent the probability that a certain string will be selected for mutation i.e. for a probability of 0.1%; one string in one thousand will be selected for mutation. Once a string is selected for mutation, a randomly chosen element of the string is changed or mutated.

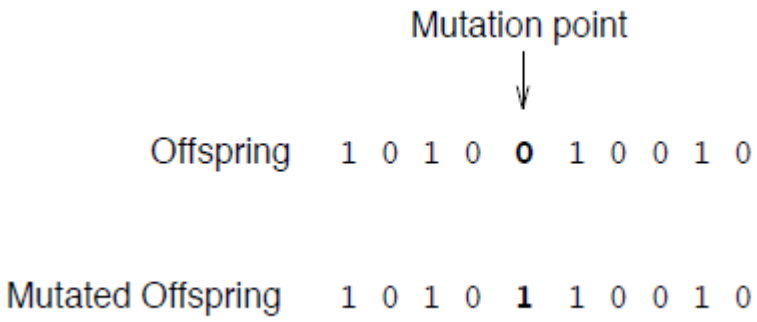


Fig. 4.5 One Single Mutation

4.2.7 Elitism

In the process of the crossover and mutation, there is high chance that the optimum solution could be lost. There is no guarantee that these operators will preserve the fittest string. To avoid this, the elitist models are often used. In this model, the best individual from a population is saved before any of these operations take place. When a new population is formed and evaluated, this model will examine to see if this best structure has been preserved. If not the saved copy is reinserted into the population The GA will then continue on as normal [78].

4.2.8 Convergence

If the GA has been correctly implemented, the population will evolve over successive generations so that the fitness of the best and the average individual in each generation increases towards the global optimum. Convergence is the progression towards increasing uniformity. A gene is said to have converged when 95% of the population share the same value. The population is said to have converged when all of the genes have converged. Fig. 4.6 shows how fitness varies in a typical GA. As the population converges, the average fitness will approach that of the best individual.

4.2.9 Flowchart of Genetic Algorithm

In this section the process of Genetic Algorithm will be summarized in a flowchart. The summary of the process will be described below:

The steps involved in creating and implementing a genetic algorithm:

1. Generate an initial, random population of individuals for a fixed size.
2. Evaluate their fitness.
3. Select the fittest members of the population.
4. Reproduce using a probabilistic method (e.g. roulette wheel).
5. Implement crossover operation on the reproduced chromosomes (choosing probabilistically both the crossover site and the mates).
6. Execute mutation operation with low probability
7. Repeat step 2 until a predefined convergence criterion is met.

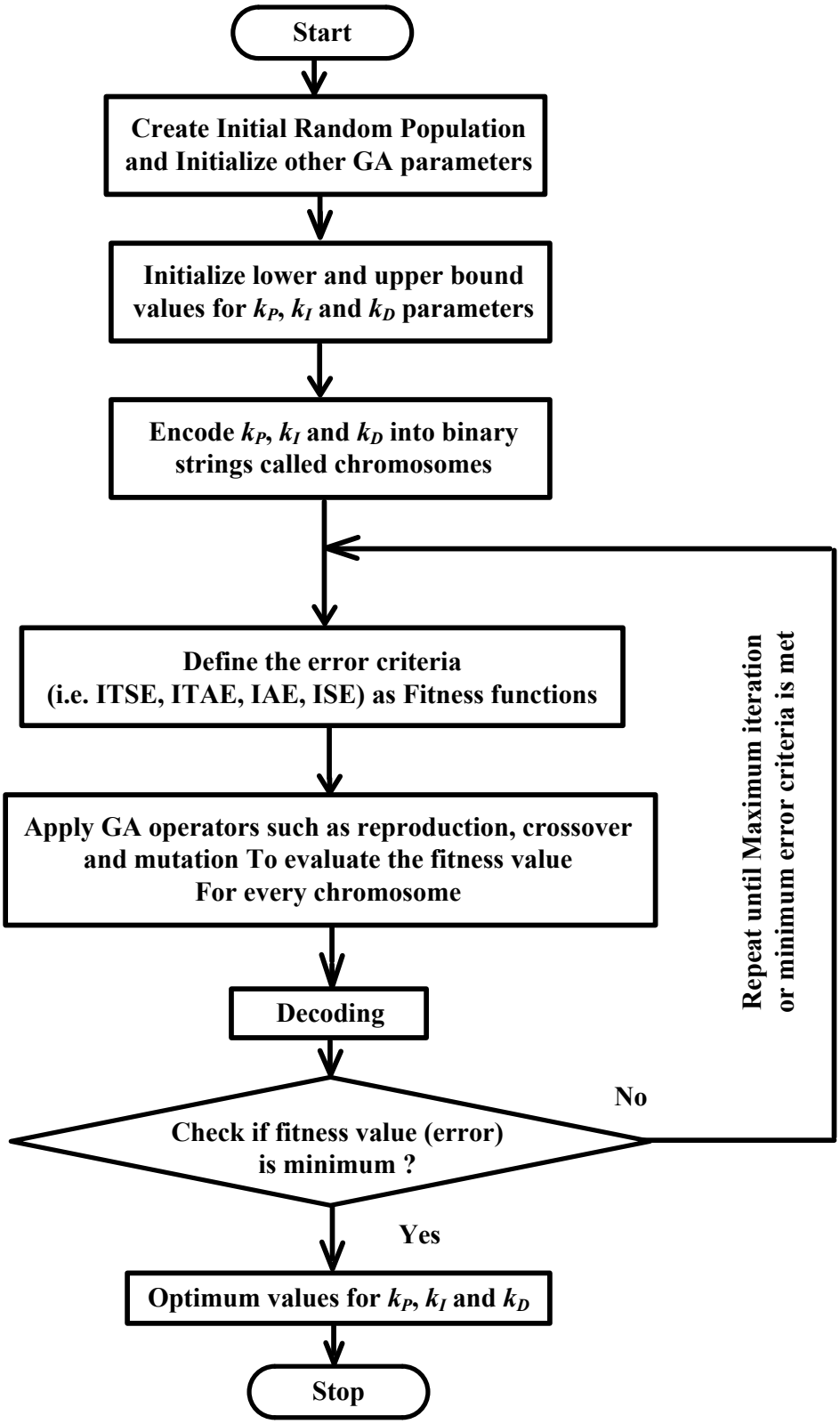


Fig. 4.6 Flow Chart of Genetic Algorithm [78]

The convergence criterion of a genetic algorithm is a user specified conditions for example the maximum number of generation or when the string fitness value exceeds a certain threshold. In this thesis, search space which means the initial population is selected by trial and error process. Different search spaces are considered (small, medium and large) and corresponding responses are observed and among them, the best suited three search spaces are taken into account. However, the upper and lower bound of the k_P, k_I and k_D are selected by observing the values of conventional PID controller's parameters value. As the conventional PID controller is able to present a stable output, the upper and lower bounds are selected accordingly so that nonlinear optimization algorithm can perform the search within that solution space and come up with the most optimized values of PID controller.

4.2.10 Objective Function or Fitness Function

The objective function is used to provide a measure of how individuals have performed in the problem domain. In the case of a minimization problem, the fit individuals will have the lowest numerical value of the associated objective function. This raw measure of fitness is usually only used as an intermediate stage in determining the relative performance of individuals in a GA. Another function that is the fitness function is normally used to transform the objective function value into a measure of relative fitness, thus where f is the objective function, g transforms the value of the objective function to a nonnegative number and F is the resulting relative fitness.

This mapping is always necessary when the objective function is to be minimized as the lower objective function values correspond to fitter individuals. In many cases, the fitness function value corresponds to the number of offspring that an individual can expect to produce in the next generation. A commonly used transformation is that of proportional fitness assignment [79].

$$IAE = \int_0^{\tau} |e(t)| dt \tag{4.1}$$

$$ITAE = \int_0^{\tau} t|e(t)| dt \tag{4.2}$$

$$ISE = \int_0^{\tau} e(t)^2 dt \tag{4.3}$$

$$ITSE = \int_0^{\tau} te(t)^2 dt \tag{4.4}$$

4.2.11 Design of GA based PID Controller

Proportional-Integral-Derivative (PID) control is one of the most widely employed methods in closed loop analysis of power converters. Hence, the technique has been employed here for observing closed loop optimized performance of SEPIC converter by utilizing Genetic Algorithm. The basic block diagram of the system is shown in Fig. 4.7.

In order to tune the parameters of PID controller through genetic algorithm, the k_P, k_I and k_D are taken and the chromosome is formed. The main objective of the study is to minimize the error between the input and the plant's output.

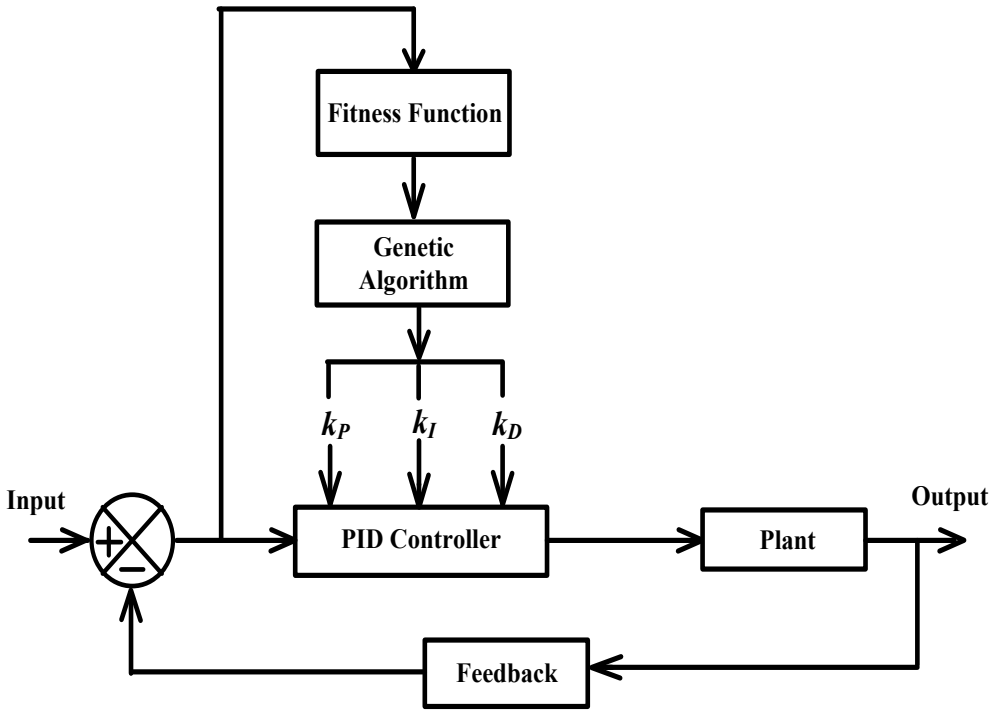


Fig. 4.7 Basic Block Diagram of Genetic Algorithm (GA) based PID Controller

4.2.12 Comparison with other techniques:

A number of other techniques have been discussed and analyzed in connection with search and optimization problems. There are a lot of optimization techniques, some of which are only applicable to limited domains, for example, dynamic programming [80].

This is a method for solving multi-step control problems which is only applicable where the overall fitness function is the sum of the fitness functions for each stage of the problem and there is no interaction between stages. Some of the more general techniques are described as follows:

i. ***Random Search****:*

The brute force approach for difficult functions is a random or an enumerated search. Points in the search space are selected randomly, or in some systematic way, and their fitness evaluated. This is a very unintelligent strategy and is rarely used.

ii. ***Gradient Methods****:*

A number of different methods for optimizing well-behaved continuous functions have been developed [75] which rely on using information about the gradient of the function to guide the direction of search. If the derivative of the function cannot be computed because it is discontinuous, these methods often fail.

Such methods are generally referred to as *Hill climbing*. They can perform well on functions with only one peak (unimodal functions). But on functions with many peaks (multimodal functions), they suffer from the problem that the first peak found will be climbed and this may not be the highest peak. Having reached the top of a local maximum, no further progress can be made. A 1-dimensional example is shown in Fig. 4.8. The *hill climb* starts from a randomly chosen starting point, X. "Uphill" moves are made and the peak at B is located. Higher peaks at A and C are not found.

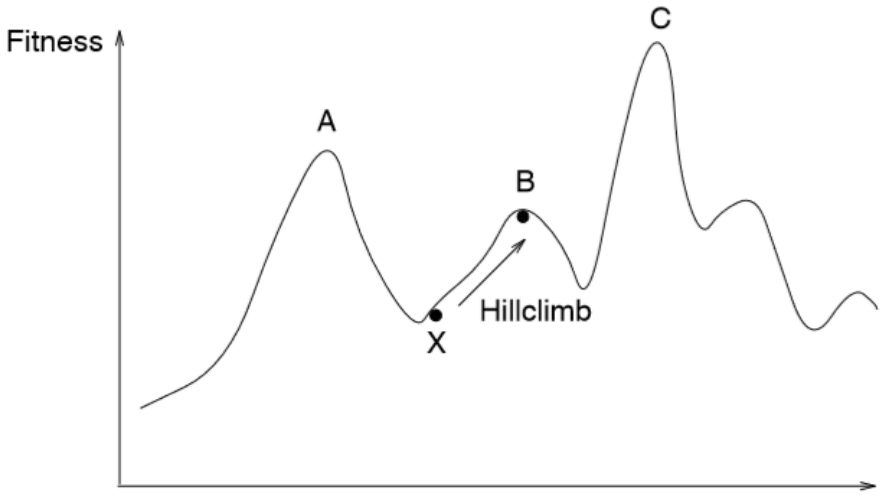


Fig. 4.8 The Hill climbing Problem

iii. ***Iterated Search****:*

Random search and gradient search may be combined to give an iterated hill-climbing search. Once one peak has been located, the hill climb is started again but with another randomly chosen starting point. This technique has the advantage of simplicity and can perform well if the function does not have too many local maxima.

However, since each random trial is carried out in isolation, no overall picture of the "shape" of the domain is obtained. As the random search progresses, it continues to allocate its trials evenly over the search space. This means that it will still evaluate just as many points in regions found to be of low fitness as in regions found to be of high fitness.

Genetic Algorithm, by comparison, starts with an initial random population and allocates increasing trials to regions of the search space found to have high fitness. This is a disadvantage if the maximum or minimum is in a small region surrounded on all sides by regions of low fitness. This kind of function is difficult to optimize by any method and here the simplicity of the iterated search usually wins the day [82].

4.2.13 Summary:

GA's is a very broad and deep subject area and most of our knowledge about them is empirical. Genetic Algorithms are adaptive methods which may be used to solve search and optimization problems. They are based on the genetic processes of biological organisms. Over many generations, natural populations evolve according to the principles of natural selection and survival of the fittest first clearly stated by Charles Darwin in The Origin of Species. By mimicking this process, genetic algorithms are able to evolve solutions to real world problems, if they have been suitably encoded. For example, GA can be used to design bridge structures for maximum strength, weight ratio or to determine the least wasteful layout for cutting shapes from cloth. It can also be used for online process control such as in a chemical plant, load balancing on multiprocessor computer system and power electronics. In this research, GA is utilized to develop optimized PID controller for SEPIC converter in order to obtain stable and fast response.

4.3 Simulated Annealing Algorithm

4.3.1 Overview of SA:

SA refers to an optimization technique, based on the principles of thermodynamics where the analogy of cooling of metal and freezing into a minimum energy level is utilized [83-84]. The objective of this algorithm is to find the global optimum value of the system. Moreover, the simulated annealing algorithm is capable of dealing complex nonlinear systems and appears to be more versatile, robust and handy than other search algorithms. However, the algorithm is metaheuristic and computing time is high.

The algorithm starts by initializing a very high temperature and perturbing the placement through a defined move. After that the score is calculated and depending on the change in score the decision is taken whether it is to be accepted or rejected. Hence the value is updated and process is repeated until freezing point is reached. The flowchart of the algorithm is illustrated in Fig. 4.9.

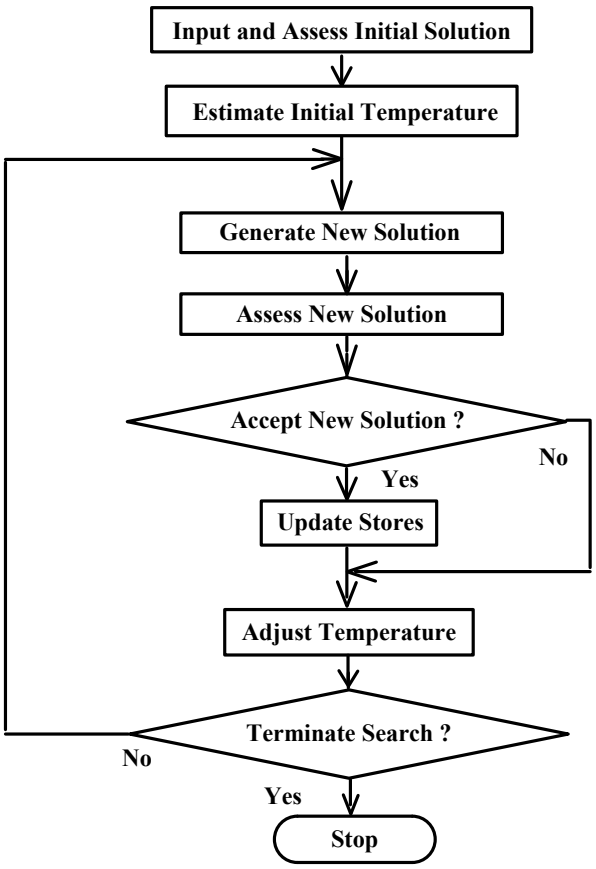


Fig. 4.9 Flow Chart of Simulated Annealing (SA) algorithm [85]

4.3.2 Methodology:

SA's major advantage over other methods is an ability to avoid becoming trapped in local minima. The algorithm employs a random search which not only accepts changes that decrease the objective function f (assuming a minimization problem), but also some changes that increase it. The latter are accepted with a probability

$$p = e^{(-\delta f/T)} \tag{4.5}$$

where δf is the increase in f and T is a control parameter, which by analogy with the original application is known as the system "temperature" irrespective of the objective function involved.

The following elements must be provided:

- a representation of possible solutions
- a generator of random changes in solutions
- a means of evaluating the problem functions and
- an annealing schedule - an initial temperature and rules for lowering it as the search progresses.

Fig. 4.10 shows the progress of a SA search on the two-dimensional Rosenbrock function,

$$f = [(1-x_1)^2 + 100(x_2 - x_1^2)]^2 \tag{4.6}$$

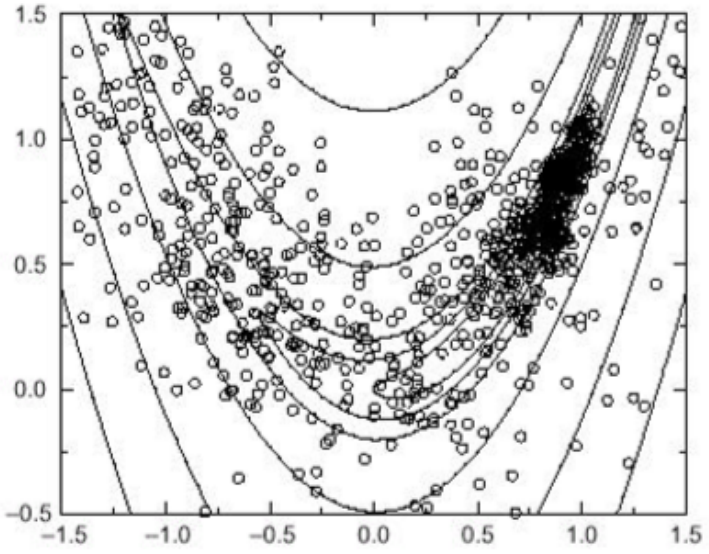


Fig. 4.10 Progress of search pattern for Rosenbrock function

Although this function is amenable to solution by more efficient methods, it is useful for purposes of comparison. Each of the solutions accepted in a 1000-trial search is shown

(marked by symbols). It is clear that the search is wide-ranging but ultimately concentrates in the neighborhood of the optimum.

The following figure Fig. 4.11 shows the progress in reducing the objective function for the same search:

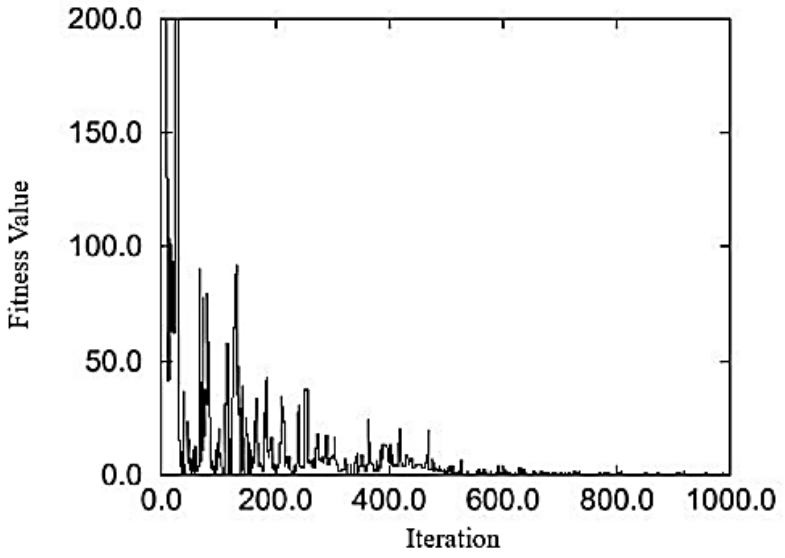


Fig. 4.11 Objective function reduction

Initially, when the annealing temperature is high, some large increases in f are accepted and some areas far from the optimum are explored. As execution continues and T falls, fewer uphill excursions are tolerated (and those that are tolerated are of smaller magnitude). The last 40% of the run is spent searching around the optimum. This performance is typical of the SA algorithm.

4.3.3 Strengths and Weaknesses:

Simulated annealing can deal with highly nonlinear models, chaotic and noisy data and many constraints. However, more particularly, major strengths can be concluded as followed.

i. It is a robust and general technique. Its main advantages over other local search methods are its flexibility and its ability to approach global optimality.
ii. The algorithm is quite versatile since it does not rely on any restrictive properties of the model.

iii. SA methods are easily "tuned". For any reasonably difficult nonlinear or stochastic system, a given optimization algorithm can be tuned to enhance its performance and since it takes time and effort to become familiar with a given code, the ability to tune a given algorithm for use in more than one problem should be considered an important feature of an algorithm.

Just like any methods, pros come with some cons as well. Since, it is also one algorithm; there are some minor weaknesses as well. Those can be pointed put as followed.

i. Since SA is a metaheuristic, a lot of choices are required to turn it into an actual algorithm.
ii. There is a clear tradeoff between the quality of the solutions and the time required to compute them.
iii. The tailoring work required to account for different classes of constraints and to fine-tune the parameters of the algorithm can be rather delicate.
iv. The precision of the numbers used in implementation is of SA can have a significant effect upon the quality of the outcome.

4.3.4 Comparison with other methods:

Any efficient optimization algorithm must use two techniques to find a global maximum or minimum: exploration to investigate new and unknown areas in the search space, and exploitation to make use of knowledge found at points previously visited to help find better points. These two requirements are contradictory, and a good search algorithm must find a tradeoff between the two.

i. Neural Nets:

The main difference compared with neural nets is that neural nets learn (how to approximate a function) while simulated annealing searches for a global optimum. Neural nets are flexible function approximators while SA is an intelligent random search method. The adaptive characteristics of neural nets are a huge advantage in modeling changing environments. However, the power-hungriness of SA limits its use as a real-time application.

ii. Genetic Algorithms:

Direct comparisons have been made between ASA/VFSR and publicly-available genetic algorithm (GA) codes, using a test suite already adapted and adopted for GA. In each case, ASA outperformed the GA problem. GA is a class of algorithms that are interesting in their own right; GA was not originally developed as an optimization

algorithm, and basic GA does not offer any statistical guarantee of global convergence to an optimal point. Nevertheless, it should be expected that GA may be better suited for some problems than SA.

iii. Random Search:

The brute force approach for difficult functions is a random, or an enumerated search. Points in the search space are selected randomly, or in some systematic way, and their fitness evaluated. This is an unintelligent strategy, and is rarely used.

iv. Gradient Method:

A number of different methods for optimizing well-behaved continuous functions have been developed which rely on using information about the gradient of the function to guide the direction of search. If the derivative of the function cannot be computed, because it is discontinuous, for example, these methods often fail. Such methods are generally referred to as hill climbing. They can perform well on functions with only one peak (unimodal functions). But on functions with many peaks, (multimodal functions), they suffer from the problem that the first peak found will be climbed, and this may not be the highest peak. Having reached the top of a local maximum or bottom of a local minimum, no further progress can be made.

v. Iterated Search:

Random search and gradient search may be combined to give an iterated hill-climbing search. Once one peak has been located, the hill-climb is started again, but with another, randomly chosen, starting point. This technique has the advantage of simplicity, and can perform well if the function does not have too many local maxima. However, since each random trial is carried out in isolation, no overall picture of the "shape" of the domain is obtained. As the random search progresses, it continues to allocate its trials evenly over the search space. This means that it will still evaluate just as many points in regions found to be of low fitness as in regions found to be of high fitness.

Both SA and GAs, by comparison, start with an initial random population, and allocate increasing trials to regions of the search space found to have high fitness. This is a disadvantage if the maximum or minimum is in a small region, surrounded on all sides by regions of low fitness. This kind of function is difficult to optimize by any method, and here the simplicity of the iterated search usually wins.

4.3.5 Suitability:

SA appears rapidly to be becoming an algorithm of choice when dealing with financial instruments [86]. Standard nested regression and local-search methods usually are applied to develop hybrid securities, e.g. combining markets in interest rates, foreign exchange, equities and commodities by linking them via options, futures, forwards, and swaps, to increase profits and reduce risks in investments as well as in trading [87].

However, the complexity and nonlinearity of these multivariate systems, and the increasing interest of including information from more sophisticated modeling into trading rules, have called for more sophisticated numerical algorithms. As such, the parameters are a mix of continuous and discrete sets, but these seem to be able to be processed quite smoothly by adaptive simulated annealing (ASA). One of the several strong features of these algorithms is their flexibility in accommodating many ad hoc constraints, rules, etc., as well as algebraic models.

The potential uses for SA in stock price modeling may be limited. However, simulated annealing has been reasonably successfully used in the solution of a complex portfolio selection model [88]. The algorithm was able to handle more classes of constraints than most other techniques. Trading constraints were, however, difficult to handle because of the discontinuities they introduced in the space of feasible portfolios.

An example of the power of SA (ASA), coupled with new statistical mechanical modeling techniques, is that interest rates can be fitted to the data much better than in previously published studies [89]. One study has used SA on a set of several econometric problems [90], including cost functions arising in the monetary theory of exchange rate determination, a study of firm production efficiency, and a neural net model which generates chaos reputed to mirror some economic and financial series. Researchers demonstrated that their SA algorithm performed better, e.g. at least more reliably finding more optima, than other numerical techniques such as a genetic algorithms and a quasi-Newton algorithm.

4.3.6 Practical Implementation:

4.3.6.1 Solution Representation and Generation:

When attempting to solve an optimization problem using the SA algorithm, the most obvious representation of the control variables is usually appropriate. However, the way in which new solutions are generated may need some thought. The solution generator should

- Introduce small random changes and
- Allow all possible solutions to be reached

For problems with continuous control values new trial solutions can be generated according to the formula:

$$x_{i+1} = x_i + Qu \tag{4.7}$$

Where, u is a vector of random numbers in the range (-√3, +√3) so that each has zero mean and unit variance, and Q is a matrix that controls the step size distribution. In order to generate random steps with a covariance matrix S, Q is found by solving

$$S = QQ^T \tag{4.8}$$

by *Cholesky* decomposition, for example. S should be updated as the search progresses to include information about the local topography:

$$S_{i+1} = (1-\alpha)S_i + \alpha\omega X \tag{4.9}$$

where matrix X measures the covariance of the path actually followed and the damping constant α controls the rate at which information from X is folded into S with weighting ω. One drawback of this scheme is that the solution of equation (4.8), which must be done every time S is updated, can represent a substantial computational overhead for problems with high dimensionality. In addition, because the probability of an increase in the objective function being accepted, given by equation (4.5), does not reflect the size of the step taken, S must be estimated afresh every time the system temperature is changed.

An alternative strategy is to generate solutions according to the formula:

$$x_{i+1} = x_i + Du \tag{4.10}$$

where u is now a vector of random numbers in the range (-1, 1) and D is a diagonal matrix which defines the maximum change allowed in each variable. After a successful trial, i.e. after an accepted change in the solution, D is updated:

$$D_{i+1} = (1-\alpha)D_i + \alpha\omega R \tag{4.11}$$

where, α and ω perform similar roles and R is a diagonal matrix the elements of which consist of the magnitudes of the successful changes made to each control variable. This tunes the maximum step size associated with each control variable towards a value giving acceptable changes.

When using this strategy it is recommended that the probability of accepting an increase in f be changed from that given by equation (4.5) to:

$$p = e^{(-\delta f / Td)} \qquad (4.12)$$

where d is the average step size, so that δf / d is a measure of the effectiveness of the change made. As the size of the step taken is considered in calculating p, D does not need to be adjusted when T is changed.

For problems with integer control variables, the simple strategy whereby new trial solutions are generated according to the formula:

$$x_{i+1} = x_i + u \qquad (4.13)$$

where u is a vector of random integers in the range (-1, 1) often suffices.

4.3.6.2 Solution Evaluation:

The SA algorithm needs to be supplied with an objective function for each trial solution it generates. Obviously, in the interests of overall computational efficiency, it is important that the problem function evaluations should be performed efficiently; especially as in many applications these function evaluations are by far the most computationally intensive activity. Some thought needs to be given to the handling of constraints when using the SA algorithm. In many cases the routine can simply be programmed to reject any proposed changes which result in constraint violation, so that a search of feasible space only is executed.

However, there are two important circumstances in which this approach cannot be followed:

- if there are any equality constraints defined on the system, or

- if the feasible space defined by the constraints is (suspected to be) disjoint, so that it is not possible to move between all feasible solutions without passing through infeasible space.

In either case the problem should be transformed into an unconstrained one by constructing an augmented objective function incorporating any violated constraints as *penalty functions*:

$$f_A(x) = f(x) + (1/T)\omega^T c_V(x) \qquad (4.14)$$

where w is a vector of nonnegative weighting coefficients and the vector c_V quantifies the magnitudes of any constraint violations. The inverse dependence of the penalty on temperature biases the search increasingly heavily towards feasible space as it progresses.

4.3.6.3 Annealing Schedule:

Through equation (4.5) or (4.12), the annealing schedule determines the degree of uphill movement permitted during the search and is thus critical to the algorithm's performance. The principle underlying the choice of a suitable annealing schedule is easily stated: the initial temperature should be high enough to "melt" the system completely and should be reduced towards its "freezing point" as the search progresses. Choosing an annealing schedule for practical purposes is something of an art.

The standard implementation of the SA algorithm is one in which homogeneous Markov chains of finite length are generated at decreasing temperatures. The following parameters should therefore be specified:

- an initial temperature T_0
- a final temperature T_f or a *stopping criterion*
- a length for the Markov chains and
- a rule for decrementing the temperature.

- **Initial Temperature**

A suitable initial temperature T_0 is one that results in an average increase of acceptance probability p_0 of about 0.8. In other words, there is an 80% chance that a change which increases the objective function will be accepted. The value of T_0 will clearly depend on the scaling of f and, hence, be problem-specific.

It can be estimated by conducting an initial search in which all increases are accepted and calculating the average objective increase observed δf+. T_0 is then given by:

$$T_0 = \frac{-\partial f^+}{\ln(p_0)} \qquad (4.15)$$

- **Final Temperature**

In some simple implementations of the SA algorithm the final temperature is determined by fixing

- the number of temperature values to be used, or
- the total number of solutions to be generated.

Alternatively, the search can be halted when it ceases to make progress. Lack of progress can be defined in a number of ways, but a useful basic definition is

- no improvement (i.e. no new best solution) being found in an entire Markov chain at one temperature, combined with
- the acceptance ratio falling below a given (small) value pf .

- **Length of Markov Chains**

An obvious choice for L_k, the length of the k-th Markov chain, is a value that depends on the size of the problem, so L_k is independent of k.

Alternatively, it can be argued that a minimum number of transitions N_{min} should be accepted at each temperature. However, as T_k approaches 0, transitions are accepted with decreasing probability so the number of trials required achieving N_{min} acceptances approaches 1. Thus, in practice, an algorithm in which each Markov chain is terminated after

- L_k transitions or
- N_{min} acceptances,

whichever comes first, is a suitable compromise.

- **Decrementing the Temperature**

The simplest and most common temperature decrement rule is:

$$T_{k+1} = \alpha T_k \tag{4.16}$$

where α is a constant close to, but smaller than, 1. This exponential cooling scheme (ECS) was first proposed with α= 0.95. In a linear cooling scheme (LCS) in which T is reduced every L trials:

$$T_{k+1} = T_k - T \tag{4.17}$$

The reductions achieved using the two schemes have been found to be comparable, and the final value of f is, in general, improved with slower cooling rates, at the expense of greater computational effort. The algorithm performance depends more on the *cooling rate* ΔT/L than on the individual values of ΔT and L. Obviously, care must be taken to avoid negative temperatures when using the LCS.

- **Random number generation**

A significant component of an SA code is the random number generator, which is used both for generating random changes in the control variables and for the (temperature dependent) increase acceptance test. It is important, particularly when tackling large scale problems requiring thousands of iterations that the random number generator used have good *spectral properties*.

4.3.7 Design of SA based PID Controller:

Proportional-Integral-Derivative (PID) controller is extensively used in improving the closed loop performance of different power converters. Here, PID controller parameters are attained with the help of Simulated Annealing (SA) algorithm. The fitness function will be evaluated and thus the optimized values of the controller will be obtained to inspect the stability of the system. The basic block diagram of SA-PID controller is displayed in Fig. 4.12.

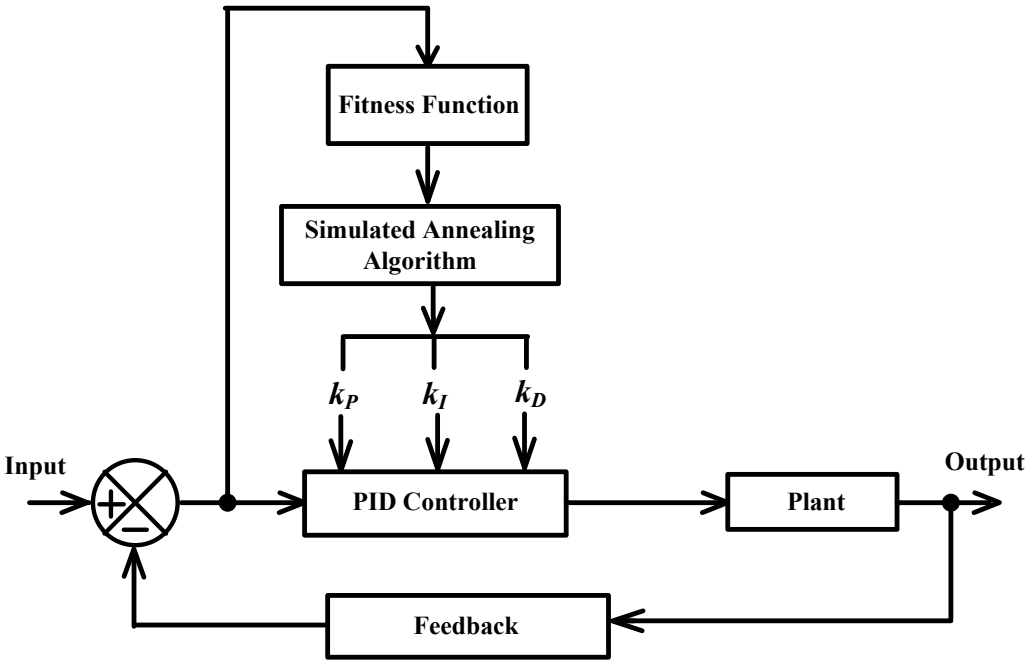


Fig. 4.12 Basic Block Diagram of SA based PID Controller.

4.3.8 Summary:

As with genetic algorithms a major advantage of SA is its flexibility and robustness as a global search method. It does not use gradient information and makes relatively few assumptions about the problem being solved. It can deal with highly nonlinear problems and non-differentiable functions as well as functions with multiple local optima. It is also amenable to parallel implementation. Simulated annealing is a very powerful and important tool in a variety of disciplines.

A disadvantage is that the SA methods are computation-intensive. There exist faster variants of basic simulated annealing, but these apparently are not as quite easily coded and so they are not widely used.

As with neural nets and GAs, SA looks highly promising for portfolio optimization and asset allocation problems, because the driving variables are highly nonlinear, noisy and often chaotic; it appears less appropriate for modeling financial time series.

CHAPTER 5

SIMULATION RESULTS AND PERFORMANCE ANALYSIS

In this thesis work, after mathematical modeling and developing the design for optimized PID controller, simulation is carried out in MATLAB environment in order to investigate the performance of the SEPIC converters for different modalities. At first, the response of the open loop and conventional closed loop system is performed and the performance parameters are presented in tabulated form as well as pictorial form.

In order to obtain enhanced performance, the responses of the system for GA and SA based PID controller are simulated for different parameters and objective functions. The values of the controller (k_P, k_I and k_D) and performance parameters are tabulated afterwards. Hence the comparative analysis among these two nonlinear techniques are carried out and optimized controller for both of the cases are investigated which will ensure stability of the SEPIC converter.

5.1 Performance Parameters

To investigate the performance of the overall system, percentage of overshoot, rise time, settling time and peak amplitude are take into account. However, initial overshoot is a major concern in case of power converters. If the initial overshoot is more than 10%, then it is not accepted. So, in this work, the investigation will be carried out so that performance of the system can be observed for less initial overshoot. Brief discussions about these parameters are stated below:

i. ***Percentage of Overshoot (%OS):***
In signal processing, control theory, electronics, and mathematics, overshoot is the occurrence of a signal or function exceeding its target. It arises especially in the step response of band limited systems such as low-pass filters.

ii. ***Rise Time (Tr):***
Time it takes for the response to rise from 10% to 90% of the steady-state response.

iii. ***Settling Time (Ts):***
Time it takes for the error between the response and the steady-state response to fall to within 2% of it.

iv. ***Peak amplitude:***
Peak absolute value of the output is referred as peak amplitude.

The response of the system can be classified in four categories based on their characteristics, they are-

i. Over-damped Response
ii. Underdamped Response
iii. Undamped Response
iv. Critically damped Response

Over-damped response is obtained when the poles are real, whereas for underdamped response the poles are complex. In case of undamped response, poles are in imaginary part and for critically damped response, poles will be real and equal. In the next section, open loop and closed loop responses are obtained for the overall system.

5.2 Open Loop and Closed Loop Responses

With the help of the equations derived earlier, the state space model is turned into a higher order transfer function for the purpose of simulating the stability of the system [91]. Model order reduction technique is carried out so that the system can be converted into a simpler form. Table 5.1 presents the converter parameters that are used for mathematical calculation and simulation of the stability of the SEPIC converter.

Table 5.1 Parameters used for SEPIC Converter [91]

Parameter	***Symbol***	***Values***
Input Voltage	V_{in}	10 V
Switching Frequency	f_s	100 KHz
Duty Cycle	d	0.5
Inductor	L_1, L_2	100 µH
Resistance	r_{L1}, r_{L2}	1 mΩ
	r_{C1}	3 mΩ
	r_{C2}	1 mΩ
Capacitor	C_1,C_2	800 µF, 3000 µF
Load Resistance	R_o	1 Ω
Output Voltage	Vo	10 V

➢ Open Loop Analysis

The output voltage waveform is shown in Fig. 3.7 with duty cycle 0.5. It is shown that the steady state is achieved approximately at 0.03 sec.

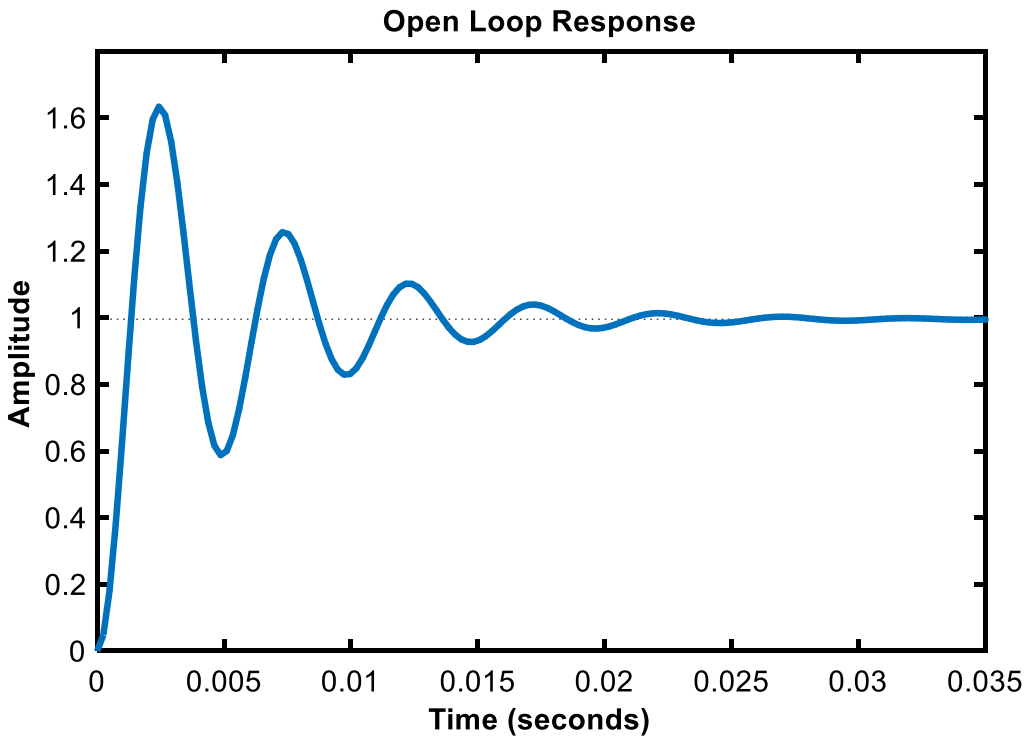


Fig. 5.1 Voltage amplitude Vs. Time for output of open loop

The output of the average model is a reflection of the response of the converter in open loop. From the output, it is observed that percentage of overshoot is 64%, peak amplitude is 1.63, rise time is 0.000902s and settling time is 0.0203s. Hence, it is evident that overshoot is really high in terms of open loop response which needs to be reduced as it is a major concern for different applications of SEPIC converter.

➢ Closed Loop Analysis with PID Controller

To enhance the performance of the converter, closed loop techniques are employed by many researchers in different times. Among various methods, PID controller is the most widely employed method [92-93] and researchers implement this control technique to investigate and improve the performance of power converters.

Firstly, conventional PID controller (Ziegler Nichols tuning method) is employed in SEPIC converter by using the concept from Table 3.2 and table 3.3 and the step response is taken to inspect the stability of the system which is shown in Fig. 5.2.

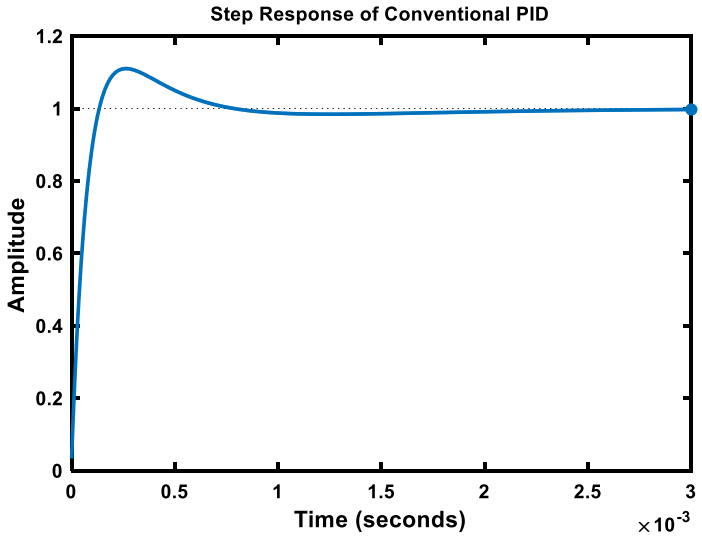


Fig. 5.2. Step Response of Conventional PID Controller

In closed loop analysis, it is observed that the overshoot it is 11% which is much less than open loop analysis. Moreover, rise time and settling time have also improved and they are 0.000954s and 0.000639s respectively. In addition, peak amplitude has also decreased and it is 1.11 which leads to less steady state error. The performance parameters; Percentage of Overshoot (%OS), Rise Time (Tr), Settling Time (Ts) and Peak Amplitude are tabulated for both open loop and close loop analysis which is presented in Table 5.2.

Table 5.2 Performance Analysis for both open loop and close loop block diagram

Performance Parameters	***Open Loop Response***	***Close Loop Response (Conventional PID controller)***
%OS	64	11
Tr	0.000902	0.000954
Ts	0.0203	0.000639
Peak Amplitude	1.63	1.11

In order to reduce the overshoot, and obtain faster settling time, closed loop response should be investigated further by employing nonlinear optimization technique. In this regard, genetic algorithm and simulated annealing algorithm are utilized to design optimized PID controller for SEPIC converter and results are simulated in the following sections.

5.3 GA based PID Controller

After open loop analysis and closed loop analysis by conventional PID controller, Genetic Algorithm (GA) is deployed in the system [94] to determine more optimum values of the PID controller. In this regard, rigorous simulation is carried out by employing genetic algorithm for three solution spaces and corresponding responses are collected and presented in the following sections. Different fitness functions (e.g IAE, ITAE. ISE, ITSE) are used to investigate the performance parameters (percentage of overshoot, rise time, fall time and peak amplitude) of the system and evaluate accordingly. Hence, the most optimized controller among the three approaches is found out and brought into play for comparative analysis.

5.3.1 GA-PID-1:

In genetic algorithm, population plays a vital role as it is referred as potential solution at the initial stage of optimizing the system. In this section, initial population is kept at 25, crossover is 0.9 and the approach is designated as 'GA-PID-1'. The optimized values of the PID controller and output of performance indices are shown accordingly for GA-PID-1. The parameters are listed in Table 5.3.

Table 5.3 Parameters of Genetic Algorithm for GA-PID-1

Population:	25
Fitness Scaling:	Rank
Selection:	Stochastic Uniform
Mutation:	Constraint Dependent
Crossover:	Constraint Dependent
Crossover Probability	0.9

5.3.1.1 GA-PID-1 Simulation Results

After rigorous simulation in MATLAB, the values of k_P, k_I and k_D are obtained for all of the three performance indices of GA based PID controller which is evident in Table 5.4 along with the conventional PID controller keeping the initial population 25. Step responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.3, Fig. 5.4, Fig. 5.5 and Fig. 5.6. The overall comparative analysis of the step responses is illustrated in Fig. 5.7.

Table 5.4 *Gain Values for GA-PID-1*

Gains	GA-PID-1			
	IAE	**ITAE**	**ISE**	**ITSE**
k_P	25.335	17.194	26.811	19.316
k_I	22303.569	25696.061	29192.84	31824.194
k_D	0.01	0.005	0.01	0.005

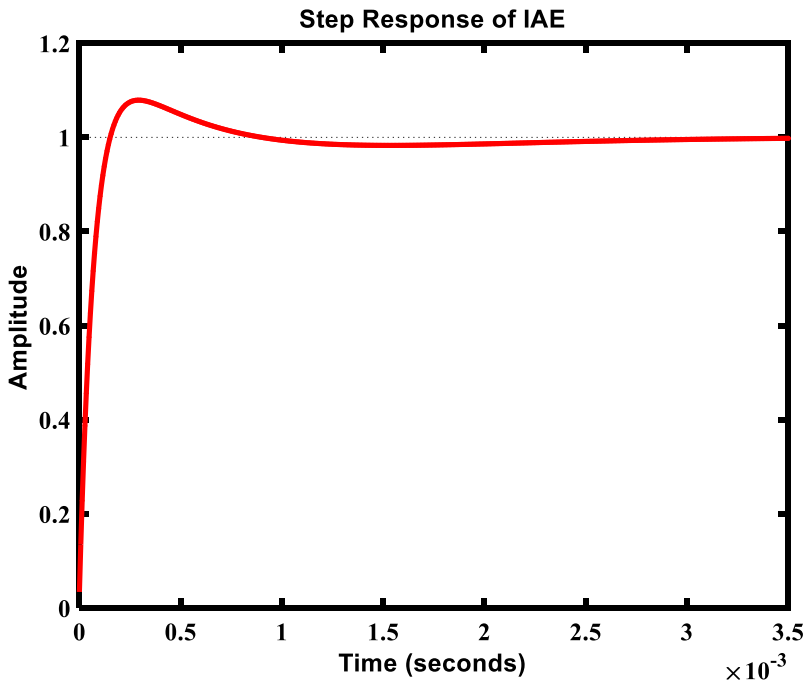


Fig. 5.3. Step Response of IAE for GA-PID-1

At first, step response of IAE is observed and exhibited in case of GA-PID-1 (Fig. 5.3). Here, rise time is 0.000104 s, settling time is 0.000696 s, overshoot is 7.95% and peak amplitude is 1.08.

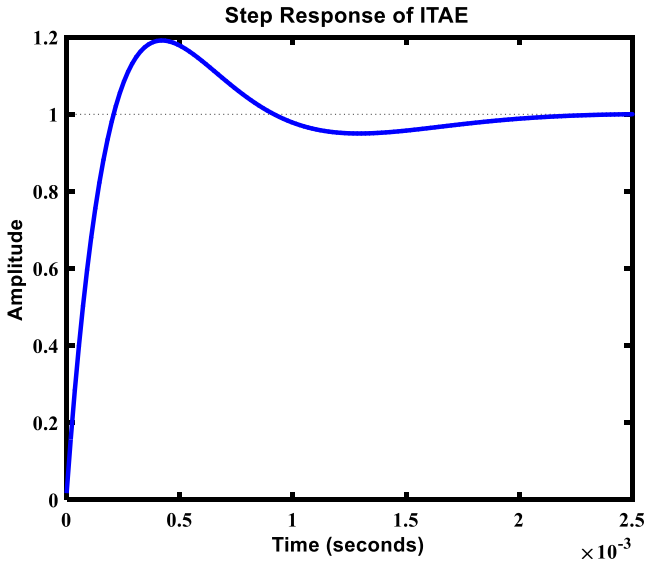


Fig. 5.4. Step Response of ITAE for GA-PID-1

Secondly, step response of ITAE is observed and presented for GA-PID-1 (Fig. 5.4). Here, rise time is 0.000158 s, settling time is 0.00183 s, overshoot is 19.6% and peak amplitude is 1.2.

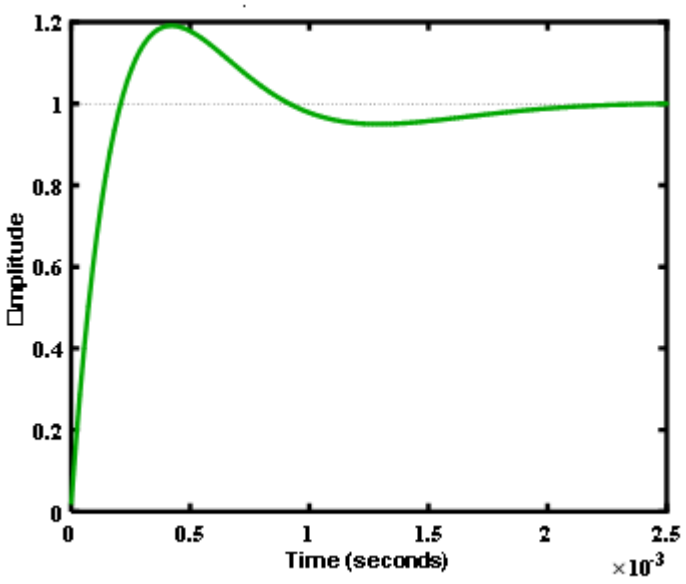


Fig. 5.5. Step Response of ISE for GA-PID-1

Thirdly, step response of ISE is illustrated in case of GA-PID-1 (Fig. 5.5). For this, rise time is 0.000104 s, settling time is 0.000724 s, overshoot is 9.24% and peak amplitude is 1.09.

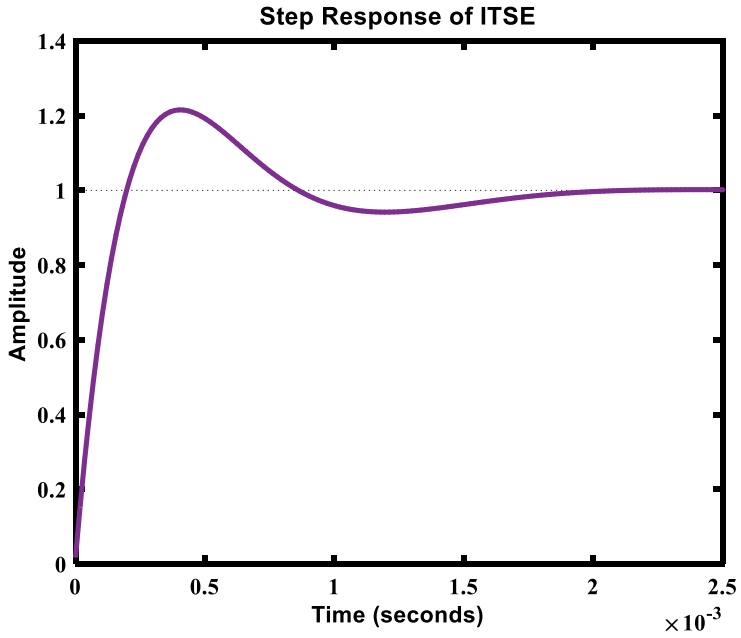


Fig. 5.6. Step Response of ITSE for GA-PID-1

Then, step response of ITSE is observed and presented for GA-PID-1 (Fig. 5.6). In case of this one, rise time is 0.000151 s, settling time is 0.0017 s, overshoot is 21.7% and peak amplitude is 1.22.

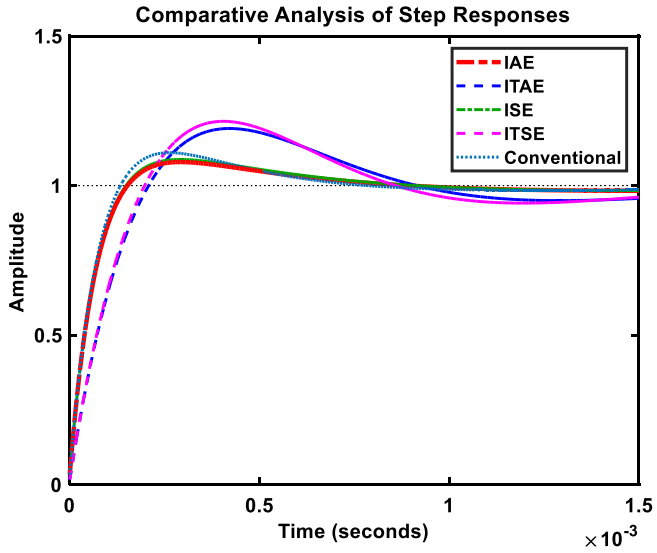


Fig. 5.7 Comparative Analysis of step responses for GA-PID-1

Finally, comparative analysis of step responses for GA-PID-1 with the conventional PID controller is observed and shown in Fig. 5.7. It is clearly visible that GA based controllers have shown better results with respect to the conventional PID controller for IAE and ISE in terms of overshoot. The rise time and settling time for all of the cases are satisfactory. Detailed quantitative analysis of the controllers and their performance indices are discussed at the end of the chapter.

The performance parameters like Percentage of Overshoot (%OS), Rise Time (Tr), Settling Time (Ts) and Peak Amplitude are tabulated for GA-PID-1 which is presented in Table 5.5

Table 5.5 *Evaluation of Performance Parameters for GA-PID-1*

Performance Parameters	***GA-PID-1***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	7.95	19.6	9.24	21.7
Tr	0.000104	0.000158	0.000104	0.000151
Ts	0.000696	0.00183	0.000724	0.0017
Peak Amplitude	1.08	1.2	1.09	1.22

5.3.2 GA-PID-2

In this section, initial population is kept at 50, crossover is 0.8 and the approach is referred as 'GA-PID-2'. The optimized values of the PID controller and output of performance indices are shown accordingly for GA-PID-2. The parameters are listed in Table 5.6.

Table 5.6 Parameters of Genetic Algorithm for GA-PID-2

Population:	50
Fitness Scaling:	Rank
Selection:	Stochastic Uniform
Mutation:	Constraint Dependent
Crossover:	Constraint Dependent
Crossover Probability	0.8

5.3.2.1 GA-PID-2 Simulation Results

Hence, the values of k_P, k_I and k_D are obtained for GA-PID-2 of all of the four performance indices which is evident in Table 5.7 keeping the initial population 50. Step responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.8, Fig. 5.9, Fig. 5.10 and Fig. 5.11. The overall comparative analysis of the step responses is illustrated in Fig. 5.12.

Table 5.7 *Gain Values for GA-PID-2*

Gains	GA-PID-2			
	IAE	**ITAE**	**ISE**	**ITSE**
k_P	28.044	18.114	31.614	16.297
k_I	26,405.394	24,115.704	30995.005	22840.309
k_D	0.0099	0.0054	0.0100	0.0047

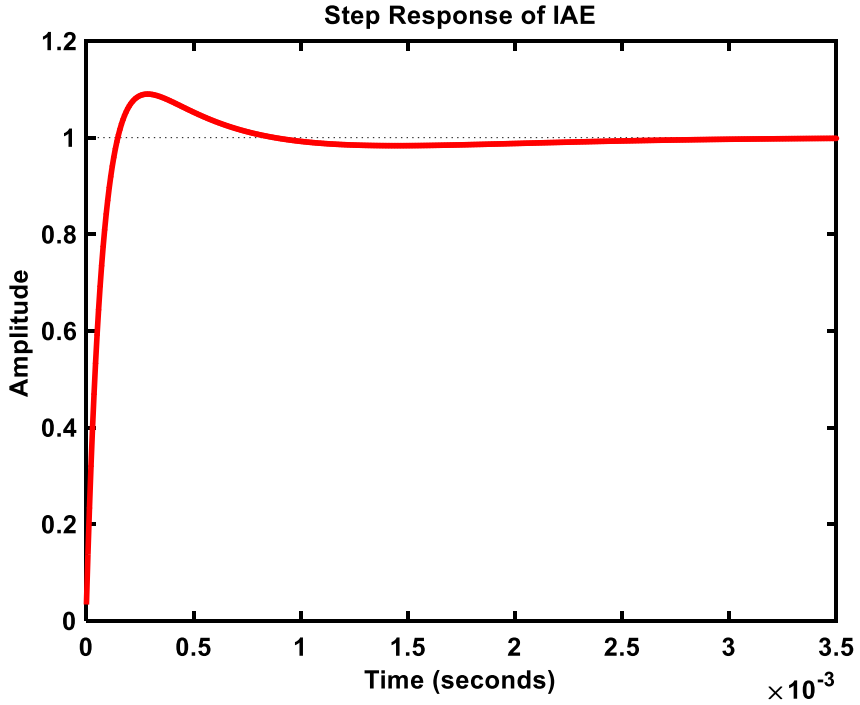


Fig. 5.8. Step Response of IAE for GA-PID-2

At first, step response of IAE is observed and exhibited in case of GA-PID-2 (Fig. 5.8). Here, rise time is 0.00012 s, settling time is 0.00418 s, overshoot is 3.43% and peak amplitude is 1.03.

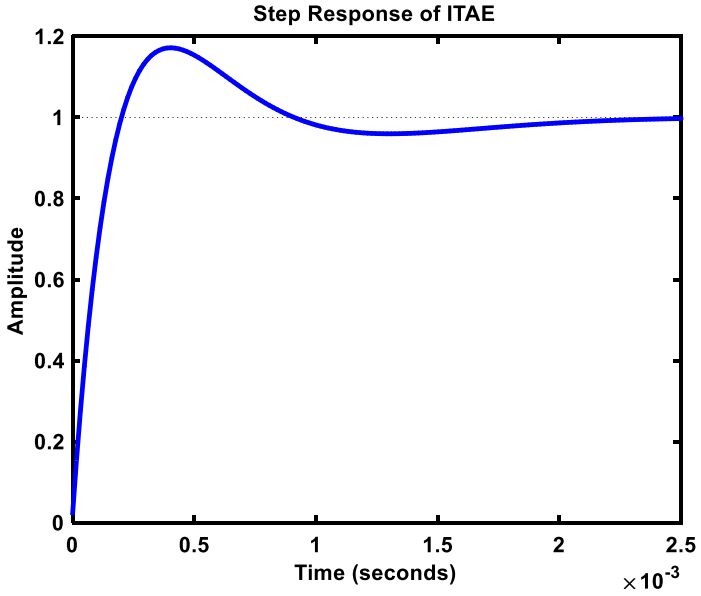


Fig. 5.9. Step Response of ITAE for GA-PID-2

Secondly, step response of ITAE is observed and presented for GA-PID-2 (Fig. 5.9). Here, rise time is 0.000109 s, settling time is 0.0013 s, overshoot is 13.7% and peak amplitude is 1.14.

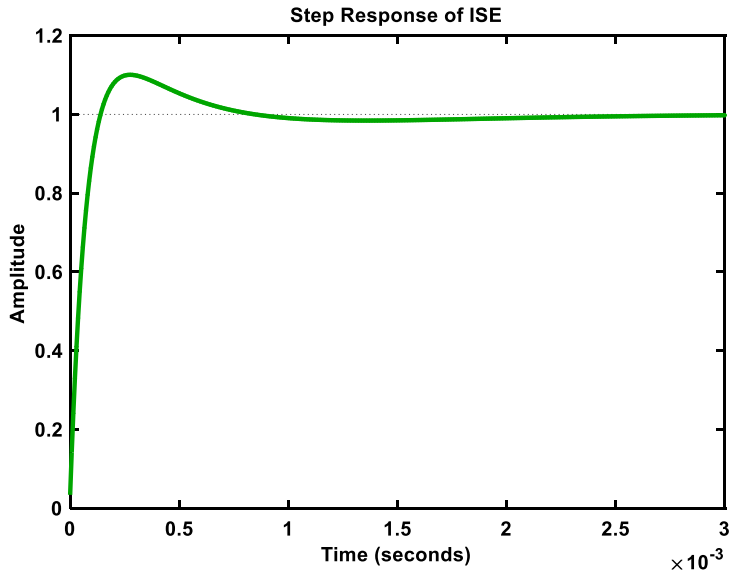


Fig. 5.10. Step Response of ISE for GA-PID-2

Thirdly, step response of ISE is illustrated in case of GA-PID-2 (Fig. 5.10). For this, rise time is 0.000102 s, settling time is 0.000676 s, overshoot is 11.3% and peak amplitude is 1.11.

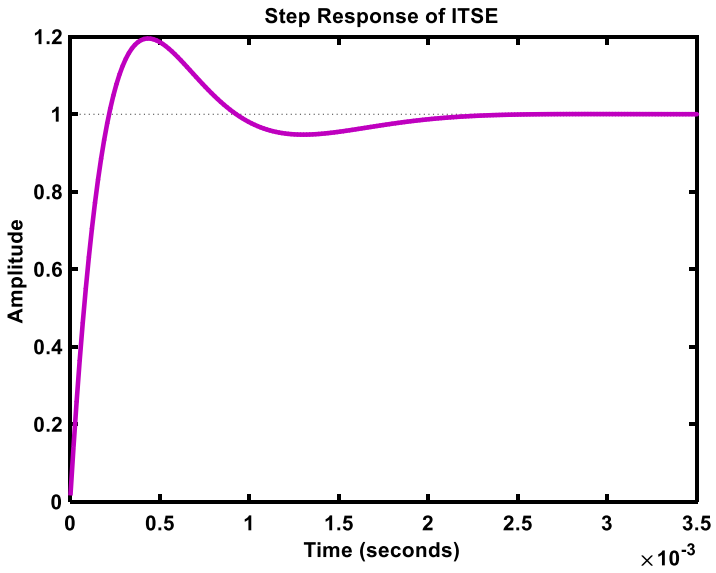


Fig. 5.11. Step Response of ITSE for GA-PID-2

Then, step response of ITSE is observed and presented for GA-PID-2 (Fig. 5.11). In case of this one, rise time is 0.000164 s, settling time is 0.00188 s, overshoot is 19.5% and peak amplitude is 1.23.

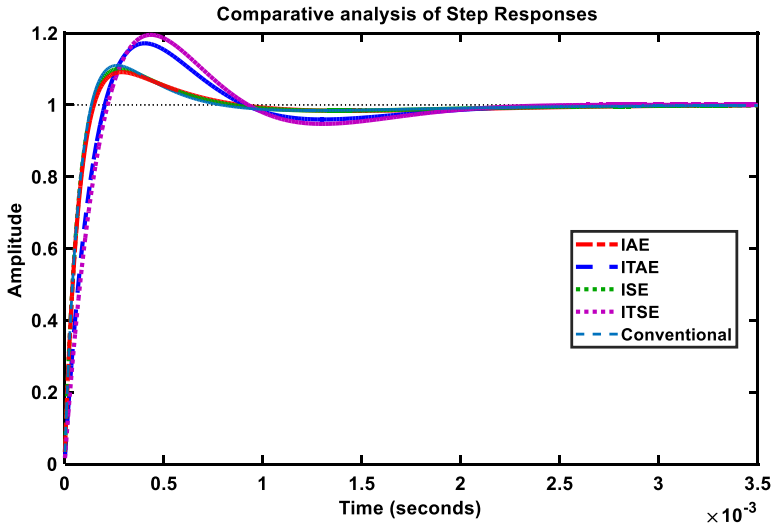


Fig. 5.12 Comparative Analysis of step responses for GA-PID-2

Finally, comparative analysis of step responses for GA-PID-2 with the conventional PID controller is observed and shown in Fig. 5.12. It is unequivocally visible that only IAE has exhibited less overshoot than conventional PID controller. The other objective functions ended up with more overshoot than the conventional one. In case of rise time, the values are satisfactory for all objective functions. Moreover, it is also seen that, IAE and ITAE have rapid settling time than the other performance indices. Detailed quantitative analysis among the controllers is discussed at the end of the chapter.

The performance parameters like Percentage of Overshoot (%OS), Rise Time (Tr), Settling Time (Ts) and Peak Amplitude are tabulated for GA-PID-2 in Table 5.8

Table 5.8 *Evaluation of Performance Parameters for GA-PID-2*

Performance Parameters	***GA-PID-2***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	3.43	13.7	11.3	19.5
Tr	0.00012	0.000109	0.000102	0.000164
Ts	0.00418	0.0013	0.000676	0.00188
Peak Amplitude	1.03	1.14	1.11	1.23

5.3.3 GA-PID-3

In this section, initial population is kept at 75, crossover is 0.7 and the approach is referred as 'GA-PID-3'. The optimized values of the PID controller and output of performance indices are shown accordingly for GA-PID-3. The parameters are listed in Table 5.9.

Table 5.9 Parameters of Genetic Algorithm for GA-PID-3

Population:	75
Fitness Scaling:	Rank
Selection:	Stochastic Uniform
Mutation:	Constraint Dependent
Crossover:	Constraint Dependent
Crossover Probability	0.7

5.3.3.1 GA-PID-3 Simulation Results

Hence, the values of k_P, k_I and k_D are obtained for GA-PID-3 of all of the four fitness functions which is evident in Table 5.10 keeping the initial population 75 and crossover 0.7. Step responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.13, Fig. 5.14, Fig. 5.15 and Fig. 5.16. The overall comparative analysis of the step responses is illustrated in Fig. 5.17.

Table 5.10 *Gain Values for GA-PID-3*

Gains	GA-PID-3			
	IAE	**ITAE**	**ISE**	**ITSE**
k_P	29.155	20.017	24.334	18.21
k_I	28076.226	31547.399	18020.711	28823.778
k_D	0.01	0.005	0.01	0.005

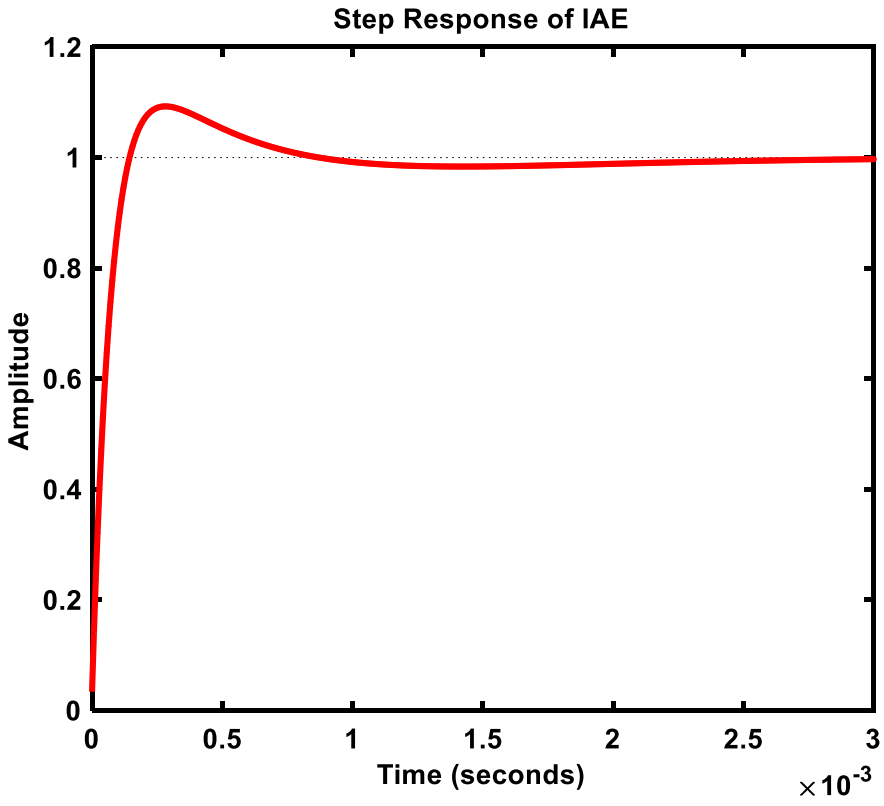


Fig. 5.13. Step Response of IAE for GA-PID-3

At first, step response of IAE is observed and exhibited in case of GA-PID-3 (Fig. 5.13). Here, rise time is 0.000101 s, settling time is 0.000695 s, overshoot is 9.14% and peak amplitude is 1.09.

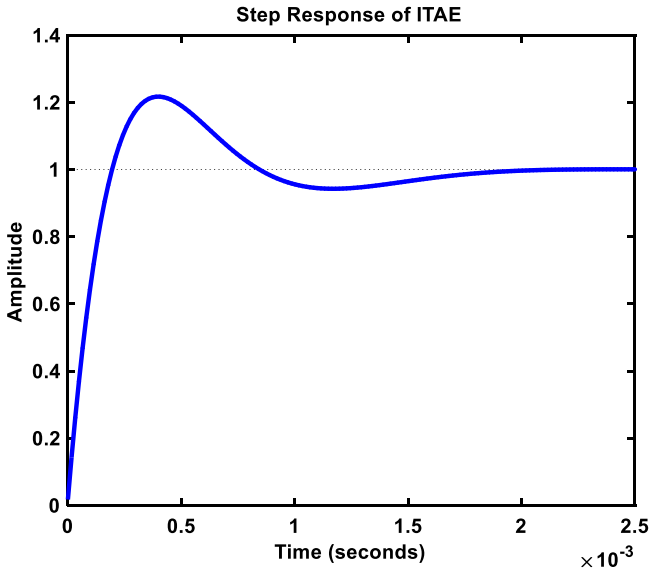


Fig. 5.14. Step Response of ITAE for GA-PID-3

Secondly, step response of ITAE is observed and presented for GA-PID-3 (Fig. 5.14). Here, rise time is 0.000143 s, overshoot is 18.8%, settling time is 0.00174 sand peak amplitude is 1.19.

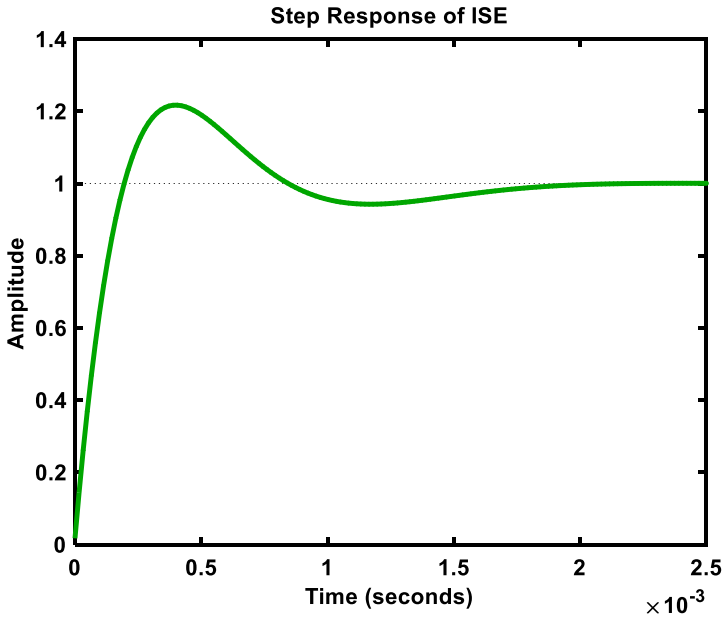


Fig. 5.15. Step Response of ISE for GA-PID-3

Thirdly, step response of ISE is illustrated in case of GA-PID-3 (Fig. 5.15). For this, rise time is 0.000108 s, settling time is 0.000682 s, overshoot is 7.97% and peak amplitude is 1.08.

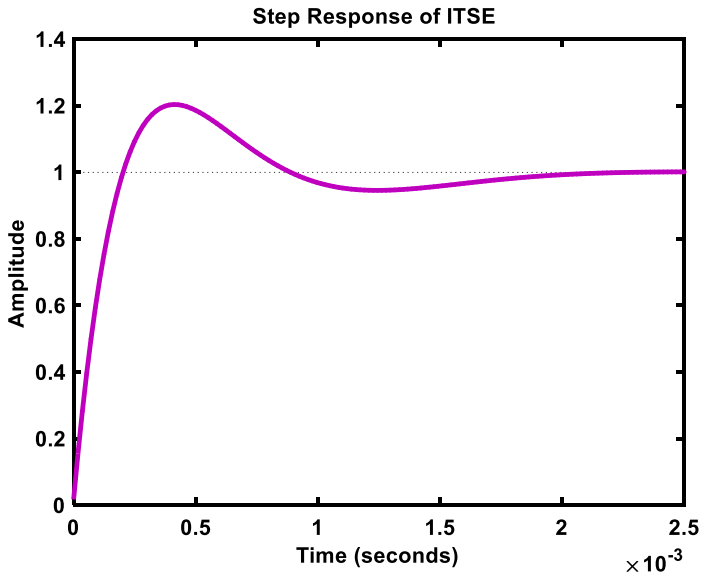


Fig. 5.16. Step Response of ITSE for GA-PID-3

Then, step response of ITSE is observed and presented for GA-PID-3 (Fig. 5.16). In case of this one, settling time is 0.00176 s, overshoot is 20.9%, rise time is 0.000155 s and peak amplitude is 1.21.

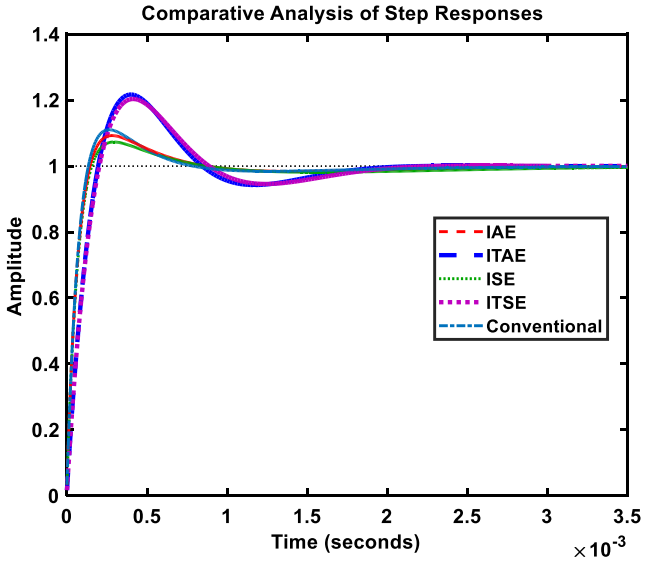


Fig. 5.17 Comparative Analysis of step responses for GA-PID-3

Finally, comparative analysis of step responses for GA-PID-3 with the conventional PID controller is observed and shown in Fig. 5.17. It is again visible that among GA based controllers, IAE and ISE exhibit less overshoot than conventional PID controller whereas, ITAE and ITSE show more overshoot than the conventional controller. Detailed quantitative analysis is provided at the end of the chapter.

Now, the performance parameters like Percentage of Overshoot (%OS), Rise Time (Tr), Settling Time (Ts) and Peak Amplitude are tabulated for GA-PID-3. This comparative analysis is then presented in Table 5.11

Table 5.11 *Evaluation of Performance Parameters for GA-PID-3*

Performance Parameters	***GA-PID-3***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	9.14	18.8	7.97	20.9
Tr	0.000101	0.000143	0.000108	0.000155
Ts	0.000695	0.00174	0.000682	0.00176
Peak Amplitude	1.09	1.19	1.08	1.21

5.4 Graphical Analysis of GA Based PID Controller

The graphical representations of the performance parameters for GA-PID-1, GA-PID-2 and GA-PID-3 are marked as blue, green and red and illustrated in Fig. 5.18, 5.19, 5.20 and 5.21 respectively in this section.

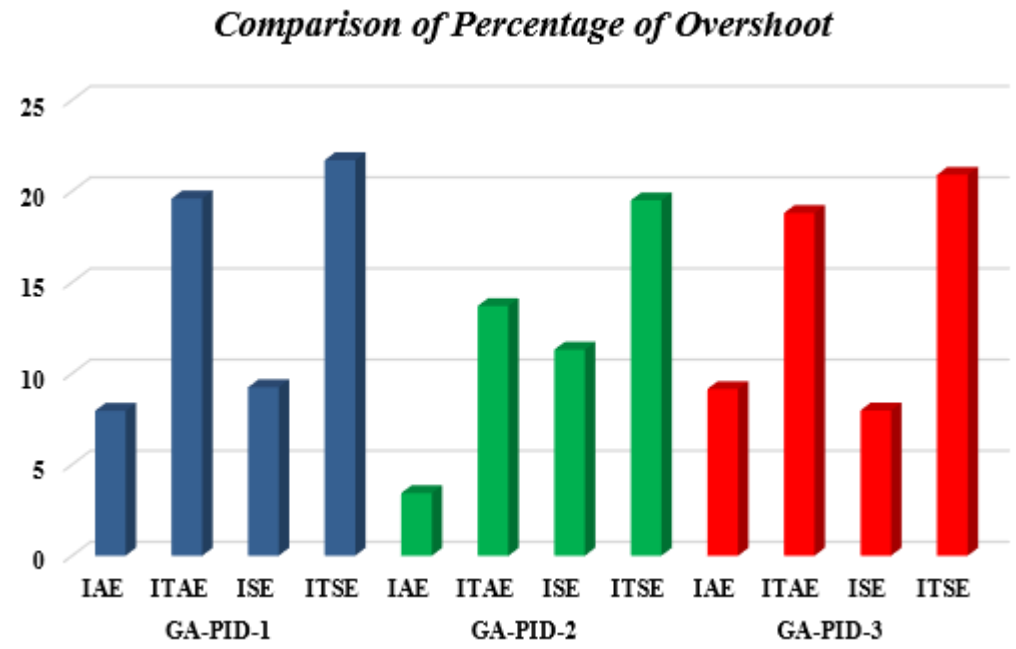


Fig. 5.18. Comparative Analysis of percentage of overshoot (%OS) for all GA based PID controllers

After carrying out the comparative analysis, it is observed that IAE of GA-PID-2 is exhibiting less overshoot than that of other performance indices. As overshoot is a major concern in a converter circuit, IAE of GA-PID-2 is more suitable than that of other approaches.

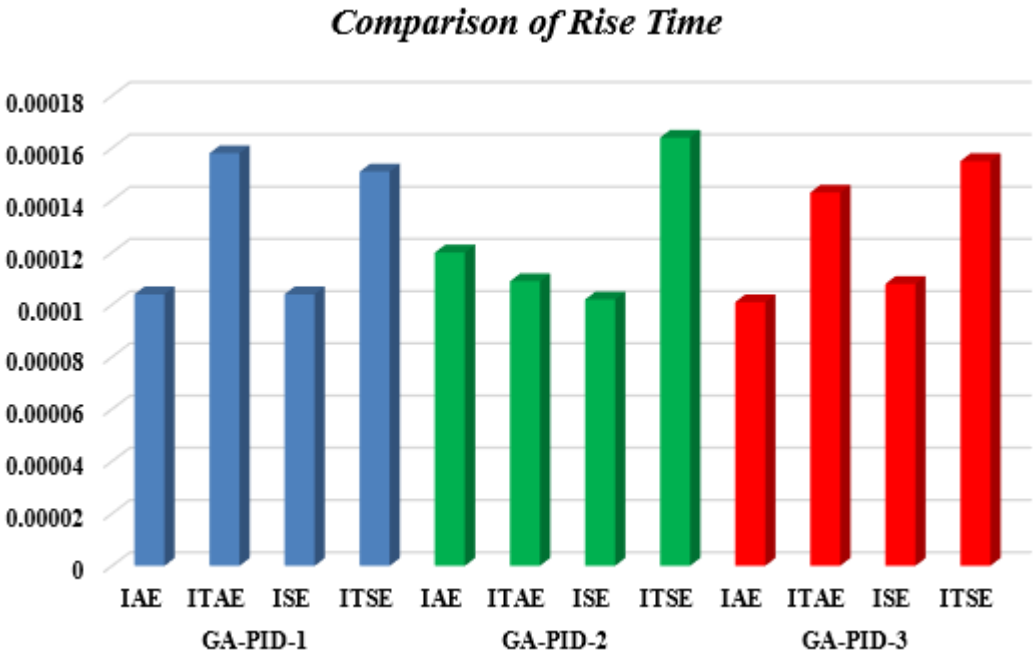


Fig. 5.19. Comparative Analysis of rise time (Tr) for all GA based PID controllers

In Fig. 5.19, comparative analysis, it is observed for each of the cases of GA based PID controller. The graphical illustration depicts that rise time is least for ISE of GA-PID-2 than that of other performance indices.

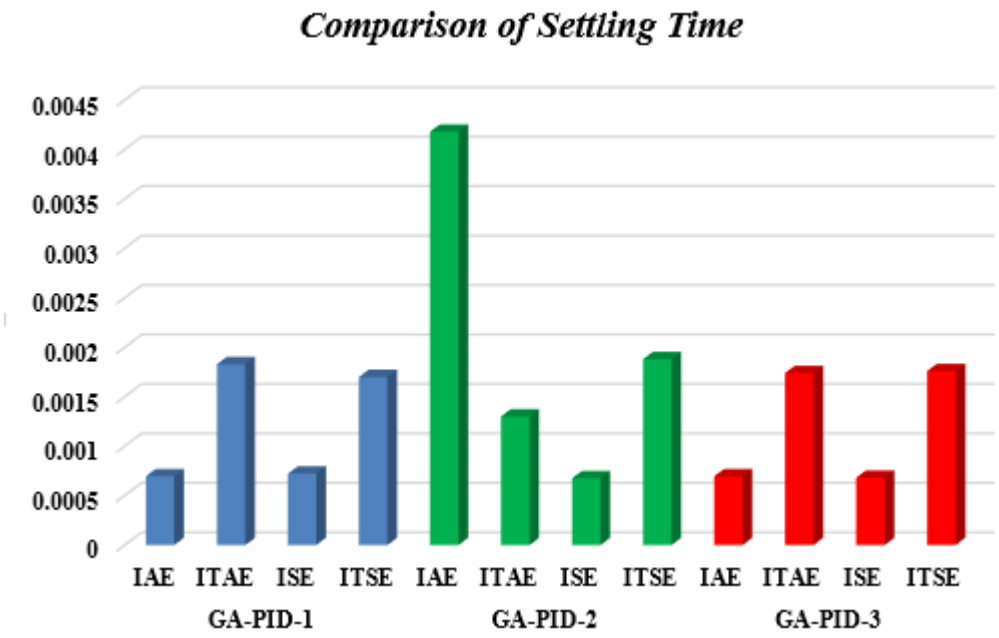


Fig. 5.20 Comparative Analysis of settling time (Ts) for all GA based PID controllers

From Fig. 5.20, it is evident that ISE of GA-PID-2 shows the most rapid settling time than other performance indices. However, IAE, ISE of GA-PID-1 and IAE, ISE of GA-PID-3 show quick settling time too. However, settling time is larger for IAE of GA-PID-2.

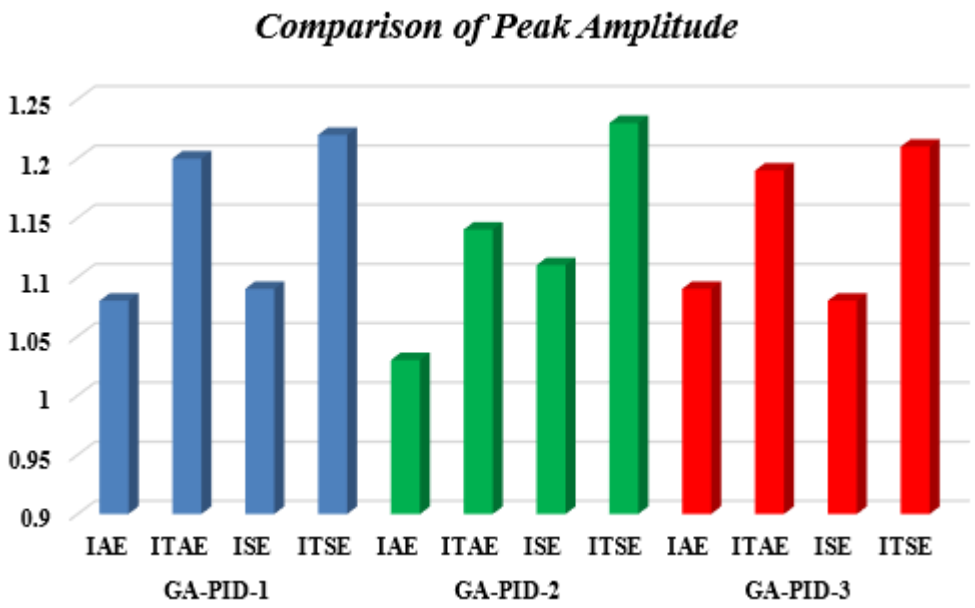


Fig. 5.21 Comparative Analysis of peak amplitude for all GA based PID controllers

In Fig. 5.21, it is shown that IAE of GA-PID-2 has the lowest peak amplitude than other approaches which ultimately leads to less steady state error.

So, it is observed that among all the performance indices of all the three approaches of GA based PID controller, IAE of GA-PID-2 is the most optimized design of the controller. Because, the overshoot is the minimum (3.43%) and peak amplitude is 1.03 which leads to less steady state error. Though it takes slightly more time (0.00418s), it is in acceptable limit. So, IAE of GA-PID is the most optimized approach among all the GA based PID controller.

5.5 SA based PID Controller

After implementing genetic algorithm (GA) based PID controller, simulating annealing (SA) algorithm based PID controller is carried out and corresponding responses for the four performance indices are collected. The objective of the fitness functions is to minimize the error between the output and input of the system. Step input is provided in the system and outputs are collected. Hence, the performances for each of the cases are discussed and comparative analysis is carried out.

5.5.1 SA-PID-1

In Simulated Annealing algorithm, initial temperature is a major concern as it determines the solution space in order to search for optimal values of the controller [95]. In this section, initial temperature is kept at 50 and the approach is designated as 'SA-PID-1'. The optimized values of the PID controller and output of performance indices are shown accordingly for SA-PID-1. The parameters are listed in Table 5.12.

Table 5.12 Parameters of Simulated Annealing Algorithm for SA-PID-1

Initial Temperature:	50
Temperature Update Function:	Exponential Temperature Update
Reannealing Interval:	100
Annealing Function:	Fast Annealing

5.5.1.1 SA-PID-1 Simulation Results

The parameters of SA-PID-1 are tabulated in Table 5.12. In Table 5.13, the gain values of PID controller for SA- PID-1 are presented.

Table 5.13 *Gain Values for SA-PID-1*

Gains	***SA-PID-1***			
	IAE	***ITAE***	***ISE***	***ITSE***
k_P	0.382	0.119	36	0.162
k_I	418.766	335.409	169.054	634.999
k_D	0.03	0.01	0.01	0.006

The responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.22, Fig. 5.23, Fig. 5.24 and Fig. 5.25 respectively.

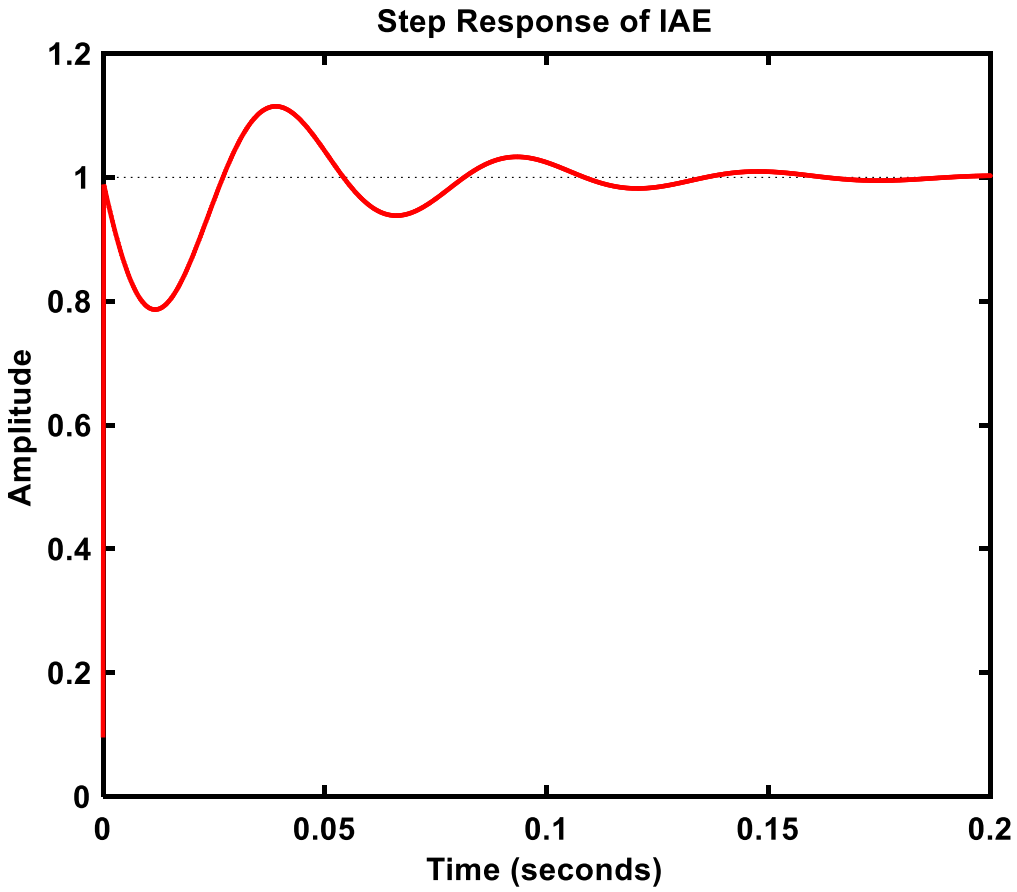


Fig. 5.22. Step Response of IAE for SA-PID-1.

At first, step response of IAE is observed and exhibited in case of SA-PID-1 (Fig. 5.22). Here, rise time is 0.000501 s, settling time is 0.102 s, overshoot is 11.5% and peak amplitude is 1.11.

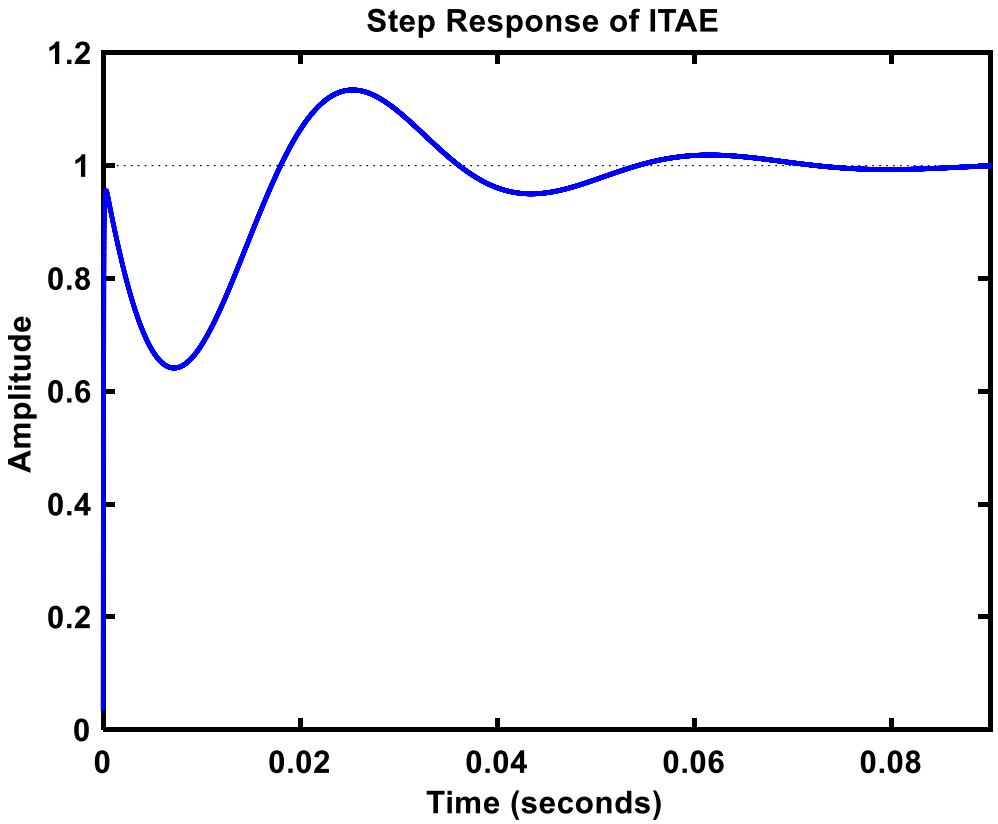


Fig. 5.23. Step Response of ITAE for SA-PID-1.

Secondly, step response of ITAE is observed and presented for SA-PID-1 (Fig. 5.23). Here, rise time is 0.000152 s, settling time is 0.0509 s, overshoot is 13.4% and peak amplitude is 1.13.

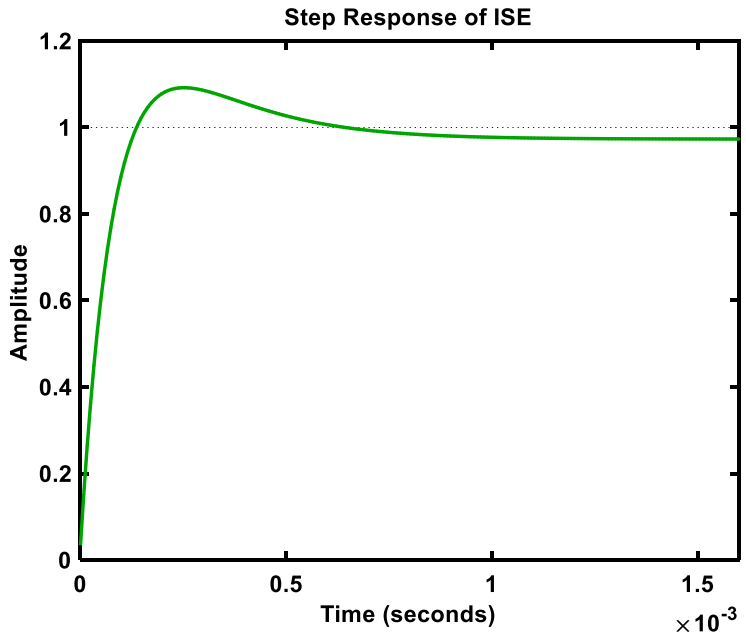


Fig. 5.24. Step Response of ISE for SA-PID-1.

Thirdly, step response of ISE is illustrated in case of SA-PID-1 (Fig. 5.24). For this, rise time is 0.000964 s, settling time is 0.000613 s, overshoot is 9.19% and peak amplitude is 1.09.

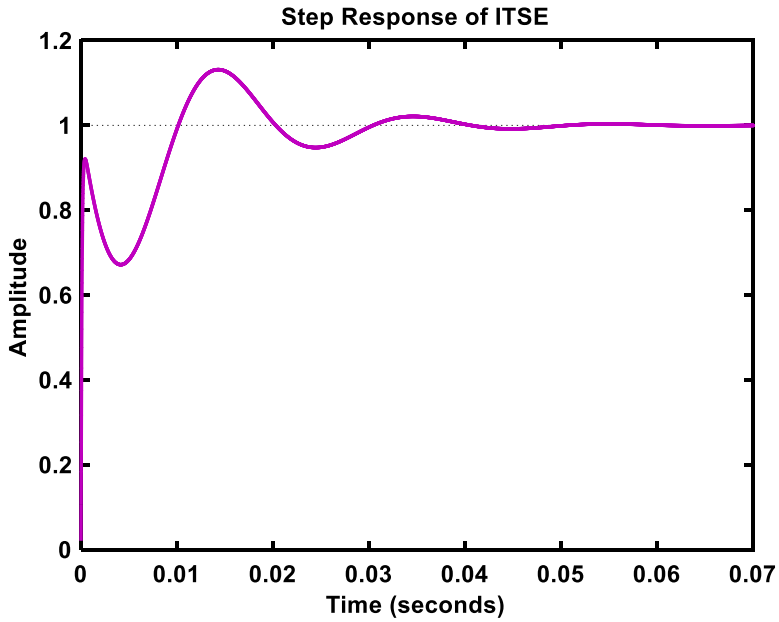


Fig. 5.25. Step Response of ITSE for SA-PID-1.

Then, step response of ITSE is evident for SA-PID-1 in Fig. 5.25. In case of this one, rise time is 0.000285 s, settling time is 0.0358 s, overshoot is 13.1% and peak amplitude is 1.13.

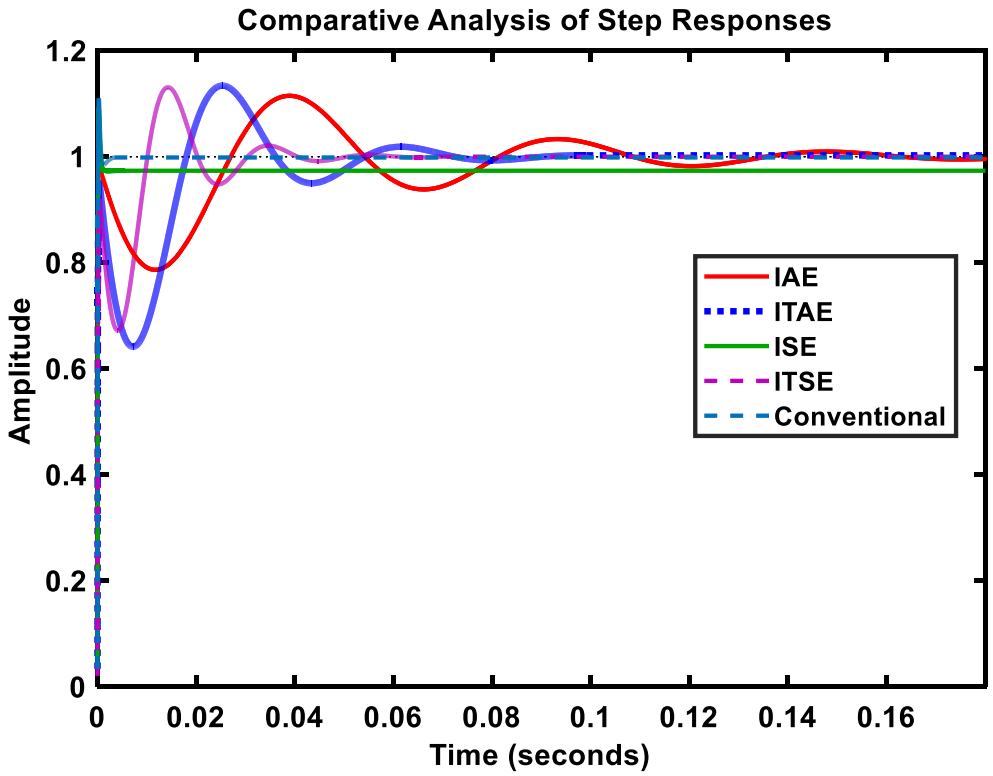


Fig. 5.26 Comparative Analysis of Step Responses for SA-PID-1.

Finally, comparative analysis of step responses for SA-PID-1 with the conventional one is observed and shown in Fig. 5.26. It is elucidated that SA based controllers have given better result with respect to the conventional PID controller in case of ISE only. Further analysis among these fitness functions of the controller is discussed in the forthcoming sections. The performance parameters are tabulated for SA-PID-1 which is presented in Table 5.14

Table 5.14 *Evaluation of Performance Parameters for SA-PID-1*

Performance Parameters	***SA-PID-1***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	11.5	13.4	9.19	13.1
Tr	0.000501	0.000152	0.000964	0.000358
Ts	0.0102	0.0509	0.00613	0.0358
Peak Amplitude	1.11	1.13	1.09	1.13

5.5.2 SA-PID-2

In Simulated Annealing algorithm, initial temperature is a major concern as it determines the solution space in order to search for optimal values of the controller. In this section, initial temperature is kept at 100 and the approach is designated as 'SA-PID-2'. The optimized values of the PID controller and output of performance indices are shown accordingly for SA-PID-2. The parameters are listed in Table 5.15.

Table 5.15 Parameters of Simulated Annealing Algorithm for SA-PID-2

Initial Temperature:	100
Temperature Update Function:	Exponential Temperature Update
Reannealing Interval:	100
Annealing Function:	Fast Annealing

5.5.2.1 SA-PID-2 Simulation Results

In Table 5.16, the gain values (k_P, k_I and k_D) of PID controller for SA- PID-2 are presented.

Table 5.16 Gain Values for SA-PID-2

Gains	***SA-PID-2***			
	IAE	***ITAE***	***ISE***	***ITSE***
k_P	23.815	0.366	39.705	0.844
k_I	1006.452	466.142	2012.13	926.984
k_D	0.02	0.02	0.02	0.02

Step responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.27, Fig. 5.28, Fig. 5.29 and Fig. 5.30. The overall comparative analysis of the step responses is illustrated in Fig. 5.31.

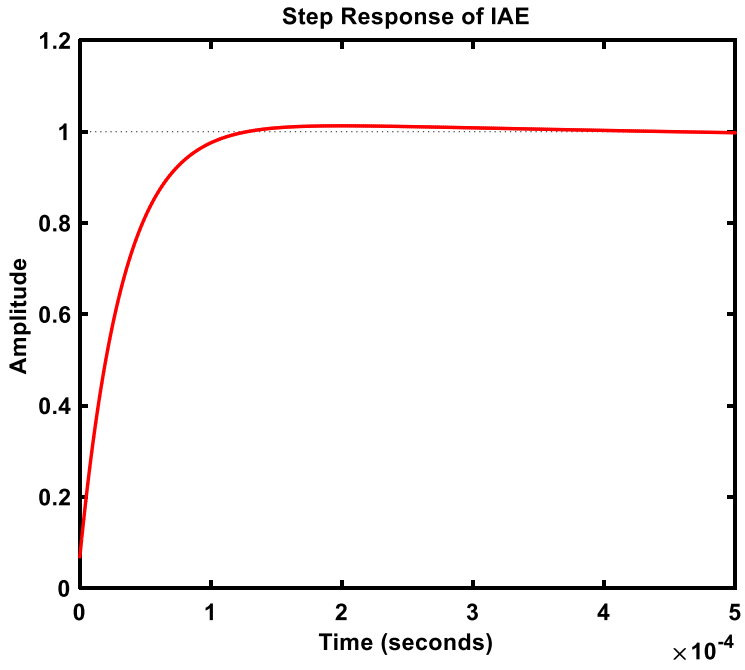


Fig. 5.27. Step Response of IAE for SA-PID-2.

At first, step response of IAE is manifested in case of SA-PID-2. Here, rise time is 0.000665 s, settling time is 0.000104 s, overshoot is 1.3% and peak amplitude is 1.01.

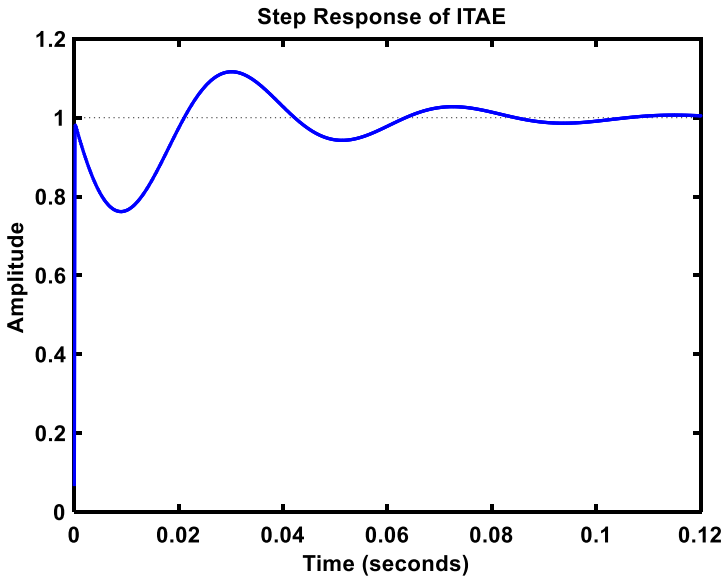


Fig. 5.28. Step Response of ITAE for SA-PID-2.

Secondly, step response of ITAE is observed and presented for SA-PID-1. Here, rise time is 0.000737 s, settling time is 0.0785 s, overshoot is 11.7% and peak amplitude is 1.12.

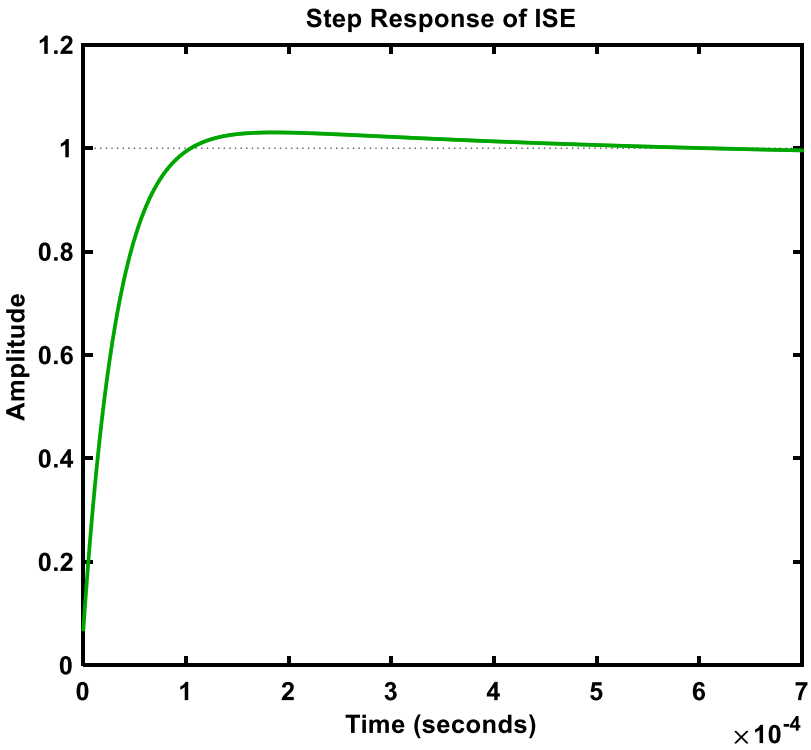


Fig. 5.29. Step Response of ISE for SA-PID-2.

Thirdly, step response of ISE is illustrated in case of SA-PID-1. For this, rise time is 0.000622 s, settling time is 0.000334 s, overshoot is 3.04% and peak amplitude is 1.03.

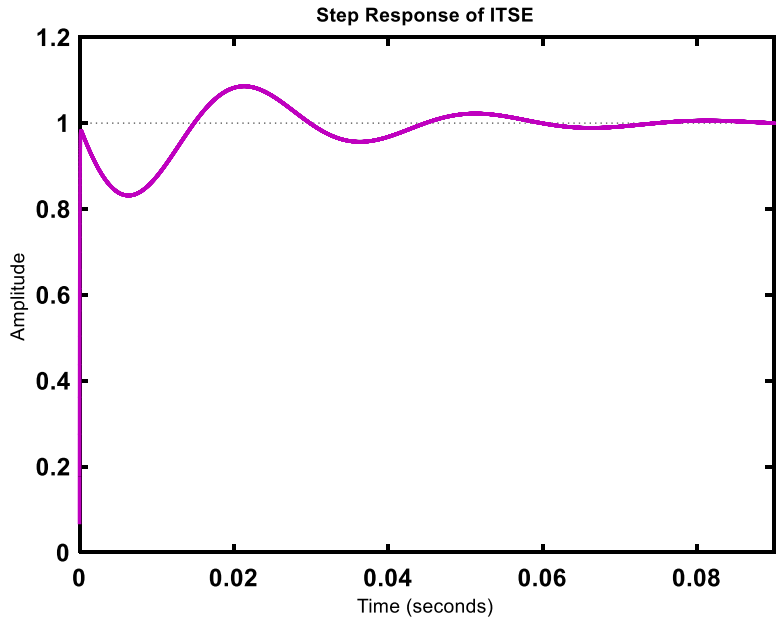


Fig. 5.30. Step Response of ITSE for SA-PID-2.

Here, step response of ITSE is evident for SA-PID-1. In case of this one, rise time is 0.000735 s, settling time is 0.0541 s, overshoot is 8.57% and peak amplitude is 1.09.

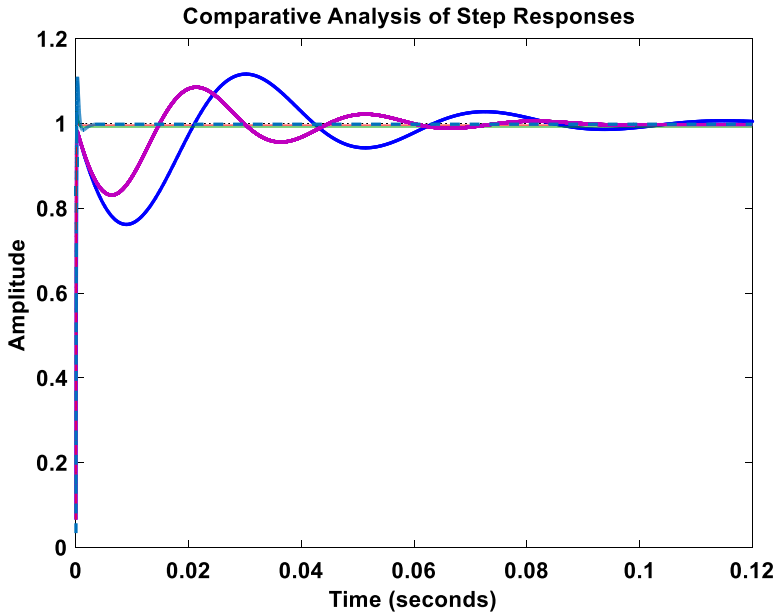


Fig. 5.31 Comparative Analysis of Step Responses for SA-PID-2.

Finally, comparative analysis of step responses for SA-PID-2 with the conventional PID controller is observed and shown in Fig. 5.31. It is evident that SA based controller have shown better result for IAE with respect to the conventional PID controller in terms of overshoot. Detailed discussion is performed at the end of the chapter. The performance parameters are tabulated for SA-PID-1 which is presented in Table 5.17

Table 5.17 Evaluation of Performance Parameters for SA-PID-2

Performance Parameters	***SA-PID-2***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	2.2	11.7	3.04	8.57
Tr	0.000665	0.000737	0.000622	0.000735
Ts	0.000104	0.0785	0.000334	0.0541
Peak Amplitude	1.01	1.12	1.03	1.09

5.5.3 SA-PID-3

In Simulated Annealing algorithm, initial temperature plays a significant role as it determines the solution space in order to search for optimal values of the controller. In this section, initial temperature is kept at 150 and the approach is designated as 'SA-PID-3'. The optimized values of the PID controller and output of performance indices are shown accordingly for SA-PID-3. The parameters are listed in Table 5.18.

Table 5.18 Parameters of Simulated Annealing Algorithm for SA-PID-3

Initial Temperature:	150
Temperature Update Function:	Exponential Temperature Update
Reannealing Interval:	100
Annealing Function:	Fast Annealing

5.5.3.1 SA-PID-3 Simulation Results

In Table 5.16, the gain values (k_P, k_I and k_D) of PID controller for SA-PID-2 are presented.

Table 5.19 Gain Values for SA-PID-3 Controller

Gains	***SA-PID-3***			
	IAE	***ITAE***	***ISE***	***ITSE***
k_P	0.855	0.324	3.418	1.162
k_I	962.705	534.417	1595.753	1169.309
k_D	0.009	0.001	0.01	0.001

Step responses for IAE, ITAE, ISE and ITSE are illustrated in Fig. 5.32, Fig. 5.33, Fig. 5.34 and Fig. 5.35. Then, the overall comparative analysis is illustrated in terms of step response in Fig. 5.36

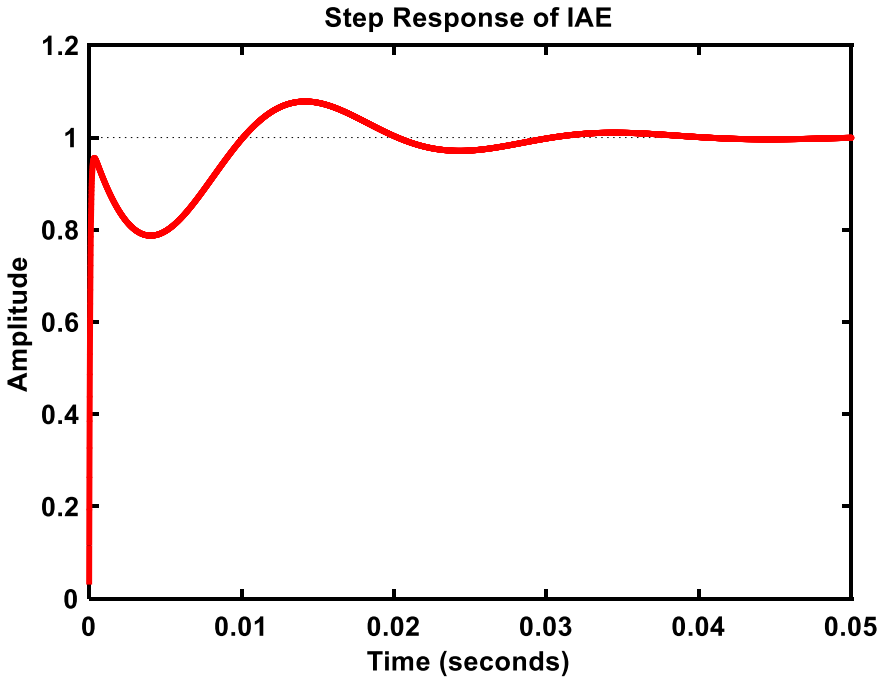


Fig. 5.32. Step Response of IAE for SA-PID-3.

At first, step response of IAE is observed in case of SA-PID-3 which is exhibited in Fig. 5.32. Here, rise time is 0.000561 s, settling time is 0.019 s, overshoot is 22.3% and peak amplitude is 1.22

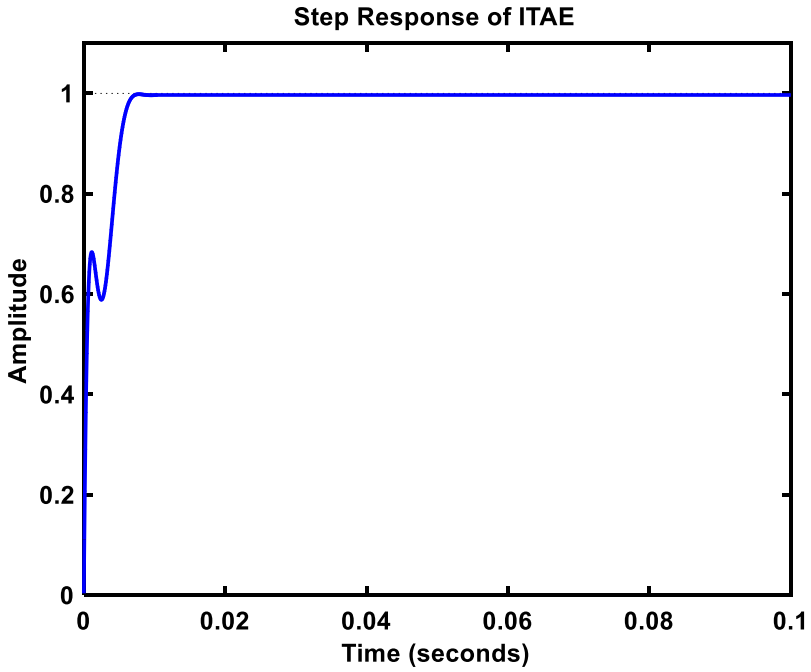


Fig. 5.33. Step Response of ITAE for SA-PID-3.

Secondly, step response of ITAE is observed and presented for SA-PID-3. Here, rise time is 0.000107 s, settling time is 0.000672 s, overshoot is 9.72% and peak amplitude is 1.1.

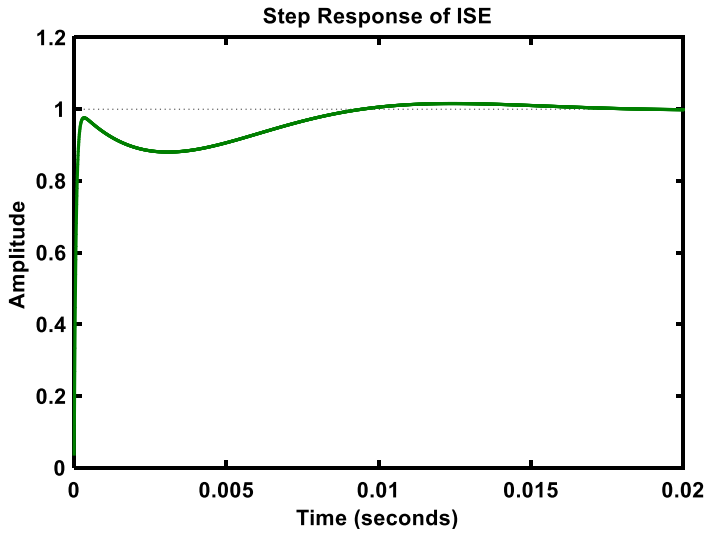


Fig. 5.34. Step Response of ISE for SA-PID-3.

Thirdly, step response of ISE is illustrated in case of SA-PID-3. For this, rise time is 0.000102 s, settling time is 0.000612 s, overshoot is 11.2% and peak amplitude is 1.11.

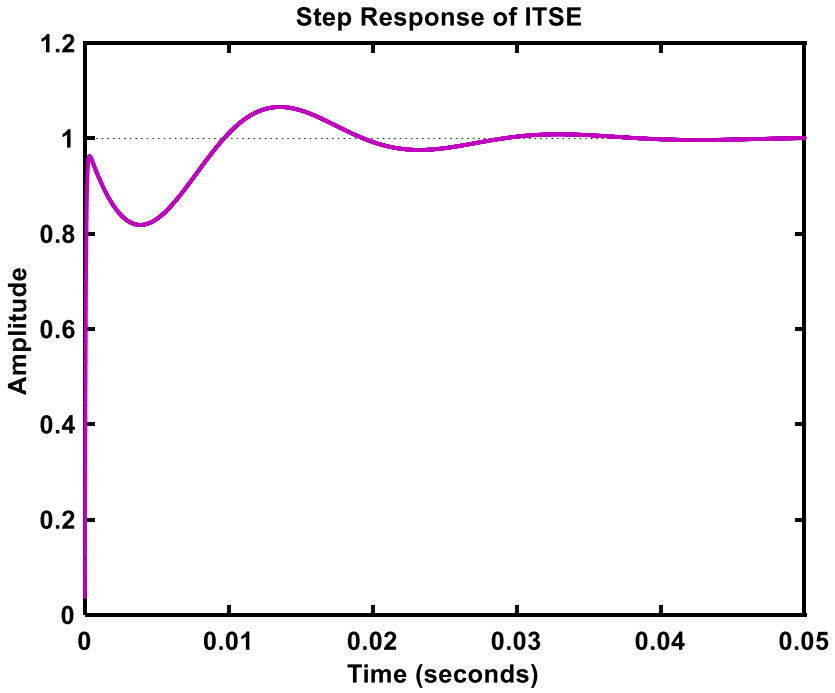


Fig. 5.35. Step Response of ITSE for SA-PID-3.

Here, step response of ITSE is evident for SA-PID-3. In case of this one, rise time is 0.000147 s, settling time is 0.0252 s, overshoot is 6.61% and peak amplitude is 1.07.

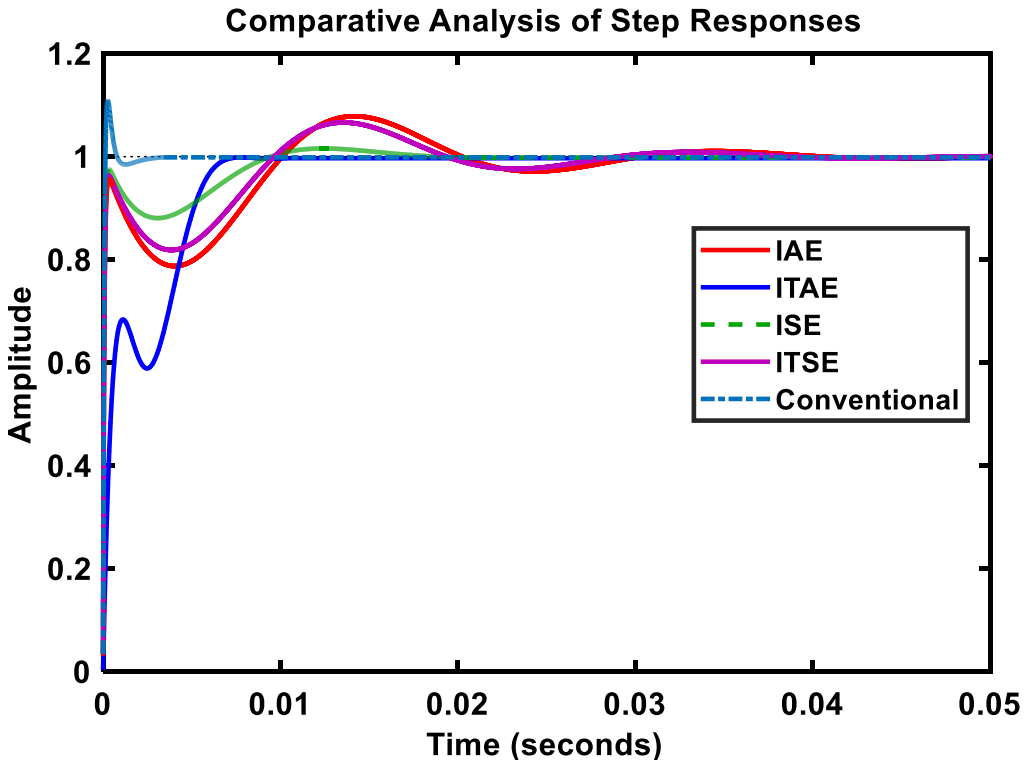


Fig. 5.36 Comparative Analysis of Step Responses for SA-PID-3.

Finally, comparative analysis of step responses for SA-PID-3 with the conventional PID controller is performed and shown in Fig. 5.36. It is seen that ITAE and ITSE show better result in terms of overshoot than other fitness functions. The performance parameters are tabulated for SA-PID-3 which is presented in Table 5.20

Table 5.20 Evaluation of Performance Parameters for SA-PID-3

Performance Parameters	***SA-PID-3***			
	IAE	***ITAE***	***ISE***	***ITSE***
%OS	22.3	9.72	11.2	6.61
Tr	0.000118	0.000525	0.00021	0.000135
Ts	0.0011	0.0299	0.0415	0.0252
Peak Amplitude	1.22	1.1	1.11	1.07

5.6 Graphical Analysis of SA Based PID Controller

The graphical representations of the performance parameters for SA-PID-1, SA-PID-2 and SA-PID-3 are marked as blue, green and red and illustrated in Fig. 5.37, Fig. 5.38, Fig. 5.39 and Fig. 5.40 respectively in this section.

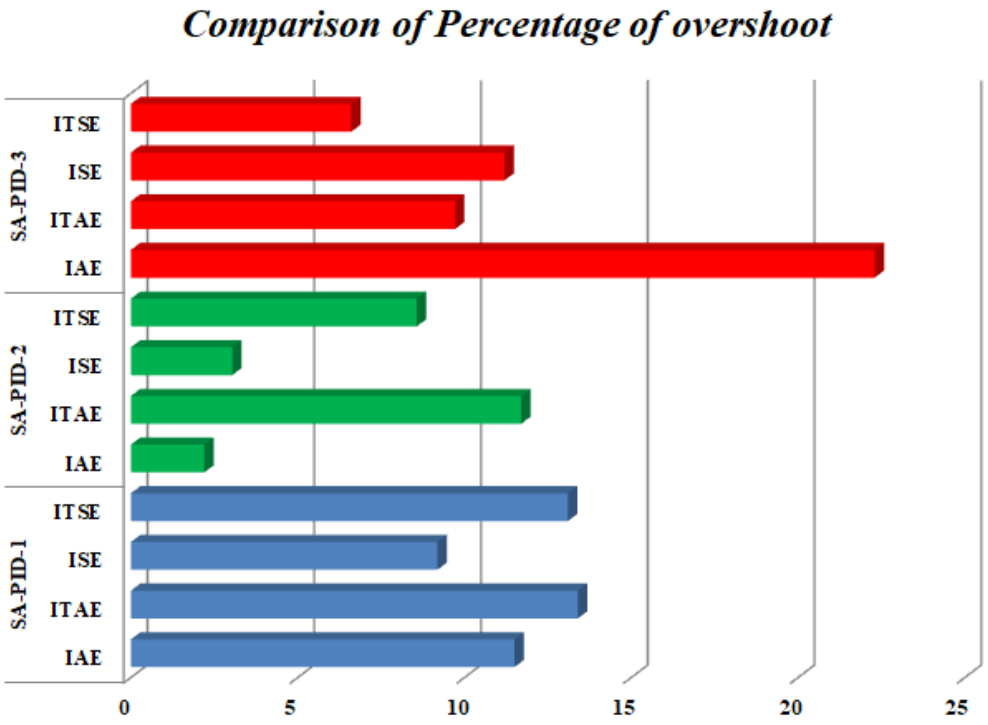


Fig. 5.37. Comparative Analysis of Percentage of Overshoot (%OS) for SA based PID Controllers.

After carrying out the comparative analysis, it is observed from Fig. 5.37 that IAE of SA-PID-2 is exhibiting less overshoot than that of other performance indices. As overshoot is a major concern in a converter circuit, IAE of SA-PID-2 is more suitable than that of other approaches.

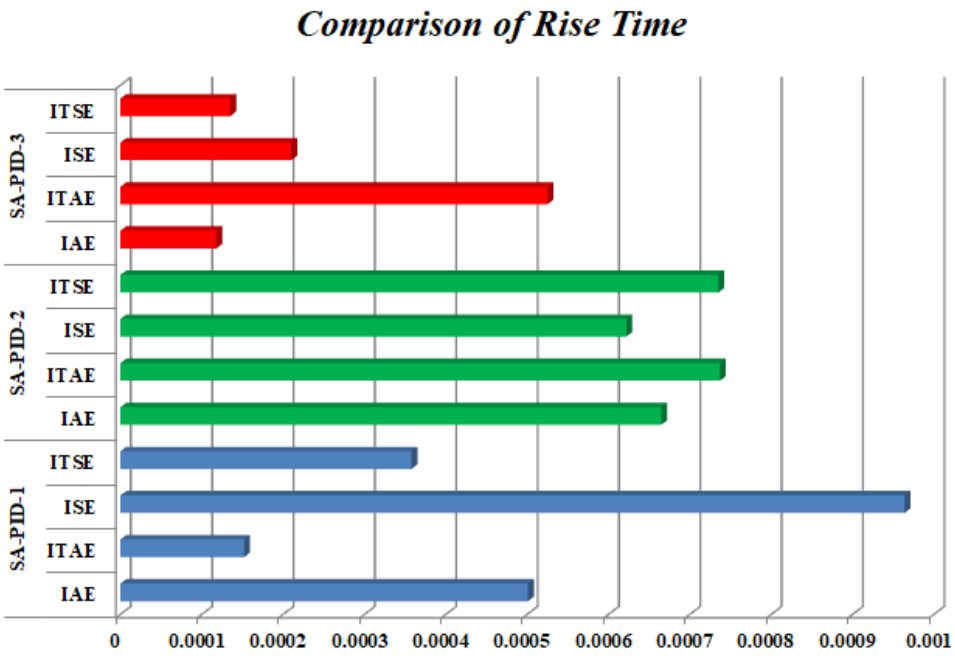


Fig. 5.38. Comparative Analysis of rise time (Tr) for SA based PID Controllers.

In Fig. 5.38, comparative analysis, it is observed for each of the cases of SA based PID controller. The graphical illustration depicts that rise time is least for IAE of SA-PID-3 than that of other performance indices.

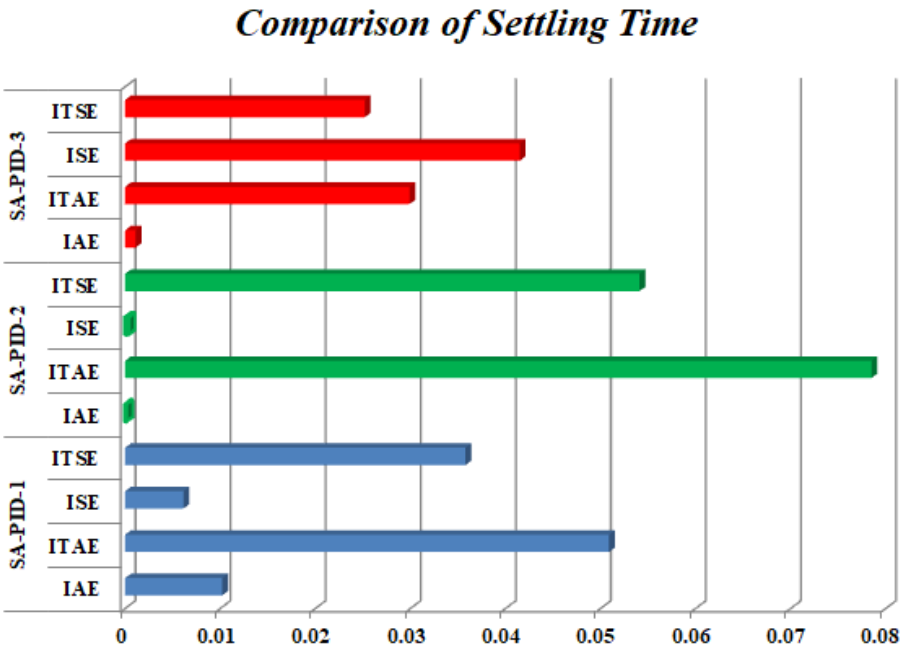


Fig. 5.39. Comparative Analysis of settling time (Ts) for SA based PID Controllers.

From Fig. 5.39, it is evident that IAE of SA-PID-2 shows the most rapid settling time than other performance indices. However, ISE of SA-PID-2 and ISE of SA-PID-3 show quick settling time too. However, settling time is larger for ITAE of SA-PID-2.

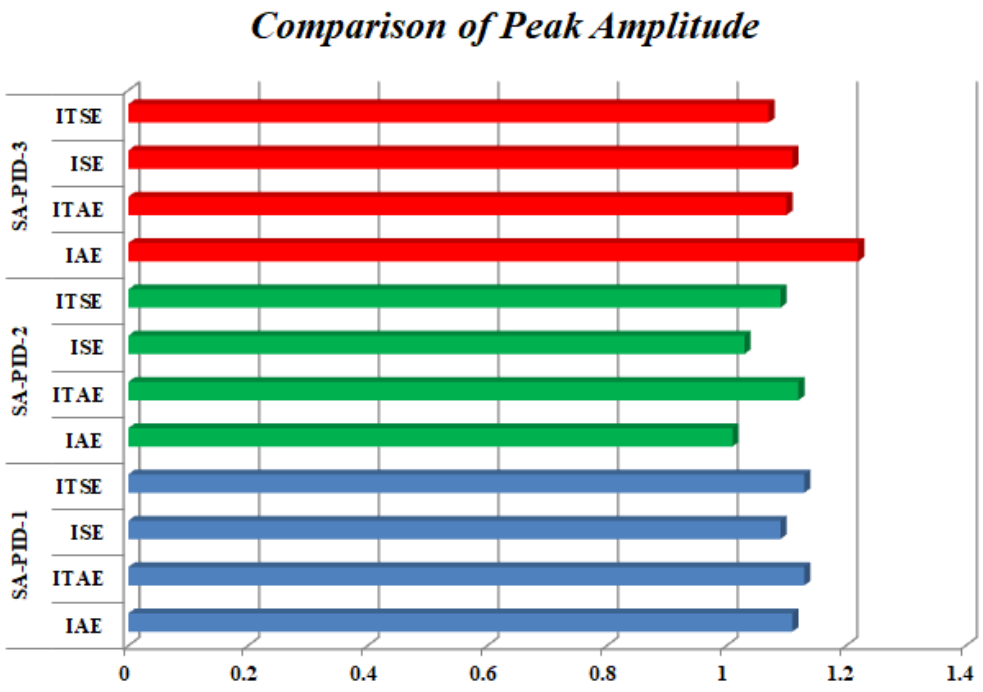


Fig. 5.40. Comparative Analysis of peak amplitude for SA based PID Controllers.

In Fig. 5.40, it is shown that IAE of SA-PID-2 has the lowest peak amplitude than other approaches which ultimately leads to less steady state error.

So, it is observed that among all the performance indices of all the three approaches of SA based PID controller, IAE of SA-PID-2 is the most optimized design of the controller. Because, the overshoot is the minimum (2.2%), settling time is rapid (0.000104s) and peak amplitude is 1.01 which leads to less steady state error. Though it takes slightly more time to rise (0.000665s), it is in acceptable limit. So, IAE of SA-PID is the most optimized approach among all SA based PID controllers.

5.7 Transfer Function and Pole-Zero Mapping:

To carry out the simulation for each of cases of GA and SA based controller, transfer functions are derived and corresponding responses are taken. After that, the map of the pole-zero are illustrated. The concept of pole-zero mapping is important to elaborate the idea of the responses obtained for each of the cases. For example, overdamped response is

obtained from the second order system when two poles are real whereas if the two poles are complex then it will showcase underdamped response. However, undamped responses will be attained when the poles are imaginary and critically damped response is obtained when the two poles are equal and realIn this section, transfer function and pole-zero mapping for GA and SA are depicted for IAE, ITAE, ISE and ITSE.

5.7.1 GA Based Controller:

The transfer functions for all the fitness functions of the GA based controllers are shown in Table 5.21

Table 5.21 Transfer Functions for all GA based PID controllers

GA-PID-1	**IAE**	$\frac{0.035s^3+1.67\times10^4 s^2+4.22\times10^7 s+3.711\times10^{10}}{1.035s^3+1.709\times10^4 s^2+4.39\times10^7 s+3.711\times10^{10}}$
	ITAE	$\frac{0.017s^3+8380s^2+2.87\times10^7 s+4.27\times10^{10}}{1.018s^3+8743s^2+3.037\times10^7 s+4.27\times10^{10}}$
	ISE	$\frac{0.035s^3+1.67\times10^4 s^2+4.47\times10^7 s+4.85\times10^{10}}{1.035s^3+1.71\times10^4 s^2+4.63\times10^7 s+4.858\times10^{10}}$
	ITSE	$\frac{0.0175s^3+8388s^2+3.22\times10^7 s+5.29\times10^{10}}{1.018s^3+8751s^2+3.39\times10^7 s+5.29\times10^{10}}$
GA-PID-2	**IAE**	$\frac{0.0348s^3+1.65\times10^4 s^2+4.67\times10^7 s+4.65\times10^{10}}{1.035s^3+1.693\times10^4 s^2+4.843\times10^7 s+4.672\times10^{10}}$
	ITAE	$\frac{0.0189s^3+9049s^2+3.023\times10^7 s+4.013\times10^{10}}{1.019s^3+9412s^2+3.19\times10^7 s+4.013\times10^{10}}$
	ISE	$\frac{0.035s^3+1.675\times10^4 s^2+5.217\times10^7 s+5.158\times10^{10}}{1.035s^3+1.711\times10^4 s^2+5.439\times10^7 s+5.158\times10^{10}}$
	ITSE	$\frac{0.0165s^3+7878s^2+2.72\times10^7 s+3.801\times10^{10}}{1.017s^3+8241s^2+2.88\times10^7 s+3.801\times10^{10}}$
GA-PID-3	**IAE**	$\frac{0.035s^3+1.67\times10^4 s^2+4.86\times10^7 s+4.67\times10^{10}}{1.035s^3+1.711\times10^4 s^2+5.02\times10^7 s+4.67\times10^{10}}$
	ITAE	$\frac{0.017s^3+8390s^2+3.34\times10^7 s+5.24\times10^{10}}{1.018s^3+8753s^2+3.50\times10^7 s+5.2\times10^{10}}$
	ISE	$\frac{0.035s^3+1.67\times10^4 s^2+4.05\times10^7 s+2.99\times10^{10}}{1.035s^3+1.709\times10^4 s^2+4.22\times10^7 s+2.99\times10^{10}}$
	ITSE	$\frac{0.017s^3+8384s^2+3.04\times10^7 s+4.79\times10^{10}}{1.018s^3+8747s^2+3.207\times10^7 s+4.79\times10^{10}}$

The pole-zero mappings for all the fitness functions of GA-PID-1 are presented in Fig. 5.41

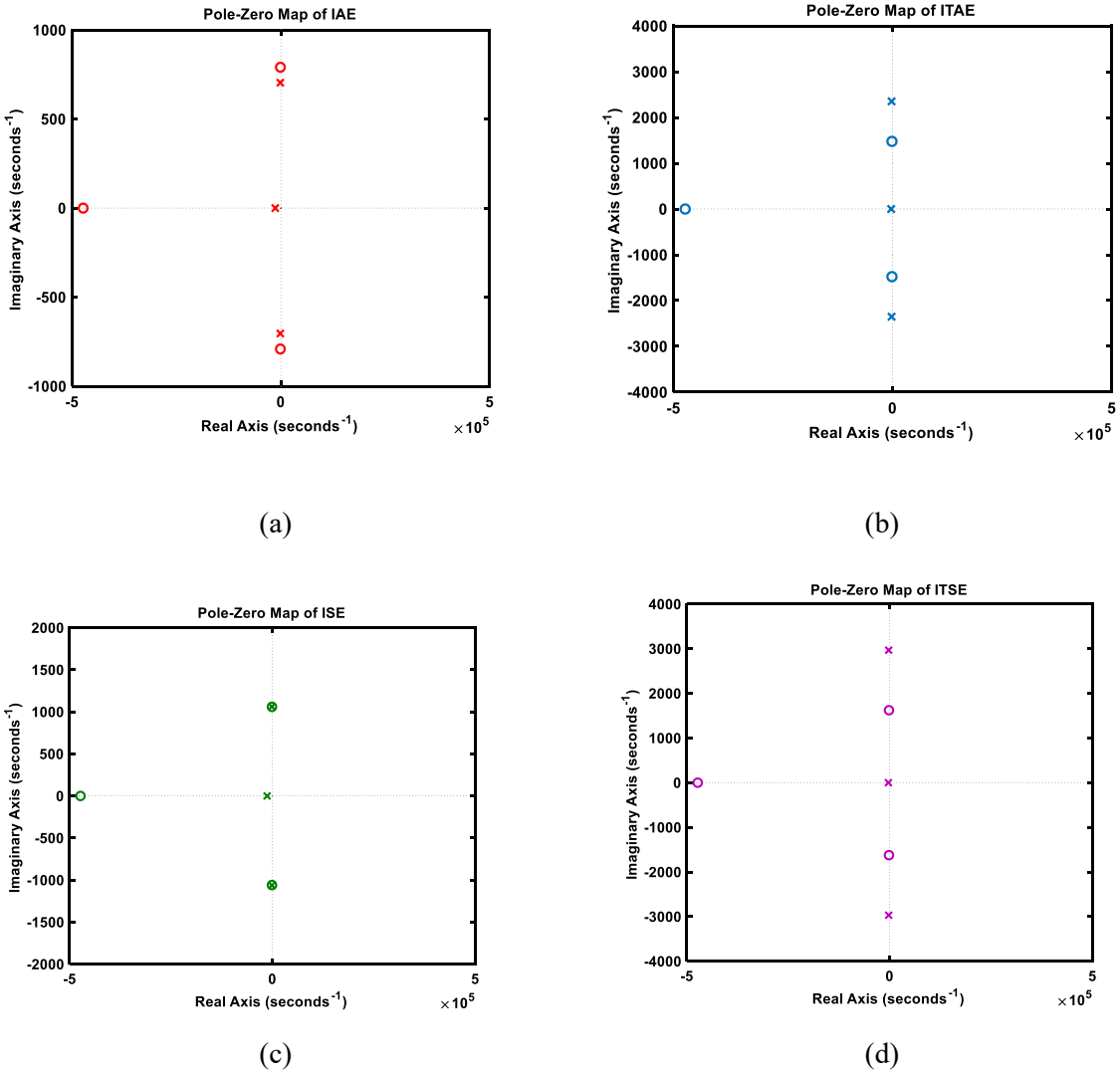


Fig. 5.41 Pole Zero Mapping for (a) IAE (b) ITAE (c) ISE (d) ITSE of GA-PID-1

The pole-zero mappings for all the fitness functions of GA-PID-2 are illustrated in Fig. 5.42

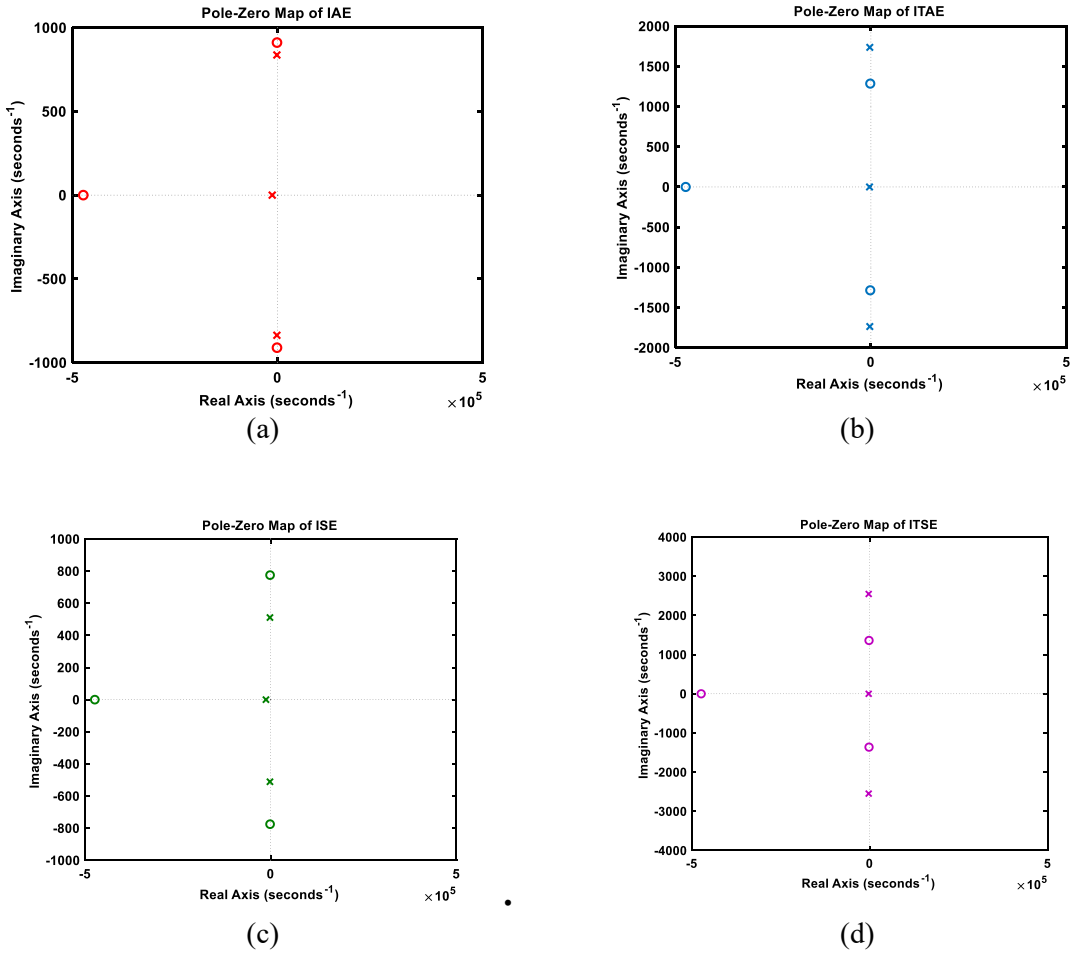


Fig. 5.42 Pole Zero Mapping for (a) IAE (b) ITAE (c) ISE (d) ITSE of GA-PID-2

The pole-zero mappings for all the fitness functions of GA-PID-3 are illustrated in Fig. 5.43

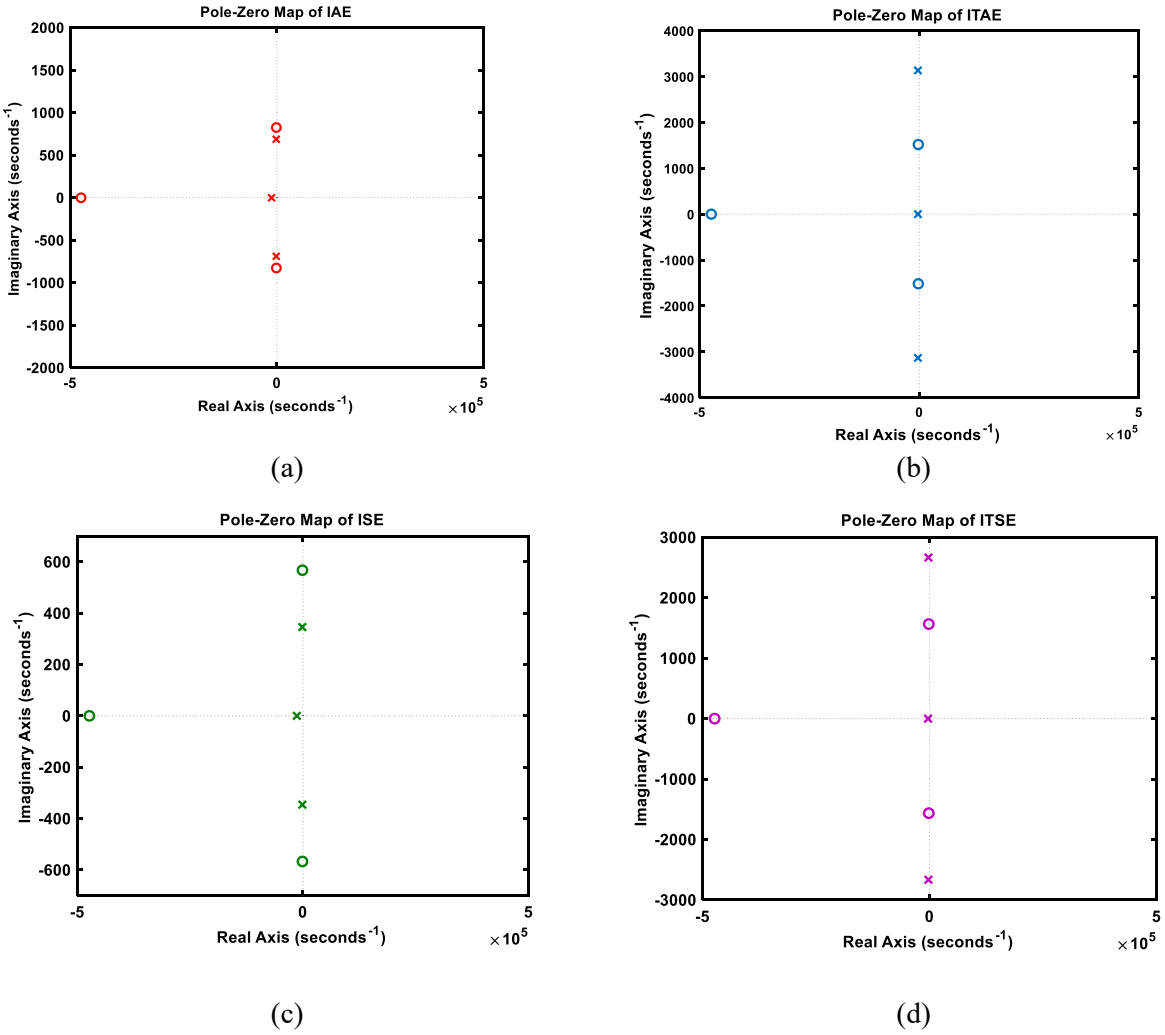


Fig. 5.43 Pole Zero Mapping for (a) IAE (b) ITAE (c) ISE (d) ITSE of GA-PID-3

The values of pole-zero mappings for all the fitness functions of GA based PID controllers are illustrated in Table 5.22

Table 5.22 Values of pole and zero for all GA based PID controllers

Nonlinear Controller	Objective Function	Pole	Zero
GA-PID-1	**IAE**	$-1.46\times10^{3}\pm704i$ -1.36×10^{4}	-4.73×10^{5} $-1.27\times10^{3}\pm791i$
	ITAE	$-2.55\times10^{3}\pm2.35\times10^{3}i$ -3.49×10^{3}	$-1.72\times10^{3}\pm1.48\times10^{3}i$ -4.73×10^{5}
	ISE	$-1.34\times10^{3}\pm1.06\times10^{3}i$ -1.34×10^{4}	-4.73×10^{5} $-1.34\times10^{3}\pm1.06\times10^{3}i$
	ITSE	$-2.66\times10^{3}\pm2.97\times10^{3}i$ -3.27×10^{3}	$-1.93\times10^{3}\pm1.62\times10^{3}i$ -4.73×10^{5}
GA-PID-2	**IAE**	$-1.66\times10^{3}\pm837i$ -1.3×10^{4}	$-1.42\times10^{3}\pm911i$ -4.73×10^{5}
	ITAE	$-2.85\times10^{3}\pm1.74\times10^{3}i$ -3.53×10^{3}	$-1.68\times10^{3}\pm1.29\times10^{3}i$ -4.73×10^{5}
	ISE	$-1.91\times10^{3}\pm511i$ -1.27×10^{4}	$-1.58\times10^{3}\pm775i$ -4.73×10^{5}
	ITSE	$-2.69\times10^{3}\pm2.55\times10^{3}i$ -2.72×10^{3}	$-1.73\times10^{3}\pm1.36\times10^{3}i$ -4.73×10^{5}
GA-PID-3	**IAE**	$-1.73\times10^{3}\pm688i$ -1.31×10^{4}	-4.73×10^{5} $-1.46\times10^{3}\pm826i$
	ITAE	$-2.87\times10^{3}\pm3.13\times10^{3}i$ -2.85×10^{3}	$-2\times10^{3}\pm1.52\times10^{3}i$ -4.73×10^{5}
	ISE	$-1.41\times10^{3}\pm346i$ -1.37×10^{4}	$-1.22\times10^{3}\pm567i$ -4.73×10^{5}
	ITSE	$-2.6\times10^{3}\pm2.67\times10^{3}i$ -3.4×10^{3}	-4.73×10^{5} $-1.82\times10^{3}\pm1.56\times10^{3}i$

5.7.2 SA Based Controller:

The transfer functions for all the fitness functions of the SA based controllers are shown in Table 5.23

Table 5.23 Transfer Functions for all SA based PID controllers

SA-PID-1	**IAE**	$\frac{0.00703s^3+3329s^2+6.371\times10^5 s+6.96\times10^8}{1.007s^3+3692s^2+2.30\times10^6 s+6.96\times10^8}$
	ITAE	$\frac{0.00351s^3+1664s^2+1.992\times10^5 s+5.58\times10^8}{1.004s^3+2027s^2+1.87\times10^6 s+5.58\times10^8}$
	ISE	$\frac{0.035s^3+1.67\times10^4 s^2+5.99\times10^7 s+2.81\times10^8}{1.035s^3+1.71\times10^4 s^2+6.15\times10^7 s+2.81\times10^8}$
	ITSE	$\frac{0.021s^3+9985s^2+2.71\times10^5 s+1.057\times10^8}{1.021s^3+1.035\times10^4 s^2+1.94\times10^6 s+1.057\times10^8}$
SA-PID-2	**IAE**	$\frac{0.3515s^3+1.66\times10^5 s^2+3.96\times10^7 s+1.67\times10^9}{1.35s^3+1.668\times10^5 s^2+4.13\times10^7 s+1.67\times10^9}$
	ITAE	$\frac{0.00351s^3+1665s^2+6.107\times10^5 s+7.757\times10^8}{1.004s^3+2028s^2+2.28\times10^6 s+7.75\times10^8}$
	ISE	$\frac{0.703s^3+3.329\times10^5 s^2+6.60\times10^7 s+3.34\times10^9}{1.703s^3+3.33\times10^5 s^2+6.77\times10^7 s+3.34\times10^9}$
	ITSE	$\frac{0.0035s^3+1667s^2+1.40\times10^6 s+1.54\times10^9}{1.004s^3+2030s^2+3.07\times10^6 s+1.54\times10^9}$
SA-PID-3	**IAE**	$\frac{0.03163s^3+1.498\times10^4 s^2+1.42\times10^6 s+1.60\times10^9}{1.032s^3+1.534\times10^4 s^2+3.097\times10^6 s+1.602\times10^9}$
	ITAE	$\frac{0.0035s^3+1665s^2+5.41\times10^5 s+8.89\times10^8}{1.004s^3+2028s^2+2.212\times10^6 s+8.89\times10^8}$
	ISE	$\frac{0.0351s^3+1.66\times10^4 s^2+5.69\times10^6 s+2.65\times10^9}{1.032s^3+1.701\times10^4 s^2+7.364\times10^6 s+2.65\times10^9}$
	ITSE	$\frac{0.0035s^3+1668s^2+1.94\times10^6 s+1.94\times10^9}{1.004s^3+2031s^2+3.62\times10^6 s+1.94\times10^9}$

The pole-zero mappings for all the fitness functions of SA-PID-1 are presented in Fig. 5.44

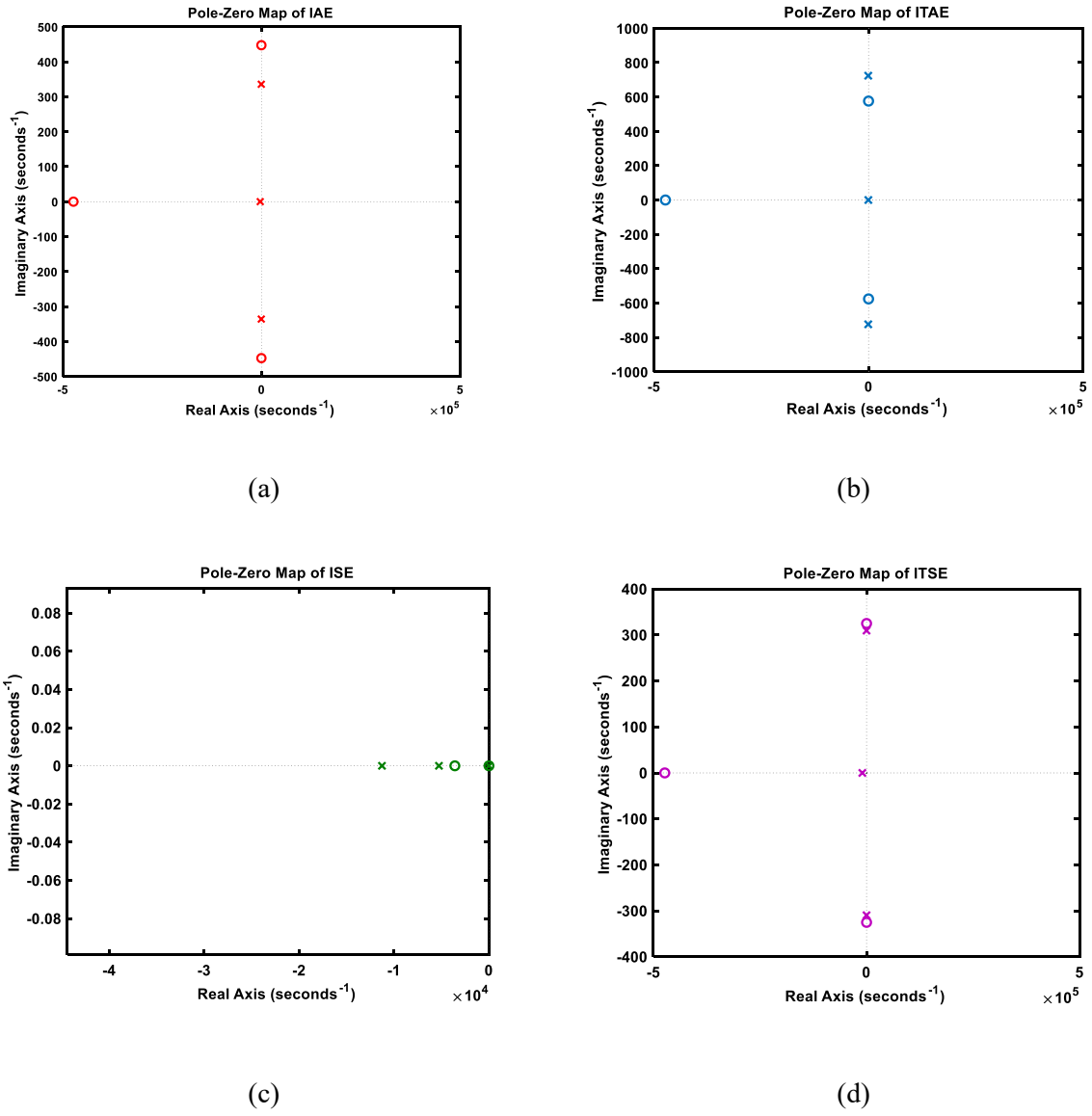


Fig. 5.44 Pole Zero Mapping for SA-PID-1 (a) IAE (b) ITAE (c) ISE (d) ITSE

The pole-zero mappings for all the fitness functions of SA-PID-2 are presented in Fig. 5.45

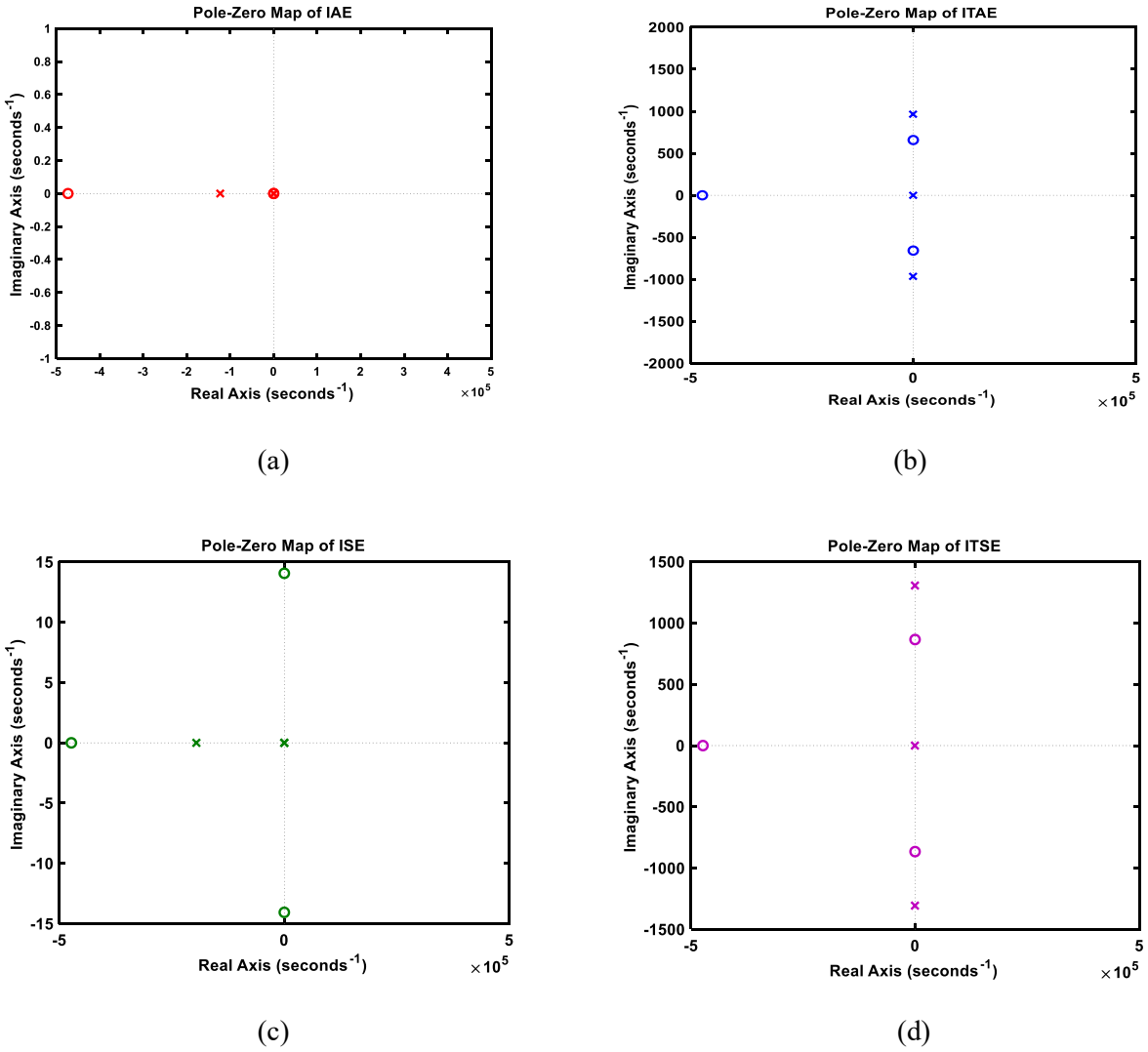


Fig. 5.45 Pole Zero Mapping of (a) IAE (b) ITAE (c) ISE (d) ITSE for SA-PID-2

The pole-zero mappings for all the fitness functions of SA-PID-3 are presented in Fig. 5.46

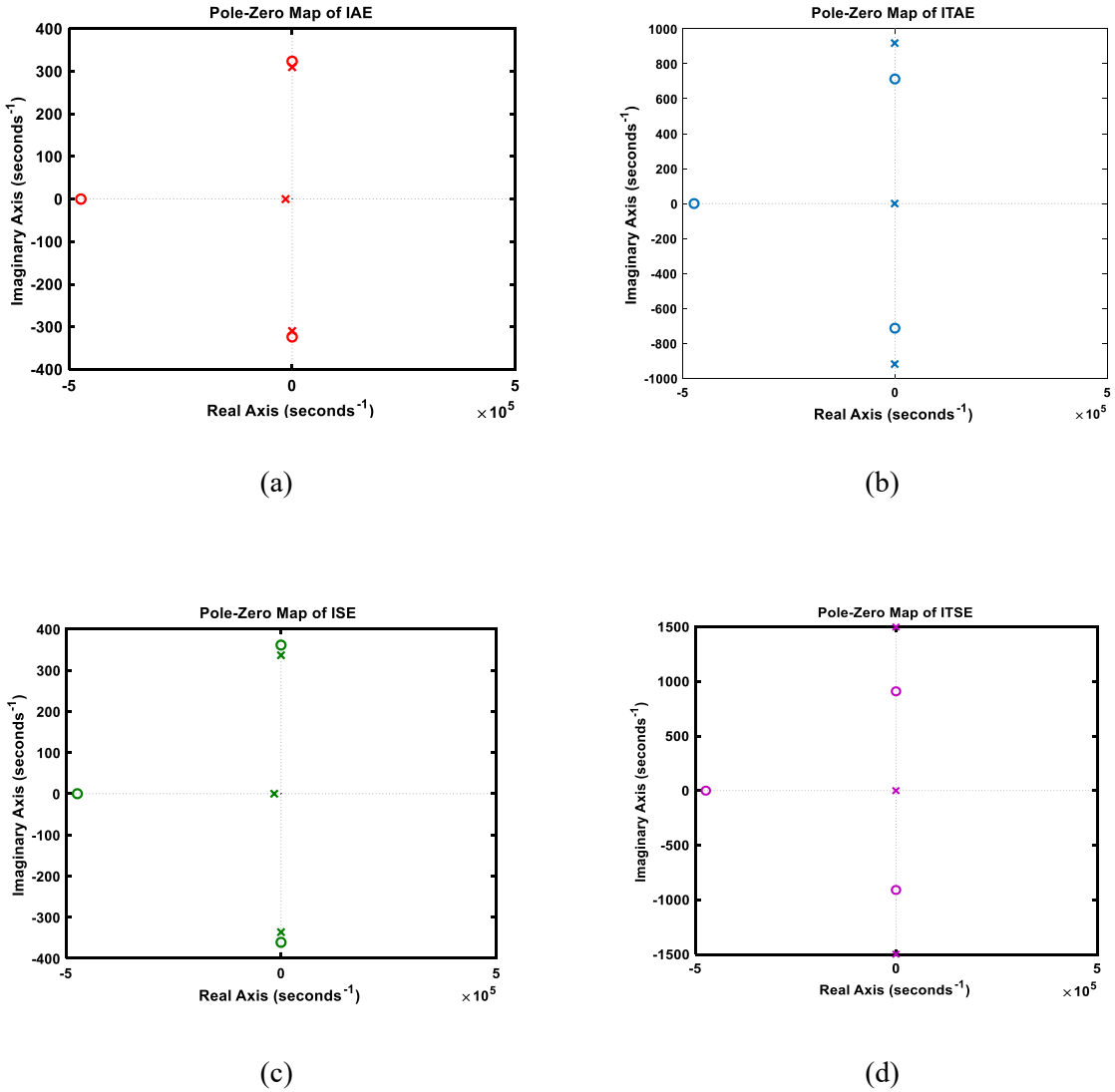


Fig. 5.46 Pole Zero Mapping of (a) IAE (b) ITAE (c) ISE (d) ITSE for SA-PID-3

The values of pole-zero mappings for all the fitness functions of SA based PID controllers are illustrated in Table 5.23

Table 5.23 Values of pole and zero for all SA based PID controllers

Nonlinear Controller	Objective Function	Pole	Zero
SA-PID-1	**IAE**	-2.97×10^{3} $-346\pm336i$	$-95.5\pm448i$ -4.73×10^{5}
	ITAE	-507 $-756\pm724i$	-4.73×10^{5} $-59.5\pm576i$
	ISE	-1.0×10^{4} -0.5×10^{4} 0	3.6×10^{3} -4.73×10^{5} 0
	ITSE	-9.95×10^{3} $-90.4\pm310i$	$-13.5\pm325i$ -4.73×10^{5}
SA-PID-2	**IAE**	-1.23×10^{5} -48 -190	-183 -50 -4.73×10^{5}
	ITAE	$-752\pm965i$ -516	-4.73×10^{5} $-183\times10^{3}\pm658i$
	ISE	-1.96×10^{5} -84.4 -120	-4.73×10^{5} $-99.3\pm14.1i$
	ITSE	$-650\times1.31\times10^{3}i$ -722	-4.73×10^{5} $-422\pm865i$
SA-PID-3	**IAE**	$-98.7\pm310i$ -1.47×10^{4}	-4.73×10^{5} $-47.5\pm324i$
	ITAE	$-666\pm918i$ -689	$-162\pm713i$ -4.73×10^{5}
	ISE	$-217\pm336i$ -1.6×10^{4}	$-171\pm361i$ -4.73×10^{5}
	ITSE	$-104\pm324i$ -1.62×10^{4}	$-58.4\pm337i$ -4.73×10^{5}

5.8 Overall Comparative Analysis:

The overall comparative analysis between all the GA and SA based controllers are presented in this section. With a view to designing a stable and robust system, less overshoot, quick rise and settling time and less peak amplitude are desirable. For this reason, three types of investigation is done for each algorithm. Hence, all the values of the performance parameters are tabulated and plotted. After carrying out the graphical analysis, it is observed that GA-PID-2 (IAE) is the most optimized controller among all the GA based PID controllers in terms of performance parameters. In this case, overshoot is the lowest (3.43%) and peak amplitude is 1.03. Moreover, rise time (0.000102s) and settling time (0.00418s) are also in acceptable limit. Again, it is observed that GA-PID-2 (ISE) shows quick rise (0.000102s) and settling time (0.000676s) but the overshoot of ISE is 11.3% which much greater than IAE of GA-PID-2. Therefore, GA-PID-2 (IAE) is chosen as the most optimized and suitable controller for SEPIC converter. However, SA-PID-2 (IAE) is the most optimized controller among all other SA based controllers. Here, the value of overshoot is 2.2% and peak amplitude is 1.01. For Rise time and settling time, the values for SA-PID-2 (IAE) are 0.000665s s and 0.000104s respectively which are in acceptable limit. Though SA-PID-3 (IAE) shows quick rise time (0.000118s), the overshoot is high (22.2%). Therefore, SA-PID-2 (IAE) is selected as the most optimized and suitable controller for SEPIC converter.

These two optimized controllers are analyzed according to the fitness function and performance parameters and tabulated in Table 5.25.

Table 5.25 Evaluation of Performance Parameters for GA and SA based PID controller

Performance Parameters	***Nonlinear Techniques***	
	GA	***SA***
%OS	GA-PID-2 (IAE)	SA-PID-2 (IAE)
Tr	GA-PID-2 (ISE)	SA-PID-3 (IAE)
Ts	GA-PID-2 (ISE)	SA-PID-2 (IAE)
Peak Amplitude	GA-PID-2 (IAE)	SA-PID-2 (IAE)

5.9 Effect of Parameter Change on Performance of controller:

The values of the inductors may get changed due to temperature, dust, moist or aging effect. Therefore, the performance of the controller is investigated again by implementing conventional PID controller and nonlinear optimization technique based controllers for changed value of the inductor. If there is a change of 5% in inductor's value, then corresponding closed loop response with conventional PID controller is given below:

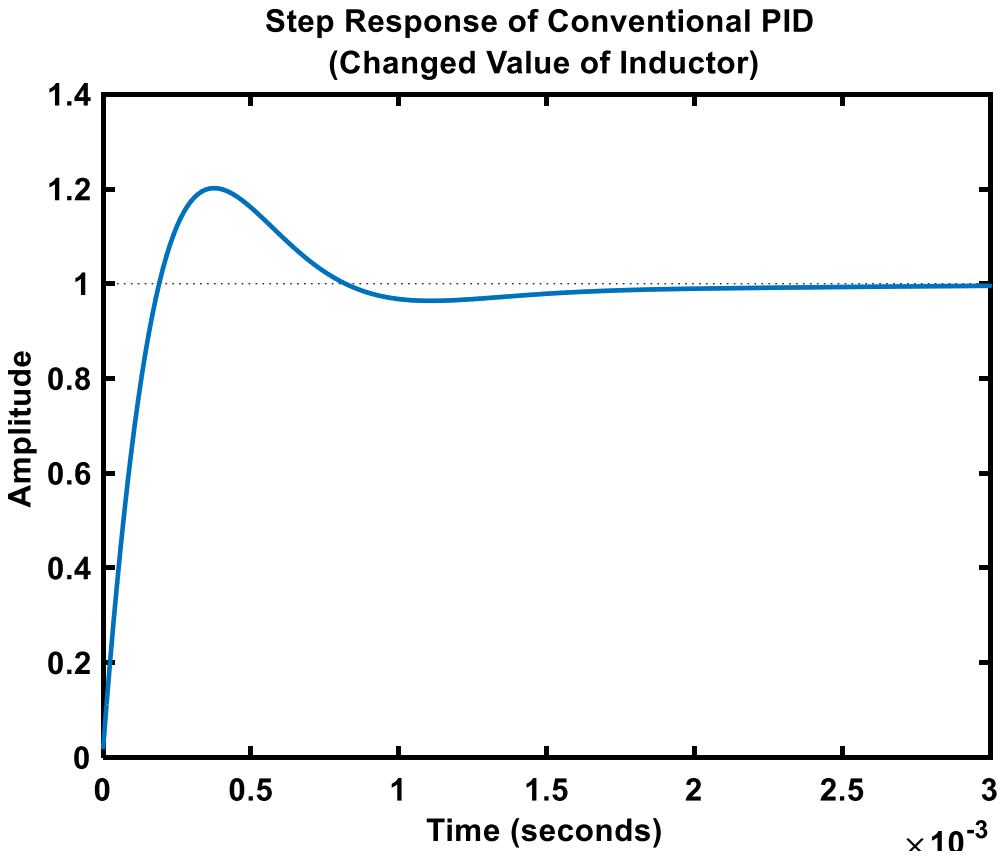


Fig. 5.47 Step Response of Conventional PID for 5% change in inductor's value

From this response, it is observed that the overshoot it is 17.3% which is much greater than previous case (overshoot 11% shown in Fig. 3.10). Now, the response of the system is investigated by employing optimized GA and SA based PID controller. From the earlier section, it is seen that IAE of GA-PID-2 and IAE of SA-PID-2 are the most optimized approach among all. Therefore, this two approaches are taken into account in order to

investigate the performance of the circuit for the changed value of the inductor which is shown in following figure:

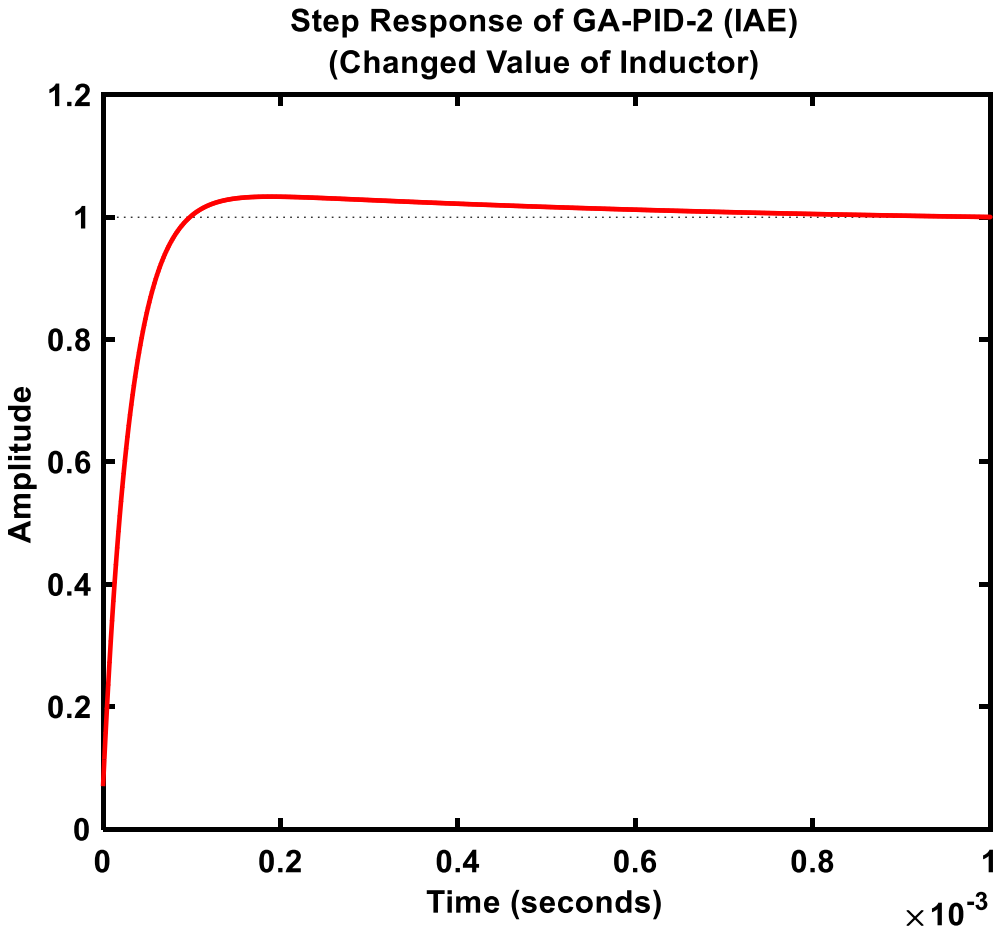


Fig. 5.48 Step Response of GA-PID-2 (IAE) for 5% change in inductor's value

At first, step response of IAE is illustrated in case of GA-PID-2 (Fig. 5.48). For this, rise time is 0.000585 s, settling time is 0.000464 s, overshoot is 3.36% and peak amplitude is 1.03.

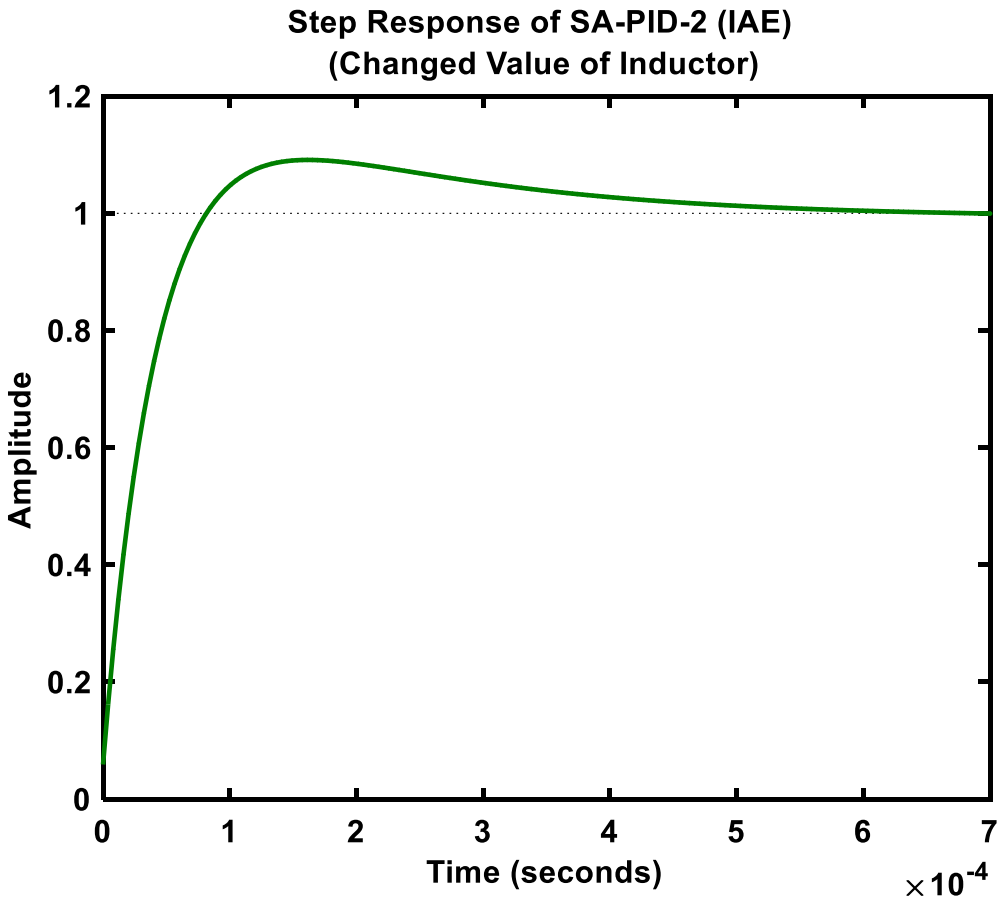


Fig. 5.49 Step Response of SA-PID-2 (IAE) for 5% change in inductor's value

Then, step response of IAE is presented in case of SA-PID-2 (Fig. 5.49). For this, rise time is 0.000570 s, settling time is 0.000453 s, overshoot is 9.12% and peak amplitude is 1.09.

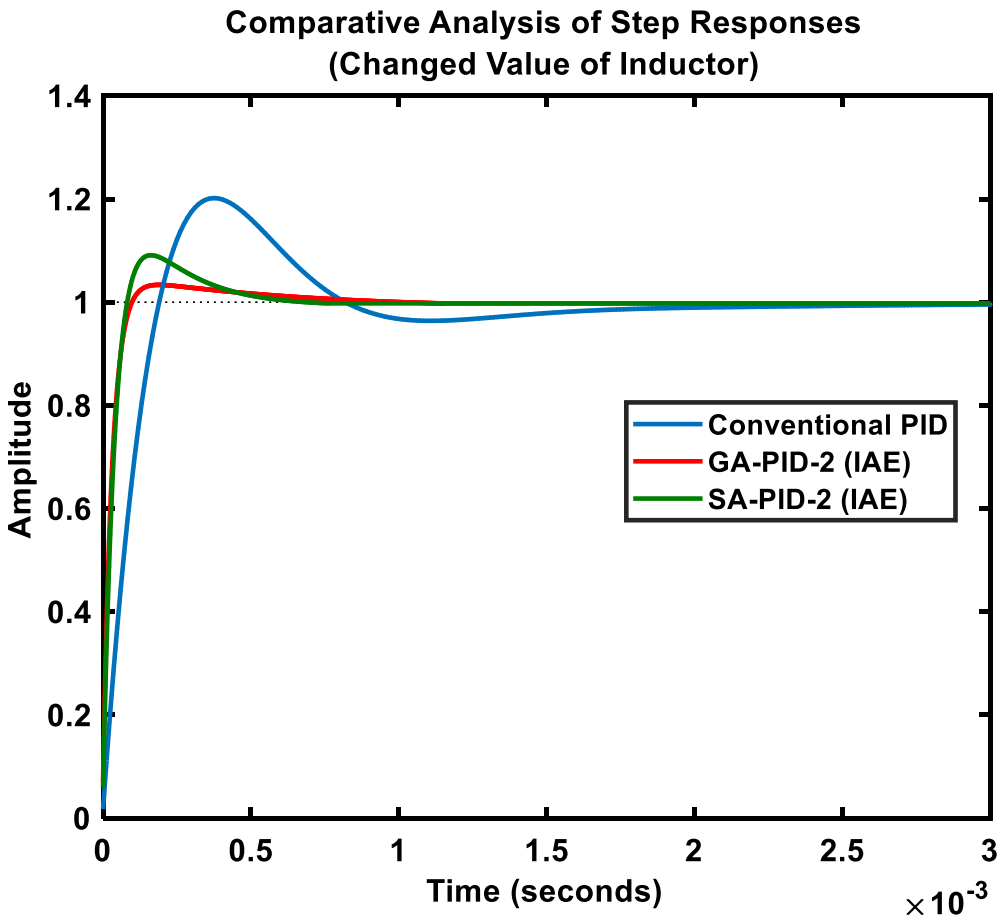


Fig. 5.50 Comparative Analysis of Step Responses of Conventional PID, GA-PID-2 (IAE) and SA-PID-2(IAE) controller for 5% change of inductor's value

After implementing GA-PID-2 (for IAE) and SA-PID-2 (for IAE), it is observed that less overshoot is obtained than conventional PID controller. (overshoot 17.3%) For GA-PID-2, the overshoot is 3.36% and for SA-PID-2 the value is 9.12%. So, it is evident that, nonlinear optimization technique based PID controller is providing more optimized result in case of any change in the value of inductor of the circuit than conventional PID controller. However, GA is more suitable option than SA in terms of designing the controller for less overshoot. Therefore, GA-PID-2 (IAE) is the most optimized controller for SEPIC converter in this investigative study.

CHAPTER 6

CONCLUSION AND FUTURE WORKS

6.1 Synopsis

This thesis focuses on studying and developing nonlinear optimization technique based PID controller for obtaining better performance of SEPIC converter. **In Chapter 2**, different types of existing widely used dc-dc converters have been discussed. The methods and analysis dc-dc converters have also been presented in details. **Chapter 3** has referred to study of conventional SEPIC converter and illustration of State Space Modeling of the converter. Then, open loop and closed loop analysis of the converter has been carried out. **In Chapter 4**, general discussion on different nonlinear optimization techniques were reported. The elaborate discussion on implementation of Genetic Algorithm and Simulated Annealing Algorithm was then depicted where overviews, objective function of the algorithm and design of the optimized PID Controller were stated. **Chapter 5** has been dealt with the simulation results of the nonlinear optimized PID controller for SEPIC converter. The performance parameters were investigated and graphical and comparative analyses were presented.

So, after carrying out the graphical analysis in chapter 5, it is observed that GA-PID-2 (IAE) is the most optimized controller among all the GA based PID controllers in terms of performance parameters. In this case, overshoot is the lowest (3.43%) and peak amplitude is 1.03. Moreover, rise time (0.000102s) and settling time (0.00418s) are also in acceptable limit. Again, it is observed that GA-PID-2 (ISE) shows quick rise (0.000102s) and settling time (0.000676s) but the overshoot of ISE is 11.3% which is much greater than IAE of GA-PID-2. Therefore, GA-PID-2 (IAE) is chosen as the most optimized and suitable controller for SEPIC converter. However, SA-PID-2 (IAE) is the most optimized controller among all other SA based controllers. Here, the value of overshoot is 2.2% and peak amplitude is 1.01. For Rise time and settling time, the values for SA-PID-2 (IAE) are 0.000665s s and 0.000104s respectively which are in acceptable limit. Though SA-PID-3 (IAE) shows quick rise time (0.000118s), the overshoot is high (22.2%). Therefore, SA-PID-2 (IAE) is selected as the most optimized and suitable controller for SEPIC converter. For changed value of inductor, the simulation is done for GA-PID-2 (for IAE) and SA-PID-2 (for IAE), it is observed that less overshoot is obtained than conventional PID controller. (overshoot 17.3%) For GA-PID-2, the overshoot is 3.36% and for SA-PID-2 the

value is 9.12%. So, it is evident that, nonlinear optimization technique based PID controller is providing more optimized result in case of any change in the value of inductor of the circuit than conventional PID controller. However, GA is more suitable option than SA in terms of designing the controller for less overshoot. Therefore, GA-PID-2 (IAE) is the most optimized controller for SEPIC converter in this investigative study.

6.2 Future Work

As future work, Fuzzy Neural Network (FNN) and Particle Swarm Optimization (PSO) will be implemented in designing optimized PID controller in order to investigate and enhance the stability of the SEPIC converter. On top of that, GA and SA can be implemented to enhance the stability for other converters. Thus, the overall comparative analysis can be carried out in a broader perspective and more stable system can be attained for different applications in power electronics. Furthermore, hardware implementation will be performed to validate and inspect the simulation results.

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