# VOLTAGE CONVERSION TECHNIQUES: DESIGN AND ANALYSIS OF HIGH GAIN HYBRID DC-DC CONVERTER USING SC-SL COMBINED STRUCTURES 

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## Abstract

## Voltage Conversion Techniques: Design and Analysis of High Gain Hybrid DC-DC Converter Using SC-SL Combined Structures

DC-DC Converter plays an important role in power electronic systems for renewable energy applications. Numerous literatures have been dedicated to improving the voltage gain of DC-DC power converters that employs various voltage boosting techniques such as using voltage multiplier cell, switched capacitor (SC), switched inductor (SL) and magnetic coupling to name a few. The objective of this work is to present and analyze two new hybrid structure that is a simultaneous combination of SC and SL structures working together to provide superior gain compared to any existing voltage up and down structure alone. The proposed structure for step up voltage conversion is applied to Zeta converter to produce a hybrid high step up Zeta converter and the proposed structure for step down voltage conversion is applied to a Ćuk converter which resulted in a hybrid high step down Ćuk converter. Both of the designed converter circuits were able to provide a theoretical and simulated voltage gain ratio up to 35 times using only one active switch and without exceeding the pulse-width modulation (PWM) duty cycle ratio of 0.9 for step up conversion and without going below 0.1 for step down conversion. Working principles of the proposed converters were described in detail and their steady state analysis in continuous conduction mode (CCM) was done to derive expressions for voltage gain, current flow through individual components, voltage and current stress on the switch and diodes. Efficiency analysis was made to derive expressions for power loss in diodes, capacitors, inductors and switch which in turn provided the total power loss and conversion efficiency of the proposed converter circuits.

## Chapter 1

## Introduction

### 1.1 Background

Power electronic converters find their usage in almost all sorts of electrical and electronic device, data \& telco centers, and renewable energy applications. They can be broadly grouped into four categories: AC-DC rectifiers, DC-AC inverters, AC-AC converters, DC-DC converters. DC-DC converters are further divided into three separate classes known as: buck (step down), boost (step up), buck-boost (step up-down). Power electronic converters provide an efficient and reliable way to convert source voltage levels and various other parameters according to load requirements. They enable us to utilize the generated power efficiently by regulating and altering the parameters of the input or source power and then supplying the output power with desired characteristics which can be used by the connected load. The DC-DC converter family can also be divided into categories such as classical, multi-quadrant, switched component, soft switching, synchronous rectifier and multi element resonant power converter. some voltage boosting techniques have been developed which provide for the large output utilizing a combination of switches and storage elements of the circuits. switched capacitor or charge pump (SC or CP), voltage multiplier, switched inductor and voltage lift (SL \& VL), magnetic coupling, and converters with multistage or multilevel structures. Switched capacitor and switched inductor structures are mainly utilized in building the hybrid DCDC structures that provide both step-up and step-down voltage ratios. DC-DC converters are also classified into several categories depending on their quadrant operations.

### 1.2 Motivation

Rapid advancement in the field of power electronics was made in last few decades and were driven mostly by some key factors. The most important being the increasing push towards the use of sustainable energy technologies and the integration of clean energy generation to limit global warming. Energy distribution systems based on HVDC, flexible AC transmission systems, rise of electric vehicles, fast and compact charging requirement were also some important driving factors. The improvement in battery storage technology means that more batteries are being used which in turn increases the demand of DC-DC power converters to make use of the batteries which stores voltage at a lower voltage level than load requirement. While using renewable energy sources the use of DCDC converter becomes obvious due to the fact that the generation voltage, storage battery voltage, and the distribution voltage levels are rarely the same. Energy from renewable sources are first stored in batteries which has a voltage level in the range of 12-48V DC. This voltage is then stepped up to a level of $350-400 \mathrm{~V}$ DC which is more convenient for transmission and distribution using power converters. Almost every electronic device or appliances used in our daily life that we take for granted have some form of power electronic circuitry in use. They could be inside a coffee maker, a medical instrument or a military equipment. Power electronic converters can take the form of an external power supply, mobile phone charger or they could be embedded inside the mobile phone itself. Wide use of the DC-DC converters makes their development to produce improved design with higher gain, better reliability and efficiency more important than ever.

### 1.3 Objective

Design a Hybrid DC-DC converter circuit with high step-up conversion based on Zeta topology:

- Use switched capacitor and switched inductor structure
- Modify and combine structures for highest voltage gain ratio
- Describe working principle of the proposed topology

Design a Hybrid DC-DC converter circuit with high step-down conversion based on Ćuk topology:

- Use switched capacitor and switched inductor structure
- Modify and combine structures for highest voltage gain ratio
- Describe working principle of the proposed topology

Perform mathematical analysis of the proposed circuits:

- Apply steady state analysis in continuous conduction mode (CCM)
- Derive expression for DC voltage gain
- Analysis of currents through each component
- Current stress analysis
- Voltage stress analysis
- Power loss and efficiency analysis

Simulation and validation of results:

- Compare between theoretical result and simulated result
- Compare obtained voltage gain between existing converter circuits
- Obtain the load regulation and voltage regulation characteristic
- Make conclusion based on the overall performance of the designed DC-DC converters.


## Chapter 2

## Brief Analysis of DC-DC Converter

### 2.1 Introduction

DC/DC converter technology is an important subject area in the field of power engineering and drives and is widely used in industrial applications and computer hardware circuits. A DC to DC converter is an electronic circuit which by electronic switching transforms a DC source voltage from one level to another.

The DC-DC converter is an electrical circuit that transfers energy from a DC voltage source to a load. Electronic switches transfer energy to the energy storage devices and then subsequently switched from storage into the load. The switches are transistors and diodes; the storage devices are inductors and capacitors (Fig 2.1). This process of energy transfer results in an output voltage that is related to the input voltage by the duty ratios of the switches.


Fig 2.1: Energy Storage Device L1 \& C1 in a DC-DC Converter
DC-DC converters use high-frequency switching and inductors, transformers, and capacitors to smooth out switching noise into regulated DC voltages.
Closed feedback loops (Fig. 2.2) maintain constant voltage output. They are generally much more efficient and smaller than linear regulators.

### 2.2 Historical Review

DC/DC converters have been under rapid development for seven decades since the 1940s. In the 1940s, the buck converter was derived from the "A"-type chopper. The boost converter was derived later from the " B "-type chopper. The buck-boost converter was invented after buck converter and boost converter, and its output voltage is negative.


Fig 2.2: Basic Block Diagram of DC-DC Converter
The 1980s and 1990s are the decades called the "DC/DC conversion prosperous decades." Hundreds of DC/DC converters were invented during this period, such as Ćuk converter, single ended primary inductance converter (SEPIC), Luo converters, and soft-switching converters. Extending the developing impetus, many new types of DC/DC converters followed, such as superlift (SL) Luo-converters, cascaded boost converters, switched-capacitor converters, and synchronous rectifier (SR) converters [1].

### 2.3 DC-DC Converter Family Tree

There are more than 800 topologies of DC/DC converters existing. There is a DC-DC converter family tree, which categorized all prototypes and defined the characteristics of all the existing prototypes [1].





Fig 2.3: DC-DC Converter Family Tree [1]

### 2.4 Development of DC-DC Conversion Techniques

DC-DC conversion techniques have undergone rapid development in recent decades. All existing prototypes of DC/DC converters are categorized into six generations in [Advanced DC/DC Converter]:

- First-generation (classical/traditional) converters
- Second-generation (multi-quadrant) converters
- Third-generation (switched-component: SI/SC) converters
- Fourth-generation (soft-switching: ZCS/ZVS/zero-transition [ZT]) converters
- Fifth-generation $(S R)$ converters
- Sixth-generation (multiple-energy-storage-element resonant [MER]) converters


### 2.4.1 Classical Converters

Classical converters perform in a single-quadrant mode and in a low power range (up to around 100 W ). Since their development lasts a long time, they have, briefly, five categories:
A. Fundamental converters
B. Transformer-type converters
C. Developed converters
D. Voltage-lift (VL) converters
E. Super-Lift (SL) converters

## A. Fundamental converters:

Three types of fundamental DC/DC topologies were constructed: buck converter, boost converter, and buck-boost converter. They can be derived from single-quadrant operation choppers.


Fig 2.4: Conventional Buck Converter circuit diagram

## Buck Converter:

Buck converter is a step-down DC/DC converter in (Fig 2.4) which works in firstquadrant. It can be derived from quadrant I chopper. The diode is replaced with a second

Transistor in modern Buck converter. There is at least one energy storage element. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=\frac{t_{o n}}{T} V_{i n}=D V_{i n} \tag{2.1}
\end{equation*}
$$

## Boost Converter:

Boost converter is a step-up DC/DC converter in (Fig 2.5). It works in second-quadrant operation. It can be derived from quadrant II chopper. A filter is added to the output to reduce voltage ripple. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=\frac{T}{T-t_{o n}} V_{i n}=\frac{1}{1-D} V_{i n} \tag{2.2}
\end{equation*}
$$



Fig 2.5: Conventional Boost Converter circuit diagram

## Buck-Boost Converter:

Buck-boost converter is a step-down/step-up DC/DC converter. It works in thirdquadrant operation. There are Two Topology for buck boost converter. The inverting topology and the 4 Switch topology. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=\frac{t_{o n}}{T-t_{o n}} V_{i n}=\frac{D}{1-D} V_{i n} \tag{2.3}
\end{equation*}
$$



Fig 2.6: Conventional Buck Boost Converter circuit diagram

## B. Transformer-type converters:

There is a linkage between the input side and the output side in the Fundamental DC/DC converters. That's why the voltage transfer gain is comparably low. To remove this problem one transformer is introduced in between. There are large number of converters such as forward converter. push-pull converter, flyback converter, half-bridge converter, bridge converter, and Zeta (or ZETA) converter use transformers.

## Forward converter:

Forward converter in (Fig 2.7) is a transformer-type buck converter with the turns ratio $N$, which works in first quadrant operation. Some industrial applications require multiple outputs. For this requirement there are multiple secondary windings and the corresponding conversion circuit available. The output voltage is calculated by the formula:


Fig 2.7: Forward Converter circuit diagram.

## Push-Pull Converter:

Boost converter works in a push-pull state, which effectively avoids the iron core saturation. A simple Push-Pull Converter with fixed $50 \%$ duty cycle is often used as a low noise transformer driver and distributed power supplies. There are two switches in the converter working alternatively. For this reason, the output voltage is doubled. The circuit diagram is depicted in (Fig 2.8). The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=2 D N V_{i n} \tag{2.5}
\end{equation*}
$$



Fig 2.8: Push Pull Converter circuit diagram.

## Fly-back Converter:

Fly-back converter in (Fig 2.9) is a transformer-type converter using the demagnetizing effect. The Fly-back converter is a buck boost converter with the inductor is replaced by a transformer. So the voltage ratios are multiplied with an additional advantages of isolation. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} N V_{i n} \tag{2.6}
\end{equation*}
$$



Fig 2.9: Fly Back Converter circuit diagram.

## Half-Bridge Converter:

The half-bridge converter was constructed to reduce the primary side in one winding by replacing the center tapped transformer with traditional transformer.
It removes the Flux Unbalanced problem of the Push Pull Converter. It uses two input switches to control the output. And it also uses two sets of diodes and two bulk capacitors which increases the efficiencies to the $90 \%$ range. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=D N V_{i n} \tag{2.7}
\end{equation*}
$$



Fig 2.10: Half Bridge Converter circuit diagram.

## Full-Bridge Converter:

Bridge converter is a DC - DC converter which employs four active switching components in a bridge configuration for control the output voltage. Therefore, gains of this converter is double. It also provides multiple output voltages simultaneously. The output voltage is calculated by the formula:

$$
\begin{equation*}
V_{o}=2 D N V_{i n} \tag{2.8}
\end{equation*}
$$



Fig 2.11: Full Bridge Converter circuit diagram.

## C. Developed converters:

In order to overcome the second fault of the fundamental DC/DC converters, Developedtype converters add a low-pass filter to reduce the output voltage ripple. The typical converters are Positive Output Luo-converter, negative-output Luo-converter, doubleoutput Luo-converter, Ćuk converter, SEPIC, and Watkins-Johnson converter. Developed converters can obtain output voltage higher or lower than the input voltage which means these converters can act as buck boost converter.

## Positive Output Luo-converter:

Positive Output ( $\mathrm{P} / 0$ ) Luo-converter is the elementary circuit of the series of new DC-DC step up converters that uses voltage lift technique. It can be derived from buck-boost converter. The output voltage is calculated using formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} V_{i n} \tag{2.9}
\end{equation*}
$$



Fig 2.12: Positive Output Luo Converter circuit diagram

## Negative-output Luo-converter:

Negative-output (N/O) Luo-converter is the elementary circuit which can also be derived from buck-boost converter. The output voltage is calculated using formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} V_{i n} \tag{2.10}
\end{equation*}
$$



Fig 2.13: Negative Output Luo Converter circuit diagram

## Double-output Luo-converter:

In order to obtain mirror symmetrical $\mathrm{P} / \mathrm{O}$ and $\mathrm{N} / \mathrm{O}$ voltage, $\mathrm{D} / \mathrm{O}$ Luo-converter was constructed. D/O Luo-converter is the elementary circuit of the series "D/O Luoconverters." The output voltage is calculated using formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} V_{i n} \tag{2.11}
\end{equation*}
$$

## Ćuk converter:

Ćuk converter is derived from boost converter. It has a output voltage magnitude either greater than or less than the input voltage. The output voltage is calculated using formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} V_{i n} \tag{2.12}
\end{equation*}
$$



Fig 2.14: Ćuk Converter circuit diagram.

## SEPIC Converter:

The SEPIC or single ended primary-inductor converter is a DC-DC converter which can be derived from boost converter. It allows the voltage at its output voltage is greater than, less than or equal to its input. The output voltage is calculated using formula:

$$
\begin{equation*}
V_{o}=\frac{D}{1-D} V_{i n} \tag{2.13}
\end{equation*}
$$



Fig 2.15: SEPIC circuit diagram

## D. Voltage-lift (VL) converters:

VL technique is a good method to lift the output voltage. It is widely applied in electronic circuit design. The voltage lift circuit has been successfully applied to several series of DC-DC converters. Using this Voltage lift method, the output voltage can be easily lifted by tens to hundreds of times. VL converters can be classed into self-lift, re-lift, triple-lift, quadruple-lift, and high-stage-lift converters. Here's an example of self-lift Ćuk Converter in Fig 2.16.


Fig 2.16: Self lift Ćuk Converter circuit diagram.

## E. Super-lift (SL) converters:

VL technique is a popular method that is widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years and has opened a way to design high-voltage-gain converters. Three-series Luo-converters are examples of VL technique implementations. However, the output voltage increases stage by stage just along the arithmetic progression. A novel approach-SL technique-has been developed, which implements the output voltage increasing stage by stage along in geometric progression. It effectively enhances the voltage transfer gain in power law. The typical circuits are sorted into five series: P/O SL Luo-converters, N/O SL Luo-converters, P/O cascaded boost converters, N/O cascaded boost converters, and ultra-lift Luoconverter. Here's an example of Positive Output Super Lift Luo Converter:


Fig 2.17: Positive Output Super Lift Luo Converter Circuit Diagram.

### 2.4.2 Multi-quadrant Converters:

Multiple-quadrant converters perform in two-quadrant operation and four-quadrant operation with medium output power range. The topologies can be sorted into two main categories:

* First are the converters derived from the multiple-quadrant choppers and/or from the first-generation converters and
* Second are constructed with transformers.

Multiple quadrant choppers were employed in industrial applications for a long time. They can be used to implement the DC motor multiple-quadrant operation. These converters are derived from multi-quadrant choppers, for example, class-B converters are derived from B-type choppers and class-E converters are derived from E-type choppers.
$\checkmark$ The class-B converter works in quadrant I and II operation, which corresponds to the forward-running motoring and regenerative braking operation of a DC motor drive.
$\checkmark$ The class-C converter works in quadrant I and VI operation.
$\checkmark$ The class-D converter works in quadrant III and VI operation, which corresponds to the reverse-running motoring and regenerative braking operation of a DC motor drive.
$\checkmark$ The class-E converter works in four-quadrant operation, which corresponds to the four-quadrant operation of a DC motor drive.

Multi-quadrant operation converters can be derived from the first-generation converters. For example, multi-quadrant Luo-converters are derived from P/O Luo-converters and N/O Luo-converters. The transformer-type multi-quadrant converters easily change the current direction by transformer polarity and diode rectifier. The main types of such converters can be derived from the forward converter, half-bridge converter, and bridge converter.


Fig 2.18: Multi-quadrant Luo Converter Circuit Diagram.

### 2.4.3 Switched-component (SI/SC) converters:

The third-generation converters are called switched-component converters and are made of either inductors or capacitors, the so-called switched inductor and switched capacitors. They can perform in two- or four-quadrant operation with high output power range.

## 1. Switched capacitors (SC) converters:

Switched-capacitor DC/DC converters consist of only capacitors. Because there is no inductor in the circuit, their size is small. They have outstanding advantages such as low power losses and low electromagnetic interference. The switched capacitor can be integrated into an integrated chip (IC). Hence, its size is largely reduced. most of the converters in the literature perform a single-quadrant operation. Some of them work in the push-pull status. In addition, their control circuit and topologies are very complex, especially for the large difference between input and output voltages.


Fig 2.19: Positive Output Push Pull Switched Capacitor Luo Converter circuit diagram.

## 2. Multiple-Quadrant Switched-Capacitor Luo-Converters:

Switched-capacitor DC/DC converters consist of only capacitors. Since their power density is very high, they are widely applied in industrial applications. Some industrial applications require multiple-quadrant operation, so multiple-quadrant switchedcapacitor Luo-converters have been developed. There are two-quadrant operation types and four-quadrant operation types.

## 3. Multiple-Lift Push-Pull Switched-Capacitor Converters:

VL technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years and has opened a way to design high voltage- gain converters. Three-series Luo-converters are examples of VL technique implementation. However, the output voltage increases stage by stage just along the arithmetic progression. A novel approach-multiple-lift push-pull technique-has been developed, which implements the output voltage, which increases stage by stage along the arithmetic progression. It
effectively enhances the voltage transfer gain. The typical circuits are sorted into two series: P/O multiple-lift push-pull switched-capacitor Luo-converters and N/O multiple-lift push-pull switched-capacitor Luo-converters.

## 4. Switched-Inductor Converters:

The switched capacitors have many advantages, but their circuits are not simple. If the difference of input and output voltages is large, many capacitors are required. The switched inductor has the outstanding advantage that only one inductor is required for one switched-inductor converter no matter how large the difference between input and output voltages is. This characteristic is very important for large power conversion.


Fig 2.20: Four Quadrant Switched Inductor DC/DC Luo Converter circuit diagram.

### 2.4.4 Soft-switching (ZCS/ZVS) converters:

The fourth-generation DC/DC converters are called soft-switching converters. There are four
types of soft-switching methods:

1. Resonant-switch converters
2. Load-resonant converters
3. Resonant-DC-link converters
4. High-frequency-link integral-half-cycle converters

This resonance method is available for working independently to load. There are three main categories: ZCS, ZVS, and ZT converters. Most topologies usually perform in singlequadrant operation in the literature. Actually, these converters can perform in two- and four-quadrant operation with high output power range.
ZCS and ZVS converters have three resonant states: over-resonance (completed resonance), optimum-resonance (critical resonance), and quasi-resonance (subresonance). Only the quasi-resonance state has two clear zero-cross points in a repeating period.

## 1. ZCS-QRCs:

ZCS-QRC equips resonant circuit in the switch side to keep the switch-on and switch-off at zero current condition. There are two states: full-wave state and half-wave state. Most of the engineers enjoy the half-wave state. This technique has half-wave current resonance waveform with two zero-cross points.


Fig 2.21: DC-DC Zero Current Switching Quasi Resonant Luo Converter for quadrant I and quadrant II

## 2. ZVS-QRCs:

ZVS-QRC equips resonant circuit in the switch side to keep the switch-on and switch-off at zero voltage condition. In Fig 2.22 there are two states: full-wave state and half-wave state. Most of the engineers enjoy the half-wave state. This technique has half-wave voltage resonance waveform with two zero-cross points.


Fig 2.22: DC-DC Zero Voltage Switching Quasi Resonant Luo Converter for quadrant I and quadrant II

## 3. ZT Converters:

Using ZCS-QRC and ZVS-QRC largely reduces the power losses across the switches. Consequently, the switch device power rates become lower and converter power efficiency is increased. However, ZCS-QRC and ZVS-QRC have large current and voltage stresses. Therefore, the device's current and voltage peak rates usually are three to five times higher than the working current and voltage. It is not only costly but also ineffective. ZT technique overcomes this fault. It implements zero-voltage plus ZCS technique without significant current and voltage stresses.


Fig 2.23: Zero-transition DC/DC Luo-converters for quadrant I and quadrant II

### 2.4.5 Synchronous Rectifier Converters or Fifthgeneration converters:

Corresponding to the development of the micro-power consumption technique and highdensity IC manufacture, the power supplies with low output voltage and strong current are widely used in communications, computer equipment, and other industrial applications. Inter-80 computers used the 5 V power supply. In order to increase the memory size and operation speed, large-scale integrated chip technique has been quickly developed. As the amount of IC manufacturing increased, the gaps between the layers became narrower. At the same time, the micropower consumption technique was completed. Therefore, new computers, such as those using Pentium I, II, III, and IV, use a 3.3 V power supply. Future computers will have larger memory and will require lower power supply voltages, for example, $2.5,1.8,1.5$, and even 1.1 V . The fundamental topology is derived from the forward converter. Active-clamped circuit, flat transformers, double-current circuit, soft-switching methods, and multiple-current methods can be used in SR DC/DC converters.

### 2.4.6 Multiple-energy-storage-element resonant [MER] power converters:

Current source resonant inverters are the heart of many systems and equipment, for example, uninterruptible power supply and high frequency annealing apparatus. Many topologies shown in the literature are the series resonant converters and parallel resonant converters that consist of two or three or four energy-storage
elements. However, they have limitations. These limitations of two-, three-, and/or fourelement resonant topologies can be overcome by special design. These converters have been categorized into three main types:

- Two-energy-storage-element resonant DC/AC and DC/AC/DC converters
- Three-energy-storage-element resonant DC/AC and DC/AC/DC converters
- Four-energy-storage-element (2L-2C) resonant DC/AC and DC/AC/DC converters
there are 8 prototypes of two-element converters, 38 prototypes of three-element converters, and 98 prototypes of four-element (2L-2C) converters.


## Chapter 3

## Voltage-Boosting Techniques

Power electronic converter employs various voltage-boosting techniques for dc-dc step up conversion of voltage levels. The boosting techniques can be broadly categorized into five major sections named as: switched capacitor or charge pump (SC or CP), voltage multiplier, switched inductor and voltage lift (SL \& VL), magnetic coupling, and converters with multistage or multilevel structures [2]. The boosting techniques are shown in Fig.3.1. The general structures of each technique are first illustrated and then described in the subsequent sections.


Figure 3.1: Broad categorizations of voltage boost techniques used for dc-dc converters [2]

### 3.1. Switched Capacitor (Charge Pump)

Switched Capacitor (SC) is one of the popular implementations of Charge Pump (CP) circuit. The SC voltage boosting technique is entirely based on CP circuit. Fig.3.2 shows some basic charge pump and switched capacitor circuits. Fig. 3.2(a) shows a schematic CP circuit, in which two switches are turned ON and OFF in succession. When switch I is turned ON, capacitor C1 charges to the input voltage level, and when switch II is turned ON, the stored energy in C1 transfers to capacitor C2 and the switches are phased alternately (odd-numbered switches (I) in phase 1, even numbered switches (II) in phase 2). This process is called pumping the energy from one capacitor to another [3]-[6].

(a)

(b)

(c)
(c)

(d)

Fig.3.2: Basic charge pump and switched capacitor circuits. (a) Basic charge pump. (b) Basic switched capacitor. (c) Doubler. (d) Series-parallel. (e) Ladder. (f) Dickson. (g) Makowski or Fibonacci.

Output voltage level can be doubled by the two-phase SC voltage doubler (TPVD) shown in Fig.3.2(b). First the capacitor C1 is charged to the input voltage then the capacitor C1 is placed in series with the input source, which doubles the output voltage level [7] TPVD can be connected in series for higher voltage gains as shown in Doubler SCs in Fig. 3.2(c). Series-parallel SC as shown in Fig. 3.2(d) use capacitors efficiently, as the capacitors in this topology are at the same voltage [8].

Main issue related to SC circuits is their high-current transients, which have a degrading effect on both power density and efficiency. One way to prevent the detrimental effects of current transients in SC circuits is to insert an inductor at the output in order to form a buck converter with the existing switch(es). This technique has the two advantages of providing efficient regulation and eliminating current transients, which together are known as the soft-charging of SC converters [9].

### 3.2. Voltage Multiplier

Voltage multipliers can be divided into two major groups from a structural point of view: 1) the in-circuit VMC, which can be implemented in the middle of a circuit usually after the main switch, in order to reduce voltage stress; and 2) the voltage multiplier rectifier (VMR), which is placed at the output stage of transformer- and coupled-inductor-based structures in order to rectify ac or pulsating dc voltage while acting as a voltage multiplier.

### 3.2.1. Voltage Multiplier Cell

Some generic voltage multiplier cell topologies are shown in Fig. 3.3. Some of these cells consist only of diodes and capacitors [Fig.3.3 (b)-(d)] and hence are known as switched/diode capacitor VMCs [10]-[12]. Other VMCs have more components, such as an auxiliary switch as in Fig.3.3(e), while some use inductors to increase the voltageboosting ratio as in Fig.11(f) and (g) [13]-[14].


Fig.3.3: (a) General topological view of the placement of voltage multiplier cells in step-up converters. (b)-(g) Various voltage multiplier cells.

All of the converters using VMCs shown in Fig. 3.3 operate by switching the main switch (S), with the exception of the VMC in Fig. 3.3(e), in which the boost converter operates only with the switch Sa of the VMC. The VMC in Fig. 3.3(f) uses a capacitor and inductors to increase the boost factor of the converters [13]. The VMC in Fig. 3.3(g) is typically inserted before the main switch to increase the voltage level of very low voltage sources (under50 V). This VMC has been used in various ultra-step-up dc-dc converters [10].

### 3.2.2. Voltage Multiplier Rectifier

This group consist solely of different configurations of diodes and capacitors and are commonly referred to as voltage multipliers. VMRs can be further grouped into half wave VMRs and full wave VMRs. General topological view of the placement of VMR is shown in Fig. 3.4.


Figure 3.4: General topological view of the placement of VMRs (a) at dc pulsating output and (b) at ac output

## A) Half Wave:

these circuits are not confined to the secondary side of isolated transformers and coupled inductors but can also be used in converters with built-in transformers and coupled inductors. Fig. 3.5(a) shows a Greinacher voltage doubler rectifier (G-VDR) which used at the output stage of many transformer-based dc-dc converters [15]. Fig. 3.5(b) shows an improved version of the G-VDR [16]. The advantage of this VMR is that the voltage stresses of all components are half of the output voltage; this allows for the use of lower voltage rating components than in conventional VMRs, which in turn leads to low-power loss and high efficiency. Fig. 3.5(c) shows a Greinacher voltage quadrupler rectifier formed by connection of one normal and one inversed G-VDR. The advantage of this VMR is that it can provide a neutral point terminal, which is necessary for half bridgebased transformer-less inverters [17]. Another well-known voltage multiplier is the Cockcroft-Walton (CW). CW-VMRs, as shown in Fig. 3.5(d), are popular for their simple cascading structures that can provide high-voltage level [18].

TABLE 3.1: VOLTAGE STRESS FOR VARIOUS VMRS

| Voltage Multiplier <br> Rectifier (VMR) | Output Voltage <br> $\left(V_{\text {out }}\right)$ | Output Diode <br> Voltage Stress | Output Capacitor <br> Voltage Stress |
| :---: | :---: | :---: | :---: |
| Greinacher Voltage <br> Doubler | $2 V_{\text {in }}$ | $V_{\text {out }}$ | $V_{\text {out }}$ |
| Improved Greinacher <br> Voltage Doubler | $2 V_{\text {in }}$ | $\frac{V_{\text {out }}}{2}$ | $\frac{V_{\text {out }}}{2}$ |
| Greinacher Voltage <br> Quadrupler | $4 V_{\text {in }}$ | $\frac{V_{\text {out }}}{2}$ | $\frac{V_{\text {out }}}{2}$ |
| Cockcroft-Walton <br> Voltage Multiplier | $n V_{\text {in }}$ | $V_{\text {out }}$ | $V_{\text {out }}$ |



Figure 3.5: Various half-wave VMRs. (a) Greinacher voltage doubler. (b) Improved Greinacher voltage doubler. (c) Greinacher voltage quadrupler. (d) CW voltage doubler. (e) CW voltage multiplier.

## B) Full Wave:

Full-wave VMRs, another well-known type of independent boosting stage, are commonly employed at the output stage of transformer-based converters. Fig. 3.6 illustrates some basic and generalized structures for even and odd voltage multiplier groups. The VMR in Fig. 3.6(a) is a full-bridge voltage doubler rectifier that, owing to its reduced voltage stress on output capacitors (it reduces the output voltage by one-half), is commonly used in various dc-dc converters [19]-[23]. The VMR in Fig. 3.6(b) is a quadrupler voltage rectifier that is considered to be a useful boosting stage in modern dc-dc converters owing to its balanced voltage stress on both capacitors and diodes [24][25]. Fig. 3.6(c) shows a multi stage structure consisting of the VMRs in Fig. 3.6(a) and (b) (even group) [26].


Figure 3.6: Various full-wave VMRs. (a) Voltage doubler rectifier. (b) Voltage quadrupler rectifier. (c) VMR (even group)

### 3.3 Switched Inductor and Voltage Lift

Voltage lift switched inductor (VL-SL) cells are shown in Fig. 3.7, with a typical placement of these cells in a step-up dc-dc converter shown in Fig. 3.7(a). The basic SL cell depicted in Fig. 3.7(b) was first introduced in [11]. In an SL cell, the inductors are magnetized in parallel and demagnetized in series. As both inductors have the same inductance value and operational condition, they can be integrated into a single core in order to reduce the size and weight of the converter. The elementary circuit of a VL circuit is shown in Fig.15(c).

Implementing an elementary VL cell in an SL cell produces the so-called self-lift SL cell, as shown in Fig. 3.7(d). Adding another diode and capacitor to a self-lift SL cell produces a double self-lift SL cell, as shown in Fig. 3.7(e) [27]. In a double self-lift SL cell, S0 is used instead of D0 in a basic SL cell with switching operation complementary to the switch S in Fig. 3.7(a).

(a)


Basic SL Cell
(a)

(c)


Elementary-Lift Cell
(b)

(d)

Figure 3.7: Voltage lift cells. (a) General placement of the voltage lift cell in step- up converters. (b)-(e) Various voltage lift switched inductor cells. [(a) Basic SL cell. (b) Elementary-lift cell. (c) Self-lift SL cell. (d) Double self-lift SL cell.]

### 3.4 Magnetic Coupling

Magnetic coupling is a popular voltage-boosting technique that is used in both isolated and nonisolated dc-dc converters. Using a coupled inductor reduces the number of magnetic cores, which are often the bulkiest components in the layout. Despite benefits such as dominant boost ability, utilization of magnetic coupling is often incurring drawbacks such as leakage inductance that may require consideration in terms of recycling the leakage energy. In this section, the various transformer-based boost techniques, as well as the inductor coupling technique, are presented.

### 3.4.1 Transformer

Transformer-based dc-dc converters are the subject of increasing research interest as the transformer turns ratio provides an additional degree of design freedom that, along with the duty cycle, can be manipulated to achieve high- voltage boost ability. Transformer converters can be broken into two types: isolated transformers, which are used to electrically isolate dc-dc converters; and nonisolated dc-dc converters de- rived from isolated converters, which are known in the literature as built-in transformers. Although their underlying circuit theories are similar; however, the performance differs by type.

## A) Isolated Transformer:

Fig. 3.8(a) shows a schematic of a basic transformer-based converter with an input dc source followed by a network of switches, diodes, and transformer that is then rectified and connected to an output filter. There are several common types of isolation transformers that can be incorporated into dc-dc converters according to their switching network layouts [28]-[29]. Full- and half-bridge converters typically use a transformer of the type shown in Fig. 3.8(b), in which one or two windings in the secondary (depending on the rectifier circuit) are used to step-up the primary voltage. One type of buck-based converter called the forward converter incorporates a three-winding transformer, as shown in Fig. 3.8(c). Push-pull based converters typically use a multi-winding transformer, as shown in Fig. 3.8(d), in which the two windings in the primary (each one activating in a switching state) are followed by one or two windings in the secondary (depending on the rectifier circuit).


Figure 3.8: Isolated dc-dc converters. (a) General layout of basic transformer- based converters. (b) Full bridge/half bridge. (c) Forward. (d) Push-pull

## B) Built-in Transformer:

Some examples of general built-in transformer-based converter structures are shown in Fig. 3.9. The primary side of such converters usually consists of switched networks to generate pulsating dc voltage, while the secondary side usually consists of SCs voltage multiplier modules [30]-[33]. In addition to the transformer shown in these circuits, various voltage multiplier circuits are used to further increase the voltage gain and reduce the built-in transformer turns ratio.


Figure 3.9: Step-up dc-dc converter consisting of built-in transformer concept. (a) General layout with the horizontal structure. (b) Comprising voltage multiplier. (c) Comprising both coupled inductor and built-in transformer.

### 3.4.2 Coupled Inductor

Coupled inductors are a valuable component of nonisolated dc-dc converters that store energy in one cycle and power the load in the other cycles. As many applications do not require electrical isolation, the use of coupled inductors provides a helpful alternative boosting technique in dc-dc converters that can be achieved by tapping or simply coupling the inductors.

## A) Tapped inductor/autotransformer:

Tapped circuits can be categorized into three types: switched-tapped, diode-tapped, and rail-tapped. Fig. 3.10(a) shows the general configuration of a tapped-inductor boost dc-dc converter [34]-[35]. Switch tapping occurs by connecting A to 1, B1 to 2, and C to 3 . Diode- tapping is obtained by connecting A to $1, \mathrm{~B} 1$ to 3 , and C to 2 . Finally, the circuit can be rail-tapped by connecting A to $3, \mathrm{~B} 2$ to 2 , and C to 1 .

Parasitic analysis shows that the gain voltage and efficiency of tapped inductor boost converters can be theoretically higher than that of PWM boost dc-dc converters. On the other hand, as the root mean square (RMS) current of the switches, RMS current of inductors, and diode-blocking voltages all increase when inductor tapping is utilized [36], designing a clamp/snubber circuit is sometimes necessary [34], [37]. Another advantageous use of tapped inductors is obtaining input current ripple cancellation in a PWM boost dc-dc converter, as demonstrated in [38].


Figure 3.10: Tapped-inductor based converters. (a) General configuration of a tapped inductor boost converter and (b) double-tapped inductor boost converter

## B) Magnetically coupled-based converters:

Fig. 3.11 shows the general configuration of a coupled-inductor-based boost converter. A basic coupled-inductor boost converter is shown in Fig. 3.12(a). The secondary winding acts as a voltage source in series with the power branch, while the clamp capacitor Cc and diode Dc are used to recover leakage energy. The clamp capacitor can be shifted within the circuit. The clamping function is similar in all placements and the leakage energy can be effectively recycled directly or through the secondary winding to the load [39].


Figure 3.11: General layout of the coupled-inductor-based step-up converter.


Figure 3.12: Coupled-inductor-based circuits. (a) Basic coupled inductor. (b) Switched coupled inductor. (c) Coupled inductor with active clamp. (d) Coupled inductor with a snubber circuit.

### 3.5 Multistage/ Multilevel

One well-known method for increasing the voltage gain of a dc-dc converter is to employ several stages of converter modules connected in various ways. This can be realized by implementing several identical/different converter modules combined with various voltage-boosting techniques. In this subsection, cascaded, interleaved, and multilevel converter topologies and their sub groups are presented. The voltage gain in multistage/ multilevel structures increases linearly or exponentially (often multiplicatively by number of stages) as a function of the topology used.

### 3.5.1 Cascaded

Cascading connection of converters is a simple approach for increasing voltage gain. Fig. 3.13 shows general layout of a cascaded dc-dc converter [40]. According to the depicted scheme, two or more boost converters can be connected in cascaded form (called a quadratic group) or different types of step-up converters can be connected in cascaded form (called a hybrid group).


Figure 3.13: General layout of the cascaded dc-dc converter.

## A) Quadratic Boost:

Fig. 3.14(a) shows a cascaded boost converter consisting of two boost converters in cascaded form [41]. To reduce the circuit complexity, the switches of the cascaded boost converter can be integrated into one switch. In a structure called a quadratic boost converter [42]. The configuration of a quadratic boost converter is shown in Fig. 3.14(b). Moreover, quadratic boost converters are advantageous for low-power applications where sophisticated magnetic designs are avoided.


Figure 3.14: Quadratic dc-dc converters. (a) Two cascaded boost converters. (b) Quadratic boost converter.

## B) Hybrid cascaded:

In this subsection, two types of cascaded converters are introduced: quadratic boostbased converters with auxiliary circuits, and hybrid connections of two different types of dc-dc converters. Fig. 3.15 shows the general structure of a hybrid cascaded two different dc-dc converter.


Figure 3.15: General layout of the cascaded connection of two different converters.

### 3.5.2 Interleaved

In step-up dc-dc converters, the input cur- rent level is higher than the output current level. As such, the multiphase interleaving technique is a promising solution for decreasing the current ripple and increasing the power density in high step-up dc-dc converters. Fig. 3.16(a) shows a schematic of a two-phase interleaved boost converter. In addition to zero reverse-recovery of output diodes, an interleaved boost converter with coupled input inductors has lower current ripple and a smaller switching duty cycle than a normal boost [43]. Fig. 3.16(b) shows a schematic of a two-phase interleaved step-up dc-dc converter with passive/active clamp circuits and a voltage multiplier module (coupled inductor or transformer, SC) between the input switches and output diodes to increase the voltage step-up gain.


Figure 3.16: Interleaved dc-dc converters. (a) and (b) General layouts of interleaved step-up converters

### 3.5.3 Multilevel

Useful in high-power high-voltage applications. Multilevel converters in a dc-dc structure can help to decrease or almost eliminate magnetic components, which leads to reduced converter size and weight [44]-[46]. From the input voltage view, multilevel dc- dc converters can be divided into two major types: multilevel converters with a single dc or multiple dc sources. Single-source multilevel modular structures are of interest for use in electric vehicle (EV) or HEV and motor traction, as multiple distributed energy sources such as batteries, PVs, and FCs can be connected through a multilevel cascaded dc-dc converter to feed into a load or the ac grid without voltage balancing problems.

## A) Single dc source (Modular):

One topology for single- input multilevel structures is the boost converter with multiple submodules consisting of switches/diodes and capacitors [47]. A schematic of this converter with several submodules is shown in Fig. 3.17(a). The main advantages of this type of converter are its simplicity, modularity, and flexibility [48]. As can be inferred from Fig. 3.17(a), this type of multilevel converter comprises several submodules and is, therefore, called a multilevel modular dc-dc converter. Two basic structures of this kind without active switching at their output stages are shown in Fig. 3.17. In Fig. 3.17(b), a PWM boost converter is employed as the base level of a proposed multilevel converter [49]. In Fig. 3.17 (c), a two-switch multilevel converter with no inductive element is shown in [50]. The main advantage of these structures is their low-voltage stress on output devices.


Figure 3.17: Interleaved dc-dc converters. (a) and (b) General layouts of interleaved step-up converters

## B) Multiple dc source (Cascaded):

To increase the out- put voltage level of PV or FC modules, such sources can be connected in series to increase their string voltage. This series-connected voltage can then be connected to a converter for regulation or further step-up purposes. On the other hand, such sources can be connected in cascaded multilevel connections, which have been claimed to have better reliability, safety/protection, and maintainability and lower cost [51]-[53]. This group of multilevel converter comprises cascaded connections of multiple lower voltage dc-dc converters [see Fig. 3.18(a)] and is therefore called multilevel cascaded dc-dc converters.


Figure 3.18: Multilevel cascaded dc-dc converters with multiple dc sources. (a) General cascaded structure.

### 3.5 Summary

The ongoing technological progress in high-voltage step-up dc-dc converter has five primary drivers-energy efficiency, power density, cost, complexity, and reliability-all of which also influence each other to some extent. Each voltage- boosting technique has its own unique features and suitable applications, and there is no one-size-fits-all solution. Nevertheless, it is generally not fair to permanently favor any particular technique or solution [2]. Table 3.2 provides a comparative summary of various voltageboosting techniques in terms of their major characteristics (i.e., power level, cost, reliability, efficiency, power density, weight, integration, and complexity).

TABLE 3.2: SUMMARY OF VOLTAGE BOOSTING TECHNIQUES \& THEIR APPLICATIONS

| Voltage Boosting Technique | Advantages | Disadvantages | Appropriate Applications |
| :---: | :---: | :---: | :---: |
| Switched Capacitor (Charge Pump) | - Cheap \& lightweight circuits <br> - Small size \& high power density. <br> - Easy to be integrated <br> - Fast dynamic response | - Startup inrush current <br> - Sensitive to the ESR of capacitors. <br> - Lack of output voltage regulation. <br> - Only discrete output voltage. | - Energy Harvesting. <br> - Mobile displays <br> (AMOLED). <br> - Automotive and vehicular applications. <br> - High gain dc-dc applications. |
| Voltage Multiplier | - Very high voltage ability with simple topology. <br> - Cell based structure. <br> - Can be integrated to various structures. | - High voltage stress on components. <br> - Need several cells with high ratings for very high voltage applications. | - Medical (X-ray, laser). <br> - Military (high power laser). <br> - Physics research |
| Switched Inductor and Voltage Lift | - High boost ability. <br> - Amenable in many converters. | - Need more passive components. <br> - Not suitable for high power applications. | - Mid-range dc-dc converters. <br> - High gain dc-dc applications. |
| Magnetic Coupling | - Versatile in boost ability due to tunable turns ratio of magnetic coupling. <br> - Switch can be implemented in low voltage side help to reduce conduction loss. <br> - High efficiency in soft switched type. | - Negative effects of leakage inductance such as large voltage spike. <br> - Need precise coupled magnetic design. <br> - Relatively bulky. | - High power/voltage applications <br> - DC microgrids. <br> - Data \& Telco Centers <br> - Bidirectional and regenerative converter <br> - Avionic and space. |
| Multi-Stage Level | - Modularity structure. <br> - High power capability. <br> - Reliable and efficient. <br> - High voltage/current level. | - Large number of components. <br> - Relatively heavy, bulky and costly. <br> - Efficiency deteriorate with number of stages/levels. | - HVDC transmission. <br> - Renewable energy systems \& distributed power generation <br> - DC micro-grids. <br> - High power DC supply <br> - Space technology \& applications |

## Chapter 4

# Design of Switched Capacitor and Switched Inductor Combined Structure 

### 4.1 Introduction

One of the main orientations in power electronics in the last decade has been the development of switching mode converters without transformers. Light weight, small size and high-power density are the result of using only switches, capacitors and inductors in the power stage of these converters. Thus, they serve as ideal power supplies for mobile electronic systems (e.g. cellular phones, personal digital assistants, and so forth). Switched-capacitor (SC) converters and Switched-inductor (SL) converter, with their large voltage conversion ratio, promise to be a response to such challenges of the 21st century as high-efficiency converters with low EMI emission and the ability to realize steep step-down of the voltage (to 3 V or even a smaller supply voltage for integrated circuits) or steep step-up of the voltage for automotive industry or internet services in the telecom industry.

The primary goal of any switching-mode power converter is to provide a constant (DC or AC ) output voltage at its load, despite variations in the input voltage or load. A control element, therefore, has to be introduced in the process of transmitting energy so that the converter (power stage) changes its topology cyclically, and the durations of the switching topologies are adjusted for regulation purposes.

## First SC Converters and Basic Principles

The first SC converters were developed by a group of researchers from Kumamoto, Japan, who processed a DC unregulated voltage toward a DC regulated voltage. The first SC converters suffered from some drawbacks. In order to solve these problems, new configuration of the SC circuit was proposed. The SC block was divided into two symmetrical SC-sub circuits. For the first half-cycle the capacitors in the first SC cell are in a charging phase, and the capacitors in the second SC cell discharge on the load. The role of the two cells is interchanged in the second half-cycle.


Fig 4.1: Basic SC step-down DC-DC converter


Fig 4.2: Step-down converter with two SC sub-circuits.
A switched-capacitor circuit can also be used in the structure of a zero-current-switching (ZCS) converter-a converter in which the transistor turns off at the instant when the current through it reaches the value zero, implying zero-turn-off switching losses.

## Switched Inductor used in Voltage Lifting

The basic SL cell depicted in Fig. 4.3 was first introduced in some literatures. In an SL cell, the inductors are magnetized in parallel and demagnetized in series. As both inductors have the same inductance value and operational condition, they can be integrated into a single core in order to reduce the size and weight of the converter.


Fig 4.3: Basic Switched Inductor cell.

### 4.2 Working Principles

The SC is a well-known voltage-boosting technique based on a CP circuit that is used in many converters. It can be used as a Voltage Multiplier cell. Voltage-level enhancement in a SC circuit comes solely from capacitive energy transfer and does not involve magnetic energy transfer.

The circuit shown in Fig. 4.4A is two-phase Switched Capacitor voltage doubler (TPVD). In the first phase, which is also shown in Fig.4.4, capacitor C1 is charged to the input voltage. In the second phase, capacitor C 1 is placed in series with the input source, which ideally doubles the output voltage level.


Fig 4.4: Basic Switched Capacitor Cell.

Some structures have been proposed in literatures for either step up and step-down purposes. These structures are formed by either two capacitors and 2-3 diodes, or two inductors and 2-3 diodes.

Fig.4.5 presents a switching blocks formed by two capacitors C1 \& C2 where C1 is equal to C2 and Diode D1, D2 \& D12. In time interval $0<T<$ DTs or ON state, capacitors C1 \& C2 of the structure are charged in series from the input voltage source. In this state, diode D12 is ON and Diode D1 \& D2 are OFF shown in Fig 4.6.


Fig 4.5: Switched Capacitor Structure for Step Down purposes.


Fig 4.6: Switching States of Switched Capacitor cell.

In time interval DTs $<$ T $<$ Ts or OFF state, capacitors $\mathrm{C} 1 \& \mathrm{C} 2$ of the structure are discharges in parallel to the output load. In this state, Diode D12 is OFF and Diode D1 \& D2 are ON.


Fig 4.7: Switched Inductor Structure for Step Up purposes.
On the other hand, for Switched Inductor structure the block is formed by two inductor L1 \& L2 and three Diode D1, D2 \& D12.

In time interval $0<\mathrm{T}<\mathrm{DTs}$ or ON state, inductor L1 \& L2 of the structure are charged in parallel from the input voltage source. In this state, Diode D12 is OFF and diode D1 \& D2 are ON shown in Fig 4.8. On the other hand, in time interval $\mathrm{DTs}<\mathrm{T}<\mathrm{Ts}$ or OFF state, inductor L1 \& L2 of the structure are discharges in series to the output load. In this state, diode D12 is ON and Diode D1 \& D2 are OFF.


Fig 4.8: Switching states of Switched Inductor cell.

### 4.3 Existing Structures

Among the many approaches to Charge Pump circuit implementation, Switched Capacitor topologies are very popular because of their structural modularity and capability for monolithic integration. It should be mentioned that some Voltage Multiplier cells consist only of diodes and capacitors and hence are known in the literature as switched/diode capacitor VMCs [10]-[12].


Fig 4.9: Switched Capacitor VM cell with auxiliary Switch.
Various Switched Capacitor DC-DC Converters are described in the literature with steep step up or step-down conversion ratios. Some of these are shown in Fig 4.10.

(a)

(b)

(c)

Fig 4.10: Various Switched capacitors DC-DC Converters.
An active switched inductor (A-SL) based converter was presented in [54]. Instead of three diodes, as in the basic SL cell shown in Fig. 4.3, only two active switches are used in an A-SL network and there is no need for an external switch in the converter circuit. In [54], an improved A-SL network that obtains increased voltage gain through the use of extra diodes and capacitors and reduces the voltage stress across S1 and S2 was introduced. A hybrid A-SL network was presented in [55]. Although it increases the voltage gain in the duty cycles to over 0.5 , the voltage stress across the switch and the number of diodes is also increased. Various A-SL networks are shown in Fig. 4.11.


Fig 4.11 (a): Basic Active Switched Inductor cell.


Fig 4.11 (b): Improved Active Switched Inductor cell.


Fig 4.11(c): Hybrid Active Switched Inductor cell.

Some coupled-inductor-based SLs, referred to as switched coupled inductors (S-CL), have been presented in the literature. Fig. 4.12. shows an S-CL boost converter, which has a higher voltage gain than a boost converter and also recycles leakage energy to the load. The S-CL circuit consists of three components, as shown as Fig. 4.13. These components have also been implemented in various other converters (buck-boost, Ćuk, SPEIC, and Zeta converters) [56]-[58].


Fig 4.12: Switched Coupled Inductor based Boost Converter.


Fig 4.13: Typical Switched Coupled Inductor Components.

Some new approaches are proposed in [11]. simple switching dual structures, formed by either two capacitors and 2-3 diodes, or two inductors and 2-3 diodes are defined. These circuit blocks can provide either a step-down of the input voltage or a step-up of it. They are inserted in classical buck, boost, buck-boost, Ćuk, SEPIC, Zeta converters to provide new power supplies with a steep voltage conversion ratio. As their complexity in terms of circuit elements is comparable to that of the quadratic converters, their performances (voltage ratio, stresses, efficiency) will be compared to that of available quadratic circuits.

The step-down switching-capacitor/switching inductor structures discussed in [11] are shown in Fig 4.14.


Fig 4.14: Basic Step-Down switching structures: (a) Dn1 (b) Dn2 \& (c) Dn3.


Fig 4.15: Switching Topology of the Dn2 step down structure


Fig 4.16: Switching Topology of the Dn3 step down structure
Switching Topologies for Dn2 \& Dn3 step down structures are presented in Fig 4.15 \& Fig 4.16. Like in a doubler-type rectifier, for blocks Dn2 \& Dn3, in topology $t_{o n}$, inductors L1 \& L2 are charged in series and in topology $t_{o f f}$, inductors L2 \& L2 are discharged in parallel.

The step-up switching-capacitor/switching inductor structures discussed in [11] are shown in Fig 4.17.

a)

b)

c)

Fig 4.17: Basic Step Up switching structures: (a) Up1 (b) Up2 \& (c) Up3.

Switching Topologies for Up1 \& Up2 Step Up structures are presented in Fig 4.18 \& Fig 4.19. Like in a doubler-type rectifier, for blocks Up1 \& Up2, in topology $t_{\text {off }}$, capacitors C1 \& C2 are charged in parallel and in topology $t_{\text {on }}$, capacitors C2 \& C2 are discharged in series.


Fig 4.18: Switching Topology of the Up1 step up structure


Fig 4.19: Switching Topology of the Up2 step up structure

The proposed C-switching and L-switching circuits in [51] are inserted in the basic buck, boost, buck-boost, Ćuk, SEPIC, and Zeta converters.

### 4.4 Applications

i) DC generation and distribution systems or DC Microgrids.
ii) Embedded systems or microelectronics with very steep voltage conversion requirement like power supplies for microprocessors.
iii) In Data and telecommunication centers where 48 V DC of the battery plant has to be boosted to a 380 V intermediate DC bus.
iv) The high intensity discharge lamps (HID) for automobile head lamps require at their start-up the increase of the voltage from the battery's 12 V to more than 100V.
v) Integration of renewable energy systems to improve reliability and stability of the power grid.
vi) Increasing use of renewable energy systems using battery storage, fuel cells which requires DC-DC converters with high gain.

# 4.5 Proposed Combination of Switched Capacitor (SC) Switched Inductor (SL) Structure 

### 4.5.1 Proposition

In order to provide such a high voltage-conversion ratio, the basic converters would have to operate with an extreme value of the duty cycle. An extreme duty cycle impairs the efficiency and imposes obstacles for the transient response. Also, to generate such an extreme duty cycle, the control circuit must incorporate a very fast, expensive comparator [59].

However, if the industrial application does not require for dc isolation, the use of a transformer would only increase the cost, the volume, and the losses. Moreover, a large transformer turns ratio ( $\mathrm{n}: 1$ ) would increase the voltage stress on the primary elements, imposing a heavy penalty on the efficiency.

Use of cascade of converters for getting the desired voltage ratio is a no-solution in the today's energy-saving conscious world, as this procedure implies an overall efficiency equal to the product of the efficiencies of each circuit. Quadratic converters can somehow alleviate the efficiency problem of cascade circuits by using a single driven transistor [60]-[61], but they may present voltage or current overstresses.

Voltage regulators have recently been developed for getting a sub-1-V supply voltage needed in microprocessors. The switched-capacitor converters, proposed in the 1990's, can provide any steep conversion ratio [62]. However, they operate with a relatively low efficiency, and put challenges in the charging path of the capacitors.

Use of cascade of converters for getting the desired voltage ratio is a no-solution in the today's energy-saving conscious world, as this procedure implies an overall efficiency equal to the product of the efficiencies of each circuit. Quadratic converters can somehow alleviate the efficiency problem of cascade circuits by using a single driven transistor [63]-[64], but they may present voltage or current overstresses. Starting from the switched-capacitor cells, switched inductor-capacitor
circuits have been developed in [65].
To alleviate all these problems, using the duality between a switching-capacitor cell and a switching inductor cell, new structures have been proposed by combining switching capacitor cell and switching inductor cell together in a single structure driven by a single switch. These structures provide very large voltage gain ratio with a high efficiency.

### 4.5.2 Proposed Structures

The combined structure depicted on Fig 4.20 provides steep step up output voltage gain. This combined structure comprises two inductors L1 \& L2, two energy transferring capacitors C1 \& C2 and five diodes D1, D2, D3, D4 \& D5. This figure is implemented on conventional Zeta converter. The input inductor of conventional zeta converter is replaced by a switched inductor which comprises two inductors L1 \& L2 and three power Diode D1, D2 \& D3. And the Diode along with the coupling capacitor of the conventional zeta converter is replaced by a switched capacitor which comprises of two capacitors C1 \& C2 and two power Diode D4 \& D5.


Fig 4.20: Combined structure for step up converter implemented on Zeta.

This combined structure for conventional Zeta converter has two modes of operations. Mode I is when the switch of the converter is ON and Mode II is when the switch is OFF.

## Mode I: Time interval $0<T<$ DTs:

In this mode of operation, when MOSFET switch is ON, the power Diode D3 of the switched inductor is turned OFF as well as the power Diode of switched capacitor D4 \& D5 are turned OFF. In this mode, Diode D1 \& D2 are ON. Some assumptions are made to simplify the circuit analysis. The inductors \& the capacitors values are kept equal so that same magnitude of current and voltage may flow through and induced in the inductors and the capacitors respectively.

In this mode of operation, the inductors L1 \& L2 are charged in parallel and the capacitors C1 \& C2 are discharged in series which is shown in Fig 4.21.


Fig 4.21: Current direction in Time interval $0<T<$ DTs (Mode I).

## Mode II: Time interval DTs<T<Ts:

In this mode of operation, when MOSFET switch is turned OFF, the power Diode D3 of the switched inductor is turned ON as well as the power Diode of switched capacitor D4 \& D5 are turned ON. In this mode, Diodes D1 \& D2 are turned OFF.


Fig 4.22: Current direction in Time interval $\mathrm{DTs}<\mathrm{T}<\mathrm{Ts}$ (Mode II).

In this mode of operation, the inductors L1 \& L2 are discharged in series and the capacitors C1 \& C2 are charged in parallel which is shown in Fig 4.22.

Another combined structure is proposed here which is depicted on Fig 4.23 that provides steep step-down output voltage gain. This combined structure comprises two energy transferring capacitors C1 \& C2, two inductors L1 \& L2 and five diodes D1, D2, D3, D4 \&

D5. This figure is implemented on conventional Ćuk converter. The output inductor of conventional Ćuk converter is replaced by a switched inductor which comprises two inductors L1 \& L2 and two power Diode D4 \& D5. And the coupling capacitor of the conventional Ćuk converter is replaced by a switched capacitor which comprises of two capacitors C1 \& C2 and three power Diode D1, D2 \& D3.


Fig 4.23: Combined structure for step down converter implemented on Ćuk.
This combined structure for conventional Ćuk converter has two modes of operations. Mode I is when the switch of the converter is turned ON and Mode II is when the switch is turned OFF.

## Mode I: Time interval $0<T<$ DTs:

In this mode of operation, when MOSFET switch is turned ON, the power Diode D3 of the switched capacitor is turned OFF as well as the power Diode of switched inductor D4 \& D5 are turned OFF. In this mode, Diode D1 \& D2 are turned ON. Some assumptions are made to simplify the circuit analysis. The inductors \& the capacitors values are kept equal so that same magnitude of current and voltage may flow through and induced in the inductors and the capacitors respectively.


Fig 4.24: Current direction in Time interval $0<T<D T s$ (Mode I).

In this mode of operation, the inductors L1 \& L2 are charged in series and the capacitors C1 \& C2 are discharged in parallel which is shown in Fig 4.24.

## Mode II: Time interval DTs $<$ T<Ts:

In this mode of operation, when MOSFET switch is OFF, the power Diode D3 of the switched capacitor is turned ON as well as the power Diode of switched inductor D4 \& D5 are turned ON. In this mode, Diodes D1 \& D2 are turned OFF.


Fig 4.25: Current direction in Time interval $\mathrm{DTs}<\mathrm{T}<\mathrm{Ts}$ (Mode II).
In this mode of operation, the inductors L1 \& L2 are discharged in parallel and the capacitors C1 \& C2 are charged in series which is shown in Fig 4.25.

## Chapter 5

## Conventional Zeta \& Ćuk circuits Analysis

### 5.1 Zeta Converter

The name of the converter has been derived from the Greek letter Zeta which is the sixth letter of the Greek alphabet. The converter provides a positive output voltage from an input voltage that varies above and below the voltage output. It's a $4^{\text {th }}$ order DC-DC converter consisting of two inductors and two capacitors \& able to operate in either stepup or step-down mode. The converter can act as Buck-Boost-Buck converter in terms of power input, and with regards to the output it acts as a Boost-Buck-Boost converter. One of the capacitors is a flying capacitor which is connected in series. The output current of the converter is continuous where the input current is discontinuous. Overall Duty ratio for the conventional converter is $\operatorname{Vo} / \operatorname{Vin}=(1-D)$. The $4^{\text {th }}$ order of the converter accounts for difficult control over the converter. Some control techniques in this converter, such as sliding mode control, are increasingly difficult to implement. The converter is being highly used to maximize energy harvesting and power applications for photovoltaic systems and wind turbines.

### 5.1.1 Converter Circuits

Figure 5.1(a) depicts a simple circuit diagram of a ZETA converter consisting of an input capacitor $C_{\text {in }}$, an output capacitor $C_{\text {out }}$, coupled inductors $L 1 a$ and $L 1 b$, an AC coupling capacitor $C_{c}$, an P-MOSFET output capacitor $Q 1$, and a diode $D 1$.


Fig 5.1 (a): Conventional Zeta Converter circuit diagram.

### 5.1.2 Operating Principle

Figures 5.1 (b) \& 5.1(c) displays the ZETA converter in CCM when SW is on and when SW is off. At first, we analyze what occurs to the circuit when SW is ON and Diode D is OFF in DC. The capacitor is charged to the output voltage $V_{\text {out }}$ as it is in parallel with $C_{\text {out }}$. The figures also show the voltages across L1 and L2 during Continuous Conduction Mode (CCM). The two stages of CCM brings out the charging and discharging characteristics of the capacitors.


Fig 5.1(b) Time interval $0<$ T<DTs. (SW ON Mode).

When SW is OFF and Diode D is ON The voltage across L2 is equal to $V_{\text {out }}$ since its parallel with $C_{\text {out }}$. The voltage across SW is equal to $\left(V_{\text {in }}+V_{\text {out }}\right)$. When SW is on, the inductor is charged with the input voltage $V_{i n}$. As the capacitor is connected in series with L2, so the diode sees $\left(V_{\text {in }}+V_{\text {out }}\right)$.


Fig 5.1(c) Time interval DTs<T<Ts. (SW OFF Mode).

Figure 5.2 shows current flows through various circuit components. Once SW is on, the input power is stored by the components L1, L2 and C1. L2 is supplying the output current. When SW is turned off, L1's current flows in addition to current discharged from C1 and L2 supplies the output current as similar to the ON state.


Fig 5.2: Component currents during ON and OFF states of CCM

### 5.1.3 Steady State Analysis

## Continuous Conduction Mode

When SW is ON and Diode D is OFF, the capacitor is charged to the output voltage $V_{\text {out }}$ as it is in parallel with $C_{\text {out }}$.

$$
\begin{gather*}
V_{L 1}=V_{i n}  \tag{5.1}\\
V_{L 2}=-V_{1}+V_{i n}-V_{o}  \tag{5.2}\\
I_{C 1}=I_{2}  \tag{5.3}\\
I_{C 2}=I_{2}-V / R \tag{5.4}
\end{gather*}
$$

When SW is OFF and Diode D is ON The voltage across L2 is equal to $V_{\text {out }}$ since its parallel with $C_{\text {out }}$. The voltage across $S W$ is equal to $\left(V_{\text {in }}+V_{\text {out }}\right)$.

$$
\begin{gather*}
V_{L 1}=V_{1}  \tag{5.5}\\
V_{L 2}=-V_{o}  \tag{5.6}\\
I_{C 1}=-I_{1}  \tag{5.7}\\
I_{C 2}=I_{2}-V_{o} /_{R} \tag{5.8}
\end{gather*}
$$

Applying Volt-sec Balance on inductor L1:

$$
\begin{gather*}
V_{L 1}=D V_{i n}+(1-D) V_{1}  \tag{5.9}\\
V_{1}=-\frac{D}{1-D} V_{i n} \tag{5.10}
\end{gather*}
$$

Again, applying Volt-sec Balance on inductor L2:

$$
\begin{gather*}
V_{L 2}=D\left(-V_{1}+V_{i n}-V_{o}\right)-(1-D) V_{o}  \tag{5.11}\\
0=-D V_{1}+D V_{i n}-V_{o} \tag{5.12}
\end{gather*}
$$

Applying equation (5.10) into equation (5.12), we get:

$$
\begin{gather*}
0=\frac{D^{2} V_{g}}{1-D}+D V_{i n}-V_{o} \\
G=V_{o} / V_{i n}=\frac{D}{1-D} \tag{5.13}
\end{gather*}
$$

This is the gain of conventional Zeta converter.

## 5.2 Ćuk Converter

The Ćuk converter is a type of DC / DC converter with an output voltage of either greater than or less than the input voltage. It's effectively a boost converter, followed by a buck converter with a capacitor. The output voltage of the converter is inverted. Hence, it's gain is also inverted. Both the input and output currents are continuous in case of the converter.

### 5.2.1 Converter Circuits

In Ćuk converter, there is an inductor at the input side, which acts as a filter for the input dc supply and it reduces the harmonic content. Moreover, the inductors eliminate the ripple content which leads to lower external filtering.

By using the duality principle on a conventional buck boost converter, a Ćuk converter can be designed. Duality relationship is established between the inductor in the buck boost regulator and the capacitor in the Ćuk regulator. Hence, in Ćuk regulator, energy transfer is associated with the capacitor. The value of the capacitance used is quite large. Thus, both the input current and the current feeding the output stage are largely ripple free.


Fig 5.3: Schematic of a non-isolated Ćuk Converter

### 5.2.2 Operating Principle

A non-isolated Ćuk converter comprises of two inductors L1 and L2, two capacitors C and Co, a switch (usually a transistor) and a diode D. The diagram can be seen as in Figure 5.3. It is an inverter, so the output voltage is negative with respect to the input voltage.

Capacitor $C$ is used to transfer energy and is alternately connected to the input and output of the converter by switching the transistor and the diode in Fig 5.4 and 5.5.

During ON state or Time interval $0<T<$ DTs:
The diode is turned off and switch is turned ON. Input inductor is charged with source voltage. Inductor currents IL1 and IL2 increase and also Capacitor charges in Fig 5.4.


Fig 5.4: ON state of a non-isolated ĆUK Converter

During OFF state or Time Interval DTs $<\mathrm{T}<\mathrm{Ts}$ :
The diode is ON and switch is OFF. Inductor currents IL1 and IL2 decreases and the capacitor discharges in Fig 5.5.


Fig 5.5: OFF state of a non-isolated ĆUK Converter

The two L1 and L2 inductors are used to transform both the input voltage source (Vi) an d the output voltage source (Vout) into current sources. The inductor can be viewed as a
current source at a short time scale as it retains a continuous current. The conversion was important because if the capacitor was connected directly to the voltage source, the current would be limited only by parasitic resistance, which would result in a high energy loss. The loading of a current source capacitor (the inductor) avoids resistive current restriction and related power loss.

As with other converters (buck converter, boost converter, buck-boost converter), the Ćuk converter can work either in continuous or discontinuous current mode. Nevertheless, unlike these converters, it can also operate in a discontinuous voltage mode (the voltage across the capacitor falls to zero during the changing cycle).


Fig 5.6: ON and OFF state of a Ćuk converter

In this figure, the diode and the switch are either replaced by a short circuit when they are on or by an open circuit when they are off. It can be seen that when in the off state, the capacitor C is being charging by the input source through the inductor L1. When in ON state, the capacitor C transfers the energy to the output capacitor through the inductance L .

Voltage and Current waveform of the Inductors L1 \& L2 for the conventional Ćuk converter are shown in Fig 5.7.


Fig 5.7: Waveform of conventional Ćuk converter.

### 5.2.3 Steady State Analysis

## Continuous Conduction Mode

In steady state, the energy stored in the inductors has to remain the same at the beginning and at the end of a commutation cycle. The energy in an inductor is given by:

$$
\begin{equation*}
E=1 / 2 L I^{2} \tag{5.14}
\end{equation*}
$$

In steady state, the energy stored in the inductors has to remain the same at the beginning and at the end of a commutation cycle. The energy in an inductor is given by

$$
\begin{equation*}
V_{L}=L^{d I} / d t \tag{5.14}
\end{equation*}
$$

This implies that the current through the inductors has to be the same at the beginning and the end of the commutation cycle. As the evolution of the current through an inductor is related to the voltage across it.

It can be seen that the average value of the inductor voltages over a commutation period have to be zero to satisfy the steady-state requirements.
If we consider that the capacitors C and $\mathrm{C}_{0}$ are large enough for the voltage ripple across them to be negligible, the inductor voltages become:

- In the off-state, inductor $L_{1}$ is connected in series with $V_{i}$ and $C$
- Therefore $\mathrm{V}_{\mathrm{LI}}=\mathrm{V}_{\mathrm{i}}-\mathrm{V}_{\mathrm{C}}$. As the diode D is forward biased (we consider zero voltage drop), $\mathrm{L}_{2}$ is directly connected to the output capacitor. Therefore $\mathrm{V}_{\mathrm{L}} 2=\mathrm{V}_{0}$
- in the on-state, inductor $L_{1}$ is directly connected to the input source. Therefore $\mathrm{V}_{\mathrm{LI}}=\mathrm{V}_{\mathrm{i}}$
- Inductor $\mathrm{L}_{2}$ is connected in series with C and the output capacitor, so $\mathrm{V}_{\mathrm{L} 2}=\mathrm{V}_{0}+\mathrm{V}_{\mathrm{C}}$

The converter operates in on state from $\mathrm{t}=0$ to $\mathrm{t}=\mathrm{DT}$, and in off state from DT to T (that is, during a period equal to (1-DT).

The average values of $V_{\mathrm{L} 1}$ and $V_{\mathrm{L} 2}$ are therefore:

$$
\begin{gather*}
V_{L 1}=D V_{i}+(1-D)\left(V_{i}-V_{C}\right)=\left(V_{i}-(1-D) V_{C}\right)  \tag{5.15}\\
V_{L 2}=D\left(V_{o}-V_{C}\right)+(1-D) V_{o}=\left(V_{o}+D V_{c}\right) \tag{5.16}
\end{gather*}
$$

As both average voltages have to be zero to satisfy the steady-state conditions, using the last equation we can write:

$$
\begin{equation*}
V_{C}=-V_{o} / D \tag{5.17}
\end{equation*}
$$

So, the average voltage across L1 becomes:

$$
\begin{equation*}
\bar{V}_{L 1}=\left(V_{i}+(1-D) \cdot \frac{V_{o}}{D}\right)=0 \tag{5.18}
\end{equation*}
$$

Which can be written as:

$$
\begin{equation*}
\frac{V_{o}}{V_{i}}=\frac{-D}{1-D} \tag{5.19}
\end{equation*}
$$

It can be seen that this relation is the same as that obtained for the Buck Boost converter.


Fig 5.8: Gain Vs Duty cycle of Conventional Ćuk.

## Discontinuous Conduction Mode

Like all DC/DC converters Ćuk converters rely on the ability of the inductors in the circuit to provide continuous current, in much the same way a capacitor in a rectifier filter provides continuous voltage. If this inductor is too small or below the "critical inductance", then the inductor current slope will be discontinuous where the current goes to zero. This state of operation is usually not studied in much depth as it is generally not used beyond a demonstrating of why the minimum inductance is crucial, although it may occur when maintaining a standby voltage at a much lower current than the converter was designed for. The minimum inductance is given by:

$$
\begin{equation*}
L_{1} \min =\frac{(1-D)^{2} R}{2 D f_{s}} \tag{5.20}
\end{equation*}
$$

Where fs is the switching frequency.

## Chapter 6

## Zeta based Combined SC-SL Structure Analysis

### 6.1 Topology of proposed circuit

The proposed converter is showed in Fig. 6.1. It shows a modified zeta converter, which combines switched inductor switched capacitor using same power switches. Proposed switched inductor comprises two inductor L1 and L2 and three power diodes D1, D1 and D3. Similarly Switched capacitor comprises two energy transferring capacitors C1, C2 and two power diodes D4 and D5. Analogous to conventional zeta converter, our proposed converter also has one output inductor L0 and output capacitor C0 and load resistor R Load.


Figure 6.1: Proposed converter circuit

### 6.2 Assumptions

To simplify the circuit analysis, the following conditions are assumed:
$\checkmark$ The power MOSFET and Diode used in this converter are ideal.
$\checkmark$ Inductors $\mathrm{L} 1 \& \mathrm{~L} 2$ and capacitors $\mathrm{C} 1 \& \mathrm{C} 2$ are equal.
$\checkmark$ Inductor current $i_{L_{1}}$ and $i_{L_{2}}$ are operated in Continuous Conduction Mode.
$\checkmark$ The output capacitor Co is large enough so that the output voltage ripple can be ignored.
Based on these assumptions, there are basically two operating status in one-switching period of the proposed circuit under Continuous Conduction Mode.

### 6.3 Working Principle

There are two operating states in one switching period of the proposed circuit under continuous conduction mode (CCM). State one is when the switch is turned on and state two is when the switch is turned off.

### 6.3.1 Time Interval: $0<\mathrm{t}<\mathrm{DT}$

In this time interval switch S is on along with Diodes D1 \& D2. And Diodes D3, D4 \& D5 are turned off. Fig. 6.2. shows the current flow path of the proposed converter in this state. Inductor L1 \& L2 connected in parallel are energized by the voltage source Vin And their respective current IL1 \& IL2 are increased linearly by the ratio Vin/L1 \& Vin/L2 respectively. The change in inductor current of the inductor IL1 \& IL2 are given by the equation (1) and (2) respectively.

$$
\begin{align*}
& \Delta I_{L_{1}}^{I}=\frac{V_{L 1}}{L_{1}}\left(t_{1}-t_{0}\right)=\frac{V_{i n}}{L_{1}} D T_{S}  \tag{6.1}\\
& \Delta I_{L_{2}}^{I}=\frac{V_{L 2}}{L_{2}}\left(t_{1}-t_{0}\right)=\frac{V_{i n}}{L_{2}} D T_{S} \tag{6.2}
\end{align*}
$$



Figure 6.2: Current flow during switch on state

At the same time two series connected capacitors $\mathrm{C} 1 \& \mathrm{C} 2$ are discharging. The output inductor L 0 is energized by the discharging of capacitor C 1 . In this time interval output capacitor C 0 is charging. The load is supplied by the capacitors $\mathrm{C} 1 \& \mathrm{C} 2$.

### 6.3.2 Time Interval: $\mathrm{DT}<\mathrm{t}<\mathrm{T}$

In this time interval Switch S is turned off. Power diodes D1 \& D2 are also turned off. Rest of the Diodes D3, D4 \& D5 are turned on. Fig 6.3. shows the current flow path of this state. In this interval, the energy stored in inductor L1 \& L2 is released to capacitors C1 \& C2. Respective current IL1 \& IL2 are decreased non-linearly.


Figure 6.3: Current flow during switch off state

Capacitors C1 \& C2 are being charged and output capacitor C0 is being discharged in this time interval. In this mode load is supplied by output capacitor C0 and output inductor L0.

### 6.4 Steady State Analysis of proposed circuit

### 6.4.1 DC gain Analysis

As shown in Fig. 6.2. Inductor L1 \& L2 are directly energized by the voltage supply Vin. And output Inductor L0 is energized by the supply voltage and capacitors. Thus, the corresponding equations can be achieved for time $0<\mathrm{t}<\mathrm{DTs}$.

$$
\begin{gather*}
V_{L 1}=V_{i n}  \tag{6.3}\\
V_{L 2}=V_{i n}  \tag{6.4}\\
V_{L 0}=V_{i n}+2 V_{C}-V_{0} \tag{6.5}
\end{gather*}
$$

In Fig. 6.3. the energy stored in series connected inductors L1 \& L2 is released to capacitors C1 \& C2 which are connected in parallel. Output inductor L0 supply energy to the load. Corresponding equations can be achieved for time DTs $<\mathrm{t}<\mathrm{Ts}$.

$$
\begin{array}{r}
2 V_{L 1}=V_{C} \\
\text { Or } \quad V_{L 1}=\frac{1}{2} V_{C} \\
V_{L 0}=V_{0}-2 V_{L 1} \tag{6.7}
\end{array}
$$

By applying voltage-second balance principles on L1 \& L2 and L0 using equation (6.3), (6.5), (6.6), (6.7), we can get,

$$
\begin{array}{ll} 
& \frac{1}{T_{S}} \int_{0}^{T_{S}} V_{L 1} d t=0 \\
\text { Or } & \frac{1}{T_{S}}\left[\int_{0}^{D T_{S}} V_{L 1} d t+\int_{D T_{S}}^{T_{S}} V_{L 1} d t\right]=0 \\
\text { Or } & V_{i n} D-\frac{1}{2} V_{C}(1-D)=0 \tag{6.8}
\end{array}
$$

And for L0 we get,

$$
\frac{1}{T_{S}} \int_{0}^{T_{S}} V_{L 0} d t=0
$$

$$
\begin{align*}
& \text { Or } \quad \frac{1}{T_{S}}\left[\int_{0}^{D T_{S}} V_{L 0} d t+\int_{D T_{S}}^{T_{S}} V_{L 0} d t\right]=0 \\
& \quad \text { Or, }\left[V_{i n}+2 V_{C}-V_{0}\right] D-\left[V_{0}-2 V_{L 1}\right](1-D)=0 \tag{6.9}
\end{align*}
$$

Solving equation (8), the voltage across the capacitors C1 \& C2 is achieved by,

$$
\begin{equation*}
V_{C 1}=2 V_{i n} \frac{D}{1-D} \tag{6.10}
\end{equation*}
$$

Substituting equation (6.6) and (6.10) into equation (6.9) and solving it, we get

$$
\begin{gather*}
V_{i n}\left(D^{2}+3 D\right)=V_{0}(1-D) \\
\frac{V_{0}}{V_{i n}}=\frac{(3+D) D}{1-D}=G \tag{6.11}
\end{gather*}
$$

Which is (3+D) times larger than the conventional converter.

### 6.4.2 Average Current Analysis

The average current of the Inductors L1 \& L2 and output inductor L0 during state I can be obtained as follows: Ignoring very small current flow in output capacitor, Ico, we can assume that

$$
\begin{align*}
& I_{L 0}=I_{0}=\frac{V_{o}}{R} \\
& I_{L O}=\frac{V_{i n}(3+D) D}{R(1-D)} \tag{6.12}
\end{align*}
$$

Average current of the capacitors C1 \& C2 during state I:

$$
\begin{equation*}
I_{C 1_{o n}}=I_{C 2_{o n}}=I_{L 0}=\frac{V_{i n}(3+D) D}{R(1-D)} \tag{6.13}
\end{equation*}
$$

By applying amp - second balance principles on the capacitors C1 \& C2 to yield:

$$
\begin{array}{r}
\frac{1}{T_{S}}\left[\int_{0}^{D T_{S}} V_{L 0} d t+\int_{D T_{S}}^{T_{S}} V_{L 0} d t\right]=0 \\
I_{C 1_{o f f}} D=-I_{C 1_{o n}} \frac{D}{1-D}=-\frac{V_{\text {in }}(3+D) D^{2}}{R(1-D)^{2}} \\
\text { and } \\
I_{C 2_{o f f}}=-\frac{V_{\text {in }}(3+D) D^{2}}{R(1-D)^{2}} \tag{6.14}
\end{array}
$$

The average current through the Inductors L1 \& L2 can be derived as follows:

$$
\begin{equation*}
I_{L 1}=I_{L 2}=I_{C 1_{O F F}}+I_{C 2_{O F F}}+I_{L 0} \tag{6.15}
\end{equation*}
$$

Substituting equation (12) \& (14) into equation (15) and solving it, we can get,

$$
\begin{align*}
I_{L 1}=I_{L 2} & =2 \frac{V_{i n}(3+D) D^{2}}{R(1-D)}+\frac{V_{i n}(3+D) D}{R(1-D)} \\
& =\frac{V_{\text {in }}(3+D) D}{R(1-D)}\left[\frac{2 D}{1-D}+1\right] \\
& =\frac{V_{\text {in }}(3+D) D}{R(1-D)}\left(\frac{1+D}{1-D}\right)  \tag{6.16}\\
I_{L 1} & =I_{L 2}=I_{0} \frac{1+D}{1-D} \tag{6.17}
\end{align*}
$$

### 6.4.3 Current Stress Analysis of Switches

The current stress of the switch S (Is) and the Diodes D1, D2, D3, D4 \& D5 denoted as ID1, ID2, ID3, ID4 \& ID5 respectively can be obtained as follows,
eq $19,20,21$
Current stress of switch S: $\quad I_{S}=2 I_{L 1}+I_{C 1_{o n}}$

$$
=\frac{2 V_{i n}(3+D) D}{R(1-D)} * \frac{1+D}{1-D}+\frac{V_{i n}(3+D)}{R(1-D)}
$$

$$
\begin{align*}
\quad & =\frac{V_{\text {in }}(3+D) D}{R(1-D)}\left(\frac{3+D}{1-D}\right) \\
\text { So } \quad I_{S} & =I_{0}\left(\frac{3+D}{1-D}\right) \tag{6.18}
\end{align*}
$$

Current stress of Diodes D1, D2 \& D3:

$$
\begin{align*}
I_{D 1} & =I_{D 2}=I_{D 3}=I_{L 1}=I_{L 2} \\
& =\frac{V_{i n}(3+D) D}{R(1-D)}\left(\frac{1+D}{1-D}\right) \\
& =I_{0}\left(\frac{1+D}{1-D}\right) \tag{6.19}
\end{align*}
$$

Current stress of Diodes D4:

$$
\begin{align*}
& I_{D 4}=I_{L 1}-I_{C 1_{o f f}} \\
& =\frac{V_{\text {in }}(3+D) D}{R(1-D)}\left(\frac{1}{1-D}\right) \\
& =I_{0}\left(\frac{1+D}{1-D}\right) \tag{6.20}
\end{align*}
$$

Current stress of Diodes D5:

$$
\begin{align*}
I_{D 5} & =I_{C 1_{o f f}}+I_{L 0} \\
& =\frac{V_{i n}(3+D) D}{R(1-D)}\left(\frac{1}{1-D}\right) \\
& =I_{0}\left(\frac{1}{1-D}\right) \tag{6.21}
\end{align*}
$$

### 6.4.4 Voltage Stress Analysis of Components

The voltage stress on the switch S (Vs) can be achieved as follows:

$$
\begin{equation*}
V_{s}=V_{i n}+2 V_{L} \tag{6.22}
\end{equation*}
$$

Substituting equation (6.6), (6.10) into equation (6.22), we get:

$$
\begin{align*}
V_{s}= & V_{i n}+V_{i n} \frac{2 D}{1-D} \\
& =V_{i n} \frac{1+D}{1-D} \tag{6.23}
\end{align*}
$$

### 6.4.5 Power Loss and Efficiency Measurement

For efficiency Estimation parasitic resistances are defined as follows:

* Switch on-state resistance: $\quad r_{D S}$
* Forward resistance of Diodes: $R_{F_{x}}$
* Threshold voltage of Diode: $\quad V_{F_{x}}$
* ESR of the Inductors: $\quad R_{L_{x}}$
* ESR of the capacitors: $\quad r_{C_{x}}$


## For Switch:

Conduction loss of the switch $\mathrm{S}\left(P_{r_{D s}}\right)$ can be obtained as follows:

$$
\begin{align*}
P_{r D S}= & r_{D S} I_{s, r m s}^{2} \\
& =r_{D S} I_{0}^{2}\left(\frac{3+D}{1-D}\right)^{2} \tag{6.24}
\end{align*}
$$

And switching loss (Psw) can be achieved as follows:

$$
\begin{equation*}
P_{s w}=f_{s} C_{s} V_{s}^{2}=f_{s} C_{s} V_{i n}^{2}\left(\frac{1+D}{1-D}\right)^{2} \tag{6.25}
\end{equation*}
$$

So total loss of switch S:

$$
\begin{equation*}
P_{s w}=P_{r D S}+\frac{1}{2} P_{s w} \tag{6.26}
\end{equation*}
$$

## For Diodes:

The losses of the Diodes D1, D2 \& D3 can be obtained as follows:

$$
\begin{equation*}
P_{D_{1,2,3}}=R_{F_{1,2,3}} I_{0}^{2}\left(\frac{1+D}{1-D}\right)^{2}+V_{F_{1,2,3}} I_{0} \tag{6.27}
\end{equation*}
$$

For Diodes D4 \& D5 losses can be obtained as follows:

$$
\begin{equation*}
P_{D_{4,5}}=R_{F_{4,5}} I_{0}^{2}\left(\frac{1}{1-D}\right)^{2}+V_{F_{4,5}} I_{0} \tag{6.28}
\end{equation*}
$$

## For capacitors:

The losses of capacitors C1, C2 \& Co can be achieved as follows:

$$
\begin{align*}
& P_{C_{1,2}}=r_{C_{1,2}} I_{C_{1,2} o n}^{2}+r_{C_{1,2}} I_{C_{1,2} o f f}^{2} \\
& =r_{C_{1,2}}\left[\frac{V_{i n}(3+D) D}{R(1-D)}\right]^{2}+r_{C_{1,2}}\left[\frac{V_{i n}(3+D) D}{R(1-D)}\right]^{2} \\
& \quad \text { So, } \quad P_{C_{1,2}}=r_{C_{1,2}} I_{0}^{2}+r_{C_{1,2}} I_{0}^{2}\left(\frac{1}{1-D}\right)^{2} \tag{6.29}
\end{align*}
$$

## For inductors:

The losses of inductors L1, L2 can be achieved as follows:

$$
\begin{align*}
& P_{L_{1,2}}=R_{L_{1,2}} I_{L_{1,2}}^{2} \\
& =R_{L_{1,2}}\left[\frac{V_{i n}(3+D) D(1+D)}{R(1-D)}\right]^{2} \\
& \text { So, } \quad P_{L_{1,2}}=R_{L_{1,2}} I_{o}^{2}\left(\frac{1+D}{1-D}\right)^{2} \tag{6.30}
\end{align*}
$$

## Total Loss:

The total loss of the proposed converter $\left(P_{\text {loss }}\right)$ can be expressed as follows:

$$
\begin{equation*}
P_{\text {loss }}=P_{s w}+P_{D_{1,2,3}}+P_{D_{4,5}}+P_{L_{1,2}}+P_{C_{1,2}} \tag{6.31}
\end{equation*}
$$

According to above equations, the efficiency of the proposed converter can be obtained as follows:

$$
\begin{equation*}
\eta=\frac{\rho_{0}}{\rho_{0}+\rho_{l o s s}}=\frac{1}{1+\frac{\rho_{\text {loss }}}{\rho_{0}}} \tag{6.32}
\end{equation*}
$$

### 6.5 Simulation Results

### 6.5.1 Assumptions

The simulations were done using the software PSIM Version 9.1 and MATLAB R2018a. All the components were assumed to be ideal.

- Switching frequency $=100 \mathrm{kHz}$
- Input Voltage, Vin = 12 V DC
- L1, L2 and L0 $=100 \mu \mathrm{H}$
- C 1 and $\mathrm{C} 2=1 \mu \mathrm{~F}$
- $\mathrm{C} 0=220 \mu \mathrm{~F}$


### 6.5.2 Waveforms of voltages and currents

Voltmeters were connected across inductors and capacitors to observe the voltage waveshapes and the ammeters were connected in series to observe the current waveshapes through the components. The simulation is performed at a duty cycle of $40 \%$. The simulated waveforms are shown in Fig 6.5 following the PSIM circuit snapshot given below in Fig 6.4.


Figure 6.4: Snapshot of proposed circuit with ammeters and voltmeters connected in PSIM


Figure 6.5: Voltage and Current waveforms of the proposed circuit

### 6.5.3 Comparison of Gain

## i) Comparison of Theoretical and Simulated gain

A graph was plotted in Fig.6.6 using the derived equation from the theoretical analysis of gain in (11) and compared with the simulation results obtained at various duty cycles taking the input voltage as 12 VDC. From the figure it is clear that the theoretical and simulated results are identical agree with each other.

TABLE 6.1: THEORETICAL AND SIMULATED GAIN OF PROPOSED STEP UP CONVERTER

| Duty | Theoretical <br> Output <br> Voltage | Theoretical <br> Gain | Simulated <br> Output <br> Voltage | Simulated <br> Gain |
| :---: | :---: | :---: | :---: | :---: |
| 0.5 | 42.00 | 3.50 | 42.40 | 3.53 |
| 0.6 | 64.80 | 5.40 | 65.60 | 5.46 |
| 0.7 | 103.60 | 8.63 | 104.90 | 8.74 |
| 0.8 | 182.40 | 15.20 | 264.00 | 15.36 |
| 0.9 | 421.20 | 35.10 | 424.00 | 35.33 |



Figure 6.6: Graph of Theoretical and Simulated gain against duty cycle.

## ii) Comparison with existing converters

Comparison of gain with the existing converters of other notable published work has been done in Fig. 6.7. It is shown that our proposed converter circuit is able to provide superior gain compared to the existing converters and other transformer less topologies with single active switch and similar parts count.

TABLE 6.2: VOLTAGE GAIN OF THE PROPOSED CONVERTER AND OTHER EXISTING STEP-UP CONVERTERS

| Duty <br> Cycle | Proposed <br> Circuit | Circuit <br> in [12] | Circuit <br> in [14] | Circuit <br> in [15] | Circuit <br> in [16] | Conventional <br> Zeta |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.5 | 3.50 | 4.00 | 3.00 | 2.00 | 4.00 | 1.00 |
| 0.6 | 5.40 | 5.00 | 4.50 | 3.00 | 4.50 | 1.50 |
| 0.7 | 8.63 | 6.67 | 7.00 | 4.67 | 5.33 | 2.33 |
| 0.8 | 15.2 | 10.00 | 12.00 | 8.00 | 7.00 | 4.00 |
| 0.9 | 35.1 | 20.00 | 27.00 | 18.00 | 12.00 | 9.00 |



Figure 6.7: Gain against duty cycle comparison between existing converter

### 6.5.4. Comparison of Voltage stress

The voltage stress across the switch of the proposed converter was analyzed. The voltage stress at various duty cycle was calculated and then compared with one of the existing converters in the Fig. 6.8.


Figure 6.8: Graph of voltage stress against gain of proposed converter compared with different modes of operation in an existing converter

### 6.5.5 Efficiency Results

In Fig. 6.9 the efficiency of our proposed converter circuit was plotted against various load resistance. From this figure we can see that efficiency peaks at around 500-1000W of power output and then it drops on either side.

TABLE 6.3: EFFICIENCY AND POWER OUTPUT OF PROPOSED CONVERTER CIRCUIT

| Power (W) | Efficiency (\%) |
| :---: | :---: |
| 202.0 | 98.30 |
| 353.3 | 98.53 |
| 403.7 | 98.55 |
| 470.9 | 98.56 |
| 705.9 | 98.56 |
| 940.5 | 98.55 |
| 1128.0 | 98.53 |
| 1408.0 | 98.49 |
| 1875.0 | 98.43 |



Figure 6.9: Converter operating efficiency at different output power.

### 6.5.6 Comparison Tables:

TABLE 6.4: COMPARISON BETWEEN PROPOSED CONVERTER AND EXISTING CONVERTER CIRCUITS

|  | Proposed <br> Circuit | Circuit in <br> [15] | Circuit <br> in [13] | Circuit <br> in [14] |
| :---: | :---: | :---: | :---: | :---: |
| Switches | 1 | 1 | 2 | 1 |
| Diodes | 5 | 2 | 1 | 3 |
| Capacitor | 3 | 4 | 3 | 5 |
| Inductor | 3 | 3 | 2 | 3 |
| Total <br> component | 12 | 10 | 8 | 12 |
| Voltage <br> stress | $\frac{V_{\text {in }}(1+D)}{1-D}$ | $\frac{V_{0}+2 V_{\text {in }}}{2 V_{\text {in }}}$ | $\frac{V_{0}}{V_{\text {in }}}$ | $\frac{V_{0}+3}{3}$ |
| Gain | $\frac{(3+D) D}{1-D}$ | $\frac{2 D}{1-D}$ | $2 D$ | $\frac{3 D}{1-D}$ |

TABLE 6.5: GAIN AND STRESS EQUATIONS OF VARIOUS CONVERTERS

| Converter | Gain | Stress |
| :---: | :---: | :---: |
| Proposed <br> Circuit | $\frac{(3+D) D}{1-D}$ | $\frac{1+D}{1-D}$ |
| Mode 1 in <br> [16] | $\frac{3-D}{1-D}$ | $\frac{1+D}{1-D}$ |
| Mode 2 in <br> [16] | $\frac{3-2 D}{1-D}$ | $\frac{2+D}{1-D}$ |
| Mode 3 in <br> [16] | $\frac{2-D}{1-D}$ | $\frac{1}{1-D}$ |

### 6.6 Conclusion

From the mathematical analysis and the simulation results, it was shown that the proposed converter provided a gain of (3+D) times more than a conventional zeta converter without the additional active switch or transformer. The converter is also capable of delivering approximately 1 kW at an efficiency above $98.5 \%$. Thus, the converter can suitably be used in battery-powered applications where high gain at low losses are required such as $12-380 \mathrm{~V}$ DC conversions in renewable energy systems.

## Chapter 7

## Ćuk based Combined SC-SL Structure Analysis

### 7.1 Topology of proposed circuit

In Fig 7.1 the structure of the proposed circuit is shown, which is Ćuk derived sC-sL based DC-DC converter. As seen, the converter combines switched capacitor and switched inductor using a single power switch. This switched inductor cell used in proposed stepdown converter comprises of two inductors L1, L2 and two power diodes D1 \& D2. Similarly switched capacitor cells used in proposed step-down converter comprises of two capacitors C1 \& C2 and three power diodes D1, D2 and D3. This converter has adjustable voltage gain, slightly lower than that of conventional step-down converter.


Figure 7.1: Proposed converter circuit

### 7.2 Assumptions

To simplify the circuit analysis, the following conditions are assumed:

- The power MOSFET and Diode used in this converter are ideal.
- Inductors $\mathrm{L} 1 \& \mathrm{~L} 2$ and capacitors $\mathrm{C} 1 \& \mathrm{C} 2$ are equal.
- Inductor current $i_{L_{1}}$ and $i_{L_{2}}$ are operated in Continuous Conduction Mode.
- The output capacitor Co is large enough so that the output voltage ripple can be ignored.
Based on these assumptions, there are basically two operating status in one-switching period of the proposed circuit under Continuous Conduction Mode.


### 7.3 Working Principle

The proposed converter contains two different operating states in one switching period of the circuit under continuous conduction mode (CCM). State ON is when the switch is turned on \& state OFF is when the switch is turned off.

### 7.3.1 Time Interval: $0<\mathrm{t}<\mathrm{DT}$

In this time interval switch S is turned on along with diodes D1 and D2. Diodes D3, D4 and D5 are turned off. Fig 7.2 shows the current flow paths of the proposed converter in this state. Input inductor Lin is energized by the voltage source Vin and the input inductor current is increased linearly by the ratio $V_{\text {in }} / L_{\text {in }}$.Thus the variations of the input inductor current $I_{L_{i n}}$ is defined by the equation:

$$
\begin{align*}
\Delta I_{L_{i n}}^{I} & =V_{\text {in }} / L_{\text {in }}\left[t_{1}-t_{0}\right] \\
& =V_{\text {in }} / L_{\text {in }} D T_{s} \tag{7.1}
\end{align*}
$$

At the same time, two parallel connected capacitors C1 and C2 are discharging. The output inductors L2 and L3 are energized by the discharging of the capacitors. In this time duration output capacitor C 0 is discharging. The load is supplied by the discharging currents of the capacitors $\mathrm{C} 1, \mathrm{C} 2$ and C 0 .


Figure 7.2: Current flow during switch on state

### 7.3.2 Time Interval: $\mathrm{DT}<\mathrm{t}<\mathrm{T}$

In this time interval switch S is turned OFF \& power diodes D1 and D2 are also turned OFF. Rest of the diodes D3, D4 and D5 are turned ON. Fig. 3 shows the current flow path of this state. During this interval of time, the energy stored in the inductor Lin is released to the series connected capacitors C1 \& C2. The input inductor current is decreased nonlinearly and can be expressed by the following equation:

$$
\begin{align*}
\Delta L_{L_{i n}}^{I I} & =V_{i n} / L_{i n}\left[t_{2}-t_{1}\right] \\
& =\frac{2 V_{c}-V_{i n}+V_{o}}{L_{i n}}[1-D] T_{s} \tag{7.2}
\end{align*}
$$



Figure 7.3: Current flow during switch off state

Capacitors C1 and C2 and also output capacitor Co are being charged in this interval. In this state, load is supplied by the output inductors L2 and L3.

### 7.4 Steady State Analysis of proposed circuit

### 7.4.1 DC gain Analysis

As shown in Fig.7.2, input inductor Lin is directly energized by the voltage supply Vin. Output inductors L1 and L2 are energized by the output voltage. Thus, the corresponding equations can be achieved for time $0<t<$ DTs:

$$
\begin{align*}
& V_{L_{i n}}=V_{i n}  \tag{7.3}\\
& V_{L_{1,2}}=\frac{1}{2}\left[V_{c}-V_{o}\right] \tag{7.4}
\end{align*}
$$

In Fig 7.3 the energy stored in input inductor Lin is released to the series connected capacitors C1 and C2 and output inductors L1 and L2 are released to the load. Corresponding equations can be derived for time DTs $<\mathrm{t}<\mathrm{Ts}$ :

$$
\begin{gather*}
-V_{i n}-V_{L_{i n}}+2 V_{c}+V_{o}=0 \\
V_{L_{i n}}=2 V_{c}-V_{i n}+V_{o} \tag{7.5}
\end{gather*}
$$

$$
\begin{equation*}
\text { And, } V_{L_{1,2}}=V_{o} \tag{7.6}
\end{equation*}
$$

By applying voltage-second balance principle on input inductor (Lin) using equation (7.3) and (7.5) we get:

$$
\begin{gather*}
\frac{1}{T_{s}} \int_{0}^{T_{s}} V_{L_{\text {in }}} d t=0 \\
\frac{1}{T_{s}}\left[\int_{0}^{D T_{s}} V_{L_{i n}} d t+\int_{D T_{s}}^{T_{s}} V_{L_{i n}} d t\right]=0 \\
\text { Or, } \quad V_{\text {in }} D-\left(2 V_{c}-V_{\text {in }}+V_{o}\right)(1-D)=0 \tag{7.7}
\end{gather*}
$$

And again, by applying voltage-second balance principle on L1 or L2 using equation (7.4) and (7.6) we get:

$$
\begin{array}{ll} 
& \frac{1}{T_{s}} \int_{0}^{T_{s}} V_{L_{1,2}} d t=0 \\
& \frac{1}{T_{s}}\left[\int_{0}^{D T_{s}} V_{L_{1,2}} d t+\int_{D T_{s}}^{T_{s}} V_{L_{1,2}} d t\right]=0 \\
\text { Or, } \quad & \frac{1}{2}\left(V_{c}-V_{o}\right) D-V_{o}(1-D)=0 \tag{7.8}
\end{array}
$$

Solving equation (7.7), voltage across the capacitor C1 or C2 is achieved by:

$$
\begin{equation*}
V_{C_{1,2}}=1 / 2\left[\frac{V_{i n}}{1-D}-V_{o}\right] \tag{7.9}
\end{equation*}
$$

By substituting $V_{c_{1,2}}$ from equation (7.9) into equation (7.8) we get:

$$
\begin{gather*}
\frac{1}{2}\left[\frac{1}{2}\left(\frac{V_{i n}}{1-D}-V_{o}\right)-V_{o}\right] D-V_{o}(1-D)=0 \\
V_{i n} \frac{D}{4(1-D)}=V_{o} \frac{(4-D)}{4} \\
\frac{V_{o}}{V_{i n}}=\frac{D}{(4-D)(1-D)}=G \tag{7.10}
\end{gather*}
$$

Which is (4-D) times lower than the conventional Ćuk converter.

### 7.4.2 Average Current Analysis

The average current of the inductor L1 or L2 and input inductor Lin during state ON can be obtained as follows:

Average input inductor current:

$$
\begin{align*}
& I_{L_{i n}}=I_{i n}=I_{o} \frac{D}{(4-D)(1-D)} \\
& I_{L_{i n}}=\frac{V_{i n}}{R}\left[\frac{D}{(4-D)(1-D)}\right]^{2} \tag{7.11}
\end{align*}
$$

Average current of the capacitors C1 and C2 during state OFF can be achieved from:

$$
\begin{equation*}
I_{C_{1,2} O F F}=I_{C_{1,2} \text { OFF }}=I_{L_{i n}}=\frac{V_{\text {in }}}{R}\left[\frac{D}{(4-D)(1-D)}\right]^{2} \tag{7.12}
\end{equation*}
$$

By applying amp-second balance principle on the capacitors C 1 and C 2 to yield:

$$
\begin{gather*}
\frac{1}{T_{s}} \int_{0}^{T_{s}} I_{C_{1,2}} d t=0 \\
\frac{1}{T_{s}}\left[\int_{0}^{D T_{s}} I_{C_{1,2} O N} d t-\int_{D T_{s}}^{T_{s}} I_{C_{1,2} O F F} d t\right]=0 \\
I_{C_{1,2} O N} D-I_{C_{1,2} O F F}(1-D)=0 \\
I_{C_{1,2} O N}=I_{C_{1,2} O F F}\left(\frac{1-D}{D}\right)  \tag{7.13}\\
I_{C_{1,2} O N}=\frac{V_{\text {in }}}{R} \frac{D}{(4-D)^{2}(1-D)} \tag{7.14}
\end{gather*}
$$

From equation (7.12)

The average current through the inductor L1 and L2 are:

$$
\begin{align*}
& I_{L_{1,2}}=I_{C_{1} O N}+I_{C_{2} O N}=2 I_{C_{1,2} O N} \\
& I_{L_{1,2}}=\frac{2 V_{i n}}{R} \frac{D}{(4-D)^{2}(1-D)} \tag{7.15}
\end{align*}
$$

Diode currents of the switched inductor ID4 and ID4 can be derived from:

$$
\begin{align*}
I_{D_{4,5}} & =I_{L_{1,2}}+I_{C_{1}}{ }_{\text {OFF }} \\
& =\frac{V_{\text {in }}}{R}\left[\frac{D(2-D)}{\{(4-D)(1-D)\}^{2}}\right] \tag{7.16}
\end{align*}
$$

Again, average output capacitor current during the state OFF can be obtained as follows:

$$
\begin{array}{ll} 
& I_{C_{O_{O F F}}}=\left(I_{L_{1,2}}+I_{D}\right)-I_{O} \\
\text { So, } & I_{C_{O_{O F F}}}=\frac{V_{i n}}{R(1-D)(4-D)}\left[\frac{2 D}{(4-D)}+\frac{D(2-D)}{(1-D)(4-D)}-D\right] \\
\text { Or, } & I_{C_{O_{O F F}}}=\frac{V_{i n}}{R}\left[\frac{D^{2}(2-D)}{\{(4-D)(1-D)\}^{2}}\right]
\end{array}
$$

Applying amp-second balance equation on output capacitor C0 we have:

$$
\begin{gather*}
\frac{1}{T_{S}} \int_{0}^{T_{s}} I_{C_{o}} d t=0 \\
\frac{1}{T_{S}}\left[\int_{0}^{D T_{s}} I_{C_{O_{O N}}} d t-\int_{D T_{S}}^{T_{S}} I_{C_{O_{O F F}}} d t\right]=0 \\
I_{C_{O_{O N}}} D-I_{C_{O_{O F F}}}(1-D)=0 \\
I_{C_{O_{O N}}}=I_{C_{O_{O F F}}} \frac{1-D}{D} \\
I_{C_{O_{O N}}}=\frac{V_{\text {in }}}{R} \frac{D(2-D)}{(4-D)^{2}(1-D)} \tag{7.18}
\end{gather*}
$$

### 7.4.3 Current Stress Analysis of Switches

The current stress of the switch S \& the diodes D1-D5 denoted as IS, ID1-ID5 can be found as below:

Switch current stress:

$$
I_{S}=2 I_{C_{1 O N}}+I_{L_{1}}
$$

So,

$$
\begin{align*}
I_{S} & =\frac{V_{\text {in }}}{R} \frac{D(2-D)}{\{(1-D)(4-D)\}^{2}} \\
I_{S} & =I_{o} \frac{(2-D)}{(4-D)} \tag{7.19}
\end{align*}
$$

Diode current stress $I_{D_{1}} \& I_{D_{2}}: I_{D_{1,2}}=I_{C_{1} O N}$

$$
\begin{align*}
& I_{D_{1,2}}=\frac{V_{i n}}{R} \frac{D}{(4-D)^{2}(1-D)} \\
& I_{D_{1,2}}=I_{o} \frac{1}{(4-D)} \tag{7.20}
\end{align*}
$$

Diode current stress $I_{D_{3}}: \quad I_{D_{3}}=I_{C_{1} \text { OFF }}$

$$
\begin{align*}
& I_{D_{3}}=\frac{V_{i n}}{R}\left[\frac{D}{(4-D)(1-D)}\right]^{2} \\
& I_{D_{3}}=I_{o} \frac{D}{(4-D)(1-D)}=I_{i n} \tag{7.21}
\end{align*}
$$

Diode current stress $I_{D_{4}} \& I_{D_{5}}: I_{D_{4,5}}=\frac{V_{\text {in }}}{R} \frac{D(2-D)}{(1-D)(4-D)^{2}}$

$$
\begin{equation*}
I_{D_{4,5}}=I_{o} \frac{(2-D)}{(4-D)(1-D)} \tag{7.22}
\end{equation*}
$$

### 7.4.4 Voltage Stress Analysis of Components

The voltage stress on the switch $S$ can be obtained as follows:

$$
\begin{equation*}
V_{s}=V_{i n}+V_{L_{i n}} \tag{7.23}
\end{equation*}
$$

Substituting (5) \& (9) into (23) we get,

$$
\begin{equation*}
V_{S}=V_{i n} \frac{1}{(1-D)} \tag{7.24}
\end{equation*}
$$

### 7.4.5 Power Loss and Efficiency Measurement

For efficiency Estimation parasitic resistances are defined as follows:

* Switch on-state resistance: $\quad r_{D S}$
* Forward resistance of Diodes: $R_{F_{x}}$
* Threshold voltage of Diode: $\quad V_{F_{x}}$
* ESR of the Inductors: $\quad R_{L_{x}}$
* ESR of the capacitors: $\quad r_{C_{x}}$

For Switch:
Conduction loss of the switch $\mathrm{S}\left(P_{r_{D S}}\right)$ can be obtained as follows:

$$
\begin{align*}
P_{r_{D S}} & =r_{D S} I_{s, r m s}^{2} \\
& =r_{D S} I_{o}^{2}\left\{\frac{(2-D)}{(4-D)}\right\}^{2} \tag{7.25}
\end{align*}
$$

And switching loss (Psw) can be achieved as follows:

$$
\begin{equation*}
P_{s w}=f_{s} C_{s} V_{s}^{2}=f_{s} C_{s} V_{i n}^{2}\left\{\frac{1}{1-D}\right\}^{2} \tag{7.26}
\end{equation*}
$$

So total loss of switch S :

$$
\begin{equation*}
P_{s w i t c h}=P_{r D S}+P_{s w} / 2 \tag{7.27}
\end{equation*}
$$

## For Diodes:

The losses of the Diodes D1 \& D2 can be obtained as follows:

$$
\begin{equation*}
P_{D_{1,2}}=R_{F_{1,2}} I_{o}^{2}\left\{\frac{1}{4-D}\right\}^{2}+V_{F_{1,2}} I_{o} \tag{7.28}
\end{equation*}
$$

For Diodes D3 losses can be obtained as follows:

$$
\begin{equation*}
P_{D_{3}}=R_{F_{3}} I_{o}^{2}\left\{\frac{D}{(4-D)(1-D)}\right\}^{2}+V_{F_{3}} I_{o} \tag{7.29}
\end{equation*}
$$

For Diodes D4 \& D5 losses can be obtained as follows:

$$
\begin{equation*}
P_{D_{4,5}}=R_{F_{4,5}} I_{o}^{2}\left\{\frac{(2-D)}{(4-D)(1-D)}\right\}^{2}+V_{F_{4,5}} I_{o} \tag{7.30}
\end{equation*}
$$

## For capacitors:

The losses of capacitors C1 and C2 can be achieved as:

$$
\begin{align*}
P_{C_{1,2}} & =r_{C_{1,2}} I_{C_{1,2} O N}+r_{C_{1,2}} I_{C_{1,2} O F F} \\
= & r_{C_{1,2}}\left[\frac{V_{\text {in }}}{R} \frac{D}{(4-D)^{2}(1-D)}\right]^{2}+r_{C_{1,2}}\left[\frac{V_{\text {in }}}{R}\left[\frac{D}{(4-D)(1-D)}\right]^{2}\right]^{2} \\
& =r_{C_{1,2}} I_{o}^{2}\left\{\frac{1}{4-D}\right\}^{2}+r_{C_{1,2}} I_{o}^{2}\left\{\frac{D}{(4-D)(1-D)}\right\}^{2} \tag{7.31}
\end{align*}
$$

And the loss of output capacitor Co can be derived as follows:

$$
\begin{align*}
P_{C_{o}} & =r_{C_{o}} I_{C_{o}}{ }^{2}+r_{C_{o}} I_{C_{O_{O F F}}}{ }^{2} \\
& =r_{C_{o}}\left[\frac{V_{\text {in }}}{R} \frac{D(2-D)}{(4-D)^{2}(1-D)}\right]^{2}+r_{C_{o}}\left[\frac{V_{\text {in }}}{R}\left[\frac{D^{2}(2-D)}{\{(4-D)(1-D)\}^{2}}\right]^{2}\right. \\
& =r_{C_{o}} I_{o}^{2}\left\{\frac{(2-D)}{(4-D)}\right\}^{2}+r_{C_{o}} I_{o}^{2}\left\{\frac{D(2-D)}{(4-D)(1-D)}\right\}^{2} \tag{7.32}
\end{align*}
$$

## For inductors:

The losses of input inductor Lin and output inductors L1 and L2 can be obtained as follows:

$$
\begin{align*}
P_{L_{i n}}=R_{L_{i n}} I_{L_{i n}} & =\frac{V_{i n}}{R}\left[\frac{D}{(4-D)(1-D)}\right]^{2} \\
& =R_{L_{i n}} I_{o}^{2}\left[\frac{D}{(4-D)(1-D)}\right]^{2} \tag{7.33}
\end{align*}
$$

And,

$$
\begin{align*}
P_{L_{1,2}}=R_{L_{1,2}} I_{L_{1,2}} & =\frac{2 V_{i n}}{R} \frac{D}{(4-D)^{2}(1-D)} \\
& =R_{L_{1,2}} I_{o}^{2}\left[\frac{2}{(4-D)}\right]^{2} \tag{7.34}
\end{align*}
$$

## Total Loss:

The total loss of the proposed converter $\left(P_{\text {loss }}\right)$ can be expressed as follows:

$$
\begin{equation*}
P_{\text {Loss }}=P_{\text {Switch }}+\sum_{n=1}^{5} P_{D_{n}}+\sum_{n=0}^{2} P_{C_{n}}+\sum_{n=1}^{3} P_{L_{n}} \tag{7.35}
\end{equation*}
$$

According to above equations, the efficiency of the proposed converter can be obtained as follows:

$$
\begin{equation*}
\mu=\frac{P_{o}}{P_{o}+P_{\text {Loss }}}=\frac{1}{1+\frac{P_{\text {Loss }}}{P_{o}}} \tag{7.36}
\end{equation*}
$$

### 7.5 Simulation Results

### 7.5.1 Assumptions

All the components were assumed to be ideal and lossless. The simulations were done using the software PSIM Version 9.1 and MATLAB R2018a. The circuit parameters were taken as:

- Switching frequency, fS = 100 kHz
- Input Voltage, Vin = 380V DC
- L 1 and $\mathrm{L} 2=1 \mathrm{mH}$
- C 1 and $\mathrm{C} 2=0.1 \mu \mathrm{~F}$
- Lin $=100 \mathrm{mH}$
- $\mathrm{C} 0=220 \mu \mathrm{~F}$


### 7.5.2 Waveforms of voltages and currents

Voltmeters were connected across inductors and capacitors to observe the voltage waveshapes and the ammeters were connected in series to observe the current waveshapes through the components. The simulation is performed at a duty cycle of $40 \%$. The simulated waveforms are shown in Fig.7.5 following the PSIM circuit snapshot given below in Fig 7.4:


Figure 7.4: Snapshot of proposed converter circuit with ammeters and voltmeters connected in PSIM


Figure 7.5: Simulated Waveforms

### 7.5.3 Comparison of Gain

## i) Comparison of Theoretical and Simulated gain

A graph was plotted in Fig.7.6 using the derived equation from the theoretical analysis of gain in (10) and compared with the simulation results obtained at various duty cycles. From the figure it is clear that the theoretical and simulated results are identical agree with each other.

TABLE 7.1: THEORETICAL AND SIMULATED GAIN OF PROPOSED STEP-DOWN CONVERTER

| Duty <br> Cycle | Theoretical <br> Output Voltage | Theoretical <br> Gain | Simulated <br> Output Voltage | Simulated <br> Gain |
| :---: | :---: | :---: | :---: | :---: |
| 0.1 | 10.82 | 0.0285 | 10.60 | 0.0279 |
| 0.2 | 25.00 | 0.0658 | 25.00 | 0.0658 |
| 0.3 | 44.02 | 0.1158 | 44.00 | 0.1158 |
| 0.4 | 70.37 | 0.1852 | 70.50 | 0.1855 |
| 0.5 | 108.57 | 0.2857 | 100.1 | 0.2634 |



Figure 7.6: Comparison of Theoretical and Simulated gain against duty cycle

## ii) Comparison with existing converters

Comparison of gain with the existing converters of other notable published work has been done in Fig.7.7. It is shown that our proposed converter circuit is able to provide superior step-down conversion ratio compared to the conventional converter and other or transformer less topologies with single active switch and similar parts count.

TABLE 7.2: VOLTAGE GAIN OF THE PROPOSED CONVERTER AND OTHER EXISTING STEP-DOWN CONVERTERS

| Duty <br> Cycle | Proposed <br> Circuit | Ćuk <br> Dn1/Dn2 <br> in [13] | Circuit in <br> [14] | Type II <br> DPDC in <br> [16] | Conventional <br> Ćuk |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0.1 | 0.0285 | 0.0556 | 0.0526 | 0.1818 | 0.1111 |
| 0.2 | 0.0658 | 0.1250 | 0.1111 | 0.3333 | 0.2500 |
| 0.3 | 0.1158 | 0.2143 | 0.1765 | 0.4615 | 0.4286 |
| 0.4 | 0.1852 | 0.3333 | 0.2500 | 0.5714 | 0.6667 |
| 0.5 | 0.2857 | 0.5000 | 0.3333 | 0.6667 | 1.0000 |



Figure 7.7: Gain against duty cycle comparison between existing converter

### 7.5.4 Load Regulation

In Fig.7.8 the output voltage is plotted against output current by varying load resistance at a fixed duty cycle to check the load regulation of this circuit. It is clear that the converter performs optimally within a maximum output current of 100A which is equivalent to a power output of 1.5 KW .

TABLE 7.3: OUTPUT VOLTAGE AND OUTPUT CURRENT OF THE PROPOSED CIRCUIT

| Output Voltage (V) | Output Current (A) |
| :---: | :---: |
| 15.12 | 15.12 |
| 15.11 | 18.88 |
| 15.10 | 25.16 |
| 15.09 | 37.73 |
| 15.07 | 75.35 |
| 15.05 | 100.33 |
| 14.80 | 123.33 |
| 13.76 | 137.60 |



Figure 7.8. Load regulation of the proposed converter circuit

### 7.5.5 Comparison Table:

TABLE 7.4: COMPARISON TABLE OF PROPOSED CONVERTER WITH EXISTING CONVERTER CIRCUITS

| Components | Proposed <br> Circuit | Circuit <br> in [16] | Circuit <br> in [15] | Cûk <br> Hybrid <br> in [13] |
| :---: | :---: | :---: | :---: | :---: |
| Switches | 1 | 4 | 5 | 1 |
| Capacitor | 3 | 2 | 3 | 3 |
| Inductor | 3 | 1 | 2 | 2 |
| Total <br> component | $(7)$ | $(7)$ | $(10)$ | $(6)$ |
| Gain | $\frac{D}{(4-D)(1-D)}$ | $\frac{2 D}{1+D}$ | $\frac{D}{3}$ | $\frac{D}{2(1-D)}$ |

### 7.6 Conclusion

The new proposed Ćuk converter topology is able to provide (4-D) times lower voltage than a conventional Ćuk converter. The converter also exhibits very high efficiency and good load regulation up to 1.5 KW of power output which makes it ideal for application with very high step-down voltage conversion requirement.

## Chapter 8

## Conclusion

### 8.1 Summary

We already know that power electronic converters hold up much importance in the day-to-day life for energy applications in order to meet consumer demands. In the last few decades, significant developments in the field of power electronics have mostly been influenced by some key factors. The most notable thing is the increasing demand towards the use of sustainable energy technology and the introduction of clean energy production to reduce global warming. Energy distribution systems based on HVDC, versatile AC transmission systems, a growth in electric vehicles, fast and lightweight charging requirements were also significant driving factors. Retaining electricity at a lower voltage level has become a rising necessity which turned out the drive towards DC-DC converters. Hence, DC-DC converters occupy great importance in power engineering mostly due to its digital and industrial uses.

In the last decade, electronic converters shifted to switching mode converters which ensure high power density of the converter. The large voltage conversion ratio dramatically answers the issues of high demand and more efficient technology. The switches are mainly diodes and transistors (such as MOSFET) where the passive elements are inductors and capacitors. They mainly contribute to the large gain through a cycle of charging and discharging. Moreover, some voltage boosting techniques have been developed which provide for the large output utilizing a combination of switches and storage elements of the circuits. The boosting techniques are mainly:
switched capacitor or charge pump (SC or CP), voltage multiplier, switched inductor and voltage lift (SL \& VL), magnetic coupling, and converters with multistage or multilevel structures. Switched capacitor and switched inductor structures are mainly utilized in building the hybrid DC-DC structures that provide both step-up and step-down voltage ratios. DC-DC converters are also classified into several categories depending on their quadrant operations.

Zeta and Ćuk converters were utilized in this research to design the hybrid converters by using SC and SL structures. These converters operate in two quadrants i.e. It's a multiquadrant converter. Mathematical analysis and simulation results state that the converters are providing higher step-up gain and lower step-down gain than their conventional counterparts. The enhanced converters are a step forward in combining various voltage boosting techniques with DC-DC converter circuits and experimentation regarding the finding of the most efficient structures in power electronics. The proposed hybrid zeta converter provides a gain of ( $3+\mathrm{D}$ ) times more than a conventional zeta and the proposed step-down hybrid Ćuk converter provides a gain of (4-D) times lower than a conventional Ćuk converter.

The endeavors lead to the completion of the objectives of the proposal by properly realizing such hybrid structures. Mathematical analysis was done for both the converters
such as deriving voltage gain expressions, Current and voltage stress equations and efficiency analysis. The experimented results were compared with the theoretical results and the legitimacy of the converters were hence proved. The voltage gain was also higher compared to other classes of converters and their regulation characteristics were observed.

### 8.2 Future Contributions

Across nearly all sectors of the electricity supply industry, innovative end-product developments continue to move towards the common goal of increased power capacity, higher power utilization and lower costs. Some industries need effective DC-DC converter power management solutions, especially the automotive industry as it transitions to electric vehicles and the health field, with the introduction of ever smaller devices requiring efficient battery storage. The highly efficient converters are the future of the industry as they may mitigate much of the power demand of the consumers and hold much electricity in power applications. This will ensure much less operation cost in the power plants as same unit generation will give more output power in the consumer side. More and more voltage boosting techniques have to be experimented on DC-DC converter structures in order to find out even more efficient hybrid structures which may take the level of development further. The loss minimization contributes a lot towards the total economy and ensures efficient and sustainable energy usage.

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