Stability Analysis of DC-DC Converters by Employing Simulated Annealing Algorithm Based Optimized PI Controller.

A Dissertation submitted in partial fulfillment of the requirement for the degree of Bachelor of Science (B. Sc.) in Electrical and Electronics Engineering.

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It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedication

We would like to dedicate this thesis book to our families, and everyone who have given us unwearied support throughout the entirety of our existence and born testament to our efforts and failures, yet who always stayed by our side, especially during the harsh times.

Acknowledgements

First, we would extend our deepest gratitude to the Almighty Allah, our Creator, Who had created us and instilled inside us, the intellect to educate ourselves with the knowledge of the world and thus conduct our research on this thesis successfully. Foremost, we are very grateful to our respected supervisor, **Prof. Dr. Md. Ashraful Hoque**, DEAN, Faculty of Science and Engineering, IUT, for his constant guidance and encouragement towards exploring the field of Electrical and Electronic Engineering. If it had not been for the inspiration he provided us, we would have lost track of our way on this long journey.

We would also like to express our immense gratitude to our mentors **Mr. Mirza Muntasir Nishat**, Lecturer, Department of Electrical and Electronic Engineering and **Mr. Fahim Faisal**, Assistant Professor, Department of Electrical and Electronic Engineering for consistent guidance from the very beginning of our journey onto this research. At a time when we were very much flustered about fixing a field of research, they paved a pathway for us to work on a subject that truly fascinated us and gave us the drive to complete this thesis.

We would like to thank all the faculty members of EEE Dept., IUT for their continuous support and encouragement. They provided a conducive environment for us to learn and grow together.

Finally, our deepest of gratitude goes to our family who always listened to our sufferings and enchanted us with their delightful words. Last but not the least, we would like to thank our friends who always supported us through this journey.

Abstract

This thesis intends to uncover the concept of optimizing the operation of DC-DC converters, using closed loop control with a PI tuner, which is tuned using a unique search algorithm called Simulated Annealing Algorithm. The concept of the algorithm is to take the Kp and Ki parameters as the variables and using performance indices, objective functions are generated, which are input into the Simulated Annealing algorithm to obtain values of Kp and Ki which facilitate the global minimum of the objective function. Thereby, the Kp and Ki parameters are implemented in each individual DC-DC converter to test whether better step response is yielded than when Kp and Ki parameters are used from conventional PI tuning.

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Chapter 1: Introduction to DC-DC converters.

In the prime age of technology, the use of power electronics has rapidly increased on a global scale. A major chunk of the demand for power electronics is contributed by power converters. The intensive research over AC-DC and DC-DC converters over the decades have resulted in numerous converter topologies being implemented over a wide range of applications. Moreover, newer techniques have been applied to improve the transient and steady state responses. Power converters have found great implications in renewable energy concerned projects and discoveries such as electric vehicles, LED drives, motor drives, inverters and smart grids. [1] Hence, the aim of research is to modernize and enhance the technology to meet the current trends and demands, particularly in dealing with load fluctuation. Stability is a characteristic of paramount importance as well.

1.1.1 Introduction

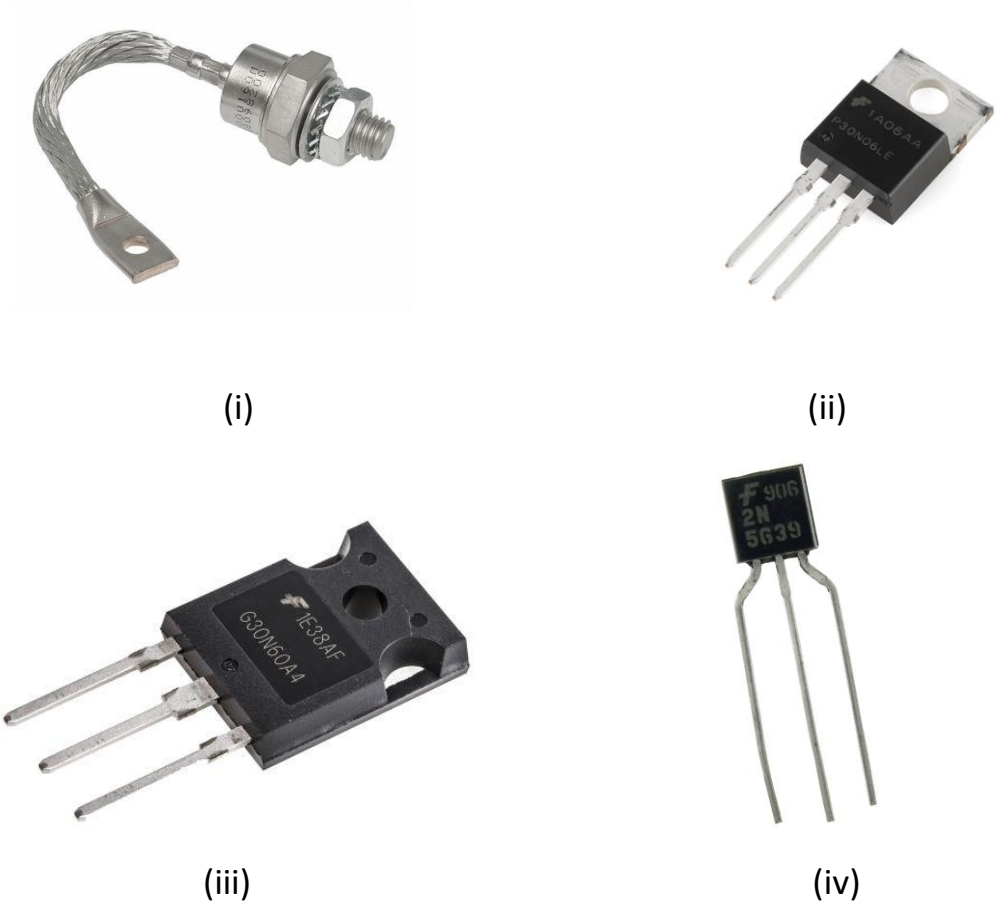
The prime concern of this research is the DC-DC converters because they are relatively simple and can be subjected to our devised algorithm to yield accurate results. DC-DC converters are observed to have a modest closed loop response which may be optimized using search algorithms which include genetic algorithm, simulated annealing algorithm, particle swarm algorithm, etc.

The first generation brought forth classical and traditional converters. They came in the form of a DC supply connected to an oscillator, a step-up transformer and finally a rectifier. They were very primitive and very inefficient. Then came the multi quadrant converters in the second generation. But until the discovery of switch mode regulators, only these expensive devices were available. In the third generation, switched inductor and switched capacitor converters debuted, which began to reduce the size of the topology. Soft switching converters were devised in the fourth generation, followed by synchronous rectifier converters and finally converters with multiple energy storage elements. [2] Such power converters are a staple use in microelectronics used in computers, mobile phones, laptops and various other applications. It is also observed that DC-DC converters mainly actuate and control the output voltage and the duty cycle so are suitable for photovoltaic devices.

1.1.2. Switching Devices for Power Conversion

Reliable switching operation is of utmost importance in converter circuits to maintain a stable duty cycle and output voltage. The suitable switches which are used for this purpose include the following:

1) Power Diodes and Bipolar Junction Transistor (BJT)
2) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
3) Insulated Gate Bipolar Transistor (IGBT)
4) Junction Gate Field Effect Transistor (JFET)
   In our research, the switches are considered lossless and ideal nature for the sake of simplicity in calculation. [3]



(i) (ii)

(iii) (iv)

Figure 1.1: Different types of switching devices (i) Power Diode (ii) Metal Oxide Semiconductor Field Effect Transistor (iii) Insulated Gate Bipolar Transistor (iv) Junction Gate Field Effect Transistor.

1.2. LITERATURE STUDY

Before the study of optimization of DC-DC converters, the characteristics of DC choppers need to be investigated. DC chopper circuits are circuits that convert an input DC voltage into an output DC voltage. The magnitude of the output voltage may be greater or less than the magnitude of the input voltage, depending on the requirement.

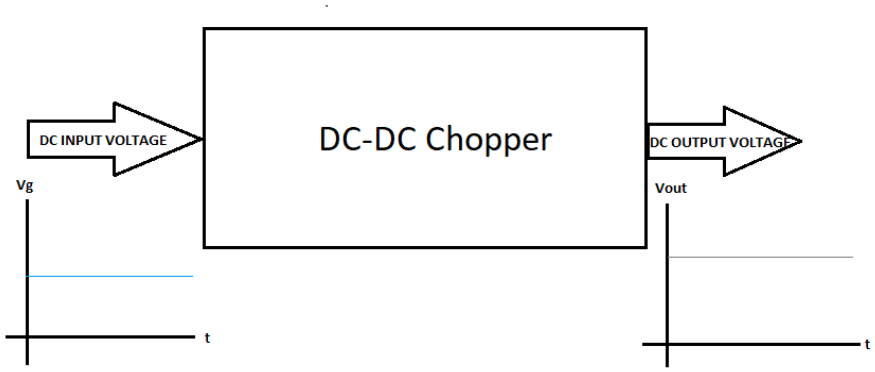


Figure 1.2: Basic DC-DC Chopper.

As shown above, the chopper circuit is connected with both the input voltage source and the output voltage source. [4] The chopper circuit consists of thyristors and other RLC elements which are connected to generate the required output voltage and duty cycle. The duty cycle is defined as the ratio of the ON time of the switch and the total time of each switching cycle. This controls the width of the DC output voltage pulse. Such kind of voltage control is called Pulse Width Modulation (PWM) control.

The DC-DC choppers which are to be discussed are:

1) Buck Converter.
2) Boost Converter.
3) Buck-Boost Converter.
4) Cuk Converter.

1.2.1 BUCK CONVERTER:

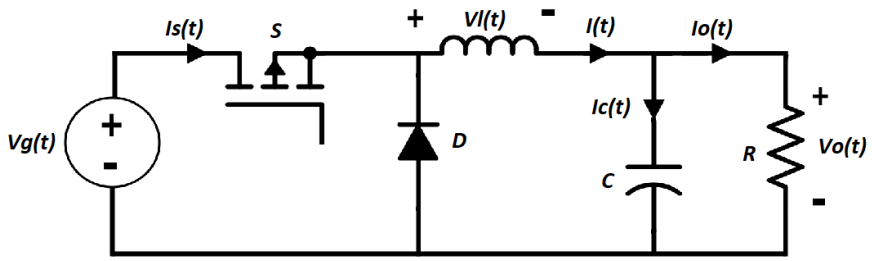


Figure 1.3: Conventional Buck Converter Circuit.

The buck converter steps down the input voltage to give a lower output voltage. It consists of an input voltage source Vg, a switch S, a diode D, an inductor L, a capacitor C and the load R across which the output voltage Vo is measured. The converter is run in the continuous conduction mode (CCM). [5] The converter's operation cycle is divided into two states as shown below:

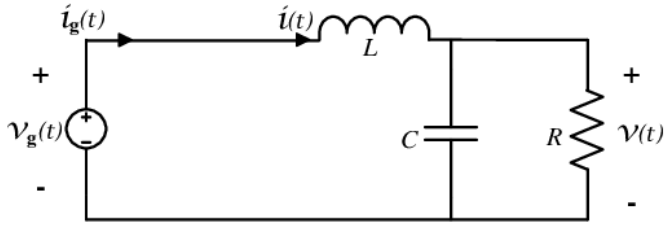


Figure 1.4(i): Buck converter in switch ON state.

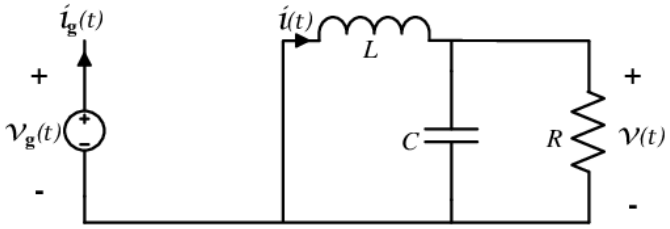


Figure 1.4(ii): Buck Converter in switch OFF state.

It is observed that when the switch S is ON, the current from source Vg flows directly to the inductor L and stores energy in it. So, the current through the inductor and the capacitor increases and inductor voltage increases. But, when S if switched OFF, then the inductor discharges energy to the circuit and since diode D is forward biased, the circuit is complete and hence, the output voltage and current remains uninterrupted. [6]

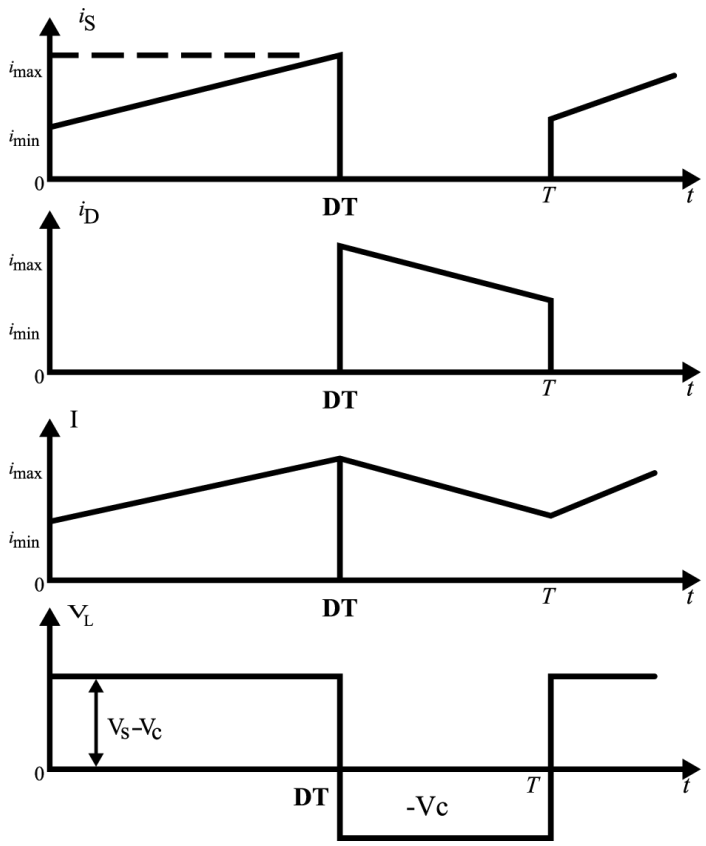


Figure 1.4(iii): Buck Converter Waveforms during operation.

The voltage and current waveforms for the operating cycle of the buck converter have been shown above. [7] Based on the ON state and the OFF state of the converter, using Kirchhoff's voltage law and Kirchhoff's current law, the state space representation of the circuit can be devised as follows:

Given that, $\frac{dx}{dt} = A.x + B.u$ and $y = C.x + D.u$

$x_{1=i_L}$, $x_{2=v_o}$ *and* $u = v_g$ are the main variables,

1) In the ON state:

$$\frac{di_L}{dt} = \frac{-v_o}{L} + \frac{v_g}{L}$$

$$\frac{dv_o}{dt} = \frac{i_L}{C} + \frac{-v_o}{RC}$$

Hence, the state space equation for ON state is given as:

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}.\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}.u$$

2) In the OFF state:

$$\frac{di_L}{dt} = \frac{-v_o}{L}$$

$$\frac{dv_o}{dt} = \frac{i_L}{C} + \frac{-v_o}{RC}$$

Hence, the state space equation for the OFF state is given as:

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}.\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \end{pmatrix}.u$$

Now, supposed the duty cycle of the converter is D. So, the proportion of the ON-time Ton is D while the proportion of the OFF-time Toff is (1-D). Accordingly, the average state space model is given as:

A' = Aon.d + Aoff.(1-d) and B' = Bon.d + Boff.(1-d)

$$A' = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}.d + \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}.(1-d) = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}$$

$$B' = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}.d + \begin{pmatrix} 0 \\ 0 \end{pmatrix}.(1-d) = \begin{pmatrix} \frac{d}{L} \\ 0 \end{pmatrix}$$

Therefore, the complete Buck Converter State Space Representation is given as:

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix}.\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{d}{L} \\ 0 \end{pmatrix}.u$$

1.2.2 Boost Converter:

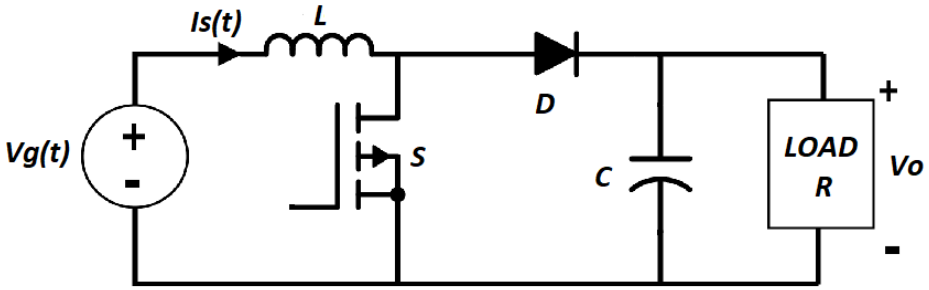


Figure 1.5: Conventional Boost Converter Circuit.

The boost converter steps up the input voltage to give a higher output voltage. It consists of an input voltage source Vg, a switch S, a diode D, an inductor L, a capacitor C and the load R across which the output voltage Vo is measured. The converter is run in the continuous conduction mode (CCM). [8] The converter's operation cycle is divided into two states as shown below:

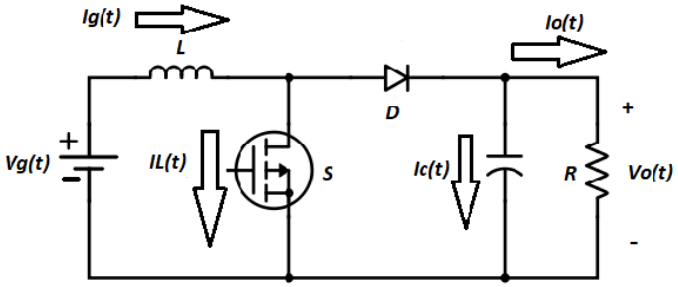


Figure 1.6(i): Boost converter in switch ON state.

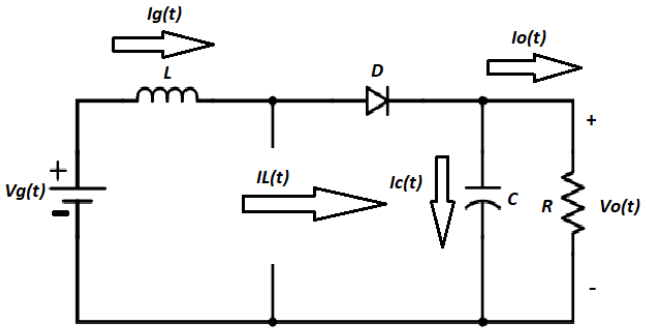


Figure 1.6(ii) Boost Converter in switch OFF state.

It is observed that when the switch S is ON, the current from source Vg flows directly through the inductor L and then bypasses through the switch. So, the inductor stores energy and the inductor voltage increases. But, when S is switched OFF, then the current path through S is opened so that current from source passes through to the capacitor C and load R. Moreover, inductor L also discharges in the circuit so that current flow increases. [9] The capacitor C stores energy so that in the next ON state, it will dissipate energy through load R so that current flow through R remains uninterrupted throughout the operation cycle. [10]

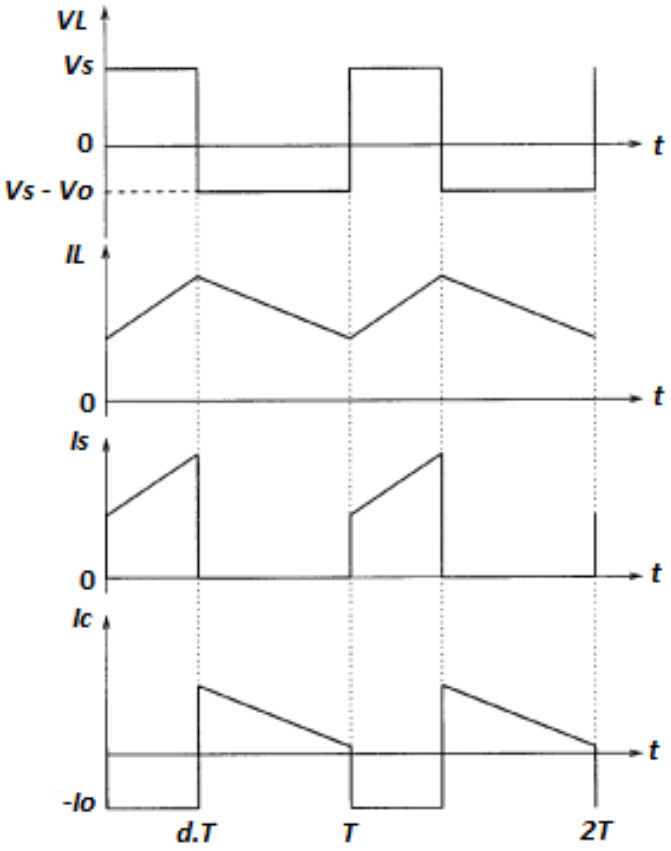


Figure 1.6(iii) Boost Converter Waveform during Operation.

The voltage and current waveforms for the operating cycle of the boost converter have been shown above. [11] Based on the ON state and the OFF state of the converter, using Kirchhoff's voltage law and Kirchhoff's current law, the state space representation of the circuit can be devised as follows:

Given that, $\frac{dx}{dt} = A.x + B.u$ and $y = C.x + D.u$

$x_{1=i_L}$, $x_{2=v_o}$ *and* $u = v_g$ are the main variables.

1) In the ON state:

$$\frac{di_L}{dt} = \frac{v_g}{L}$$

$$\frac{dv_0}{dt} = \frac{-v_0}{RC}$$

Hence the state space equation for the ON condition is given as:

$$\begin{pmatrix} x_1' \\ x_2' \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{pmatrix} . \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} . u$$

2) In the OFF state:

$$di_L/dt = \frac{-v_0}{L} + \frac{u}{L}$$

$$dv_c/dt = \frac{i_L}{C} - \frac{v_c}{RC}$$

So that the state space equation in the OFF state is given as:

$$\begin{pmatrix} x_1' \\ x_2' \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix} . \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} . u$$

Now, supposed the duty cycle of the converter is D. So, the proportion of the ON-time Ton is D while the proportion of the OFF-time Toff is (1-D). Accordingly, the average state space model is given as:

A' = Aon.d + Aoff.(1-d) and B' = Bon.d + Boff.(1-d)

$$A' = \begin{pmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{pmatrix} . d + \begin{pmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{pmatrix} . (1-d) = \begin{pmatrix} 0 & -\frac{1-d}{L} \\ \frac{1-d}{C} & \frac{-1}{RC} \end{pmatrix}$$

$$B' = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} . d + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} . (1-d) = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}$$

Therefore, the complete Boost Converter State Space Representation is given as:

$$\begin{pmatrix} x_1' \\ x_2' \end{pmatrix} = \begin{pmatrix} 0 & -\frac{(1-d)}{L} \\ \frac{1-d}{C} & \frac{-1}{RC} \end{pmatrix} \cdot \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} \cdot u_1$$

1.2.3 Buck Boost Converter:

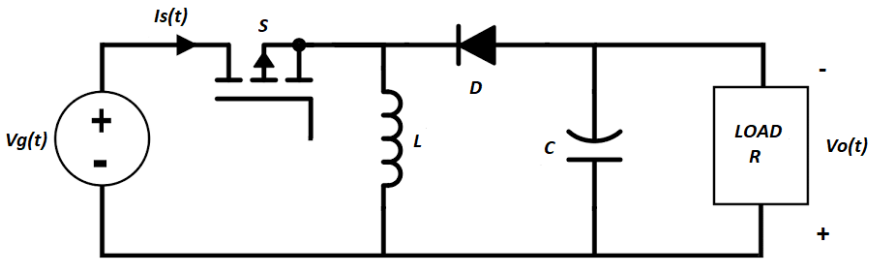


Figure 1.7: Conventional Buck-Boost Converter Circuit.

The buck boost converter operates on the input voltage to give either a higher or a lower output voltage, as per requirement. It consists of a source voltage Vg, load resistor R, an inductor L and a capacitor C as well as a diode D and a MOSFET switch S. [12] Designing a controller for this converter is more challenging owing to the fact that it is a non-minimum phase system and has a zero in the right half plane of the pole-zero plot. In other words, since the control input of this converter (the duty cycle of triggering pulse) exists in both voltage and current equations, the state equations solution and the control of this regulator poses greater difficulty. Furthermore, the converter has an inverting nature which causes the output to be the negative of the input. The converter's operation may be demonstrated in two states, as shown below.

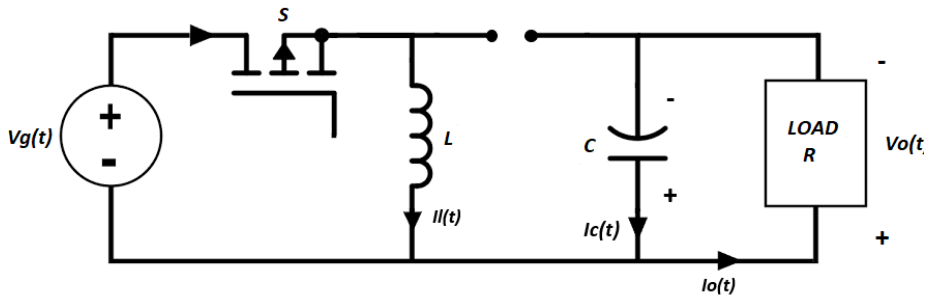


Figure 1.8(i): Buck-Boost Converter in Switch ON state.

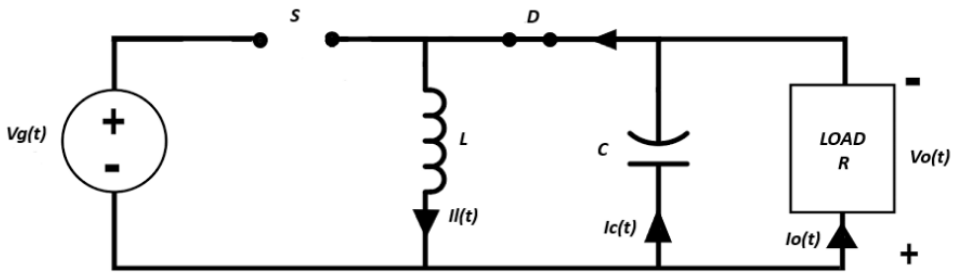


Figure 1.8(ii): Buck-Boost Converter in Switch OFF state.

It can be observed from the above that when the switch is in ON state, the source Vg causes a current to flow through the inductor L, which stores energy inside it. [13] In the meantime, the capacitor C dissipates its energy across the load resistor R so that a current passes through R.

In the switch OFF state, the energized inductor L dissipates its energy across the capacitor C and resistor R so that I_L splits up into the two current components as shown. This way, the current flowing through R remains uninterrupted throughout the entire cycle. However due to the polarity of diode D, the circuit is an inverting circuit and the output V_o will always be inverted with the polarity of input Vg. [14]

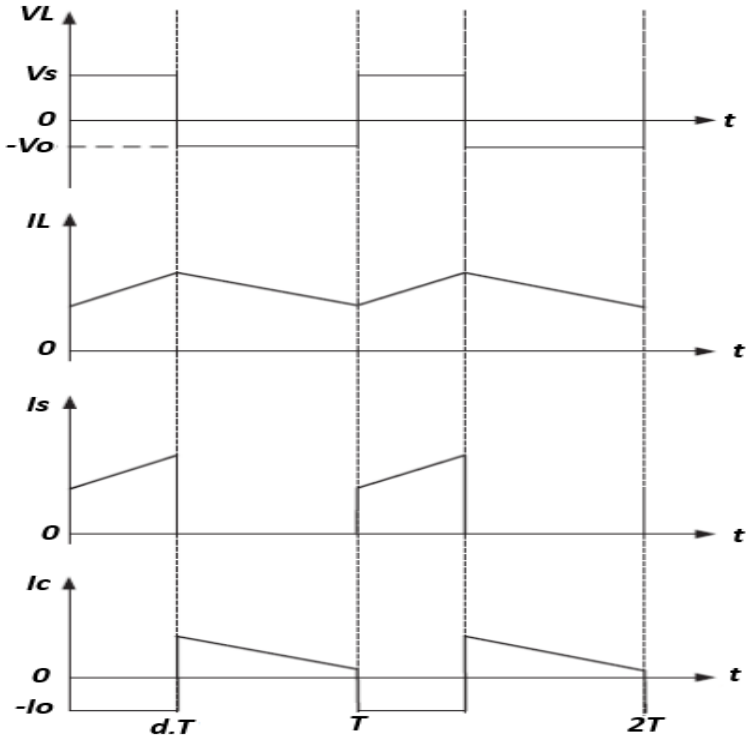


Figure 1.8(iii) Buck-Boost Converter Waveforms during Operation.

The voltage and current waveforms for the operating cycle of the buck-boost converter have been shown above. [15] [16] Based on the ON state and the OFF state of the converter, using Kirchhoff's voltage law and Kirchhoff's current law, the state space representation of the circuit can be devised as follows:

Given that, $\frac{dx}{dt} = A.x + B.u$ and $y = C.x + D.u$

$x_{1 = i_L}$, $x_{2 = v_o}$ *and* $u = v_g$ are the main variables.

1) In The ON state:

$$\frac{di_L}{dt} = \frac{v_g}{L}$$

$$\frac{dv_0}{dt} = -\frac{v_0}{R.C}$$

Hence the state space equations for the ON state may be given as:

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & \frac{-1}{R.C} \end{pmatrix}.\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}.u$$

2) In the OFF state:

$$\frac{di_L}{dt} = \frac{v_o}{L}$$

$$\frac{dv_0}{dt} = \frac{i_L}{C} - \frac{v_0}{R.C}$$

Hence, the state space equation for the OFF state may be given as:

$$\frac{d}{dt}\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{1}{L} \\ \frac{1}{C} & \frac{-1}{R.C} \end{pmatrix}.\begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \end{pmatrix}.u$$

Now, supposed the duty cycle of the converter is D. So, the proportion of the ON-time Ton is D while the proportion of the OFF-time Toff is (1-D). Accordingly, the average state space model is given as:

A' = Aon.d + Aoff.(1-d) and *B' = Bon.d + Boff.(1-d)*

$$A' = \begin{pmatrix} 0 & 0 \\ 0 & \frac{-1}{R.C} \end{pmatrix}.d + \begin{pmatrix} 0 & \frac{1}{L} \\ \frac{1}{C} & \frac{-1}{R.C} \end{pmatrix}.(1-d) = \begin{pmatrix} 0 & \frac{1-d}{L} \\ \frac{1-d}{C} & \frac{-1}{R.C} \end{pmatrix}$$

$$B' = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} . d + \begin{pmatrix} 0 \\ 0 \end{pmatrix} . (1 - d) = \begin{pmatrix} \frac{d}{L} \\ 0 \end{pmatrix}$$

Therefore, the complete Buck-Boost Converter State Space Representation is given as:

$$\begin{pmatrix} x_1' \\ x_2' \end{pmatrix} = \begin{pmatrix} 0 & \frac{1-d}{L} \\ \frac{1-d}{C} & \frac{-1}{R.C} \end{pmatrix} . \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} \frac{d}{L} \\ 0 \end{pmatrix} . u_1$$

1.2.4 CUK CONVERTER:

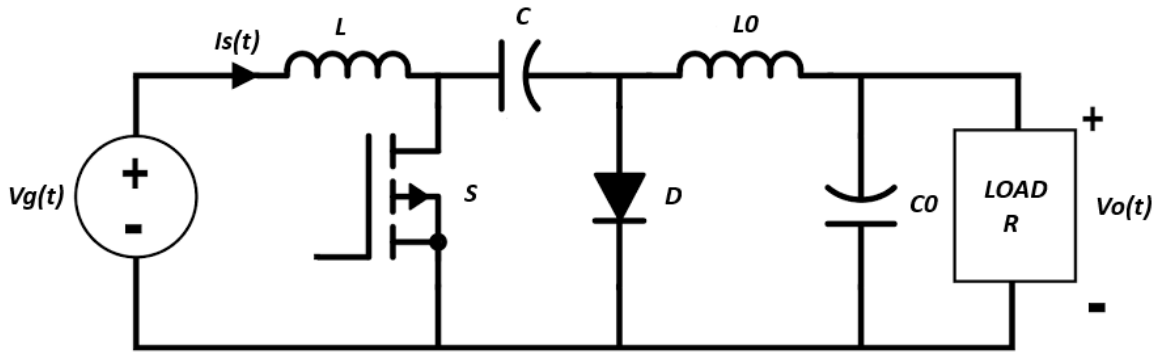


Figure 1.9: Conventional Cuk Converter Circuit.

The Cuk converter is yet another switching mode regulator. But it produces uses a constant DC suply voltage to produce a variable output. It observes a continous inductor current that is a considerable advantage when compared to other switch mode regulators. When used in discontinous conduction(DCM) mode, the Cuk converter operates as a power factor preregulator with a constant duty cycle ratio. Moreover, the Cuk converter may be used as a power factor preregulator in continous conduction(CCM) mode as well. [17] This has been proven by the special average current mode control technique. When used in CCM, it functions suitably for high power requirements which are unachievable at DCM state. On top of that, the Cuk converter shares a common mode with the Sepic converter, called the discontinous capacitor voltage (DCV) mode, which sets it apart from the other converters that have been discussed so far. However, one key disadvantage of this converter is that there are a large number of reactive components in the circuit. This results in high current stress exerted on the switch S, diode D and the energy transfer capacitor C.

The circuit for this converter consists primarily of a voltage source Vg, an inductor L on the source side, a MOSFET switch S, an energy transfer capacitor C, a diode D, a filter inductor L0 on the load side, a filter capacitor C0 on the load side and the load resistance R. [18]

The operation of the Cuk converter may be shown in two modes as shown below:

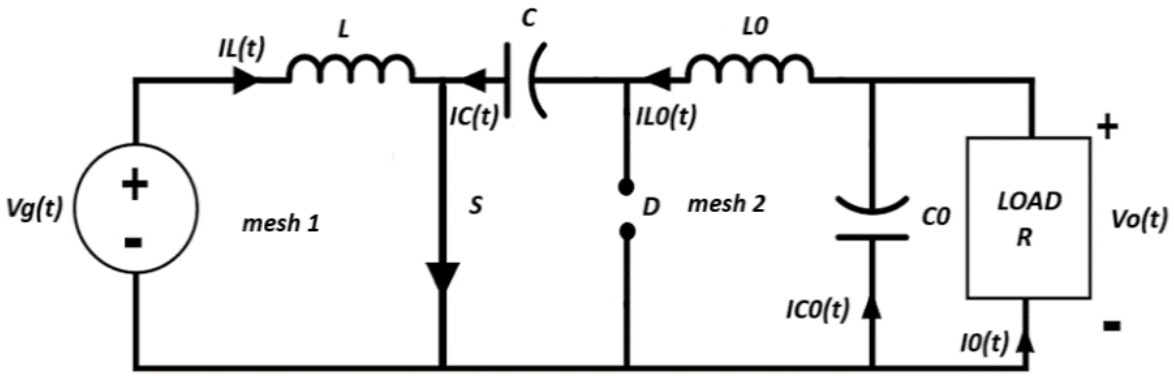


Figure 1.10(i): Cuk Converter in Switch ON State.

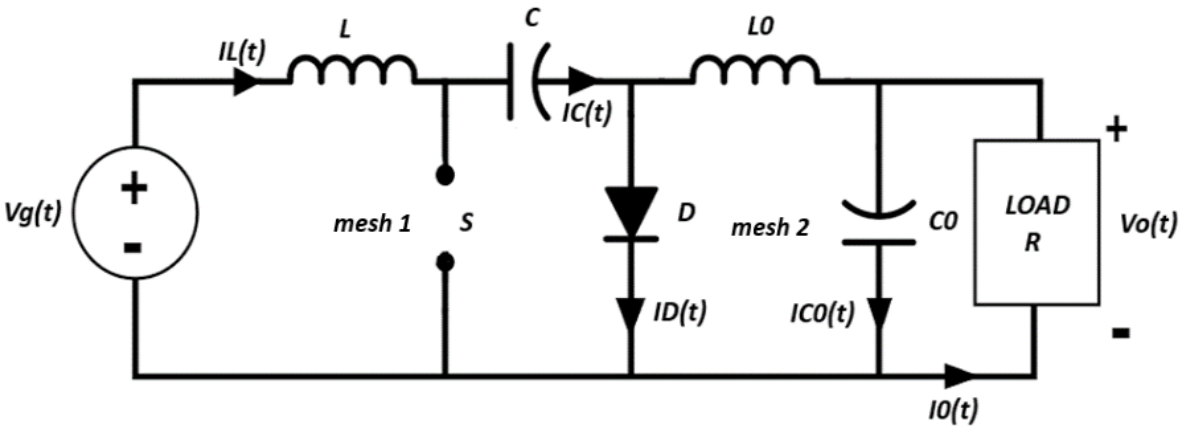


Figure 1.10(ii): Cuk Converter in Switch OFF State.

It is evident from the above figures that the Cuk converter behaves quite differently from the other converters in its two switch states. During the ON state of the switch, it is observed that the current that originates from the source Vg passes through input inductor L and is shorted across the switch so that it does not get transferred to the energy transfer capacitor C. Rather, during this state, C dissipates across the filter capacitor and inductor C0 and L0, and the load resistance R. The diode D is reverse biased and hence, this pathway is open at this part of the operating cycle. There are two meshes at work at this stage. [19]

On the other hand, when the switch S is in its OFF state, the source voltage Vg powers the entire circuit so that Vg and input inductor L dissipates across the circuit and recharges the energy transfer capacitor C. On top of that, the diode D is in forward biased so that C is shorted to the ground and the filter capacitor C0 powers the load resistance R at this state, as shown in

figure 1.10(ii) during this part of the operating cycle. Thus the circuit forms two different meshes than the alternate state.

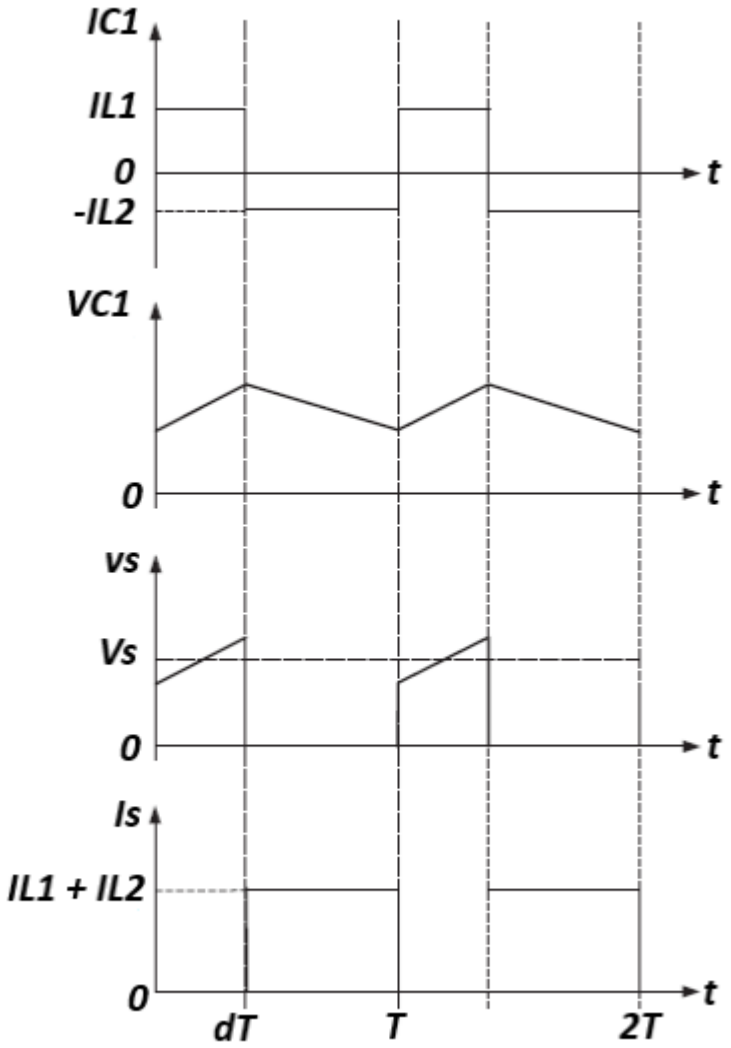


Fig: Cuk converter Waveforms

Based on the current and voltage waveforms displayed above, the continous conduction mode operation may be observed so that inductor currents do not reach zero at any instance at all. [20] Considering parasitic resistances to be negligible, the entire operating cycle of the Cuk converter may be divided into two segments:

1) ON State = d.T
2) OFF State = (1-d).T

1) In the ON State: **0<t<d.T**

In mesh 1,

$$L.\frac{di_L}{dt} = V_g$$

$$\frac{di_L}{dt} = \frac{V_g}{L}$$

In mesh 2,

$$C.\frac{dv_C}{dt} = -i_{L0}$$

$$\frac{dv_C}{dt} = -\frac{i_{L0}}{C}$$

$$L_0\frac{di_{L0}}{dt} = v_C - v_0$$

$$\frac{di_{L0}}{dt} = \frac{v_C - v_0}{L_0}$$

$$C_0.\frac{dv_0}{dt} = (i_{L0} - \frac{v_0}{R})$$

$$\frac{dv_0}{dt} = \frac{1}{C_0}.(i_{L0} - \frac{v_0}{R})$$

Both starting inductor L and energy transfer capacitor C are grounded by the switch S. Therefore:

$$i_S = i_C + i_L$$

2) In the OFF State: **d.T<t<T**

In mesh 1

$$L.\frac{di_L}{dt} = v_g - v_C$$

$$\frac{di_L}{dt} = \frac{v_g - v_C}{L}$$

$$C.\frac{dv_C}{dt} = i_L$$

$$\frac{dv_C}{dt} = \frac{i_L}{C}$$

In mesh 2,

$$L.\frac{di_{L1}}{dt} = -v_0$$

$$\frac{di_L}{dt} = -\frac{v_0}{L}$$

$$C.\frac{dv_0}{dt} = \frac{1}{C}.(i_{L0} - \frac{v_0}{R})$$

$$\frac{dv_0}{dt} = \frac{1}{C}.(i_{L0} - \frac{v_0}{R})$$

At this part of the cycle, a resultant current is passing through the diode D and this current is the summation of both inductor currents.

$$i_D = i_L + i_{L0}$$

Now, by combining the circuit behavior in both the ON and the OFF state, the state space average model may be constructed. Here, the duty cycle used is 'd'. To form the state space equations for the model, the equations in the ON state are multiplied with 'd' and the equations of the OFF state are multiplied with (1-d).

$$D.\left(\frac{di_L}{dt} = \frac{v_g}{L}\right) + (1-D)(\frac{di_L}{dt} = \frac{v_g - v_c}{L})$$

$$D.\left(\frac{dv_C}{dt} = -\frac{i_{L0}}{C}\right) + (1-D)(\frac{dv_C}{dt} = \frac{i_L}{C})$$

$$D.\left(\frac{di_{L0}}{dt} = \frac{v_C - v_0}{L_0}\right) + (1-D)(\frac{di_{L0}}{dt} = \frac{-v_0}{L_0})$$

$$D.\left(\frac{dv_0}{dt} = -\frac{1}{C}.(i_{L0} - \frac{v_0}{R})\right) + (1-D).(\frac{dv_0}{dt} = \frac{1}{C_0}\left(i_{L0} - \frac{v_0}{R}\right))$$

The above equations are solved to get the average state space representation.

$$\frac{di_L}{dt} = \frac{v_g}{L} - \frac{(1-D).v_C}{L}.D$$

$$\frac{dv_C}{dt} = -\frac{D.i_{L0}}{C} + \frac{(1-D).i_L}{C}$$

$$\frac{di_{L0}}{dt} = \frac{D.v_C}{L_0} - \frac{v_0}{L_0}$$

$$\frac{dv_0}{dt} = \frac{i_{L0}}{C} - \frac{v_0}{C.R}$$

Hence, the starting model equations for steady state and dynamic model derivations are found. The variables in the state space average and dynamic model are the combination of steady state and perturbed variables. In steady state, the operation variables are constant so that all derivatives of steady state variables are equal to zero. In the following derivation, the steady state variables are represented by upper case and the perturbed variables are shown as lower case with hat $'\widehat{\ }'$ symbol.

$$v_g = V_g + \widehat{v_g}$$

$$i_L = I_L + \widehat{i_L}$$

$$v_C = V_C + \widehat{v_C}$$

$$i_{L0} = I_{L0} + \widehat{i_{L0}}$$

$$v_0 = V_0 + \widehat{v_0}$$

$$D = D + \hat{d}$$

Yet, in this scenario, the system is nonlinear. But, assuming that perturbed values are negligible compared to steady state values, the product of perturbed variables may be discarded to linearize the system.

$$\frac{d\widehat{i_L}}{dt} = \frac{V_g}{L} - \frac{(1-D).V_C}{L} + \frac{\widehat{v_g}}{L} - \frac{(1-D).\widehat{v_C}}{L} + \frac{V_C}{L}.\hat{d}$$

$$\frac{d\widehat{v_C}}{dt} = -\frac{D.I_{L0}}{C} + \frac{(1-D).I_L}{C} - \frac{D.\widehat{i_{L0}}}{C} + \frac{(1-D).\widehat{i_L}}{C} - \frac{I_L + I_{L0}}{C}.\hat{d}$$

$$\frac{d\widehat{i_{L0}}}{dt} = \frac{D.V_C}{L_0} - \frac{V_0}{L_0} + \frac{D.\widehat{v_C}}{L_0} - \frac{\widehat{v_0}}{L_0} + \frac{V_C}{L_0}.\hat{d}$$

$$\frac{d\widehat{v_0}}{dt} = \frac{I_{L0}}{C} - \frac{V_0}{C.R} + \frac{\widehat{i_{L0}}}{C} - \frac{\widehat{v_0}}{C.R}$$

But these developed equations are a combination of steady state and dynamic model equations. The steady state model may be used to obtain the relationship between the input v_g and the output v_0.

$$V_g = (1 - D).V_C$$

$$I_{L0} = \frac{1 - D}{D}.I_L = \frac{V_0}{R}$$

$$V_0 = D.V_C = \frac{D}{1-D}.V_g$$

$$V_C = V_g + V_0$$

In a similar manner, the dynamic model of the system may also be evolved to obtain a relationship voltages and currents as shown below.

$$\frac{d\widehat{\imath_L}}{dt} = \frac{\widehat{v_g}}{L} - \frac{(1 - D).\widehat{v_c}}{L} + \frac{V_C.\hat{d}}{L}$$

$$\frac{d\widehat{v_C}}{dt} = -\frac{D.\widehat{\imath_{L0}}}{C} + \frac{(1 - D).\widehat{\imath_L}}{C} - \frac{(I_L - I_{L0}).\hat{d}}{C}$$

$$\frac{d\widehat{\imath_{L0}}}{dt} = \frac{D.\widehat{v_C}}{L_0} - \frac{\widehat{v_0}}{L_0} + \frac{V_C.\hat{d}}{L_0}$$

$$\frac{d\widehat{v_0}}{dt} = \frac{\widehat{\imath_{L0}}}{C} - \frac{\widehat{v_0}}{C.R}$$

In the dynamic model, the perturbed duty cycle '$\hat{d}$' is present which can be observed in open loop and closed loop systems alike. In case of a closed loop system, the feedback relationship between the duty cycle D and output v_0 may be substituted into the main model.

At last, the matrix form of the state space representation of the dynamic model is given as:

$$\begin{pmatrix} \frac{d\widehat{\imath_L}}{dt} \\ \frac{d\widehat{v_C}}{dt} \\ \frac{d\widehat{\imath_{L0}}}{dt} \\ \frac{d\widehat{v_0}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & \frac{1-D}{L} & 0 & 0 \\ \frac{1-D}{C} & 0 & \frac{-D}{C} & 0 \\ 0 & \frac{D}{L_0} & 0 & \frac{-1}{L_0} \\ 0 & 0 & \frac{1}{C} & \frac{-1}{C.R} \end{pmatrix} . \begin{pmatrix} \widehat{\imath_L} \\ \widehat{v_C} \\ \widehat{\imath_{L0}} \\ \widehat{v_0} \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \end{pmatrix} . \widehat{v_g} + \begin{pmatrix} \frac{V_C}{L} \\ \frac{-(I_L + I_{L0})}{C} \\ \frac{V_C}{L_0} \\ 0 \end{pmatrix} . (\hat{d})$$

Chapter 2: Motivation and Methodology Of Research

2.1 Motivation for Research:

In the modern age of software simulations, various optimization techniques have evolved, leading to more efficient designing of power electronics circuitry. A simple example of such is the use of the manual PID tuner in MATLAB. This tool may be extensively used to obtain optimal PID values that can be implemented upon closed loop circuits to attain the desired response. However, there need not be any boundary regarding the improvement of such optimization techniques.

Primarily, we have been motivated to undertake this research in order to devise a technique for generating further optimization that woul be able to draw up the PID values that accommodate an even better step response when tested on the concerned. Simulated Annealing Algorithm(SAE) is one of the numerous smart search algorithms. Harnessing this algorithm, iterations may be carried out to obtain the global optimum operating level of the concerned converter topology. This way, greater stability and more precise values of Kp, Ki and Kd may be obtained.

Therefore, this research has been conducted in an effort to use SA algorithm in order to automate the optimization procedure for closed loop PID control of the concerned converter model.

2.2 Methodology:

This section shall deal with a breakdown of the technique of Simulated Annealing Algorithm for optimization of the Buck, Boost, Buck-Boost and Cuk Converters. It includes an overview of SAE and its inner workings. Moreover, the algorithm shall be explained using block diagrams and the implication of objective functions on the optimization procedure.

2.2.1. Overview Of Simulated Annealing Algorithm:

The concept of simulated annealing stems from the thermodynamical notion of annealing. Annealing is a process by which a metal is heated to a base temperature and is then left to cool down and crystallize. This is done multiple times until the crystalline structure of minimum energy is obtained. The same strategy is applied analogously to the smart algorithm of Simulated Annealing and hence, the general system is tested to obtain a minimum point. This technique forms the base of optimization for combinatorial problems and such. [21]

Non linear problem cases are difficult to solve, owing to their nature. To overcome this, Simulated Annealing was discovered in 1983. It attempts to mitigate the global optimization issue by starting at a high energy level, i.e. a high temperature. This allows the objective function to explore high energy regions for a solution since the objective is to EXPLORE, not IMPROVE. The exploration procedure continues as the temperature drops from the initial value and due to this the objective function starts to lose its transience and is trapped in the lower energy levels. A Generating Distribution monitors the possible states that may be explored in the lower levels. An Acceptance Distribution may also be generated, which relies on the difference between the value of the objective function at the current energy level to be searched and the previous energy level that was saved. [22] Hence, the Acceptance Distribution shall stochastically decide whether it is better to remain in the current energy level or skip to a new energy level that will better accommodate the solution. Each and every Generating and Acceptance Distribution are reliant on the temperature of the energy level.

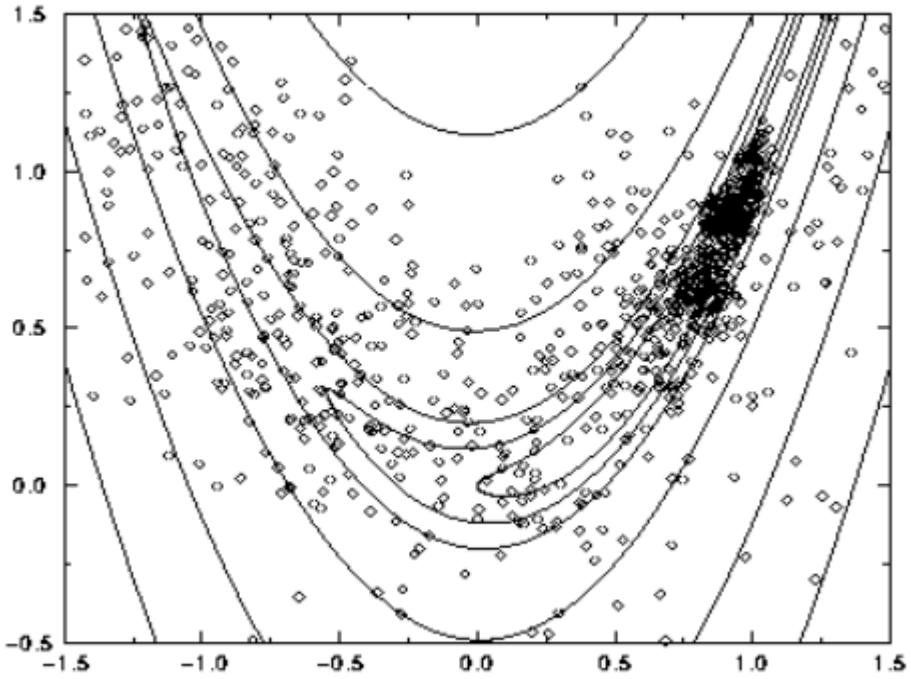


Figure 2.1: Minimization of the Two-dimensional Rosenbrock Function by Simulated Annealing

The research goes on to prove that by meticulous monitoring of the rate of cooldown of the system, the global optimum operating level may be determined. But this is a time consuming process and requires heavy computation power. [23] [24]To speed up the process, techniques of Fast Annealing(FA), Boltzmann Annealing(BA), Very Fast Simulated Re-annealing(VFSR) or Adaptive Simulated Annealing(ASA) may be utilized to quicken the entire process.

2.2.2 Simulated Annealing Function:

A key benefit of implementing SA as an optimization algorithm in lieu of other techniques is that this technique will prevent the solution being stuck in local minimas. During the explorative course of the objective function, it is bound to encounter multiple local minimas which may be confused as the global minima when viewed by other algorithms, but that is an avoidable scenario in this case. Having said that, the search algorithm will begin with a random search so that as the objective function progresses, not only will a decrease in the value of the objective function be registered, but an increase in said value as well. [25] The probability of accepting a change in the value of the objective function is given as:

$$P = e^{\frac{-\delta f}{T}}$$

Where, δf = Change in the objective function, 'f'

T = Control parameter in system that is analogous to annealing temperature.

The block diagram for Simulated Annealing procedure has been shown in the next page. In order to function properly, the algorithm requires the following information:

1) Representation of possible solutions.
2) Random change generator in solutions.
3) A means of evaluating the problem statement and function.
4) A annealing schedule which includes an initial temperature and conditions for the decrease in temperature during the course of the search.

Over time, the objective function values decreases until a minimum value is reached which indicates the global optimal point of operation. Off course, during the initial iterations, the annealing temperature is high and large changes in the objective function value are explored, even if the regions are far from the optimum level. Gradually, temperature drops and with it the tolerance for peaks of the objective function. Eventually, the final 40% of the total iterations are used by the algorithm to meticulously search around the region of the global optimum to unravel it and release the results.

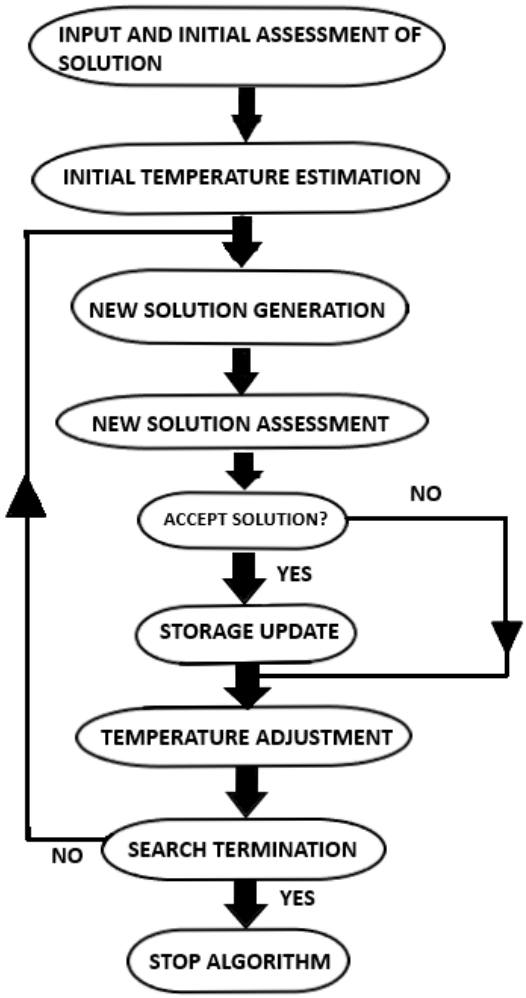


Figure 2.2: Block Diagram Outlining the Simulated Annealing Algorithm.

The figure above gives a plain demonstration of how the Simulated Annealing Algorithm performs on an objective function and reiterates over and over again until a desirable result is obtained. It is evident that at the beginning, a very high temperature is used for the initialization. Using the input value, the initial solutions are derived. From them a new starting temperature and resultantly, a new set of solutions is produced. This new set is analysed for suitability. If found suitable, then the new solutions are saved into the storage. Otherwise, the temperature is adjusted again. Afterwards, the search may either be terminated, or if not, then the adjusted temperature can be used to reiterate and generate a new set of solutions. This process goes on and on until desirable solutions for the objective function are obtained, so that termination takes place and stops the program.

There are numerous advantages of implementing the Simulated Annealing Algorithm in our research, which include the following:

Simulated Annealing is is a universal technique that may be used for the optimization of of various control systems.

1) It is robust in nature and can handle non linear models that display constraints such as chaotic and noisy data.
2) It is quite flexible, easy to comprehend, use and reach global optimal point of operation.
3) It is a versatile algorithm because it is not dependant on any restrictions of the model.
4) Simulated Annealing algorithms are easy to tune and depending on the problem statement, can be used over a wide range of applications. This especially favours the analysis of converter topology, as shown in our research.

Yet, regardless of its merits, there are still a number of weaknesses that are present in the Simulated Annealing algorithm, which need to be considered during implementation. They are:

1) It is a metaheuristic algorithm, which causes it to make a lot of decisions to produce the actual algorithm.
2) The quality of solutions degrades with a decrease in the time provided to compute the solutions. Hence, these two factors need to be carefully balanced.
3) The fine tuning of the algorithm according to different constraints is a delicate process.
4) The precision of the values used in the actualization of the algorithm make create a large impact on the quality of the output.

2.2.3: Objective Functions:

In our research, we have made use of four different performance indices in our objective functions which are operated on by the algorithm. Each of these performance indices are integrals of the error signal '$e(t)$' which are minimized to mimick and demonstrate the behaviour of the PID controller that takes the feedback from each controller and thereby generates the actuating signal that will go to the plant. The plant is composed of the respective converter that is used in the control system and which operates to produce an output. There are 4 performance indices which have been considered in our research [26] , as follows:

1) Integral of Absolute Error (IAE).
2) Integral of Time multiplied by Absolute Error (ITAE).
3) Integral of Squared Error (ISE).
4) Integral of Time multiplied by Squared Error (ITSE).

The 4 equations for the performance indices have been given below:

1) $IAE = \int_0^\tau |e(t)|.dt$
2) $ITAE = \int_0^\tau t.|e(t)|.dt$
3) $ISE = \int_0^\tau e(t)^2.dt$
4) $ISE = \int_0^\tau t.e(t)^2.dt$

2.2.4 Design of the Simulated Annealing PI Controller:

Since the primary concern of this research is the optimization and stability analysis of DC-DC converters, an appropriate controller designed for this purpose is the Proportional-Integral(PI) controller. It has found great success in improving the closed loop performance of power converters. Hence, we will not consider any values of 'K_D', that is, any Derivative values. Throughout the course of this research, $K_D = 0$.

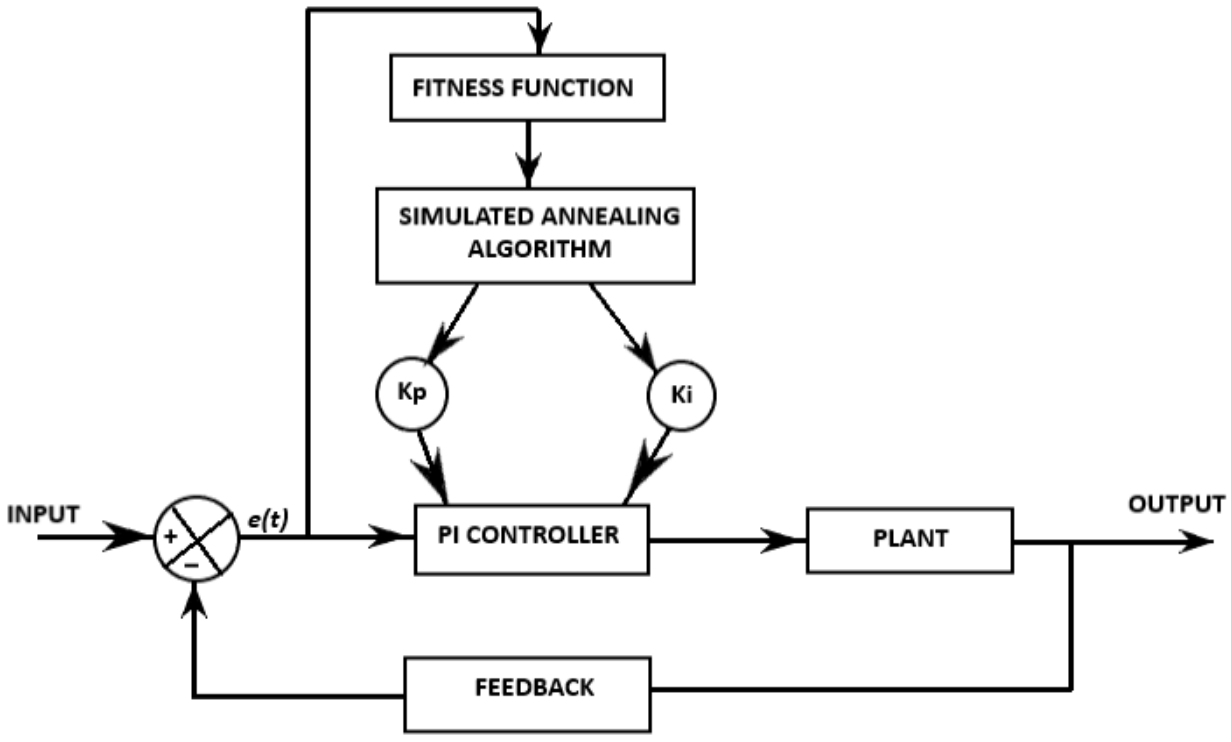


Figure 2.3: Basic Block Diagram of the Simulated Annealing

As shown in the block diagram, a closed loop controller has been designed in which the output voltage $'v_0(t)'$ is compared with the input voltage $'v_g(t)'$ and the error signal '*e(t)*' formed is incorporated into the respective fitness function (objective function). The fitness function is operated with the Simulated Annealing Algorithm to solve for the optimal values of K_P and K_I.

These values are fed into the PI controller which generates the actuating signal. This signal is processed by the plant to produce the output again. The feedback pathway of the output signal means that the error signal is constantly being monitored.

In the plant portion of the block diagram, each of the four discussed converters will be used, one at a time. Depending on their respective input/output relationships and the parameters provided, the open loop transfer functions may be determined. For this purpose, the average state space representation of each of the converters come to great aid.

In the next chapter, the procedure and simulation portion of this research will be discussed.

Chapter 3: Procedure of Simulation

In this chapter of our research, we will demonstrate the complete outline of how the Simulated Annealing Algorithm is implemented on each of the converters discussed previously. The SA algorithm is a search algorithm which may be simulated in MATLAB. Since the PI controller integrated with each converter may be represented as a single closed loop transfer function, MATLAB operates on these transfer functions to obtain their step reponse. The SA algorithm then derives the error signal '*e(t)*', using it to further determine the ideal PI parameters for the seamless operation of the entire control system.

3.1 Performance Parameters:

This section features the individual programming and tuning of the SA algorithm for Buck, Boost, Buck-Boost and Cuk converter. Initially the performance parameters of each system, their transfer functions and also the operating conditions of the search algorithm need to be determined.

3.1.1 Performance Parameters of the Buck Converter:

NAME OF COMPONENT	VALUE OF PARAMETER
CAPACITOR (C)	200µF
INDUCTOR (L)	145 µH
LOAD RESISTANCE (R)	1 Ω
INPUT VOLTAGE (v_g)	12 V
OUTPUT VOLTAGE(v_0)	5.574 V
DUTY CYCLE (D)	0.4645
SWITCHING FREQUENCY(F_s)	20 KHz

TABLE 1: Performance Parameters of Buck Converter.

Given the performance parameters, it is possible to derive the open loop transfer function of the Buck converter.

$$G = \frac{v_0}{v_g} = \frac{0.5}{[(2.9e-08) * s^2 + 0.000145 * s + 1]}$$

Therefore the code for the open loop step response of the system is given as:

```
num = [0.5];
den = [2.9e-08 0.000145 1];
plant = tf(num, den);
step(plant, 'b');
```

3.1.2 PERFORMANCE PARAMETERS OF THE BOOST CONVERTER:

NAME OF COMPONENT	VALUE OF PARAMETER
CAPACITOR (C)	1000µF
INDUCTOR (L)	72 µH
LOAD RESISTANCE (R)	26 Ω
INPUT VOLTAGE (v_g)	12 V
OUTPUT VOLTAGE(v_0)	24 V
DUTY CYCLE (D)	0.5
SWITCHING FREQUENCY(F_s)	20 KHz

TABLE 2: Performance Parameters of Boost Converter.

Given the performance parameters, it is possible to derive the open loop transfer function of the Boost converter.

$$G = \frac{v_0}{v_g} = \frac{3415 * s + 6.825e06}{[s^2 + (4.781e07) * s + (2.336e09)]}$$

Therefore the code for the open loop step response of the system is given as:

```
num = [3415 6.825e06];
den = [1 4.781e07 2.336e09];
plant = tf(num, den);
step(plant, 'g');
```

3.1.3 PERFORMANCE PARAMETERS OF THE BUCK-BOOST CONVERTER:

NAME OF COMPONENT	VALUE OF PARAMETER
CAPACITOR (C)	2,280.16µ
INDUCTOR (L)	10.41 µH
LOAD RESISTANCE (R)	9.655 Ω
INPUT VOLTAGE (v_g)	10 V – 34.9 V
OUTPUT VOLTAGE(v_0)	28 V
DUTY CYCLE (D)	0.74
SWITCHING FREQUENCY(F_s)	31.372 KHz

TABLE 3: Performance Parameters of Buck-Boost Converter.

Given the performance parameters, it is possible to derive the open loop transfer function of the Boost converter.

$$G = \frac{v_0}{v_g} = \frac{(-1.751e-04) * s + 28}{[(1.757e-08) * s^2 + (7.977e-07) * s + 0.0944]}$$

Therefore the code for the open loop step response of the system is given as:

```
num = [-1.751e-04 28];
den = [1.757e-08 7.977e-07 0.0944];
plant = tf(num, den);
step(plant, 'r');
```

3.1.4 PERFORMANCE PARAMETERS OF THE CUK CONVERTER:

NAME OF COMPONENT	VALUE OF PARAMETER
ENERGY TRANSFER CAPACITOR (C)	2,280.16µF
INPUT INDUCTOR (L)	68.7 µH
LOAD RESISTANCE (R)	12 Ω
INPUT VOLTAGE (v_g)	12 V
OUTPUT VOLTAGE(v_0)	24 V
FILTER CAPACITOR(C_0)	984 µF
SWITCHING FREQUENCY(F_s)	100 KHz
FILTER INDUCTOR(L_0)	2.2mH
DUTY CYCLE (D)	0.667

TABLE 4: Performance Parameters of Cuk Converter.

Given the performance parameters, it is possible to derive the open loop transfer function of the Boost converter.

$$G = \frac{v_0}{v_g} = \frac{-0.4904 * s^3 + 7923 * s^2 + (1.074e07) * s + (3.502e09)}{[(5e-06) * s^4 + 1.001 * s^3 + 129.1 * s^2 + 410600 * s]}$$

Therefore the code for the open loop step response of the system is given as:

```
num = [-0.4904 7923 1.074e07 3.502e09];
den = [5e-06 1.001 129.1 410600 0];
plant = tf(num, den);
step(plant, 'r');
```

3.2 OBJECTIVE FUNCTION PROGRAMMING:

The programming for the search algorithm of each individual converter has been provided in this section of the chapter.

3.2.1 SA ALGORITHM PROGRAM FOR BUCK CONVERTER:

--For the Integral of Absolute Error (IAE):

```
function [J] = pidoptimbuck(x)

s = tf('s');
num = [0.5];
den = [2.9e-08 0.000145 1];
plant = tf(num,den); %%buck tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(abs(e)*dt);        %IAE
```

--For the Integral of Time multiplied by Absolute Error(ITAE):

```
s = tf('s');
num = [0.5];
den = [2.9e-08 0.000145 1];
plant = tf(num,den); %%buck tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;
```

```
step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(t'.*(abs(e))*dt);  %ITAE
```

--For the Integral of Square of Absolute Error(ISE):

```
s = tf('s');
num = [0.5];
den = [2.9e-08 0.000145 1];
plant = tf(num,den); %%buck tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))

e= 1 - step(feedback(plant*cont,1),t);

J = sum(((e).^2)*dt);       %ISE %
```

--For the Integral ofTime multiplied by Square of Absolute Error(ITSE):

```
s = tf('s');
num = [0.5];
den = [2.9e-08 0.000145 1];
plant = tf(num,den); %%buck tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))

e= 1 - step(feedback(plant*cont,1),t);
```

```
J = sum(t'.*((e).^2)*dt);      %ITSE
```

3.2.2 SA ALGORITHM PROGRAM FOR BOOST CONVERTER:

--For the Integral of Absolute Error (IAE):

```
function [J] = pidoptimboost(x)

s = tf('s');
num = [3415 6.825e06];
den = [1 4.781e07 2.336e09];
plant = tf(num,den); %%boost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;
step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(abs(e)*dt);        %IAE
```

--For the Integral of Time multiplied by Absolute Error(ITAE):

```
function [J] = pidoptimboost(x)

s = tf('s');
num = [3415 6.825e06];
den = [1 4.781e07 2.336e09];
plant = tf(num,den); %%boost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;
step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(t'.*(abs(e))*dt);  %ITAE
```

--For the Integral of Square of Absolute Error(ISE):

```
function [J] = pidoptimboost(x)

s = tf('s');
num = [3415 6.825e06];
den = [1 4.781e07 2.336e09];
plant = tf(num,den); %%boost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;
step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);


J = sum(((e).^2)*dt);
```

--For the Integral ofTime multiplied by Square of Absolute Error(ITSE):

```
function [J] = pidoptimboost(x)

s = tf('s');
num = [3415 6.825e06];
den = [1 4.781e07 2.336e09];
plant = tf(num,den); %%boost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;
step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);


J = sum(t'.*((e).^2)*dt);      %ITSE
```

3.2.3 SA ALGORITHM PROGRAM FOR BUCK-BOOST CONVERTER:

--For the Integral of Absolute Error (IAE):

```
function [J] = pidoptimbuckboost(x)



s = tf('s');
num = [-1.751e-04 28]
den = [1.757e-08 7.977e-07 0.0944];
plant = tf(num,den); %%buckboost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(abs(e)*dt);        %IAE
```

--For the Integral of Time multiplied by Absolute Error(ITAE):

```
function [J] = pidoptimbuckboost(x)



s = tf('s');
num = [-1.751e-04 28]
den = [1.757e-08 7.977e-07 0.0944];
plant = tf(num,den); %%buckboost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);
J = sum(t'.*(abs(e))*dt);  %ITAE
```

--For the Integral of Square of Absolute Error(ISE):

```
function [J] = pidoptimbuckboost(x)



s = tf('s');
num = [-1.751e-04 28]
den = [1.757e-08 7.977e-07 0.0944];
plant = tf(num,den); %%buckboost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

J = sum(((e).^2)*dt);       %ISE
```

--For the Integral of Time multiplied by Square of Absolute Error(ITSE):

```
function [J] = pidoptimbuckboost(x)



s = tf('s');
num = [-1.751e-04 28]
den = [1.757e-08 7.977e-07 0.0944];
plant = tf(num,den); %%buckboost tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);


J = sum(t'.*((e).^2)*dt);   %ITSE
```

3.2.4 SA ALGORITHM PROGRAM FOR CUK CONVERTER:

--For the Integral of Absolute Error (IAE):

```
function [J] = pidoptimcuk(x)



s = tf('s');
num = [-0.4904 7923 1.074e07 3.502e09]
den = [5e-06 1.001 121.9 410600 0];
plant = tf(num,den); %%Cuk tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);

%J = sum(abs(e)*dt);        %IAE
```

--For the Integral of Time multiplied by Absolute Error(ITAE):

```
function [J] = pidoptimcuk(x)

s = tf('s');
num = [-0.4904 7923 1.074e07 3.502e09]
den = [5e-06 1.001 121.9 410600 0];
plant = tf(num,den); %%Cuk tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);
J = sum(t'.*(abs(e))*dt);  %ITAE
```

--For the Integral of Square of Absolute Error(ISE):

```
function [J] = pidoptimcuk(x)



s = tf('s');
num = [-0.4904 7923 1.074e07 3.502e09]
den = [5e-06 1.001 121.9 410600 0];
plant = tf(num,den); %%Cuk tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);


J = sum(((e).^2)*dt);       %ISE
```

--For the Integral of Time multiplied by Square of Absolute Error(ITSE):

```
function [J] = pidoptimcuk(x)



s = tf('s');
num = [-0.4904 7923 1.074e07 3.502e09]
den = [5e-06 1.001 121.9 410600 0];
plant = tf(num,den); %%Cuk tf
Kp = x(1);
Ki = x(2);
Kd = x(3);

cont = Kp + Ki/s + Kd*s;
dt = 0.01;
t  = 0:dt:1;

step(feedback(plant*cont,1))
e= 1 - step(feedback(plant*cont,1),t);


J = sum(t.*((e).^2)*dt);   %ITSE
```

3.3 OPTIMIZATION ALGORITHM CONFIGURATION AND OPERATION:

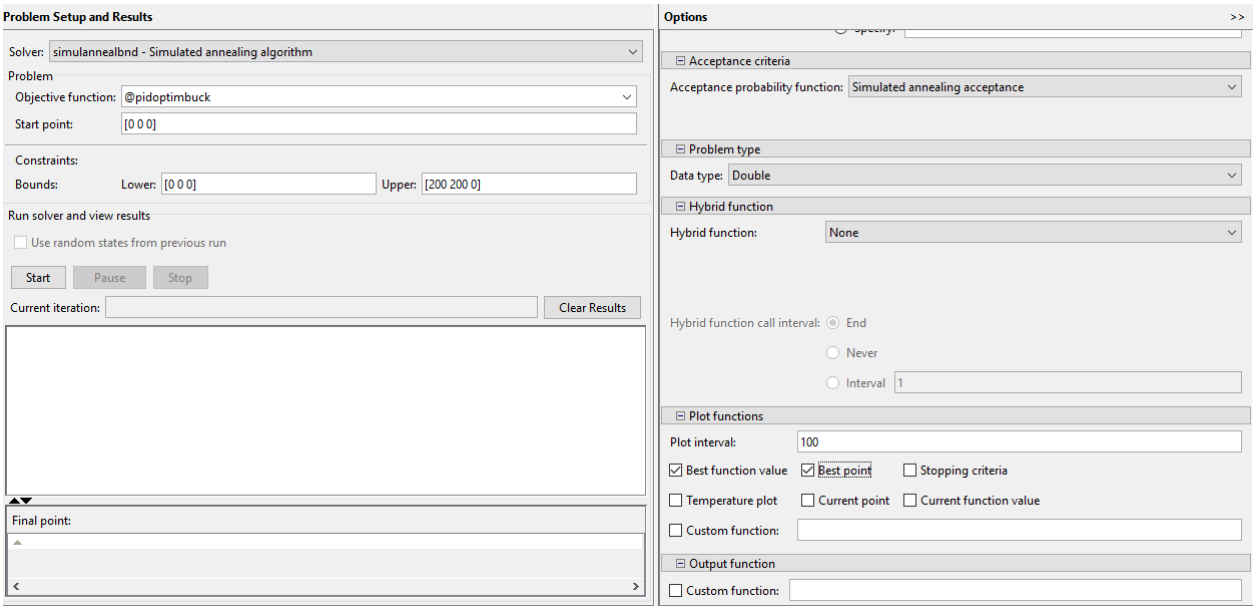


Figure: 3.1 Layout of Optimization Toolbox in MATLAB.

The Optimization toolbox is used to run the SA solver for determining the best value of the fitness function as well as the ideal parameters of Kp and Ki. Before running the solver, the respective objective function needs to be mentioned. The lower bound and upper bound values of Kp and Ki need to be specified as well.

INITIAL TEMPERATURE	100
TEMPERATURE UPDATE FUNCTION	EXPONENTIAL TEMPERATURE UPDATE
REANNEALING INTERVAL	100
ANNEALING FUNCTION	FAST ANNEALING

TABLE 5: Parameters of Simulated Annealing Algorithm.

After the SA iterations are conducted, the ideal values of Kp and Ki are applied into the transfer function of each converter topology to get their step response. Each converter will demonstrate the step response for IAE, ITAE, ISE and ITSE with respect to their obtained Kp and Ki values, and furthermore, a comparison may be drawn between the conventional PID tuning of each converter and each performance indice.

Chapter 4: SIMULATION RESULTS

4.1 Open Loop Step Response of Converters:

Initially, the open loop response of each of the converter topologies is analysed to compare the rise time, settling time and percentage overshoot of each circuit.

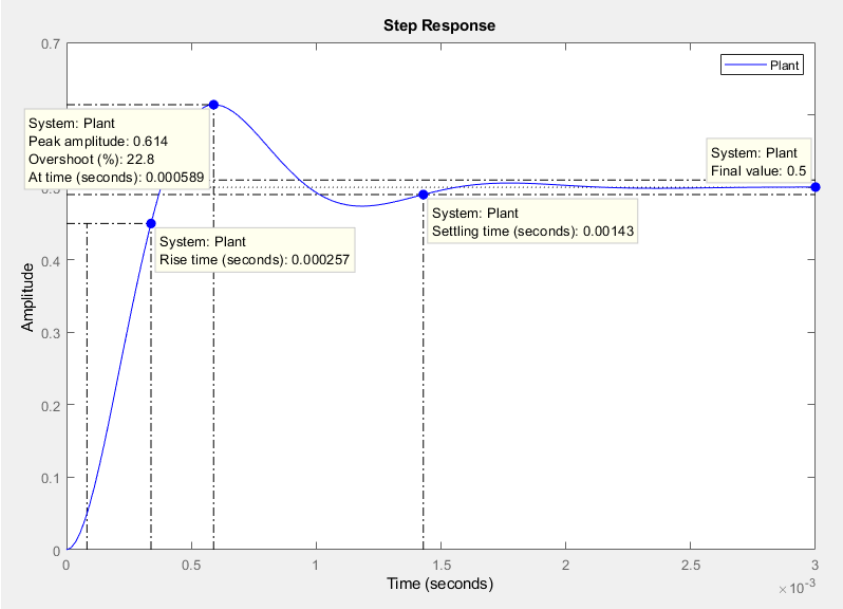


Figure 4.1: Open Loop Step Response of Buck Converter.

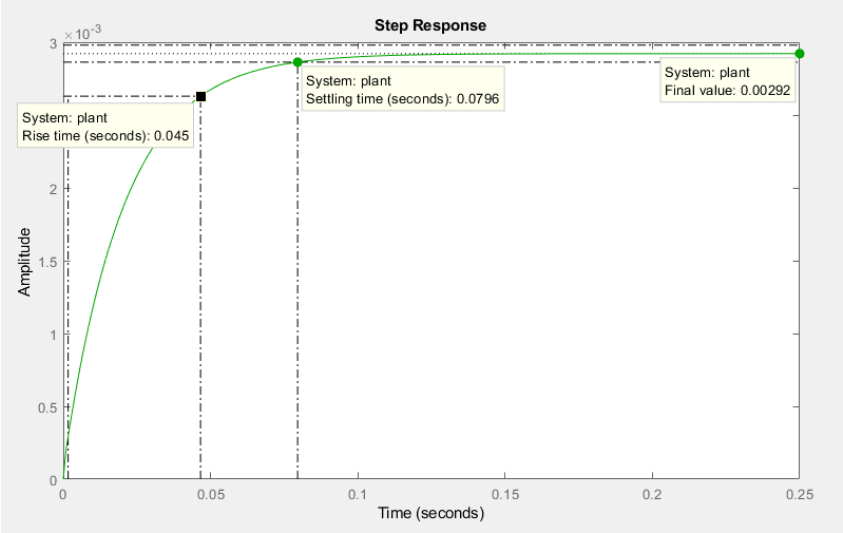


Figure 4.2: Open Loop Step Response of Boost Converter.

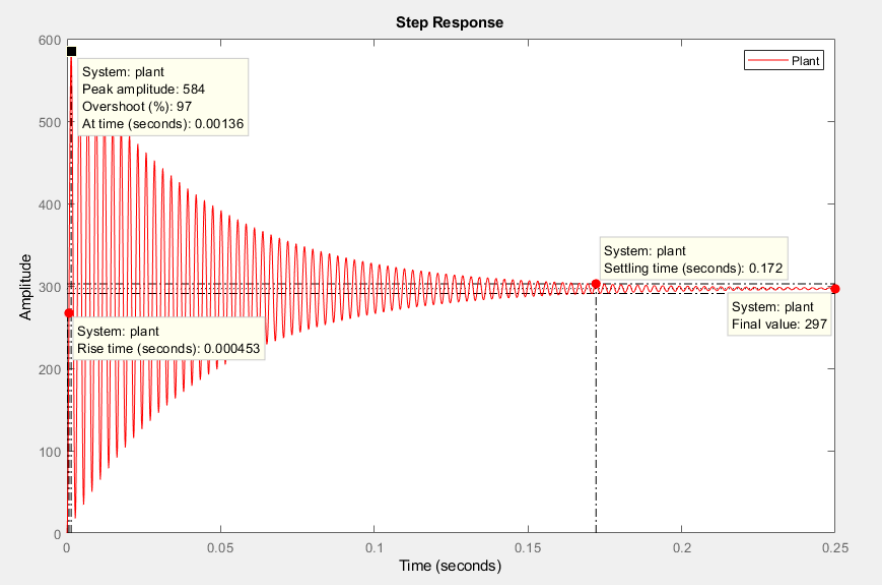


Figure 4.3: Open Loop Step Response of Buck-Boost Converter.

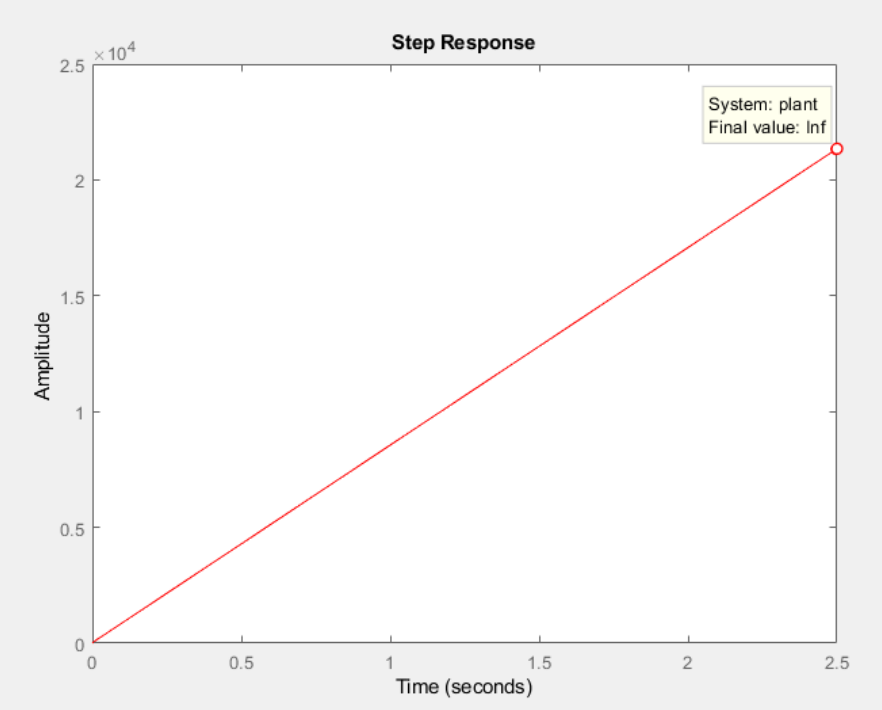


Figure 4.4: Open Loop Step Response of Cuk Converter.

	Rise Time(Tr)	Settling Time(Ts)	% Overshoot	Final Value
Buck Converter	0.000257	0.00143	22.8%	0.5
Boost Converter	0.045	0.0796	0	0.00292
Buck Boost Converter	0.000453	0.172	97%	297
Cuk Converter	-	-	inf	inf

TABLE 6: Comparison of Open Loop Performance Parameters of Converter Topologies.

4.2 Conventional PI Tuned Step Response of Converters:

After intial assessment, each converter's plant is taken as input into the built-in PID tuner of MATLAB. This is executed to obtain the improved step response of each topology due to the conventional PI control.

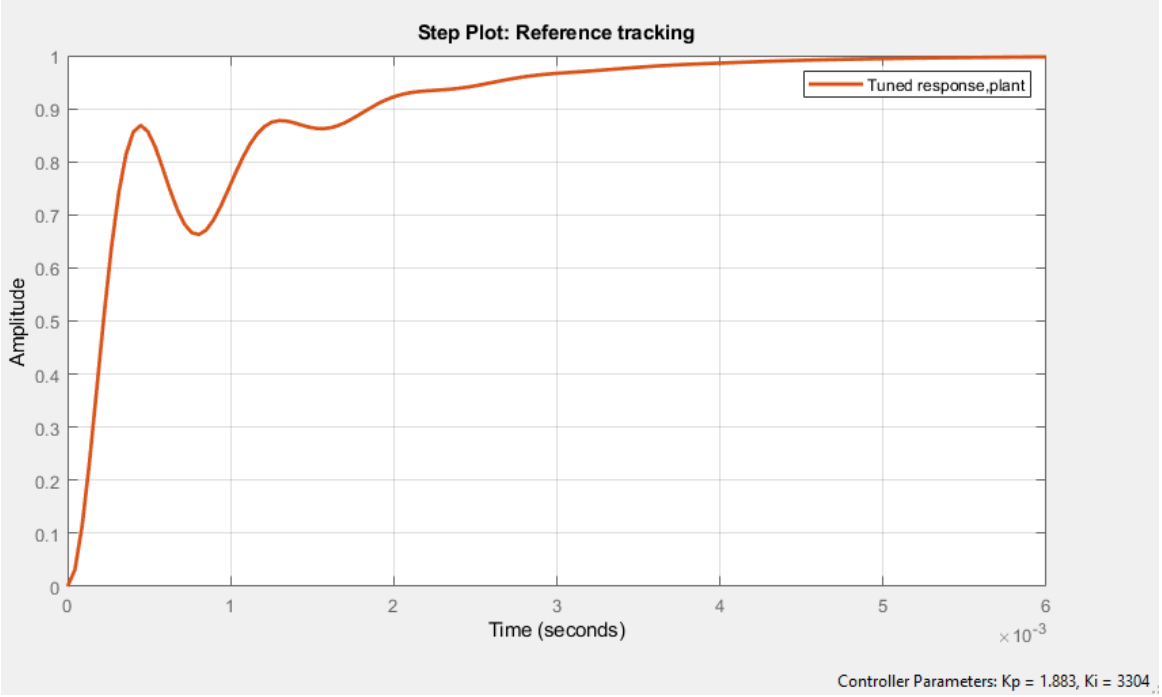


Figure 4.5 : Conventional PI Tuned Step Response of Buck Converter.

Controller Parameters

	Tuned
Kp	1.8832
Ki	3304.0451
Kd	n/a
Tf	n/a

Performance and Robustness

	Tuned
Rise time	0.00177 seconds
Settling time	0.00359 seconds
Overshoot	0 %
Peak	0.999
Gain margin	Inf dB @ Inf rad/s
Phase margin	61 deg @ 6.53e+03 rad/s
Closed-loop stability	Stable

TABLE 7.1: Performance Parameters of Conventional PI Tuned Buck Converter.

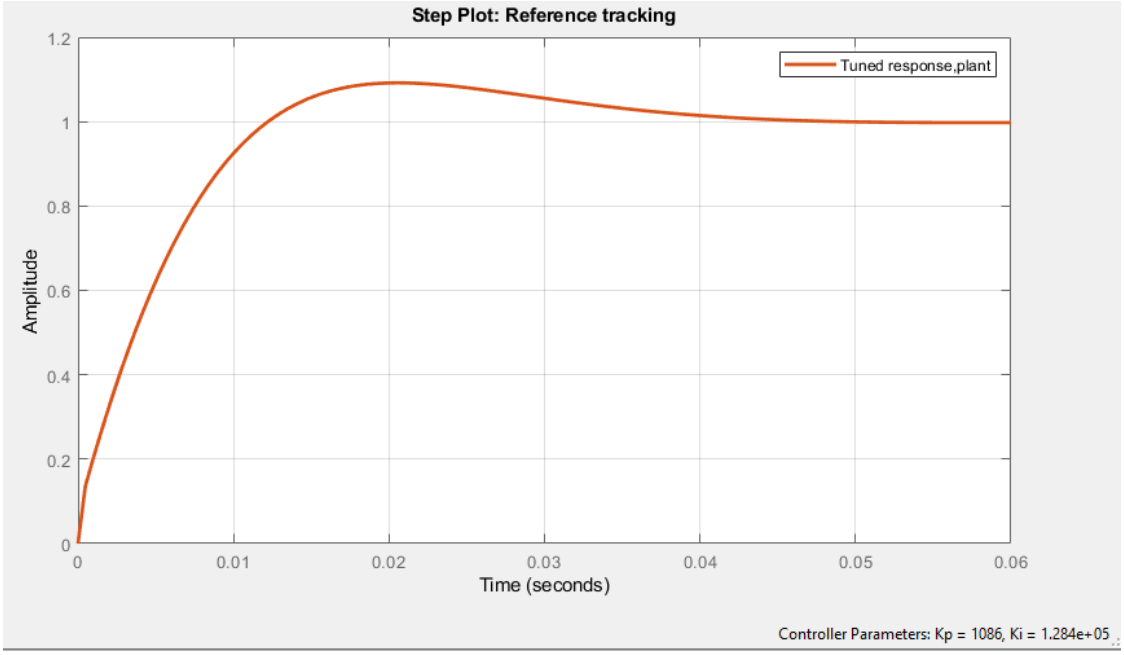


Figure 4.6 : Conventional PI Tuned Step Response of Boost Converter.

Controller Parameters

	Tuned
Kp	1085.852
Ki	128449.9056
Kd	n/a
Tf	n/a

Performance and Robustness

	Tuned
Rise time	0.00908 seconds
Settling time	0.0381 seconds
Overshoot	9.19 %
Peak	1.09
Gain margin	Inf dB @ NaN rad/s
Phase margin	77 deg @ 180 rad/s
Closed-loop stability	Stable

TABLE 7.2: Performance Parameters of Conventional PI Tuned Boost Converter.

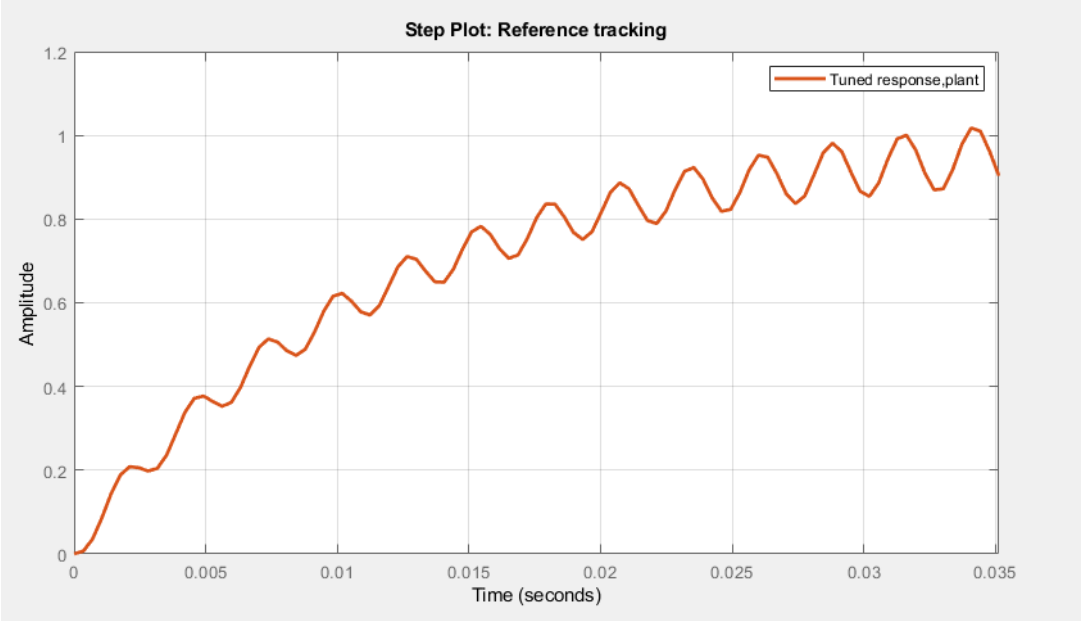


Figure 4.7 : Conventional PI Tuned Step Response of Buck-Boost Converter.

Controller Parameters

	Tuned
Kp	4.3154e-05
Ki	0.28849
Kd	n/a
Tf	n/a

Performance and Robustness

	Tuned
Rise time	NaN seconds
Settling time	NaN seconds
Overshoot	NaN %
Peak	Inf
Gain margin	-5.49 dB @ 2.33e+03 rad/s
Phase margin	-40.3 deg @ 2.36e+03 rad/s
Closed-loop stability	Unstable

TABLE 7.3: Performance Parameters of Conventional PI Tuned Buck-Boost Converter.

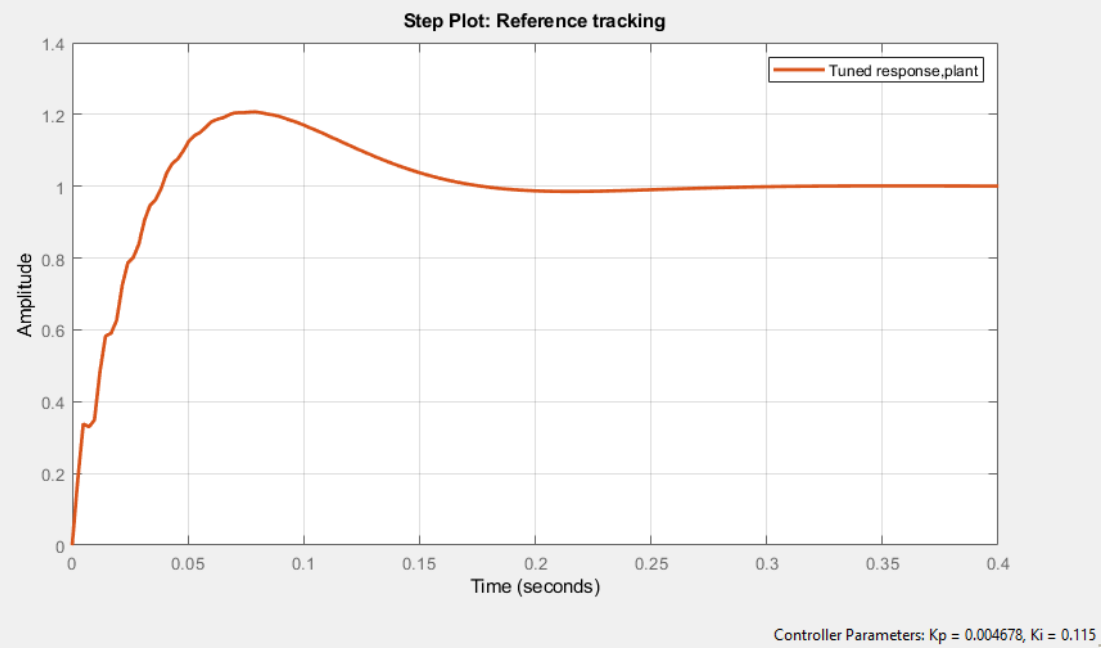


Figure 4.8 : Conventional PI Tuned Step Response of Cuk Converter.

Controller Parameters

	Tuned
Kp	0.0046784
Ki	0.11499
Kd	n/a
Tf	n/a

Performance and Robustness

	Tuned
Rise time	0.0297 seconds
Settling time	0.16 seconds
Overshoot	20.7 %
Peak	1.21
Gain margin	52.7 dB @ 5.68e+04 rad/s
Phase margin	69 deg @ 45.8 rad/s
Closed-loop stability	Stable

TABLE 7.4: Performance Parameters of Conventional PI Tuned Cuk Converter.

	Kp	Ki	Rise Time(Tr)	Settling Time(Ts)	%Overshoot	Final Value
Buck Converter	1.8832	3304.0451	0.00177s	0.00359s	0%	0.999
Boost Converter	1085.852	128449.9056	0.00908s	0.0381s	9.19%	1.09
Buck-Boost Converter	4.315e-05	0.28849	n/a	n/a	n/a	Inf
Cuk Converter	0.0046784	0.11499	0.0297s	0.16s	20.7%	1.21

TABLE 7.5: Combined Gain Values and Performance Chart for Conventional PI Tuned Converters.

4.3 SA Algorithm Implemented PI Tuned Step Response of Converters:

4.3.1: Buck Converter:

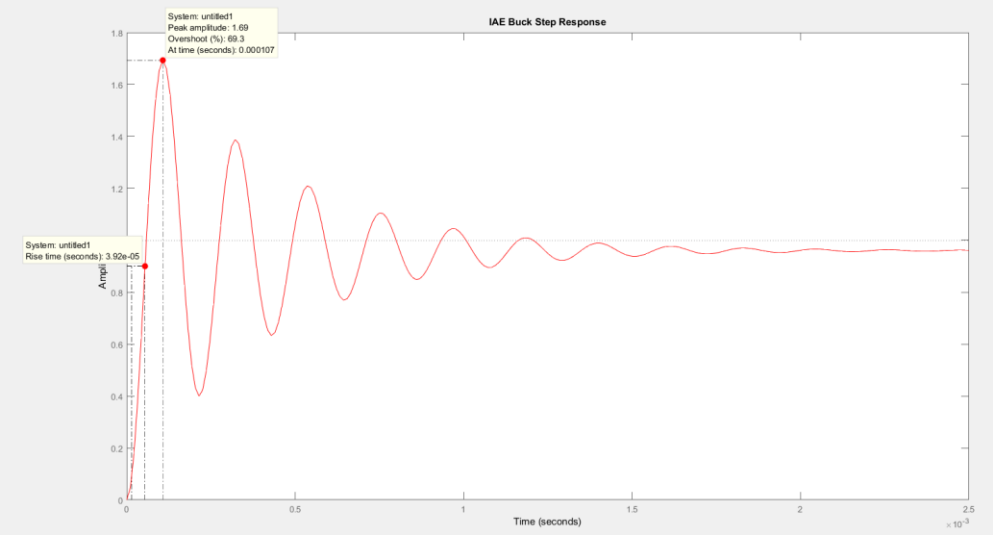


Figure 4.9(i): IAE PI Tuned Closed Loop Response of Buck Converter.

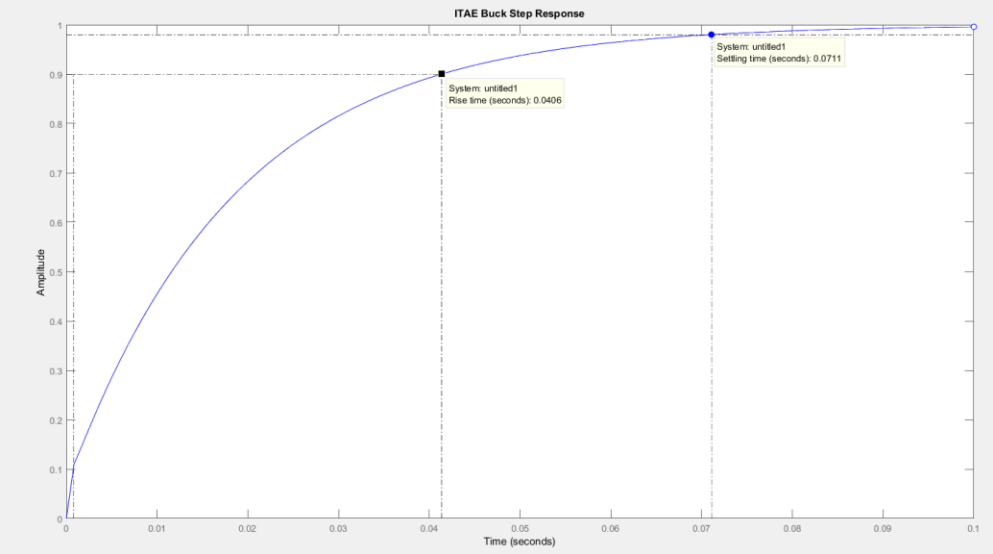


Figure 4.9(ii): ITAE PI Tuned Closed Loop Response of Buck Converter.

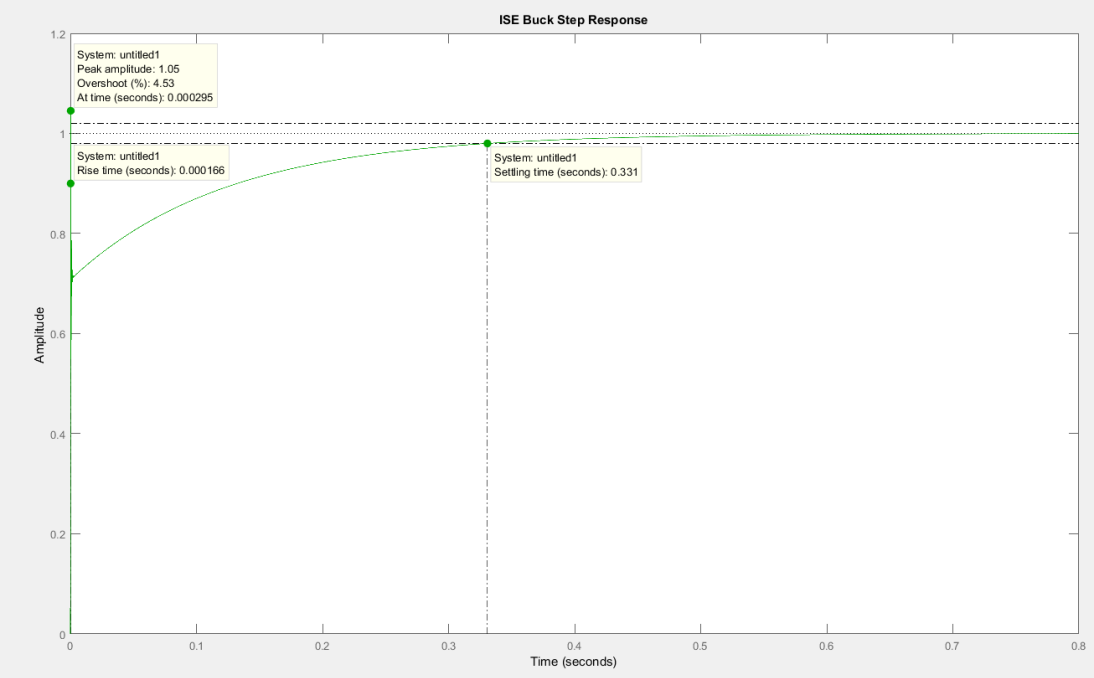


Figure 4.9(iii): ISE PI Tuned Closed Loop Response of Buck Converter.

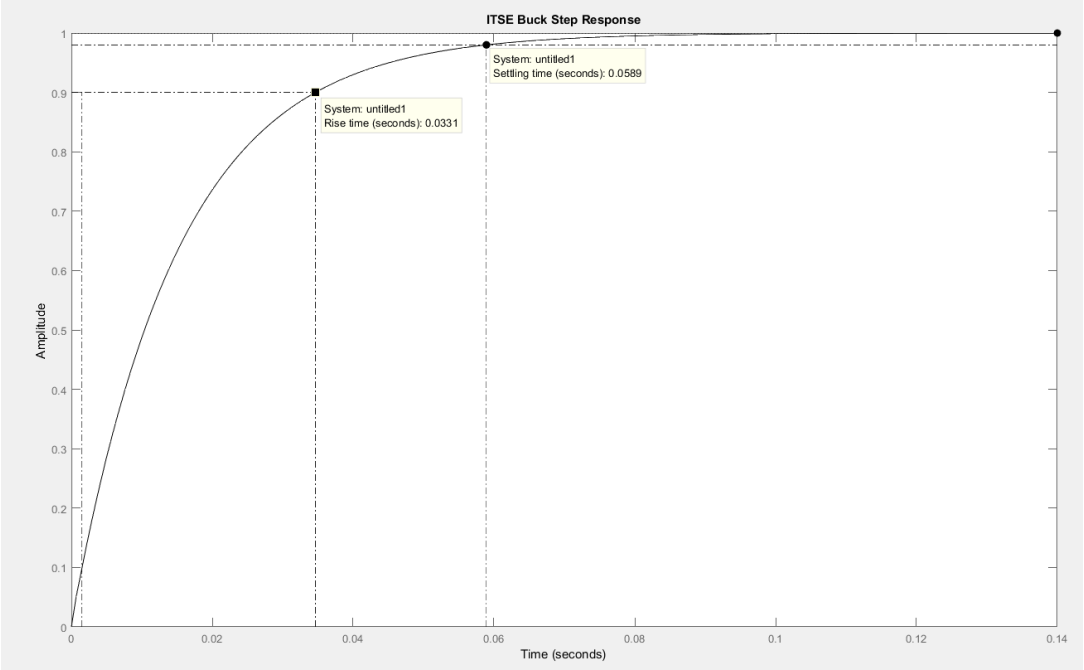


Figure 4.9(iv): ITSE PI Tuned Closed Loop Response of Buck Converter.

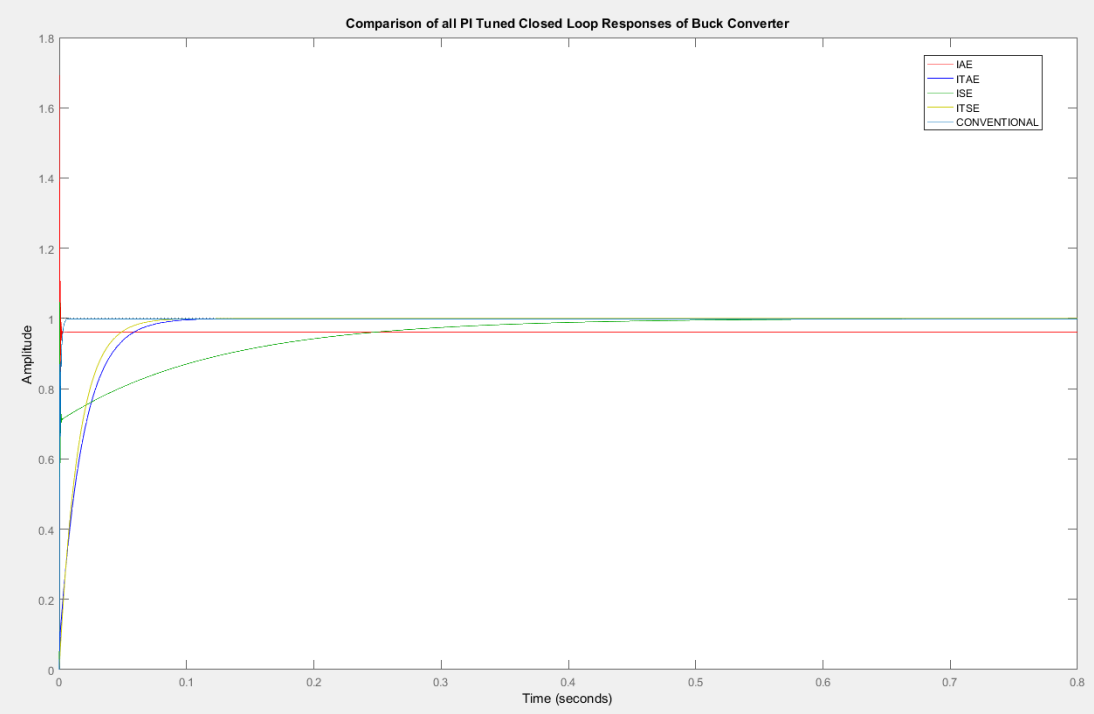


Figure 4.9(v): Comparison of all PI Tuned Closed Loop Responses of Buck Converter.

	Kp	Ki	Rise time(Tr)	Settling Time(Ts)	% Overshoot	Best Function Value
IAE	47.756	157.178	**3.92e-05**	**0.000107**	69.3	0.227745
ITAE	0.15	115.512	0.0406	0.0711	**0**	0.00596746
ISE	2.82	**55.433**	0.000166	0.331	4.53	0.010139068
ITSE	**0.029**	133.25	0.0331	0.0589	**0**	**0.000645732**
CONVENTIONAL	1.8832	3304.0451	0.00177s	0.00359s	**0**	n/a

TABLE 7.6: Combined Gain Value and Performance Chart for SA PI Tuned Buck Converter.

4.3.2: BOOST CONVERTER:

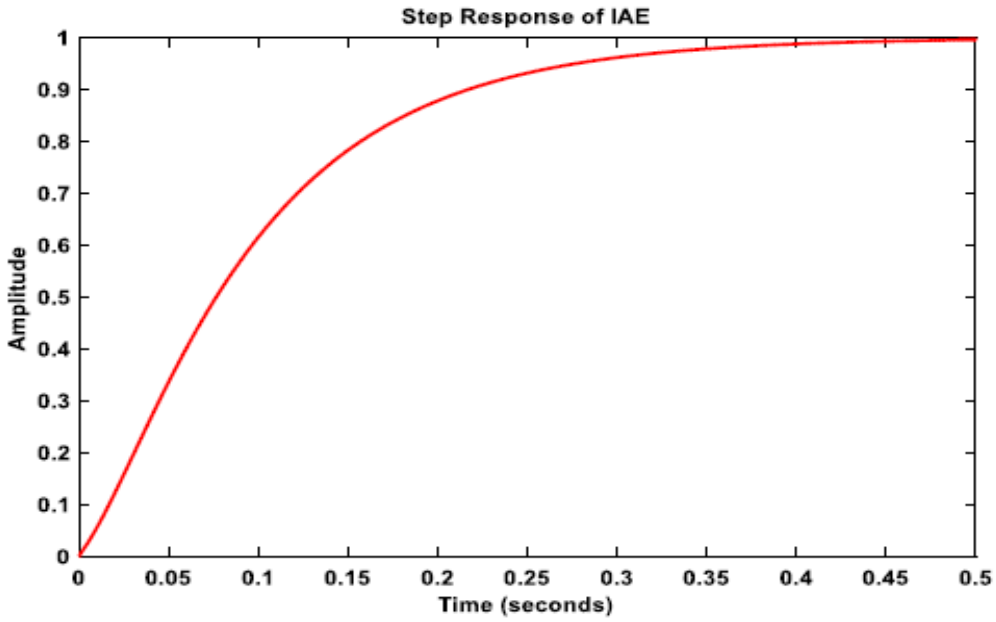


Figure 4.10(i): IAE PI Tuned Closed Loop Response of Boost Converter.

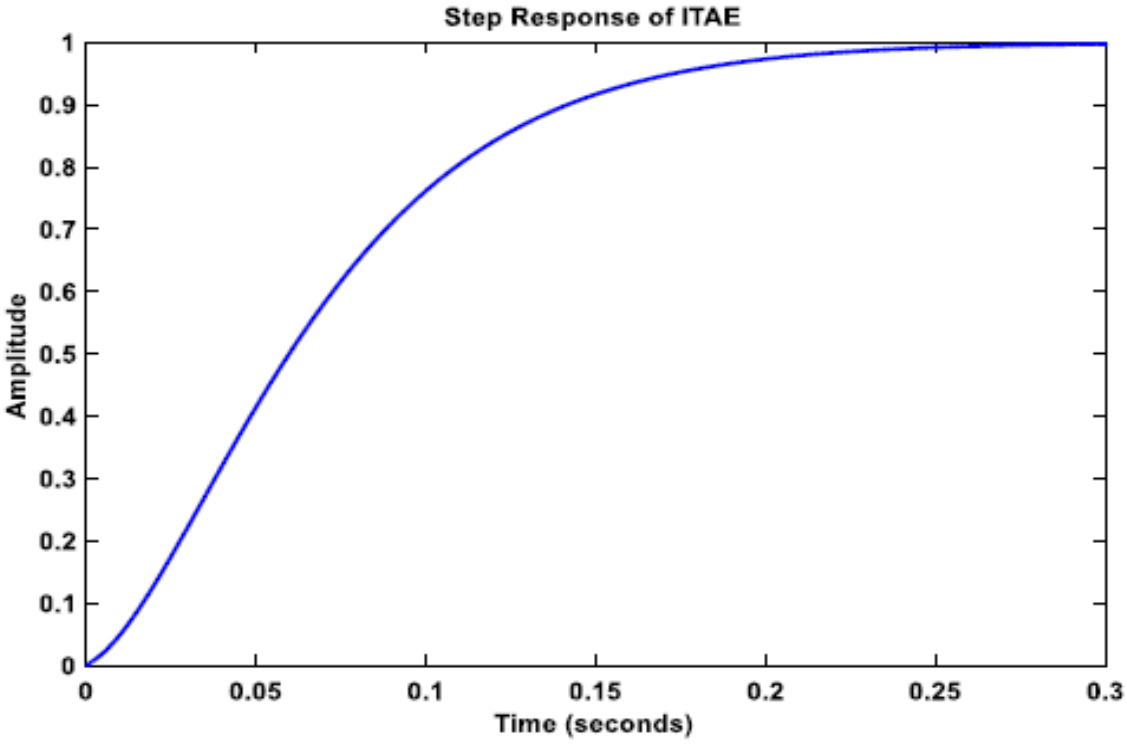


Figure 4.10(ii): ITAE PI Tuned Closed Loop Response of Boost Converter.

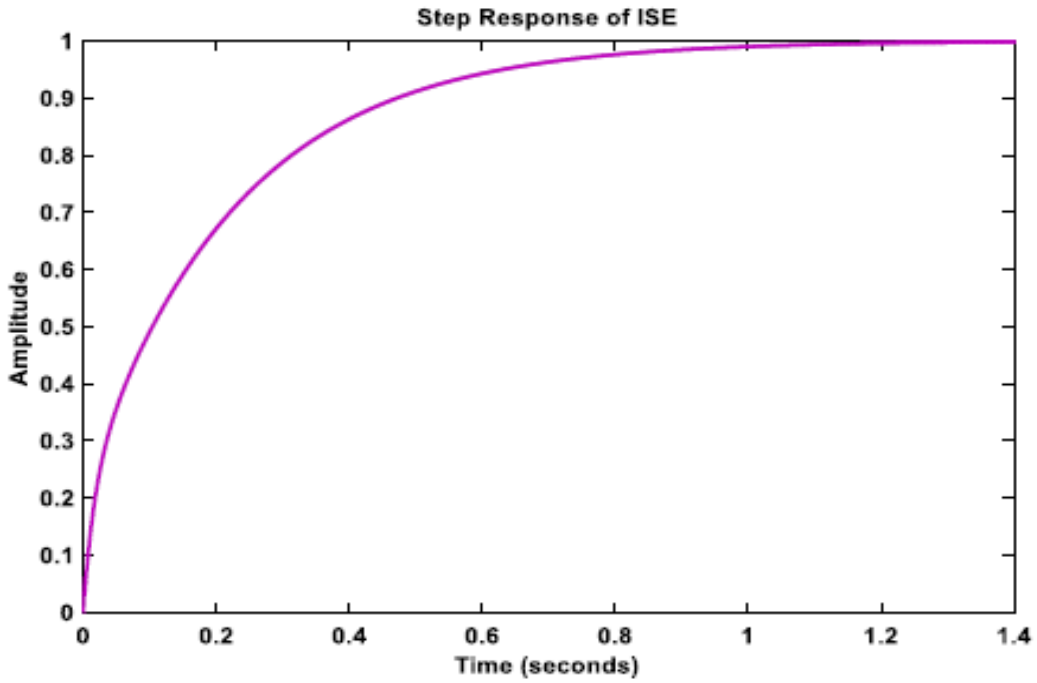


Figure 4.10(iii): ISE PI Tuned Closed Loop Response of Boost Converter.

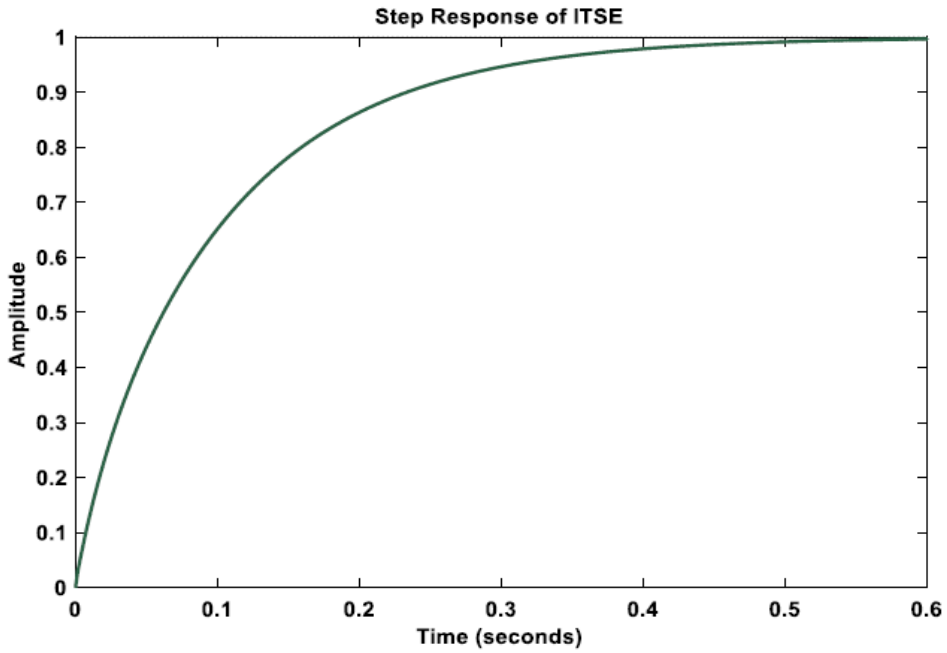


Figure 4.10(iv): ITSE PI Tuned Closed Loop Response of Boost Converter.

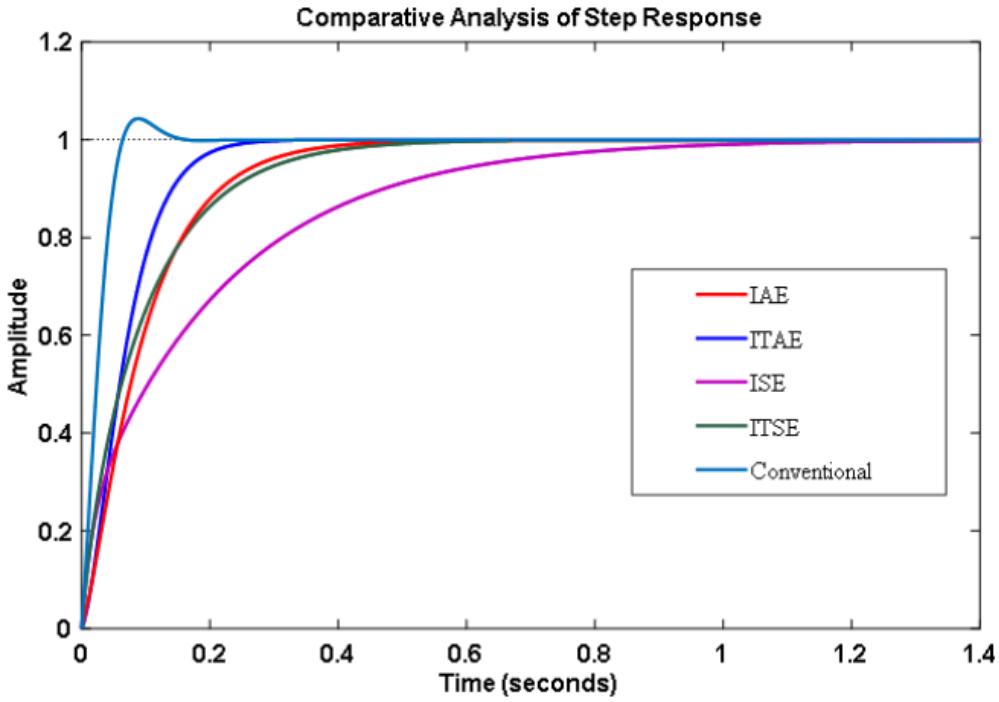


Figure 4.10(v): Comparison of all PI Tuned Closed Loop Responses of Boost Converter.

	Kp	Ki	Rise time(Tr)	Settling Time(Ts)	% Overshoot	Best Function Value
IAE	29.368	3390.13	0.2	0.355	**0**	0.106007
ITAE	**16.008**	4796	0.125	0.212	**0**	0.00354099
ISE	114.996	**1868.1**	0.465	0.84	**0**	0.080074
ITSE	99.9	3536	0.465	0.84	**0**	**0.00224663**
CONVENTIONAL	111.7133	14692.05	**0.044**	**0.122**	4	n/a

TABLE 7.7: Combined Gain Value and Performance Chart for SA PI Tuned Boost Converter.

4.3.3: BUCK-BOOST CONVERTER:

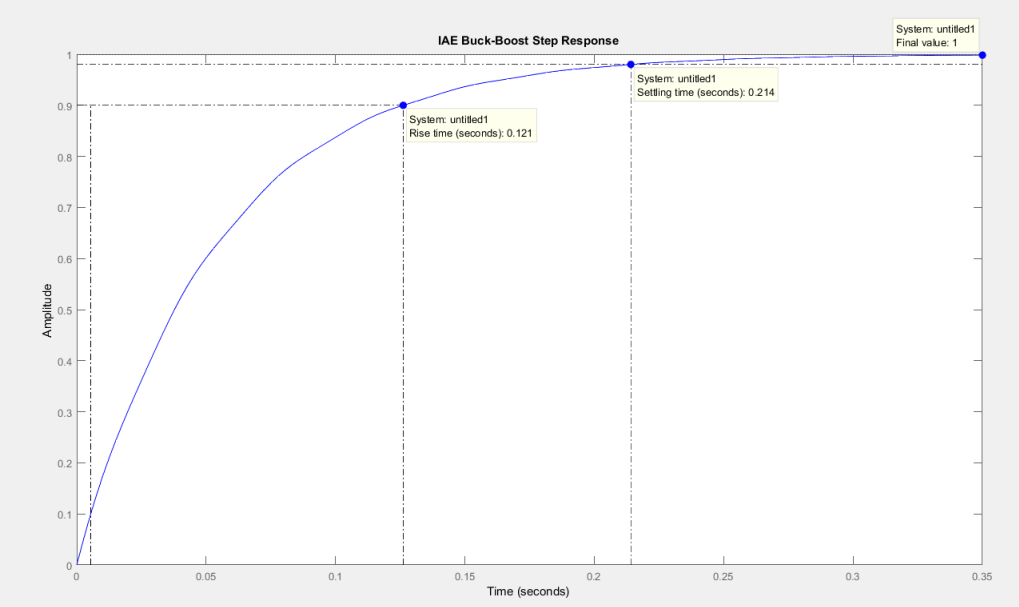


Figure 4.11(i): IAE PI Tuned Closed Loop Response of Buck-Boost Converter.

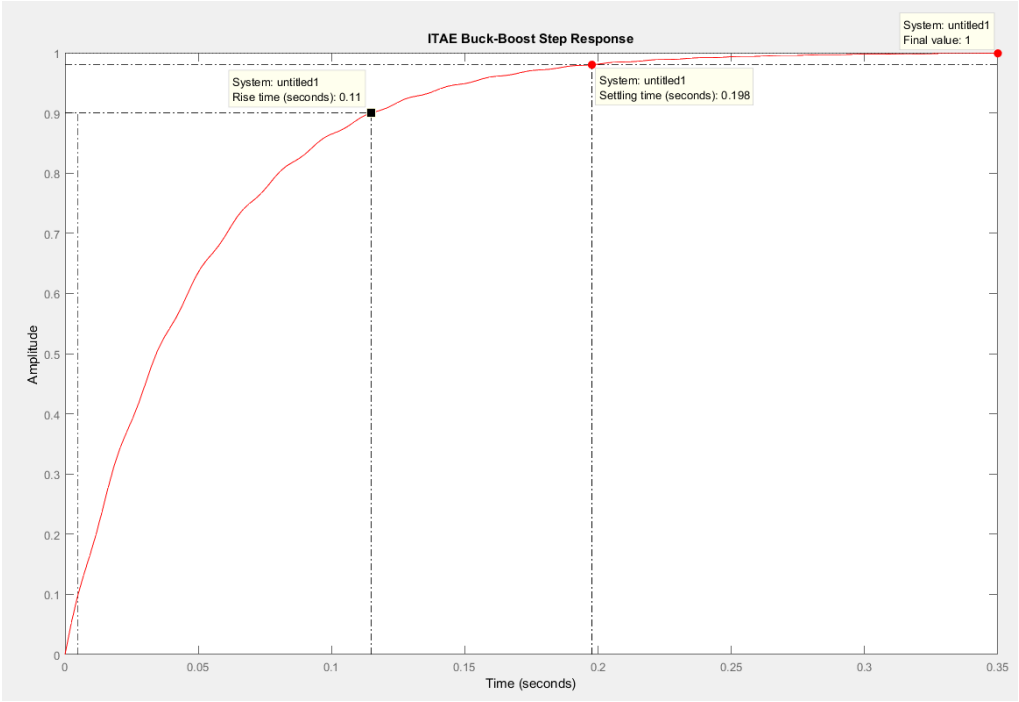


Figure 4.11(ii): ITAE PI Tuned Closed Loop Response of Buck-Boost Converter.

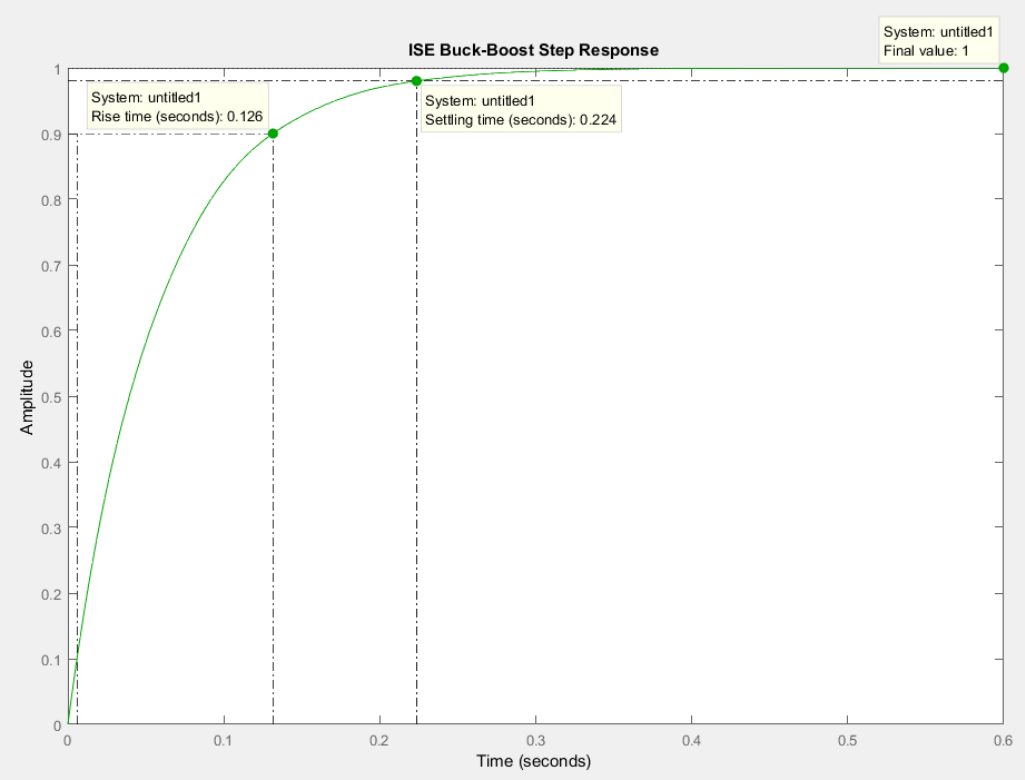


Figure 4.11(iii): ISE PI Tuned Closed Loop Response of Buck-Boost Converter.

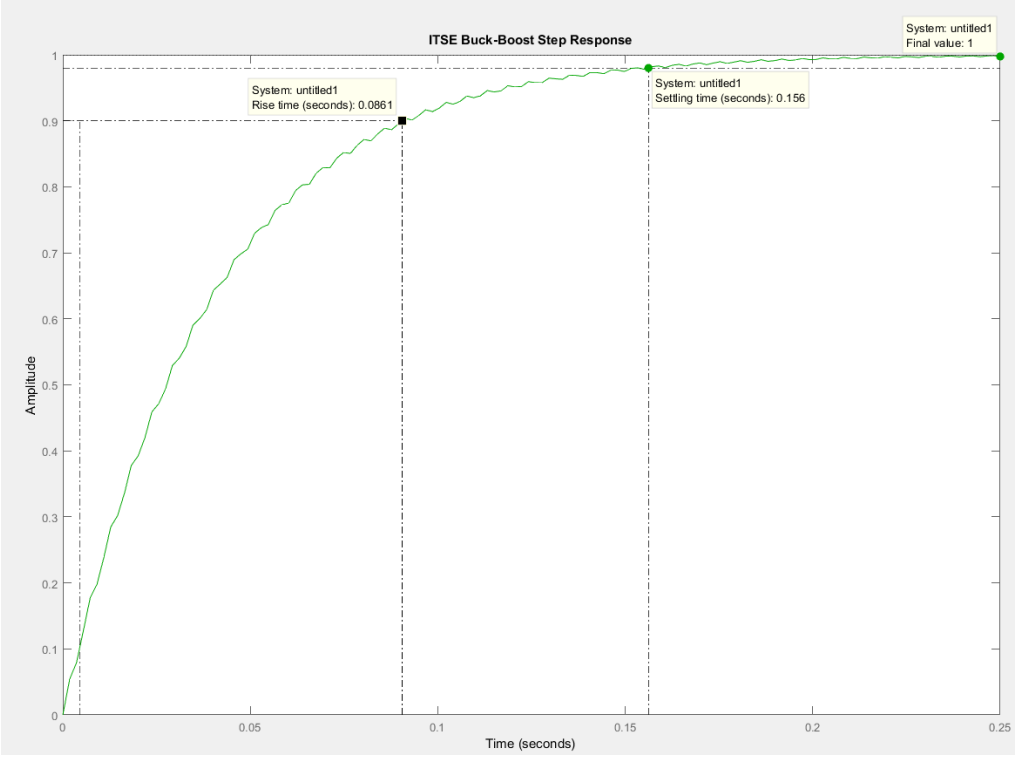


Figure 4.11(iv): ITSE PI Tuned Closed Loop Response of Buck-Boost Converter.

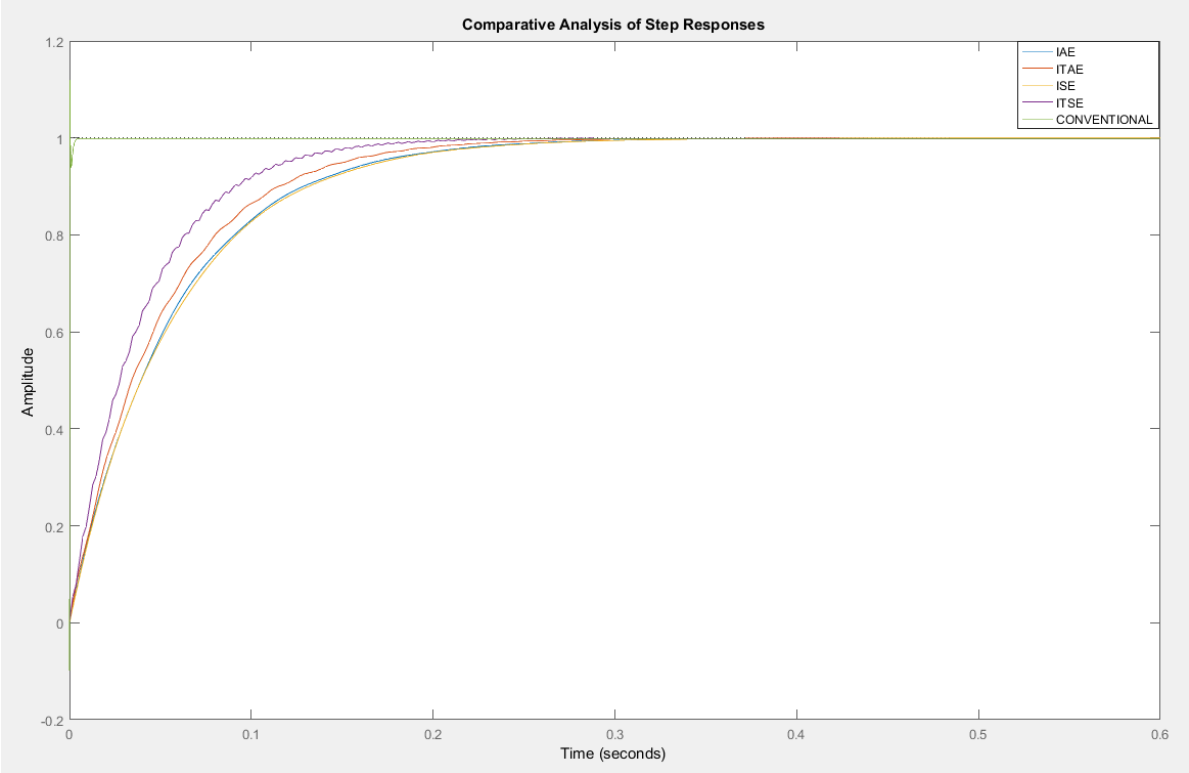


Figure 4.11(v): Comparison of all PI Tuned Closed Loop Responses of Buck-Boost Converter.

	Kp	Ki	Rise time(Tr)	Settling Time(Ts)	% Overshoot	Best Function Value
IAE	**0**	0.06016	0.121	0.214	**0**	0.106007
ITAE	**0**	0.06725	0.11	0.198	**0**	0.00354099
ISE	**0**	**0.059**	0.126	0.224	**0**	0.080074
ITSE	**0**	0.085	**0.0861**	**0.156**	**0**	**0.00224663**
CONVENTIONAL	0.03294	29.9927	n/a	n/a	n/a	n/a

TABLE 7.8: Combined Gain Value and Performance Chart for SA PI Tuned Buck-Boost Converter.

4.3.4: CUK CONVERTER:

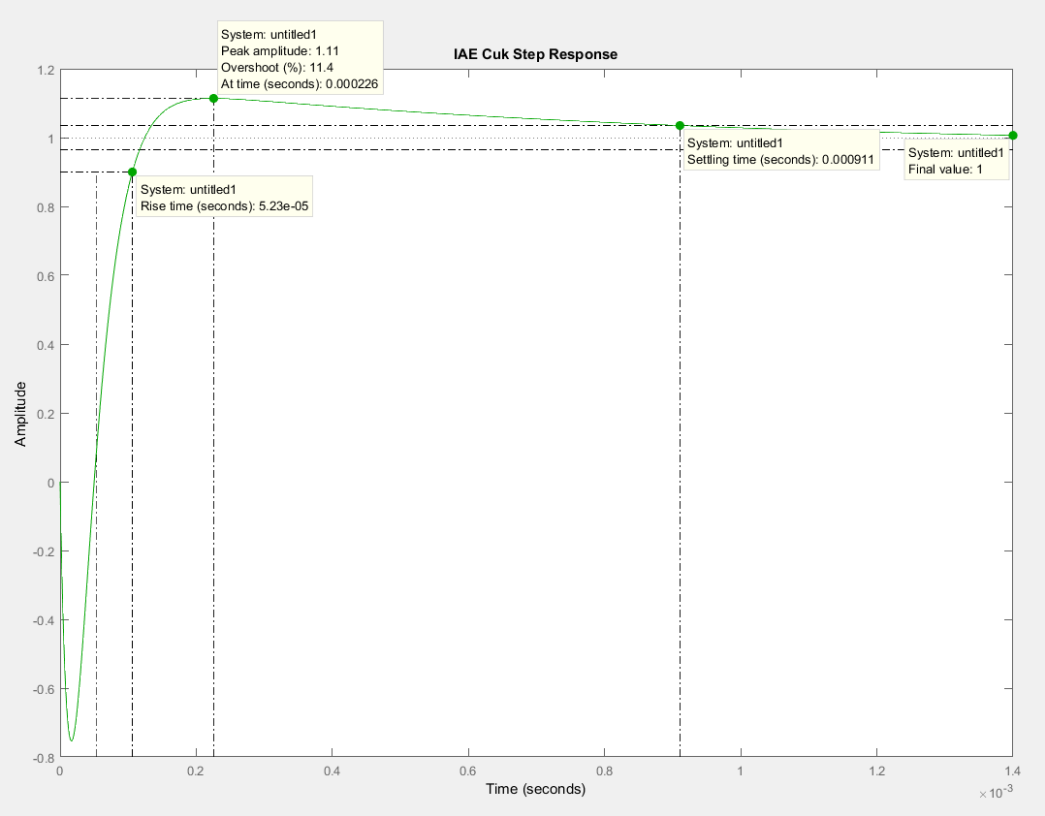


Figure 4.12(i): IAE PI Tuned Closed Loop Response of Cuk Converter.

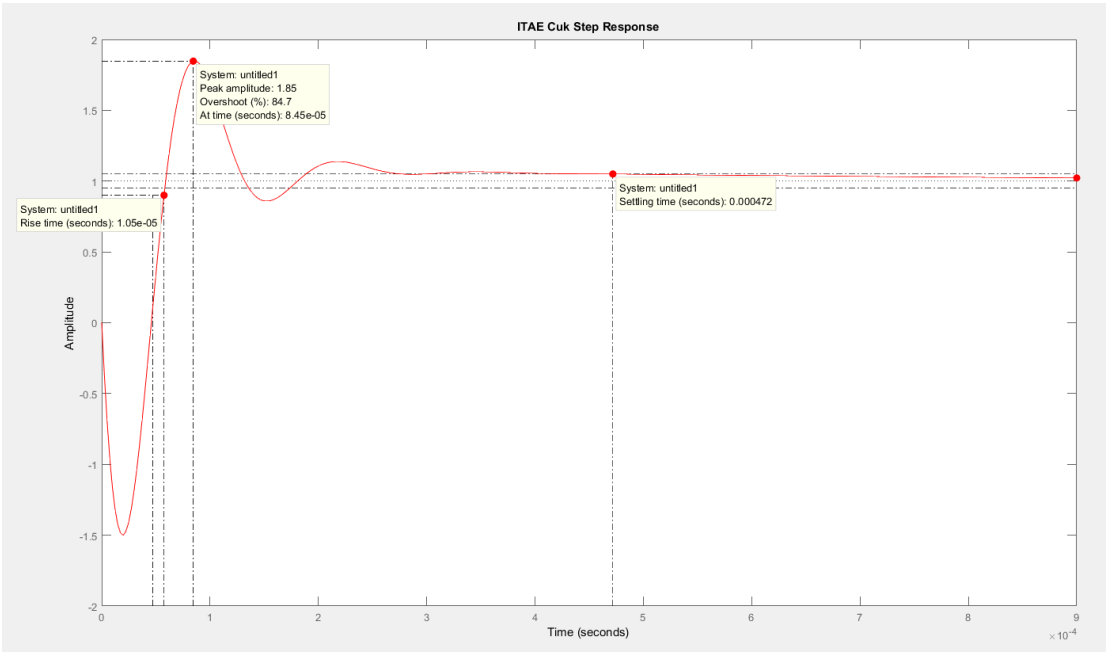


Figure 4.12(ii): ITAE PI Tuned Closed Loop Response of Cuk Converter.

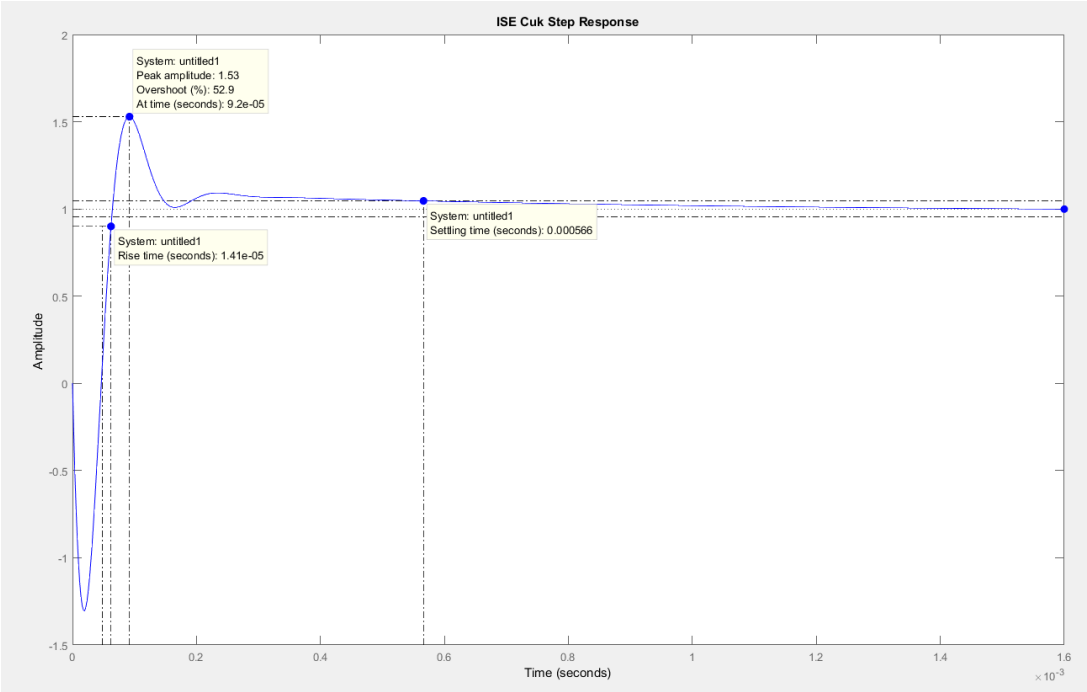


Figure 4.12(iii): ISE PI Tuned Closed Loop Response of Cuk Converter.

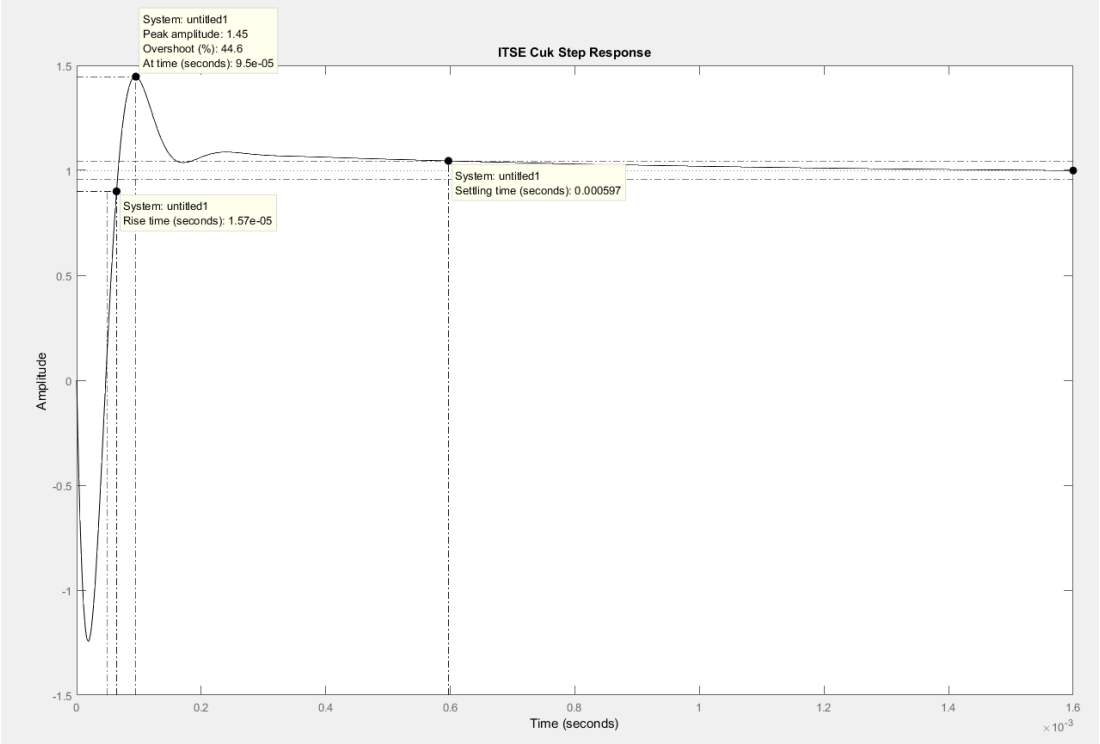


Figure 4.12(iv): ITSE PI Tuned Closed Loop Response of Cuk Converter.

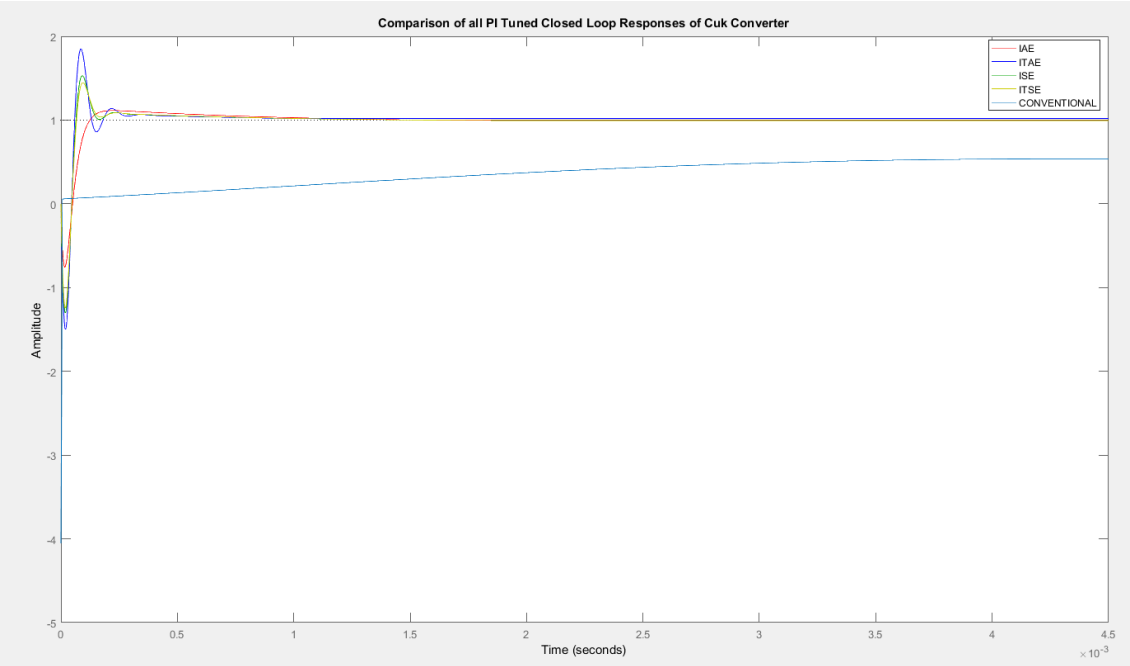


Figure 4.12(v): Comparison of all PI Tuned Closed Loop Responses of Cuk Converter.

	Kp	Ki	Rise time(Tr)	Settling Time(Ts)	% Overshoot	Best Function Value
IAE	1.154	0	5.23e-05	0.000911	**11.4**	0.106007
ITAE	1.649	**0.3948**	**1.05e-05**	**0.000472**	84.7	0.00354099
ISE	1.547	2.143	1.41e-05	0.000566	52.9	0.080074
ITSE	1.513	0.543	1.57e-05	0.000597	44.6	**0.00224663**
CONVENTIONAL	**0.009146**	0.44534	0.0297	0.16	20.7	n/a

TABLE 7.9: Combined Gain Value and Performance Chart for SA PI Tuned Cuk Converter.

Chapter 5: Discussion of Results and Conclusion

In this chapter, the results obtained from the simulation will be discussed as well as the future prospects of our research and a conclusion that shall be derived from the entire study.

5.1 DISCUSSION OF RESULTS:

This section of the chapter goes through the discussion of the simulation results obtained from the optimization of the converter topologies and provides reasoning for the best obtained values of Kp and Ki. The results shown from TABLE 7.6 to TABLE 7.9 give a clear observation of the improvement in Rise time(Tr), Settling time(Ts) and percentage Overshoot, due to the implementation of SA algorithm in obtaining Kp and Ki.

5.1.1 OBSERVATION OF BUCK CONVERTER OPTIMIZATION:

The following observations have been made from **TABLE 7.6**:

- The lowest value of Kp was determined from the SA algorithm employed on the **ITSE** objective function. This value of Kp is observed as **0.029**.
- The lowest value of Ki was determined from the SA algorithm employed on the **ISE** objective function. This value of Ki is observed as **55.433**.
- According to the step response characteristics, the lowest value of Tr is observed to be **3.92e-05** seconds in the **IAE** PI tuned closed loop response. This is significantly smaller than the rise time of **0.00177** seconds, obtained in conventional PI tuned configuration.
- The lowest value of Ts is observed to be **0.000107** seconds that is also obtained from **IAE** PI tuned closed loop response. This value is markedly reduced from the settling time of **0.00359** seconds obtained in the conventional PI tuned configuration.
- However, the Conventional PI tuned response successfully observed a **0%** overshoot, in comparison to the **69.3%** overshoot in **IAE** PI tuned response. Yet, it must be recognised that the overshoot occurs over a very short period of time and is hence, a manageable tradeoff.
- Thereby, the employment of the SA algorithm on the closed loop response of the Buck converter to obtain improved Kp and Ki values has been successfully established by the SA algorithm optimization executed with **IAE** as the objective function.

5.1.2 Observation of Boost Converter Optimization:

The following observations have been made from **TABLE 7.7**:

- The lowest value of Kp was determined from the SA algorithm employed on the **ITAE** objective function. This value of Kp is observed as **16.008**.
- The lowest value of Ki was determined from the SA algorithm employed on the **ISE** objective function. This value of Ki is observed as **1868.1.**
- According to the step response characteristics, the lowest value of Tr is observed to be **0.044** seconds in the Conventional PI tuned closed loop response. This is comparatively smaller to its closest contender **of 0.125** seconds, obtained in **ITAE** PI tuned configuration.
- The lowest value of Ts is observed to be **0.122** seconds that is also obtained from Conventional PI tuned closed loop response. However, this value is half of the settling time of **0.212** seconds also obtained in the **ITAE** PI tuned configuration so that the latter configuration is close to the former.
- However, the Conventional PI tuned response observed a **4%** overshoot, in comparison to the no overshoot in any of the SA employed PI tuned responses. Hence, the system appears to provide greater stability when it is run on PI parameters obtained from employing SA algorithm.
- Thereby, the employment of the SA algorithm on the closed loop response of the Boost converter will successfully provide greater stability than conventional PI tuned configuration. But, on employing the former, the value of Tr and Ts will increase as a tradeoff, which may be manageable. The optimized response is produced by the PI tuned configuration of the closed loop Boost Converter using **ITAE** as the objective fuction for optimization.

5.1.3 Observation of Buck-Boost Converter Optimization:

The following observations have been made from **TABLE 7.8**:

- The value of Kp obtained from employing SA algorithm on the closed loop response of the Buck-boost converter was **0** for all the performance indices used in the optimization of the objective function. This is relatively close to the minimal Kp value of **0.03924** obtained by conventional PI tuning of the system.
- The lowest value of Ki was determined from the SA algorithm employed on the ISE objective function. This value of Ki is observed as **0.059** and is much smaller than the Ki value of **29.9927** obtained from convetional PI tuning of the system.

- According to the step response characteristics, the lowest value of Tr is observed to be **0.0861** seconds in the ITSE PI tuned closed loop response. It is observed that when the Buck-Boost converter is tuned using the conventional tuning method, the rise time cannot be calculated as the response diverges away instead of reaching a steady value. Hence, the conventional PI tuned response of the system failed to reach stability.
- The lowest value of Ts is observed to be **0.0.156** seconds that is also obtained from ITSE PI tuned closed loop response. In this case, the conventional PI tuned response once again failed to provide a settling time since the closed loop response of the Buck-Boost converter does not converge to a steady value so that there is no settling time.
- As in the case of overshoot being encountered, the optimization of the closed loop converter response yields **0** overshoot when it is tuned with any of the 4 performance indices in SA algorithm. On the other hand, the overshoot produced by conventional PI tuning appears to be incalculable due to the closed loop response indefinitely diverging out.
- Therefore, according to the results procured from the simulation, the employment of the SA algorithm on the closed loop response of the Buck-Boost converter to obtain improved Kp and Ki values has been successfully established by the SA algorithm optimization executed with **ITSE** as the objective function.

5.1.4 Observation of Cuk Converter Optimization:

The following observations have been made from **TABLE 7.6**:

- The lowest value of Kp was determined from the Conventional PI tuned configuration. This value of Kp is observed as **0.009146**.
- The lowest value of Ki was determined from the SA algorithm employed on the **ITAE** objective function. This value of Ki is observed as **0.3948**.
- According to the step response characteristics, the lowest value of Tr is observed to be **1.05e-05** seconds in the **ITAE** PI tuned closed loop response. This is significantly smaller than the rise time of **0.0297** seconds, obtained in conventional PI tuned configuration.
- The lowest value of Ts is observed to be **0.000472** seconds that is also obtained from **ITAE** PI tuned closed loop response. This value is markedly reduced from the settling time of **0.16** seconds obtained in the conventional PI tuned configuration.
- However, the Conventional PI tuned response successfully observed a 20.7**%** overshoot, in comparison to the **84.7%** overshoot in **ITAE** PI tuned response. This large value of overshoot could be dangerous for the system.
- Compared to the ITAE PI tuned closed loop response of the Cuk converter, the IAE PI tuned closed loop response yields a modest Tr of **5.23e-05** seconds, a Ts of **0.000911**

seconds and an overshoot of only **11.4%.** Hence, this configuration yields very close results to the ITAE PI tuned system, but mitigates the problem of having a large overshoot.

- Thereby, the employment of the SA algorithm on the closed loop response of the Cuk converter to obtain improved Kp and Ki values has been successfully established by the SA algorithm optimization executed with **IAE** as the objective function.

5.2 CONCLUSION:

In the motivation of our research, we had mentioned that the core purpose of our analysis is to derive improved values of Kp and Ki to seamlessly operate the DC-DC controllers and reap better closed loop responses. The media of our analysis implements the SA algorithm as its optimization search algorithm.

After conducting rigorous simulations on the four DC-DC converter topologies, the results have been proven to be coherent with the objective of our research. Implementing the SA optimization algorithm on the closed loop DC-DC converter systems have successfully yielded better closed loop responses. Testing for the improvement of Rise Time, Settling Time, and Percentage Overshoot have provided clear representations of the improved step characteristics of the Buck, Boost, Buck-Boost and Cuk converters, with reference to Figures 4.9(v), 4.10(v), 4.11(v) and 4.12(v).

Therefore, in conclusion to this research, the Simulated Annealing Algorithm has been proven to be a successful metaheuristic algorithm that can be implemented to obtain better PI parameters for tuning the closed loop DC-DC converter performances. Instead of manually assessing the circuit using Zeigler-Nichols method, or making use of the manual PID tuner of MATLAB which is conventionally used, the unique search algorithm was implemented. Furthermore, the 4 performance indices have broadened the entire analysis on each converter topology, giving numerous alternative responses from which the best could be chosen. Hence, this procedure will aid designers to simulate more robust responses on closed loop DC-DC converters and employ them on a variety of electronic applications.

5.3 Future Working Proposal:

Our research was centred around the operation of non-isolated converters which included the Buck, Boost, Buck-Boost and Cuk converters. However, in future, we intend to implement our optimization technique on isolated converters such as Flyback converter and Sepic converters to widen the reach of this optimization technique in aiding design for various electronic applications.

References

[1] DC-DC Power Converters, Robert W. Erickson, Department of Electrical and Computer Engineering, University of Colorado.

[2] Control Systems Engineering, 6th Edition, Norman S. Nise.

[3] Microelectronic Circuits, 6th Edition, Adel S. Sedra, Kenneth C. Smith.

[4] Power Electronics, 3rd Edition, Muhammad H. Rashid.

[5] Open Loop Small-Signal Control-to-Output Transfer Function of PWM Buck Converter for CCM: Modeling and measurements, M. Bartoli, A. Reatti, Member, IEEE, Universita' degli Studi di Firenze.

[6] Open-Loop Peak Voltage Feed Forward Control of PWM Buck Converter, Marian K. Kazimierczuk, Senior Member, IEEE, and Anders J. Edström.

[7] Digital Controller Design for Buck and Boost Converters Using Root Locus Techniques, Liping Guo, John Y. Hung and R. M. Nelms, Department of Electrical & Computer Engineering, Auburn University

[8] Modelling and Design of a Current Mode Control Boost Converter, Hong Yao, Department of Electrical and Computer Engineering, Colorado State University.

[9] Analysis of Boost Converter Using PI Control Algorithms, Mitulkumar R. Dave, K.C. Dave, International Journal of Engineering Trends and Technology - Volume 3, Issue 2, 2012.

[10] Performance Analysis of Boost Converter Using Fuzzy Logic and PID Controller, S.S.Shinde, Control system Engineering, College of Engineering Ambejogai, S.S.Sankeshwari, Electrical Electronics and Power Engineering, College of Engineering Ambejogai.

[11] Stability Analysis of DC-DC Boost Converter by Employing Simulated Annealing Algorithm Based Optimized PI Controller, Mirza Muntasir Nishat, Fahim Faisal, Md Ashraful Hoque, Syed Sabeth Salwa Al Musawi, S.M Rafi Uddin, Kaiser Hossain Evan and S.M Taif-Ul-Kabir, Department of Electrical and Electronic Engineering, Islamic University of Technology.

[12] Design, Modelling and Simulation of a PID Controller for Buck Boost and Cuk Converter, Priyadarshini, 1M-Tech, Department of ECE, Canara Engineering College, Dr. Shantharam Rai, Professor, Deparment of ECE, Canara Engineering College.

[13] Modeling and Simulation of Buck-Boost Converter with Voltage Feedback Control, Xuelian Zhou, Qiang He, College of Computer and Information Science, Southwest University.

[14] Development of Power Electronics,Buck Boost Converter, Based PI-PID Control On Horizontal Wind Turbine Generation, For Low Rate Wind speed, Ali Musyafa, Associate Professor, Department Of Engineering Physics, Sepuluh Nopember Institute of Technology, Andi Rahmadiansyah, Lecturer, Department Of Engineering Physics, Sepuluh Nopember Institute of Technology, Ronny Dwi Noriyati, Senior Lecturer, Department Of Engineering Physics, Sepuluh Nopember Institute of Technology.

[15] An Efficient Control Approach for DC-DC Buck-Boost Converter, Faruk Yalçın, Faculty of Technology, Department of Mechatronics Engineering Sakarya University, Felix A. Himmelstoss, Department of Electronic Engineering University of Applied Sciences Technikum Wien.

[16] Buck-Boost DC-DC Converter Control by Using the Extracted Model from Signal Flow Graph Method, Leila Mohammadian, Ebrahim Babaei, Mohammad Bagher Bannae Sharifian, International Journal of Applied Mathematics, Electronics and Computers.

[17] Analysis and Design of CUK Converter using PI Controller for PV Application, IJSRD - International Journal for Scientific Research & Development| Vol. 2, Issue 02, 2014. Y. Bhaskar S S Gupta, Sri Rama Lakshmi, Assistant Professor, School of Electrical and Electronics VIT, Chennai.

[18] Analysis of Cuk Converter using PI and OCC Control Method, M. Bildirici, A. Karaarslan, Faculty of Engineering and Natural Sciences, Yildirim Beyazit University. ICTPE Conference, 13th International Conference on “Technical and Physical Problems of Electrical Engineering”.

[19] Controller Design for Cuk Converter Using Model Order Reduction, Brijesh Kumar Kushwaha and Mr. Anirudha Narain, 2012 2nd International Conference on Power, Control and Embedded Systems.

[20] Analysis and Design of a Cuk Switching Regulator, Zekiye Gunaydin, Elec. Electronics Engineering Dept., Middle East Technical University.

[21] M. M. Nishat, F. Faisal and M. A. Hoque. “Modeling and Stability Analysis of a DC-DC SEPIC Converter by Employing Optimized PID Controller Using Genetic Algorithm” International Journal of Electrical & Computer Sciences IJECS-IJENS 19, no. 01(2019)

[22] Busetti, F. (2003). Simulated annealing overview. World Wide Web URL www. geocities. com/francorbusetti/saweb. pdf.

[23] Milano, M., Hayes, W., Veltri, P., Cannataro, M., & Guzzi, P. H. (2018, August). SL-GLAlign: Improving the Local Alignment of Biological Networks through Simulated Annealing. In Proceedings of the 2018 ACM International Conference on Bioinformatics, Computational Biology, and Health Informatics (pp. 577-578). ACM.

[24] Wei, L., Zhang, Z., Zhang, D., & Leung, S. C. (2018). A simulated annealing algorithm for the capacitated vehicle routing problem with two-dimensional loading constraints. European Journal of Operational Research, 265(3), 843-859.

[25] GirirajKumar, S. M., Rakesh, B., & Anantharaman, N. (2010). Design of controller using simulated annealing for a real time process. International Journal of computer applications, 6(2), 20-25.

[26] Soni, Y. K., & Bhatt, R. (2013). Simulated Annealing Optimized PID Controller Design using ISE IAE IATE and MSE Error Criterion. International Journal of Advanced Research in Computer Engineering & Technology, 2.

Image References

FIGURE1.1(i): https://www.indiamart.com/proddetail/stainless-steel-power-diode-14505637912.html

FIGURE 1.1(ii): https://www.sparkfun.com/products/10213

FIGURE 1.1(iii): https://au.rs-online.com/web/p/igbts/1241304/

FIGURE 1.1(iv):https://www.goldmine-elec-products.com/prodinfo.asp?number=G23223

FIGURE 1.3: https://www.allaboutcircuits.com/technical-articles/utilization-of-simple-converters-circuits/

FIGURE 1.4(i): https://www.researchgate.net/figure/Buck-converter-equivalent-circuit-in-ON-state-2-Off-state-period-As-shown-in-Fig-1-when_fig5_287487841

FIGURE 1.4(ii): https://www.researchgate.net/figure/Buck-converter-equivalent-circuit-in-OFF-state_fig6_287487841

FIGURE 1.4(iii): https://www.allaboutcircuits.com/technical-articles/analysis-of-four-dc-dc-converters-in-equilibrium/

FIGURE 1.5: https://www.allaboutcircuits.com/technical-articles/analysis-of-four-dc-dc-converters-in-equilibrium/

FIGURE 1.6(i): https://www.researchgate.net/figure/Mode-1-operation-of-boost-converter-b-Mode-2-In-this-mode-switch-S-is-OFF-the-inductor_fig3_305648380

FIGURE 1.6(ii): https://www.researchgate.net/figure/Mode-2-operation-of-boost-converter_fig4_305648380

FIGURE 1.6(iii):Power Electronics Handbook by Dr. Muhammad Harunur Rashid

FIGURE 1.7: https://www.eetimes.com/document.asp?doc_id=1273276

FIGURE 1.8(i): https://www.eetimes.com/document.asp?doc_id=1273276

FIGURE 1.8(ii): https://www.eetimes.com/document.asp?doc_id=1273276

FIGURE 1.8(iii): Power Electronics Handbook by Dr. Muhammad Harunur Rashid

FIGURE 1.9: https://www.allaboutcircuits.com/technical-articles/analysis-of-four-dc-dc-converters-in-equilibrium/

FIGURE 1.10(i): https://www.allaboutcircuits.com/technical-articles/analysis-of-four-dc-dc-converters-in-equilibrium/

FIGURE 1.10(ii): https://www.allaboutcircuits.com/technical-articles/analysis-of-four-dc-dc-converters-in-equilibrium/

FIGURE 1.10(iii): Power Electronics Handbook by Dr. Muhammad Harunur Rashid

FIGURE 2.1: https://www.phy.ornl.gov/csep/mo/node34.html

FIGURE 2.2: Franco Busetti- "Simulated annealing overview"

FIGURE 2.3: Stability Analysis of DC-DC Boost Converter by Employing Simulated Annealing Algorithm Based Optimized PI Controller-Mirza Muntasir Nishat, Fahim Faisal, Md Ashraful Hoque, Syed Sabeth Salwa Al Musawi, S.M Rafi Uddin, Kaiser Hossain Evan and S.M Taif-Ul-Kabir