Chapter 1
Introduction

1.1 Introduction

A converter is the basic element of a power electronics system. It employs power semiconductor devices and possible energy storage elements like inductors and capacitors. Depending on the frequency on the two sides, converters can be branched to the following categories:

i) AC to DC converter

ii) DC to DC converter

iii) DC to AC converter

iv) AC to AC converter

Based on how the devices within the converter are switched, there are three classifications:
1)Line frequency converter: Here, the devices are switched on and off at line frequencies of 50 or 60 Hz.

2) Switching converters: In these converters, the switching frequency is very much higher compared to line frequency.

3) Resonant converters: Here, the controllable switches are turned on and off at zero voltage or zero current [1].

There has been a deep study in switched-mode power converters. They are classified as single inductor converters like Buck, Boost and Buck-Boost and double inductor converters like C*û*k, SEPIC, and Zeta[2-11].One modification of the converters is done utilizing a tapped-inductor in which the tapping of the inductor is connected to other components such as primary switching device, freewheeling diode, input or output rails[12-14]. There has been a constant urge to escalate the switching frequency for allowing the usage of smaller filters and energy storage elements [15-17]. This has brought a change in switched-mode power conversion in attaining greater power density and finer dynamic performance.

Solid-state devices often contain parasitic capacitances. As the energy stored in these capacitances change abruptly, there occurs a switching loss at turn-on. Output capacitance also stores energy in solid-state electronic devices. This energy is consumed in the device when the transistor turns on. Rectifiers have junction capacitance, which is charged by the switch in a dissipative manner. Leakage inductance is mainly responsible for the switching loss when the transistor turns off. The sharp di/dt induces a voltage spike across the leakage inductance when an active switch is turned off[18]. Numerous types of recent portable appliances, computers and various other applications integrate a broad number of low-power switch-mode power supplies. These devices process power from a chunk of watt to a few hundreds of watts. In this SMPS, there exist reactive components like inductors. These inductors take an important fraction of total device volume and weight. In numerous applications, they take up more than 25% of overall device volume thus creating a significant hurdle to further system minimization [19].

1.2 AC-DC Switch-Mode Converters

AC-DC converters have many applications, including industrial and domestic ones like uninterruptible power supplies and small-scale wind energy conversions systems [20-23].

A double-stage AC-DC Buck-Boost converter was presented in [24,25]. Here the first phase serves as a Boost converter and the second phase serves as a Buck converter. The main deficiency of the converter is that control becomes arduous in the time of shifting between step-up and step-down topologies. A one-stage AC-DC Buck-Boost converter was proposed in [26,27]. It operates in continuous conduction mode. The converter needs a controller in closed-loop system to activate PFC. The main demerit of the converter is that; it suffers from large spikes of discontinuous current in the input capacitor side which causes extreme potential stress at switching equipment's [28]. Several topologies are proposed that operate in a discontinuous conduction mode(DCM) for reduced cost and control complexity [29-30]. The drawback of these converters is that they suffer from switch high current stress. The use of recently developed power converters is increasing day by day and with this trend, the power quality of ac systems arises as a significant issue. In a power grid, several devices are connected together. Harmonic voltage distortion in one device can alter the operation of other devices. Active power factor correction (PFC) became essential on power supplies to lessen harmonic contamination in power lines and improve transmission efficiency. Power factor correction schemes have been carried out mainly for heavy industrial loads such as induction motors, induction heating furnaces, etc. However, PFC has

become a crucial aspect even for low power application electronic equipment [31-34]. PFC circuits produce imperceptible harmonics in the input line current. These circuits lead to almost unity load power factor. PFC circuits and SMPS contain a bridge rectifier. A high-frequency DC-DC converter follows this rectifier. Conduction losses occur due to diode forward voltage drop. It lessens the overall efficiency of the system. With the increase of power level there is risk of destruction of individual diode due to the generation of heat in the bridge rectifier. Traditional full-wave diode bridge rectifiers suffer from distorted input current. Another deficiency is that; power factor remains low at input side. Various approaches have been taken to work out these demerits. One approach is to use an input filter but the solution requires bulky inductor and capacitor. This method can provide low input current THD but it comes at the cost of low power factor. Switch-mode converters have been introduced to overcome the problems. Traditional single-phase AC-DC switch-mode converter has a full-wave bridge rectifier. A DC-DC converter follows this rectifier [33,35-39]. Switch-mode converters using a Boost DC-DC converter after the bridge rectifier are the most found ones. Buck, Buck-Boost, C$\hat{u}$k and SEPIC topologies may also be implemented[39-42]. Traditional AC-DC converters for the Buck, Boost, Buck-Boost, C$\hat{u}$k, SEPIC, and Zeta topologies are not furnished to provide the required voltages from the line voltages for many updated applications. In the coming days, microprocessors will use any dimension of power from 1V to 3V rather than using a 5V power supply. This is to lessen the CPU power loss. In recent times, as demanded by numerous appliances, the voltage transformation ratio of the converters is needed to be acutely high and acutely low. At start-up, automobile headlamps need 100V at 35W. The supply is to come from 12V car battery. The case is same for high-intensity discharge lamps (HID) [43]. Some AC-DC converters, which are not controlled, contain a capacitor interface with the bridge rectifier. These circuits have certain disadvantages like non-sinusoidal source current and high THD. These demerits lead to the degradation of power quality at the point of common coupling (PCC) and affects other consumers linked to it. For restricting this, strict harmonic standards such as IEC 61000-3-2[44,45] are introduced. PFC can be implemented by passive or active ways. Passive PFC circuits employ bulky filters. Moreover, filter components required in these circuits are costly and lossy which leads to reduced efficiency [46-48]. Single-stage and double-stage topologies are used in active PFC circuits [49,50]. In single-stage topology, only one power transformation phase is used. In double-stage topology, the first phase is for power factor improvement. The second phase is a DC-DC converter whose task is to provide a reasonable voltage gain. The DC-DC converter is also responsible for output voltage regulation and ripple contraction. PFC converters can also be categorized on the basis of isolated and non-isolated

schemes. An analysis of these categories and control procedures in single-phase PFC is given in is [35]. Active PFC circuits are being used in modern power supply and power chargers. This is essential to fulfill certain harmonic regulation like IEC 61000-3-2[51]. PFC techniques are best suited to be implemented in boost converters as this type of converters are less costly and provide high performance. Normally, in AC-DC converters there is a bulky capacitor, which is placed after the diode bridge rectifier. The goal is to attain a smooth DC-link potential. A DC-DC converter is used to regulate this voltage to obtain a steady output voltage (DC). The DC-DC converter is operated at high switching frequencies. These type converters have certain disadvantages like input current harmonics and reduced power factor [52,53]. The DC-DC converter can take different forms based on the applications. They can be presented as full-bridge or flyback converter. The DC-DC converter in flyback form is best suited for low power appliances (< 100W). Generally, buck converters are used as step down converters where the output DC voltage is always less than the input voltage. Boost converters are step up converters where the output DC voltage is always higher than the input voltage. In numerous applications, DC power is required for DC loads. In inverter, a DC power source is needed. DC power supplies also require DC power sources. In this context, AC-DC converters are extensively used to fetch DC power from the AC grid. Traditionally used AC-DC converters like diode bridge rectifiers or thyristor rectifiers suffer from high input current THD and low input power factor [54,55].

1.3 Problem Identification

It is observed that the conventional converters involving transformers suffer from leakage inductance, causing massive voltage spike across the switches, diode bridge loss, and low power factor. Moreover, the size and the cost of these converters are significant because of the transformer, isolated sensors, and controllers. Like the isolated converters, coupled type non-isolated converters also suffer from leakage inductance of the coupled inductor. Conventional AC-DC converters use a full-wave bridge rectifier that has drawbacks like pulsating input current, high electromagnetic interference (EMI), high crest factor, low input power factor, low efficiency, and harmonic pollution at power system, etc. One approach is to use an input filter but the solution requires bulky inductor and capacitor. This method can provide low input current THD but it comes at the cost of low power factor. Switch-mode converters have been proposed to overcome these problems. As stated before, it is observed that different topologies of switch-mode converters have distinct disadvantages like difficult control during transitions between Buck and Boost modes, the requirement of multiple switches, and complex circuit operation due to an increased number of components. So, there is a

necessity to design such converters that have simple circuit operation with increased efficiency, power factor, and low THD. In this thesis, a single-phase single switch non-isolated AC-DC Buck-Boost converter is proposed with improved performance. Instead of using a single-phase rectifier followed by a DC-DC converter, two inductors and two capacitors are used with a suitable combination of switch and diodes.

1.4 Thesis Objective

The main objective of this thesis is to develop a new topology of modified input switched bridgeless AC-DC Buck-Boost converter. However, more particularly, the goals include:

i) To develop a non-isolated AC-DC Buck-Boost converter topology with improved performance.

ii) To analyze the performance of the proposed AC-DC converter and compare with the existing AC-DC converters.

1.5 Thesis Organization

This thesis focuses on the development of a novel Single Phase non-isolated AC-DC Buck-Boost Converter to improve efficiency, PF, and reduce THD of the system.

- In chapter 1, introduction of the thesis with background is discussed. Problem statements and objectives of the thesis are also included in this chapter.
- In chapter 2, a review of existing AC-DC converters is done. The review is based on the open-loop analysis of conventionally used single-phase AC-DC converters and of some recent single-phase AC-DC Buck-Boost converters. In the open-loop analysis voltage gain, overall efficiency, input power factor, and total harmonic distortion (THD) are analyzed with the variation of the duty cycle. A voltage gain comparison between the conventional converters is also provided.

- In chapter 3, the proposed single-phase non-isolated AC-DC Buck-Boost converter is discussed. Principle of operation of the proposed converter is stated with suitable figures. Voltage gain, overall efficiency, input power factor, and total harmonic distortion (THD) are analyzed with the variation of duty cycle, load, and frequency. The ideal voltage gain equation of the proposed converter is derived. A comparison is done between theoretical and simulation results of the proposed Buck-Boost converter. Simulation results are also provided.
- In chapter 4, a performance analysis is done between the proposed converter and existing converters.
- In chapter 5, a detailed analysis is given for the feedback controller used with the proposed converter. The dynamic response of the converter is inspected, and relevant simulation results are also provided.
- In chapter 6, the conclusion and the concise summary of the thesis is given. Some recommendations have also been provided along with discussing scopes of future works.

Chapter 2
Review of Existing AC-DC Converters

2.1 Conventional Circuit Topologies

Traditional AC-DC converters contain a full-wave bridge rectifier. A DC-DC converter follows this rectifier. The DC-DC converter controls the voltage gain characteristic of that specific converter. Traditional AC-DC circuit topologies like Buck, Boost, Buck-Boost, C$\hat{u}k$ and SEPIC are discussed from section 2.1.1 to 2.1.5. The open-loop performance analysis of the converters mentioned above is also done. Voltage gain, overall efficiency, input power factor, and total harmonic distortion (THD) are analyzed with the variation of the duty cycle. Voltage gain comparison of conventional converters is provided in Table 2.11.

2.1.1 Buck Converter

The conventional AC-DC Buck converter is shown in figure 2.1. The function of this converter is to step down the input signal. An inductor is used as an energy storage element. An input filter is used with the conventional circuit to reduce harmonics.

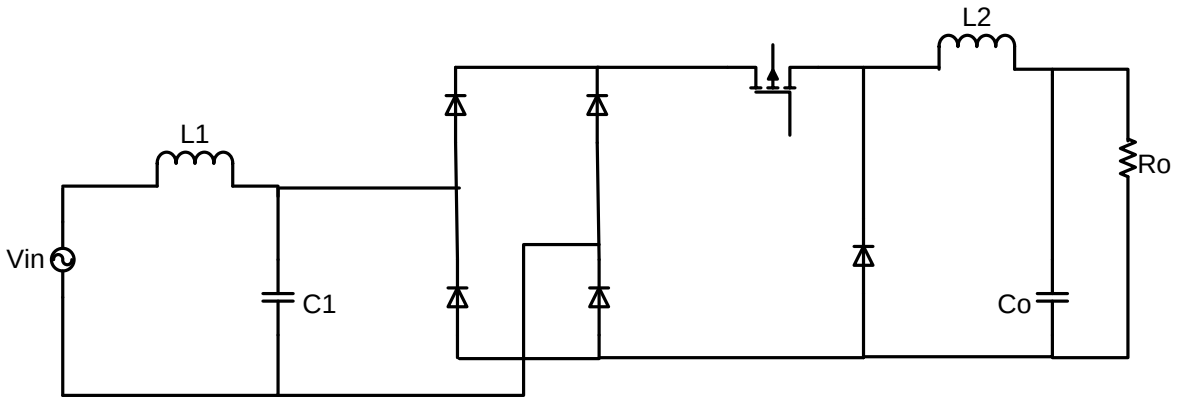


Figure 2.1 Conventional AC-DC Buck Converter with Input Filter

2.1.1.1 Open-loop data analysis

The simulation of the conventional Buck converter with an input filter has been performed using software simulation. The results obtained are presented in Table 2.2. Here MOSFET is acting as the switching device. The value of different circuit components is given in Table 2.1.

Table 2.1 Parameter Table for Conventional Buck Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mh
Inductor (L2)	1.5mh
Capacitance (C1)	1uf
Load across (Co)	220uf
Load Resistor (Ro)	100Ω

Table 2.2 Performance Analysis of Conventional Buck Converter under Duty Cycle Variation

Duty Cycle	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
0.1	2.29	0.68	8.27	0.168
0.2	8.134	0.77	15.45	0.314
0.3	14.29	0.73	21.56	0.312
0.4	25.43	0.73	35.67	0.406
0.5	8.95	0.72	59.7	0.504
0.6	43.62	0.69	72.35	0.599
0.7	51	0.66	83.7	0.690
0.8	56.72	0.63	88.1	0.773
0.9	60.79	0.60	89.45	0.86

2.1.2 Boost Converter

The conventional AC-DC Boost converter is shown in figure 2.2. The function of this converter is to step up the input signal. An inductor is used to preserve and transfer energy. An input filter is used with the conventional circuit to reduce harmonics.

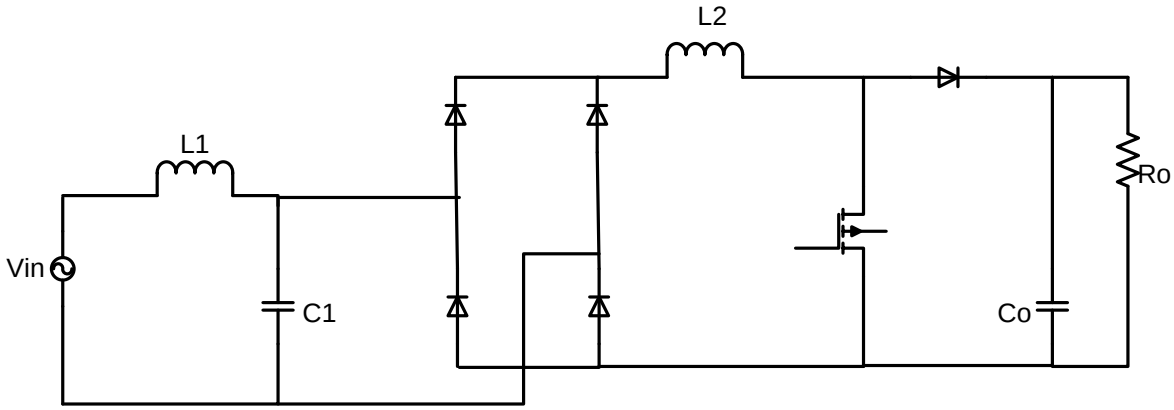


Figure 2.2 Conventional AC-DC Boost Converter with Input Filter

2.1.2.1 Open-loop data analysis

The simulation of the conventional Boost converter with an input filter has been performed using software simulation. The results obtained are presented in Table 2.4. Here MOSFET is acting as the switching device. The value of different circuit components is given in Table 2.3.

Table 2.3 Parameter Table for Conventional Boost Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mH
Inductor (L2)	1.5mH
Capacitance (C1)	1uF
Load across (Co)	220uF
Load Resistor (Ro)	100Ω

Table 2.4 Performance Analysis of Conventional Boost Converter under Duty Cycle Variation

Duty Cycle	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
0.1	90.22	0.62	107	1.5
0.2	90.24	0.65	178	1.66
0.3	90.30	0.66	114	1.89
0.4	90.27	0.68	119	2.17
0.5	90	0.68	58.6	2.60
0.6	89.70	0.68	121	2.93
0.7	88.79	0.65	122	3.44
0.8	87.04	0.59	122	4.02
0.9	81.01	0.31	100	3.57

2.1.3 Buck-Boost Converter

The conventional AC-DC Buck-Boost converter is shown in figure 2.3. The function of this converter is to step up and step down the input signal. The converter provides negative output voltage in its inverting topology. For duty ratio of 0.5 and higher, the circuit behaves as a step-up converter. For duty ratio of 0.4 and lower, the circuit behaves as a step-down converter.

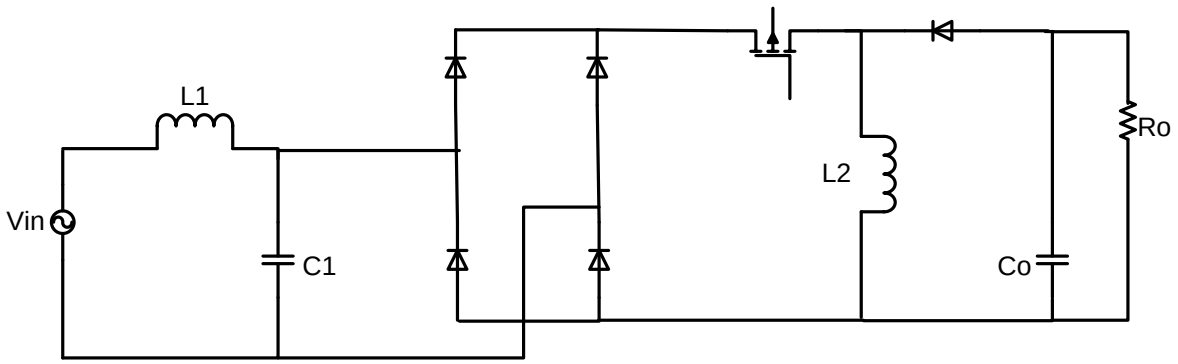


Figure 2.3 Conventional AC-DC Buck-Boost Converter with Input Filter

2.1.3.1 Open-loop data analysis

The simulation of the conventional Buck-Boost converter with an input filter has been performed using software simulation. The results obtained are presented in Table 2.6. Here MOSFET is acting as the switching device. The value of different circuit components is given in Table 2.5.

Table 2.5 Parameter Table for Conventional Buck-Boost Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mH
Inductor (L2)	1mH
Capacitance (C1)	1uF
Load across (Co)	220uF
Load Resistor (Ro)	100Ω

Table 2.6 Performance Analysis of Conventional Buck-Boost Converter under Duty Cycle Variation

Duty Cycle	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
0.1	96.601	0.847	6.595	0.22
0.2	98.206	0.969	7.317	0.45
0.3	98.509	0.976	6.921	0.708
0.4	98.617	0.981	10.933	1.006
0.5	98.642	0.953	29.656	1.49
0.6	98.629	0.961	25.751	1.98
0.7	98.565	0.953	24.266	2.59
0.8	98.358	0.898	20.724	3.59
0.9	97.507	0.627	6.103	4.74

2.1.4 Cûk Converter

The conventional AC-DC Cûk converter is shown in figure 2.4. Like the inverting topology of the Buck-Boost converter, this converter delivers an inverted output. Cûk converter has a capacitor as energy storage element, which is the main point of contrast with other converters.

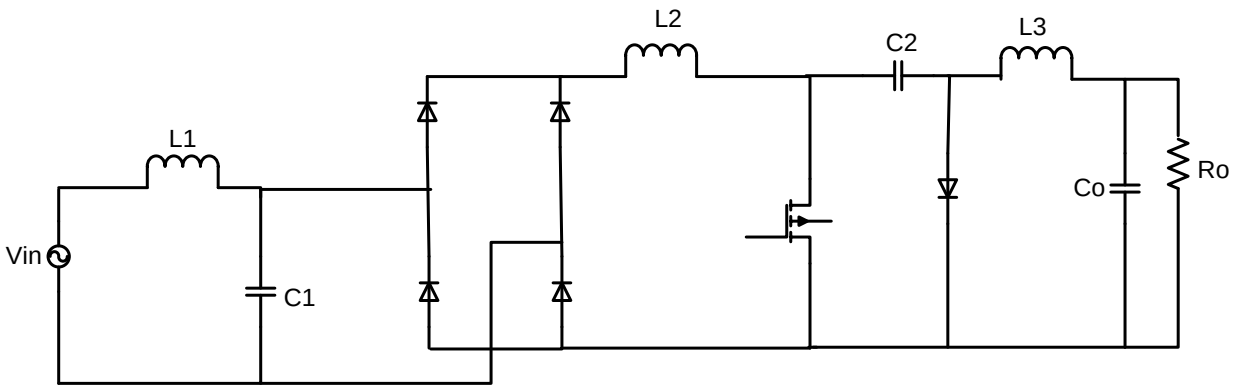


Figure 2.4: Conventional AC-DC Cûk converter with input filter

2.1.4.1 Open-loop data analysis

The simulation of the conventional Cûk converter with an input filter has been performed using software simulation. The results obtained are presented in Table 2.8. Here MOSFET is acting as the switching device. The value of different circuit components is given in Table 2.7

Table 2.7 Parameter Table for Conventional C*û*k Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mH
Inductor (L2)	1.5mH
Inductor (L3)	1.5mh
Capacitance (C1)	1uf
Capacitance (C2)	4.5uf
Load across (Co)	220uf
Load Resistor (Ro)	100Ω

Table 2.8 Performance Analysis of C*û*k Converter under Duty Cycle Variation

Duty Cycle	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
0.1	62.1	0.81	31.4	0.27
0.2	78.7	0.89	19.5	0.54
0.3	83	0.88	11.5	0.81
0.4	85	0.82	7.20	1.10
0.5	87.9	0.74	8.5	1.45
0.6	88.4	0.73	29.1	2.06
0.7	87.8	0.71	33.9	2.85
0.8	85.6	0.65	77.8	3.76
0.9	77.54	0.37	5.8	3.70

2.1.5 SEPIC Converter

The conventional AC-DC SEPIC converter is shown in figure 2.5. This converter produces output voltage, which can be higher, fewer, or equal to its input voltage. The switching device within the converter controls the output voltage of the converter.

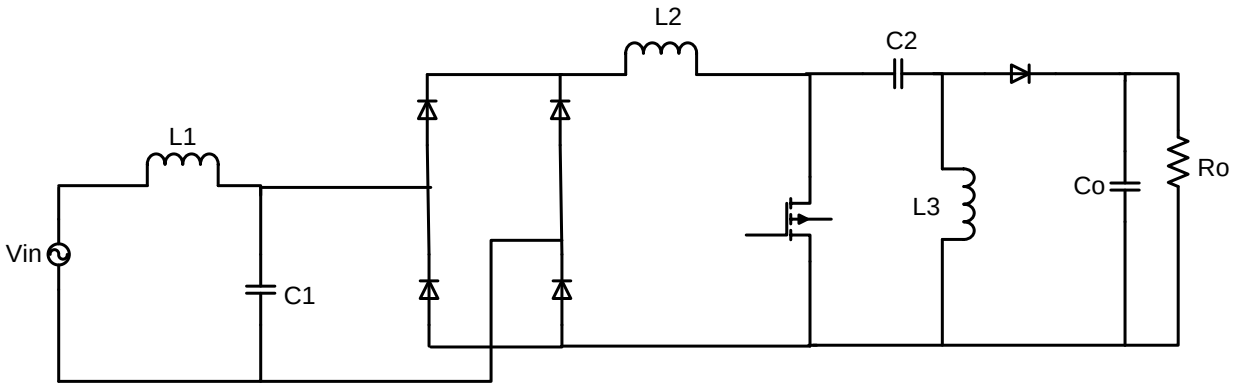


Figure 2.5: Conventional AC-DC SEPIC converter with input filter

2.1.5.1 Open-loop data analysis

The simulation of the conventional SEPIC converter with an input filter has been performed using software simulation. The results obtained are presented in Table 2.10. Here MOSFET is acting as the switching device. The value of different circuit components is given in Table 2.9

Table 2.9 Parameter Table for Conventional SEPIC Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mh
Inductor (L2)	1.5mh
Inductor (L3)	1.5mh
Capacitance (C1)	1uf
Capacitance (C2)	4.5uf
Load across (Co)	220uf
Load Resistor (Ro)	100Ω

Table 2.10 Performance Analysis of SEPIC Converter under Duty Cycle Variation

Duty Cycle	Efficiency (%)	Power Factor	THD (%)	Voltage Gain
0.1	63	0.82	31.5	0.27
0.2	79.6	0.91	20.1	0.54
0.3	83.9	0.90	11.8	0.81
0.4	86.1	0.84	7.09	1.09
0.5	88.2	0.75	7.4	1.44
0.6	88.7	0.73	28.6	2.04
0.7	88.09	0.72	33.7	2.85
0.8	85.94	0.66	23.9	3.77
0.9	77.96	0.37	5.7	3.71

Table 2.11 Voltage gain comparison of Conventional Converters

Name of the Converter	Voltage gain
Buck	D
Boost	$\frac{1}{(1-D)}$
Buck-Boost	$-\frac{D}{1-D}$
C$\hat{u}$k	$-\frac{D}{1-D}$
SEPIC	$\frac{D}{1-D}$

2.2 Recent Topologies of AC-DC Buck-Boost Converter

Throughout the decades, there have been modifications to improve different aspects of the conventional AC-DC Buck-Boost converter. Specific converter topologies have been developed to meet desired load characteristics. Some recent topologies of single-phase AC-DC Buck-Boost converter have been discussed from section 2.2.1 to 2.2.4. The open-loop performance analysis of the converters is also done. Voltage gain, overall efficiency, input power factor, and total harmonic distortion (THD) are analyzed with the variation of the duty cycle.

2.2.1 Input switched single phase Buck-Boost AC-DC Converter

The given converter in figure 2.6 is a Buck-Boost converter with enhanced power quality. There are three inductors and two capacitors in the circuit. As the input filter inductor L3 and capacitor C2 is used. The other two inductors operate as Buck-Boost inductors. The circuit has ten diodes. Capacitor C1 is the output capacitor and resistor R1 is used as load. IGBT is used as the switching device [56].

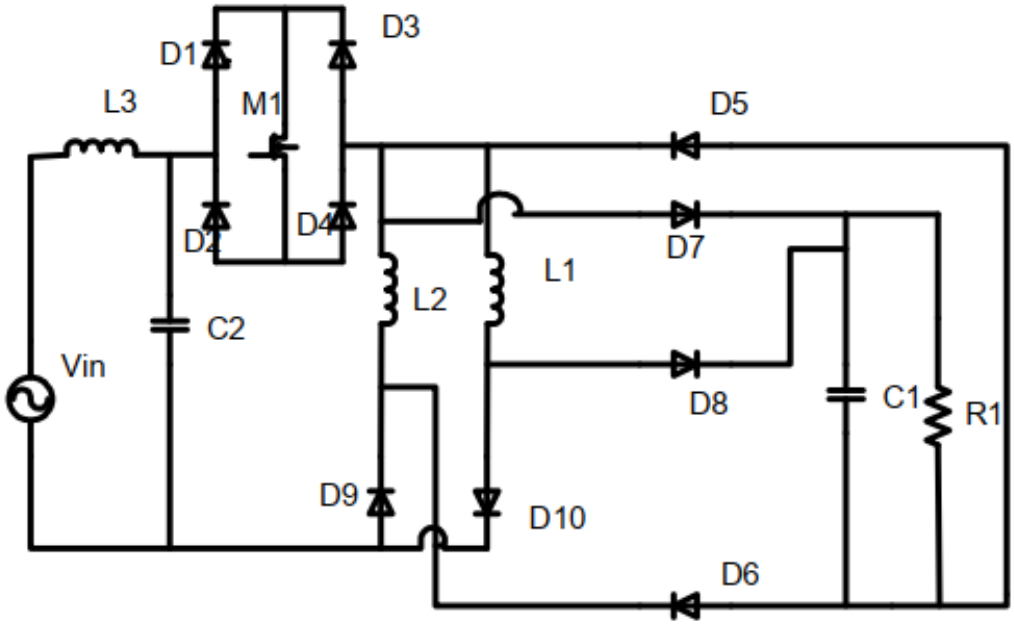


Figure 2.6: Input switched single -phase AC-DC Buck-Boost Converter

2.2.1.1 Open-loop data analysis

Table 2.12 Parameter Table for Input switched single-phase AC-DC Buck-Boost Converter [56]

Parameters	Value
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mH
Inductor (L2)	5mH
Inductor (L3)	5mH
Capacitance (C1)	2.5uF
Capacitance (C2)	5uF
Load Resistor (R1)	100Ω

In [56], the results are shown in graphical comparison diagram from where it is difficult to get the exact values of THD, power factor and efficiency. For this reason, using the circuit parameters mentioned in [56], the results are obtained using software simulation and given in table 2.13. From the information that can be gathered from [56], it is seen that the input current THD approximately varies from 0.35% to 3.3% over the variation of duty cycle. The power factor remains above 0.9 over the variation of duty cycle except for duty ratio of 0.9 where it is close to 0.5. For some duty ratio's like for duty ratio of 0.6 and 0.7 the power factor is close to unity. The circuit represents over 90% conversion efficiency for duty ratio of 0.4 to 0.9. The lowest efficiency is for duty ratio of 0.1 which is approximately 75% [56].

Table 2.13 Performance Analysis of Input switched single -phase AC-DC Buck-Boost Converter under duty cycle variation

Duty cycle	THD	Power factor	Voltage gain	Efficiency
0.1	3%	0.94	0.64	74%
0.2	2.7%	0.97	0.73	81.28%
0.3	3.15%	0.97	0.79	87.34%
0.4	3.28%	0.97	0.84	92.54%
0.5	2.7%	0.98	0.89	97.16%
0.6	2%	0.99	1.33	98.62%
0.7	1.7%	0.99	2.06	98.35%
0.8	1%	0.93	3.28	96.98%
0.9	0.4%	0.5	3.51	86.40%

From the above analysis, it is seen that the circuit achieves low input current THD throughout the variation of the duty cycle. The circuit has a high input power factor over the variation of duty cycle except for duty cycle 0.9. The circuit shows excellent conversion efficiency except for a very low duty cycle. From the data of voltage gain, it is seen that, the circuit can at best achieve 36% lower voltage than the input signal. The circuit can boost the voltage over three times than the input voltage.

2.2.2 High-efficiency single-phase switched capacitor AC to DC step up-down converter

The given converter in figure 2.7 is a Buck-Boost converter with improved efficiency. The circuit uses Buck-Boost topology in two stages. Stage one is a full-wave diode bridge rectifier. The second stage is a switched-capacitor DC-DC topology, which operates at a high frequency. The circuit has two inductors among which inductor L1 is used as the Buck-Boost inductor. There are four capacitors in the circuit. Inductor Lin along with capacitor Cin form the input filter. Capacitor C1 is the output capacitor and resistor R1 is used as load. The circuit has a switch and a total of eight diodes [57].

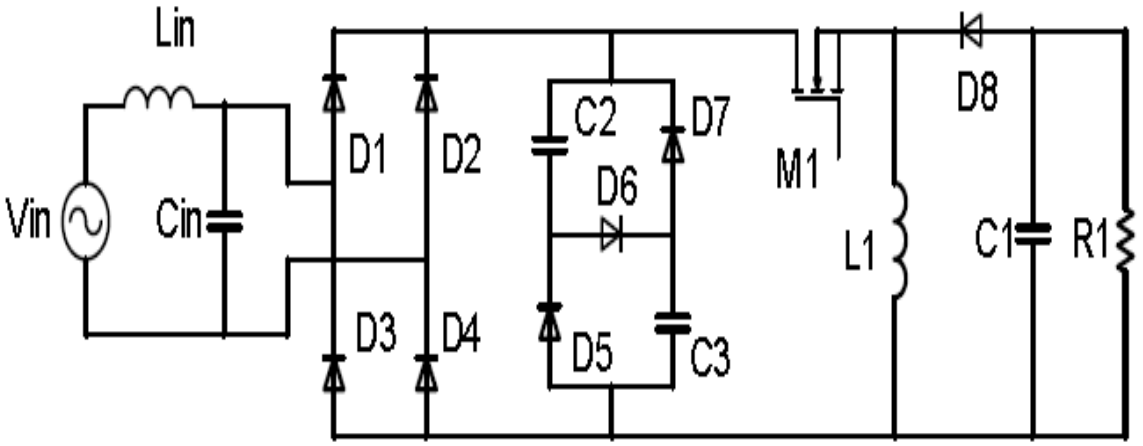


Figure 2.7: Single-phase AC-DC Buck-Boost converter in two-stage

2.2.2.1 Open-loop data analysis

Table 2.14 Parameter Table for high-efficiency single-phase switched capacitor AC to DC step up-down converter [57]

Parameters	Value
Input voltage (Vi) Peak	300 V
Switching Frequency (S)	10kHz
Inductor (Lin)	40mH
Inductor (L1)	400uH
Capacitance (Cin)	50uF
Capacitance (C1)	50uF
Capacitance (C2)	1uF
Capacitance (C3)	1uF
Load Resistor (R1)	100Ω

In [57], the results are shown in graphical comparison diagram from where it is difficult to get the exact values of THD, power factor and efficiency. For this reason, using the circuit parameters mentioned in [57], the results are obtained using software simulation and given in table 2.15. However, it is given that, THD (%) of the converter is considerably low but the input power factor is very low for some cases. It is also given that the overall conversion efficiency is reasonably high [57].

Table 2.15 Performance Analysis of Single phase AC-DC Buck-Boost converter in two-stage under duty cycle variation

Duty cycle	THD	Power factor	Voltage gain	Efficiency
0.1	23.3%	0.12	0.42	80%
0.2	0.8%	0.39	0.84	90.88%
0.3	0.25%	0.73	1.25	93.46%
0.4	0.20%	0.94	1.62	94.72%
0.5	0.14%	0.99	1.90	95.25%
0.6	0.27%	0.95	2.08	95.49%
0.7	4.5%	0.78	2.20	95.99%
0.8	3.18%	0.40	1.69	95.95%
0.9	24.2%	0.10	0.77	93.06%

From the analysis of the above data, it is seen that the circuit achieves very low input current THD throughout the variation of the duty cycle. Only for duty ratio of 0.1 and 0.9, THD is above the IEEE standards. The circuit has a high input power factor for mid duty ratio's but shows very poor input power factor for lower and higher duty ratios. The maximum boost voltage that the circuit can achieve is double the input voltage. The circuit attains fairly impressive conversion efficiency over the variation of duty cycle with a maximum efficiency of 95.99%.

2.2.3 Bridgeless AC-DC Buck-Boost converter with switched capacitor for low power applications

The given circuit in figure 2.8 is a Buck-Boost converter designed for low power applications. The circuit consists of three inductors, five capacitors, and twelve diodes. During T_{on}, (for the positive half cycle and negative half cycle) the Buck-Boost inductor L_0 and output capacitor C_0 are charged by the switched capacitors (C_1, C_2 for the positive half cycle and C_3, C_4 for negative half cycle) with half of the DC link voltage. During T_{off} (for the positive half cycle and negative half cycle) C_1, C_2 for the positive half cycle and C_3, C_4 for the negative half cycle are charged in series with the DC link voltage. Current in the Buck-Boost inductor L_0 continuing through the freewheeling diode D0 charges the output capacitor C_0 [58].

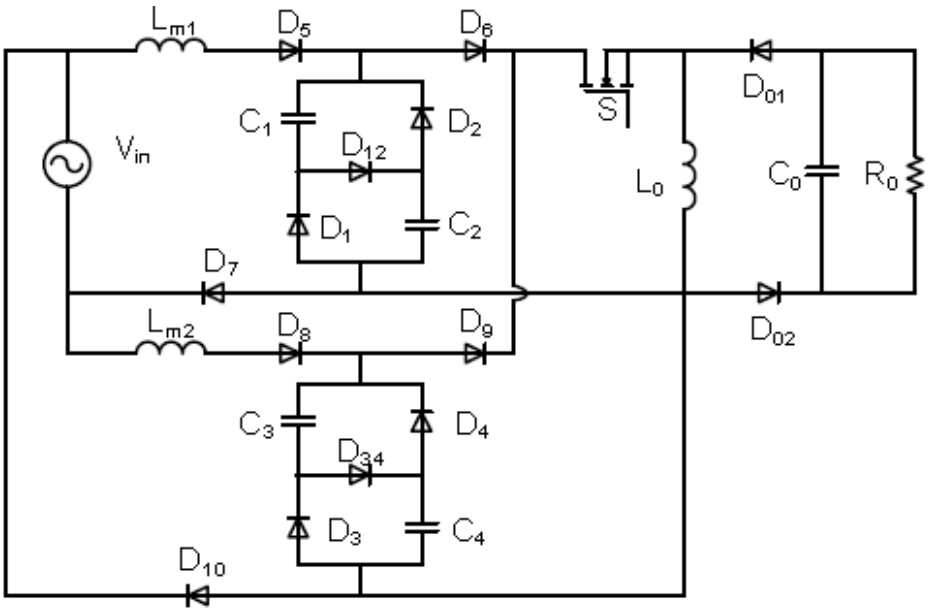


Figure 2.8: Bridgeless AC-DC Buck-Boost converter with switched capacitor

2.2.3.1 Open-loop data analysis

Table 2.16 Parameter Table for bridgeless AC-DC Buck-Boost converter with switched capacitor [58]

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L_{m1})	10mH
Inductor (L_{m2})	10mH
Inductor (L_0)	5mH
Capacitance (C_1)	1uF
Capacitance (C_2)	1uF
Capacitance (C_3)	1uF
Capacitance (C4)	1uF
Capacitance (C_0)	330uF
Load Resistor (R_0)	100Ω

The circuit is designed for very low power applications (like microprocessors). In results, it is shown that, the converter achieves better power factor and conversion efficiency than the conventional converter. In terms of THD (%) it is shown that, it represents lower THD than the conventional one [58]. However, from our analysis we find a different scenario. To achieve very low amount of power the converter has to sacrifice quality performance in terms of THD (%), power factor and conversion efficiency.

Table 2.17 Performance Analysis of bridgeless AC-DC Buck-Boost converter with switched capacitor under duty cycle variation

Duty cycle	THD	Power factor
0.1	224%	0.37
0.2	176%	0.43
0.3	155%	0.50
0.4	134%	0.57
0.5	115%	0.64
0.6	105%	0.68
0.7	102%	0.69
0.8	100%	0.70
0.9	100%	0.70

2.2.4 Modified single-phase PFC AC-DC Buck-Boost converter

The given circuit in figure 2.9 is a modified single-phase PFC AC-DC Buck-Boost converter. The circuit consists of two inductors, two capacitors, six diodes and two switches. During T_{on}, (for the positive half cycle and negative half cycle) the Buck-Boost inductor gets charged. During, T_{off} (for both the cycles), the inductor is discharged [29].

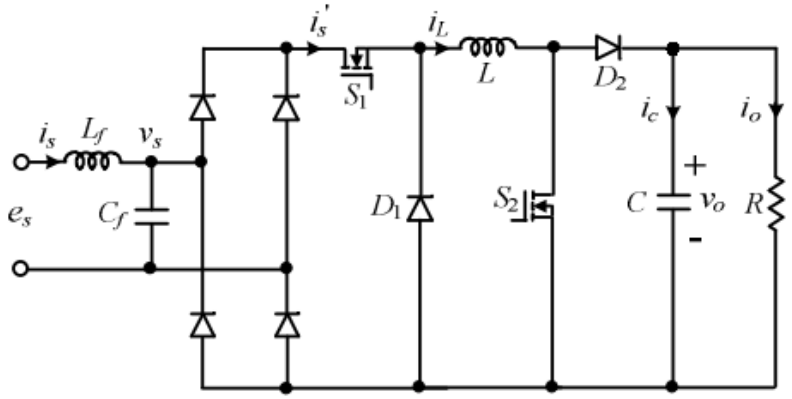


Figure 2.9: Modified single-phase PFC AC-DC Buck-Boost converter

2.2.4.1 Open-loop data analysis

Table 2.18 Parameter Table for modified single-phase PFC AC-DC Buck-Boost converter [29]

Parameters	**Value**
Input voltage (Vi) Peak	311V
Switching Frequency (S)	10kHz
Inductor (L_f)	2mH
Inductor (L)	162uH
Capacitance (C_f)	330nF
Capacitance (C)	680uF
Load Resistor (R)	100Ω

From [29], we didn't get the results in our desired form of open loop analysis. However, it is mentioned that, the circuit achieves quality power factor [29]. For our analysis, we took the parameter values from [29] and the results are obtained using software simulation for the performance analysis.

Table 2.19 Performance Analysis of modified single-phase PFC AC-DC Buck-Boost converter under duty cycle variation

Duty cycle	THD	Power factor	Voltage gain	Efficiency
0.1	85.5%	0.74	0.407	28.1%
0.2	86.3%	0.75	0.348	17.83%
0.3	82.04%	0.77	0.36	17.45%
0.4	69.74%	0.82	0.428	17.34%
0.5	53.98%	0.88	0.528	17.62%
0.6	38.25%	0.93	0.68	18.41%
0.7	24.34%	0.97	0.97	20.87%
0.8	13.82%	0.98	1.56	25.33%
0.9	9.83%	0.96	3.27	34.10%

From the above analysis, it is seen that the converter achieves low input current THD at high duty ratio. The input power factor also improves with the increase of duty ratio and is closer to unity above duty ratio of 0.6. The converter can step up the voltage three times of input voltage and can step down the input voltage about 60%. The most concerning factor is that the converter shows very poor efficiency both at low duty ratio and also at high duty ratio. Thus, the improvement of power factor and input current THD comes at the cost of very poor efficiency.

Chapter 3

Proposed Single-Phase Non-isolated AC-DC Buck-Boost Converter

3.1 Proposed AC-DC Buck-Boost Converter

Buck-Boost converter is a type of converter that can be regulated to provide an output voltage that is higher or lower than the input voltage. The proposed converter provides an output voltage that is in the same polarity of the input signal. There is no isolating instrument between the source and the load. There are three inductors (L1 to L3), three capacitors (C1 to C3), six diodes (D1 to D6) , and a switch M1. The inductor L1 and the capacitor C1 form the input filter. Inductors L2 and L3 act as Buck-Boost inductors. Capacitors C2 and C3 are used as output capacitors, and resistor R is used as a load.

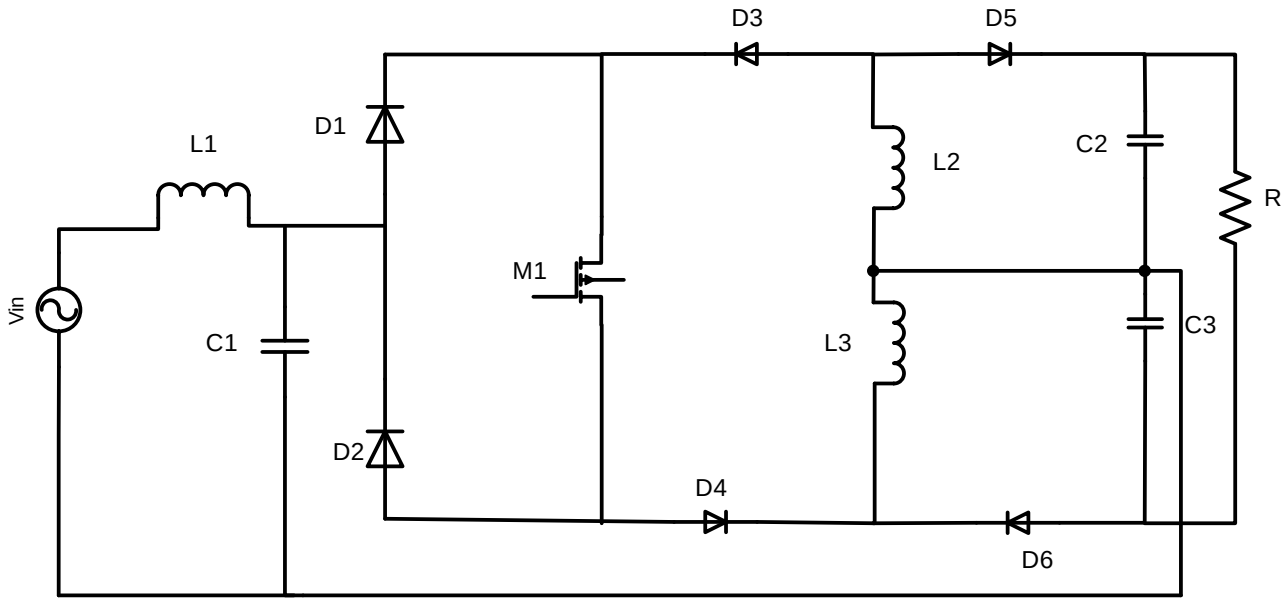
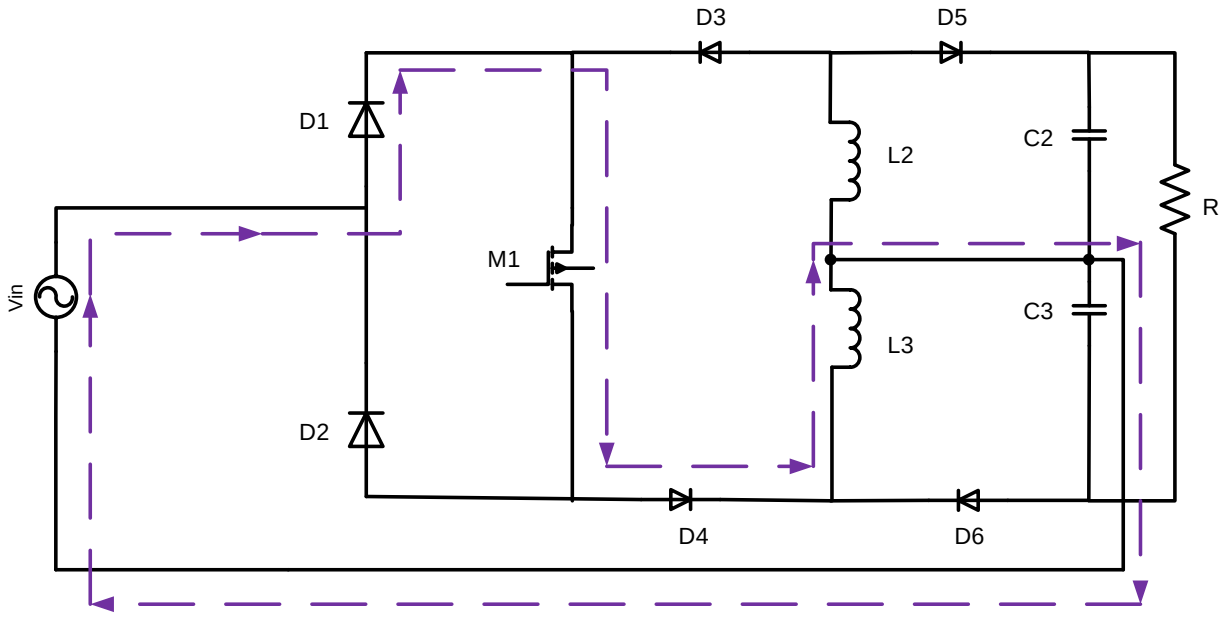


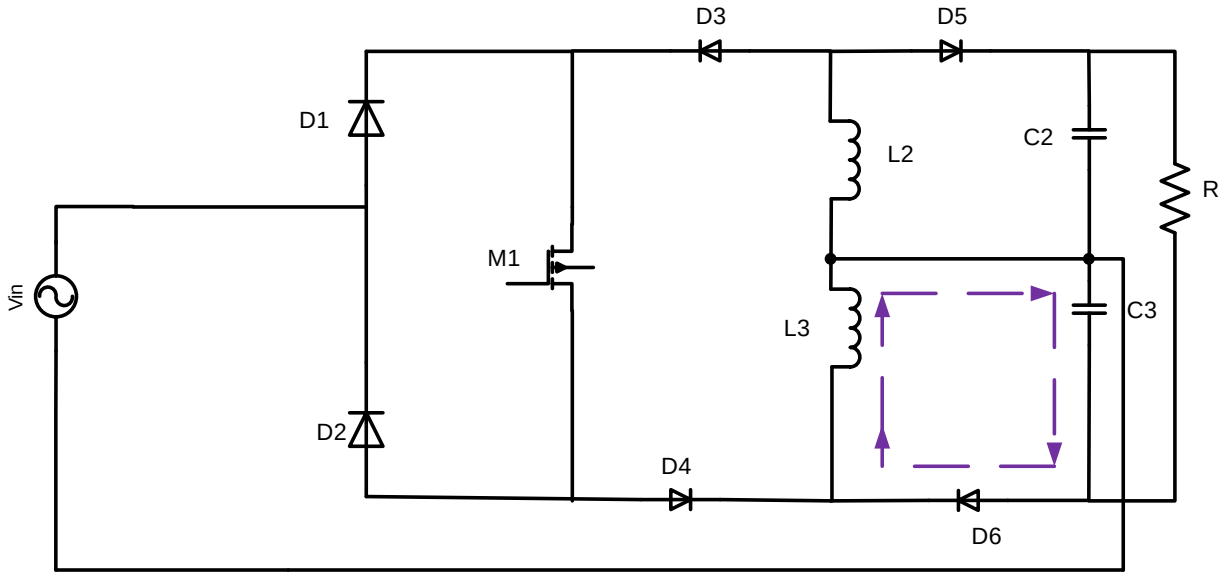
Figure 3.1: Proposed Single-Phase Non-isolated AC-DC Buck-Boost Converter

3.2 Principle of Operation

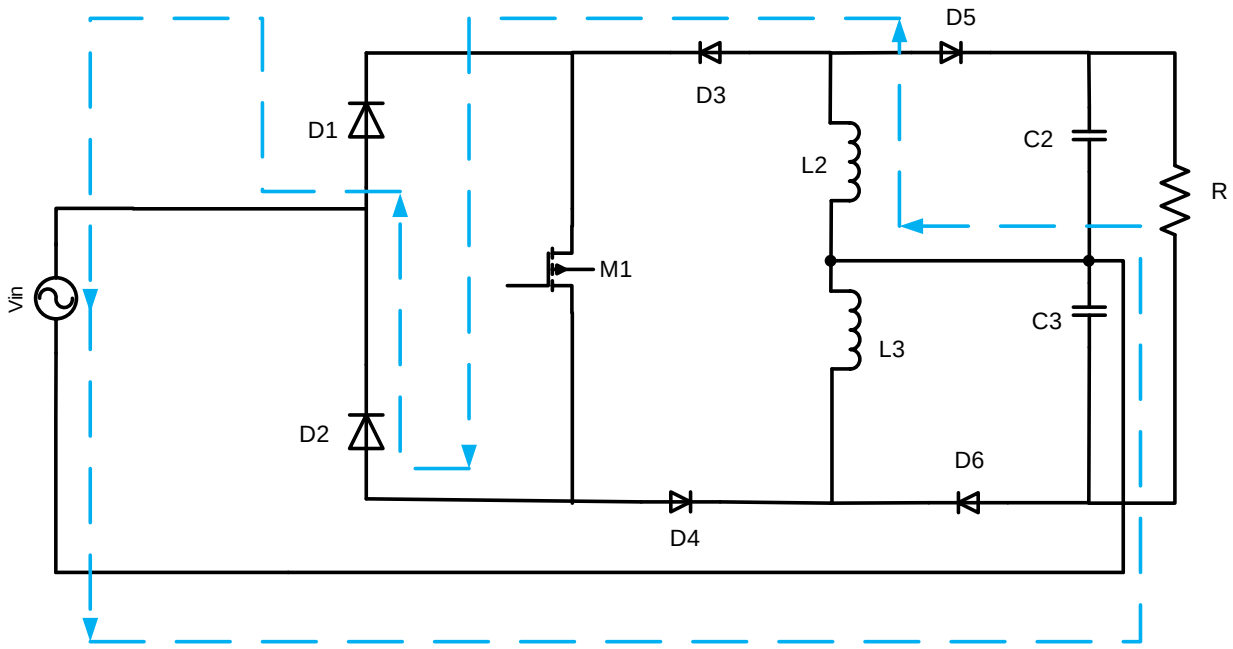
The four modes of operation of the proposed converter are provided in the following figure



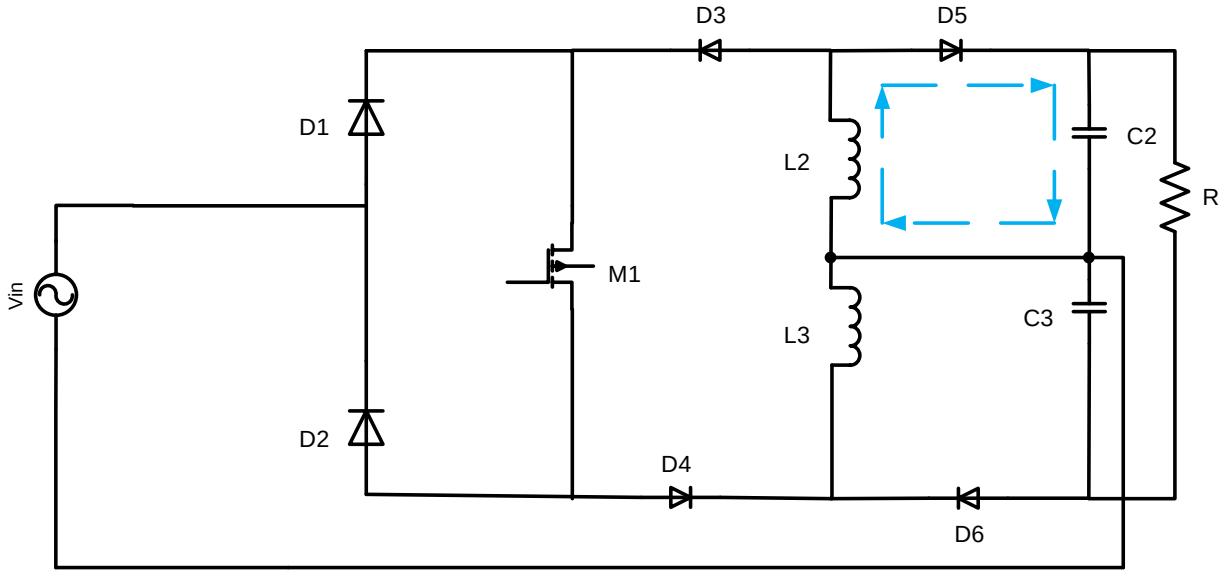
(a)



(b)



(c)



(d)

Figure 3.2 Four Modes of Operation of Proposed AC-DC Buck-Boost Converter (a) Mode 1:Proposed circuit in the positive half cycle when M1 is ON.(b) Mode 2:Proposed circuit in the positive half cycle when M1 is OFF.(c) Mode 3:Proposed circuit in the negative half cycle when M1 is ON.(d)Mode 4:Proposed circuit in the negative half cycle when M1 is OFF.

Mode 1: When the switch (M1) is ON during the positive half cycle of the input signal, inductor L3 charges from the source. Current flows through D1, M1, D4, and L3, as shown in fig 3.2(a). Diodes D2, D3, D5, and D6 remain off.

Mode 2: In the positive half cycle of the input signal, when the switch (M1) is OFF, the source is isolated from the rest of the circuit, as shown in fig 3.2(b). The inductor (L3) changes its polarity, and the inductor voltage forward biases the output diode (D6) and charges the output capacitor (C3).

Mode 3: When the switch (M1) is ON during the negative half cycle of the input signal inductor L2 charges from the source. Current flows through D2, M1, D3, and L2 as shown in fig 3.2(c). Diodes D1, D4, D5, and D6 remain off.

Mode 4: In the negative half cycle of the input signal, when the switch (M1) is OFF, the source is isolated from the rest of the circuit, as shown in fig 3.2(d).The inductor (L2) changes its polarity, and the inductor voltage forward biases the output diode (D5) and charges the output capacitor (C2).

3.3 Open-loop Data Analysis

Table 3.1 Parameter Table for Single-Phase Non-isolated AC-DC Buck-Boost Converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Inductor (L1)	5mH
Inductor (L2)	1mH
Inductor (L3)	1mH
Capacitance (C1)	1uF
Capacitance (C2)	110uF
Capacitance (C3)	110uF
Load Resistor (R)	100Ω

Table 3.2 Performance Analysis of Single-Phase Non-isolated AC-DC Buck-Boost Converter under duty cycle variation

Duty cycle	Efficiency (%)	Power factor	THD (%)	Voltage gain
0.1	97.587	0.712	40.295	0.238
0.2	99.061	0.767	57.147	0.548
0.3	99.288	0.748	61.188	0.854
0.4	99.276	0.812	50.792	1.35
0.5	99.158	0.901	37.724	2.08
0.6	99.045	0.967	25.646	3.009
0.7	98.719	0.969	15.753	4.147
0.8	98.025	0.823	7.332	5.322
0.9	95.292	0.342	1.535	4.02

Table 3.3 Performance Analysis of Single-Phase Non-isolated AC-DC Buck-Boost Converter under load variation (for duty ratio of 0.2)

Load(Ω)	Efficiency (%)	Power factor	THD (%)	Voltage gain
50	94.61	0.77	54.63	0.36
70	94.44	0.76	59.95	0.42
90	94.30	0.76	59.06	0.47
110	94.16	0.79	53	0.51
130	94.26	0.79	57.04	0.57
150	94.26	0.83	50.62	0.61

Table 3.4 Performance Analysis of Single-Phase Non-isolated AC-DC Buck-Boost Converter under load variation (for duty ratio of 0.6)

Load(Ω)	Efficiency (%)	Power factor	THD (%)	Voltage gain
50	99.21	0.97	23.78	2.10
70	99.08	0.97	23.94	2.56
90	99.98	0.96	25.23	2.86
110	99.01	0.96	26.78	3.12
130	98.97	0.96	28.14	3.37
150	99.05	0.95	30.04	3.59

Table 3.5 Performance Analysis of Single-Phase Non-isolated AC-DC Buck-Boost Converter under frequency variation (for duty ratio of 0.2)

Frequency(kHz)	Efficiency (%)	Power factor	THD (%)	Voltage gain
10k	99.15	0.76	56.49	0.509
20k	98.84	0.63	68.74	0.43
30k	98.35	0.58	70.32	0.41
40k	98.01	0.56	71.95	0.40
50k	97.69	0.55	70.28	0.39
60k	97.09	0.55	71.65	0.38
70k	96.50	0.54	71.42	0.38
80k	96.45	0.53	71.34	0.38
90k	96.42	0.53	73.33	0.38
100k	96.54	0.52	73.95	0.37

Table 3.6 Performance Analysis of Single-Phase Non-isolated AC-DC Buck-Boost Converter under frequency variation (for duty ratio of 0.6)

Frequency(kHz)	Efficiency (%)	Power factor	THD (%)	Voltage gain
10k	98.71	0.96	25.64	3.00
20k	97.99	0.88	41.27	3.15
30k	97.71	0.86	44.36	3.16
40k	97.42	0.85	45.30	3.15
50k	96.94	0.85	45.64	3.13
60k	96.91	0.84	46.05	3.13
70k	96.72	0.84	46.15	3.12
80k	96.49	0.84	46.17	3.10
90k	96.18	0.84	46.24	3.10
100k	95.35	0.84	46.20	3.08

3.4 Ideal Voltage Gain Equation

The given circuit in Figure 3.3 is the proposed Buck-Boost converter where the output voltage V_0, voltage across the inductor (L3) V_{L3} and the voltage across the output capacitor (C3) V_{C3} is shown.

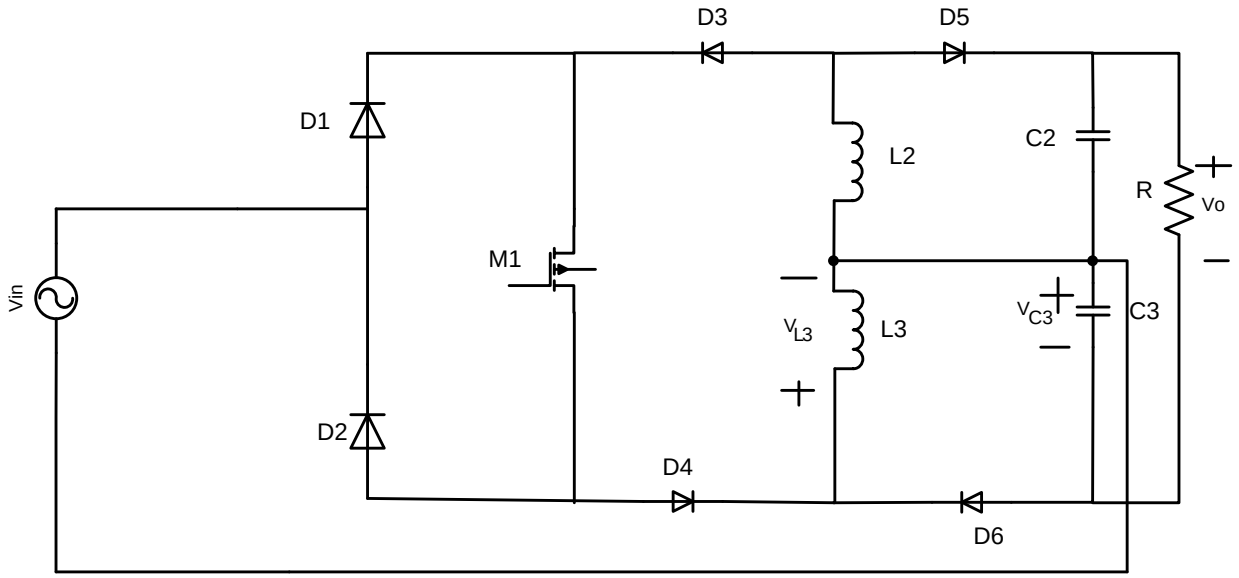


Figure 3.3: Proposed Buck-Boost Converter with output voltage, the voltage across the inductor and output capacitor

From figure 3.3

When the switch is on,

$$v_{L3} = v_{in}$$

When the switch is off,

$$-v_{L3} = v_{C3} = \frac{1}{2} v_0$$

Or, $v_{L3} = -v_{C3} = -\frac{1}{2} v_0$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-sec balance for one switching cycle is therefore

$$\int_{ti}^{t_i+T_{sw}} v_{L3}\ dt\ = \int_{t_i}^{t_i+DT_{sw}} v_{in}\, dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -\frac{1}{2} v_0\, dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period

$$\sum_{n=1}^{N} \int_{ti}^{t_i+T_{sw}} v_{L3}\, dt = \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} v_{in}\, dt + \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} -\frac{1}{2} v_0\ dt \ldots\ldots\ldots (3.1)$$

$$v_{in} = V_{in\,max} \sin(\omega t - \theta_{in})$$
$$v_0 = V_{0\,max} \sin(\omega t - \theta_0)$$

From equation 4.1,

$$\sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} V_{in\,max} \sin(\omega t - \theta_{in}) dt$$
$$= \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} \frac{1}{2}\ V_{0\,max} \sin(\omega t - \theta_0)\ dt$$

$$\Rightarrow \sum_{n=1}^{N} \int_{t_i}^{t_i+DT_{sw}} 2\, V_{in\,max} \sin(\omega t - \theta_{in}) dt$$
$$= \sum_{n=1}^{N} \int_{t_i+DT_{sw}}^{t_i+T_{sw}} V_{0\,max} \sin(\omega t - \theta_0)\ dt$$

$$\Rightarrow \sum_{n=1}^{N} [-2\ \frac{V_{in\,max}}{\omega} \cos(\omega t - \theta_{in})]_{t_i}^{t_i+DT_{sw}}$$
$$= \sum_{n=1}^{N} [\ -\frac{V_{0\,max}}{\omega} \cos(\omega t - \theta_0)]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\Rightarrow \sum_{n=1}^{N} 2\,V_{in\,max}[\cos(\omega t_i + \omega D T_{sw} - \theta_{in}) - \cos(\omega t_i - \theta_{in})]$$

$$= \sum_{n=1}^{N} V_{0\,max}\,[\cos(\omega t_i + \omega T_{sw} - \theta_0) - \cos(\,\omega t_i + \omega D T_{sw} - \theta_0)]$$

$$\Rightarrow \sum_{n=1}^{N} 2 \times 2\,V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right) \sin(-\,\frac{\omega D T_{sw}}{2})$$

$$= \sum_{n=1}^{N} 2V_{0\,max} \sin(\frac{\omega T_{sw} + \omega D T_{sw}}{2} + \omega t_i - \theta_0) \sin(\frac{\omega D T_{sw} - \omega T_{sw}}{2})$$

$$\Rightarrow \sum_{n=1}^{N} 2\,V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right) \sin(\,\frac{\omega D T_{sw}}{2})$$

$$= \sum_{n=1}^{N} V_{0\,max} \sin(\frac{\omega T_{sw} + \omega D T_{sw}}{2} + \omega t_i - \theta_0) \sin\frac{\omega T_{sw}(1-D)}{2}$$

$$\Rightarrow \sum_{n=1}^{N} V_{0\,max} \sin(\frac{\omega T_{sw}(1+D)}{2} + \omega t_i - \theta_0)$$

$$= \frac{\sin(\,\frac{\omega D T_{sw}}{2})}{\sin\frac{\omega T_{sw}(1-D)}{2}} \times \sum_{n=1}^{N} 2\,V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right)$$

$$\Rightarrow \sum_{n=1}^{N} V_{0\,max} \sin(\frac{\omega T_{sw}(1+D)}{2} + \omega t_i - \theta_0)$$

$$= \frac{\frac{\sin(\frac{\omega D T_{sw}}{2})}{\frac{\omega D T_{sw}}{2}} \times D}{\frac{\sin\frac{\omega T_{sw}(1-D)}{2}}{\frac{\omega T_{sw}(1-D)}{2}} \times (1-D)} \times \sum_{n=1}^{N} 2\, V_{in\,max} \sin\left(\omega t_i - \theta_{in} + \frac{\omega D T_{sw}}{2}\right)$$

Using identities,

$i) \lim_{\theta \to 0} \frac{sin\theta}{\theta} = 1$ and

$ii) \frac{\omega D T_{sw}}{2} \to 0\ as\ T_{sw} \to 0$

$iii)\ \frac{\omega T_{sw}(1+D)}{2} \to 0\ as\ T_{sw} \to 0$

$$\Rightarrow \sum_{n=1}^{N} V_{0\,max} \sin(\ \omega t_i - \theta_0) = \frac{D}{1-D} \times \sum_{n=1}^{N} 2\, V_{in\,max} \sin(\omega t_i - \theta_{in})$$

$$\Rightarrow \sum_{n=1}^{N} V_{0\,max} \sin(\ \omega t_i - \theta_0) = \frac{2D}{1-D} \times \sum_{n=1}^{N} V_{in\,max} \sin(\omega t_i - \theta_{in})$$

Thus, the average voltage can be found as

$$V_{0avg} = \frac{1}{\pi} \int_0^{\pi} V_{0\,max}\ sin\theta d\theta$$

$$= \frac{1}{\pi} \int_0^{\pi} V_{in\,max} \times \frac{2D}{1-D}\ sin\theta d\theta$$

$$= \frac{V_{in\,max}}{\pi} \times \frac{2D}{1-D} \int_0^{\pi} sin\theta d\theta$$

$$= \frac{V_{in\,max}}{\pi} \times \frac{2D}{1-D}\ [-cos\theta]_0^{\pi}$$

$$= \frac{2V_{in\,max}}{\pi} \times \frac{2D}{1-D}$$

$$= \frac{2D}{1-D} \times \frac{2V_{in\,max}}{\pi}$$

Table 3.7 Comparison between theoretical and simulation results of the proposed Buck-Boost converter

Duty Cycle	V_{0avg}(Theoretical)	V_{0avg}(Simulation)
0.1	43V	51V
0.2	96V	107V
0.3	164V	181V
0.4	255V	288V
0.5	382V	441V
0.6	573V	637V
0.7	892V	879V
0.8	1528V	1128V
0.9	3438V	852V

From the comparison, it is seen that there are some differences between the theoretical and simulation results for high order of duty cycles. The reason is that, it is expected to have some deviations between the theoretical and simulation results for extremely high and low duty ratio's.

3.5 Simulation results of the Proposed Single-Phase Non-isolated AC-DC Buck-Boost Converter under duty cycle variation

Performance analysis of proposed single-phase non-isolated AC-DC Buck-Boost Converter under duty cycle variation was presented in table 3.2. In this section, simulation results for three specific duty ratios are provided. For these duty cycles the figures of input current waveform, input voltage waveform and output voltage waveform are provided.

For Duty Cycle 0.1:

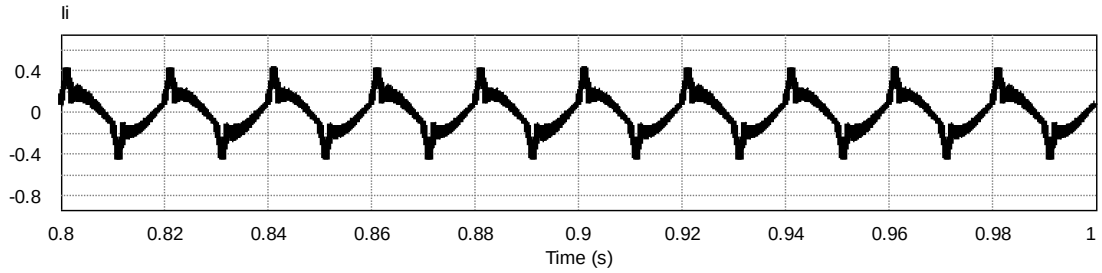


Figure 3.4 (a): Input Current waveform of the proposed Buck-Boost converter

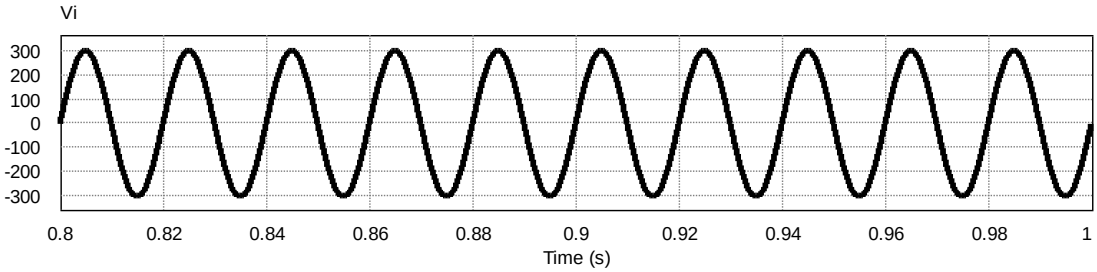


Figure 3.4 (b): Input Voltage waveform of the proposed Buck-Boost converter

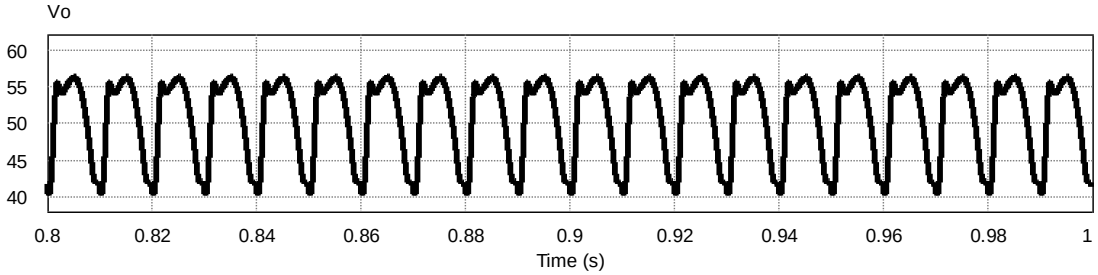


Figure 3.4(c): Output Voltage waveform of the proposed Buck-Boost converter

For Duty Cycle 0.6:

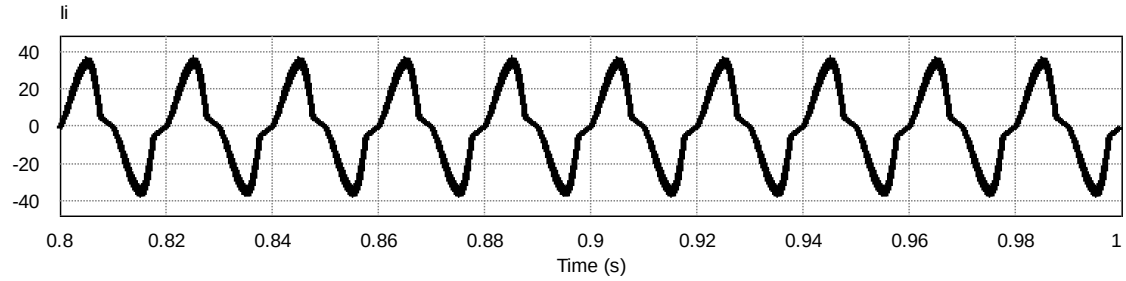


Figure 3.5 (a): Input Current waveform of the proposed Buck-Boost converter

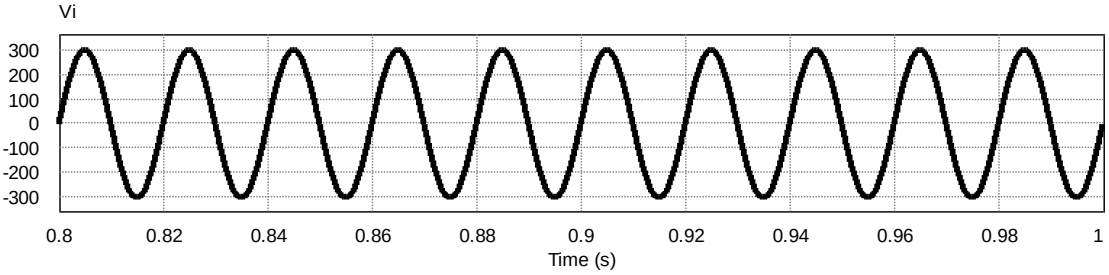


Figure 3.5 (b): Input Voltage waveform of the proposed Buck-Boost converter

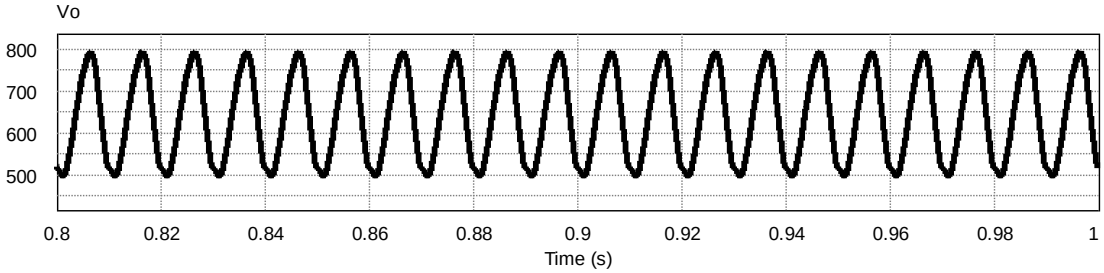


Figure 3.5(c): Output Voltage waveform of the proposed Buck-Boost converter

For Duty Cycle 0.9:

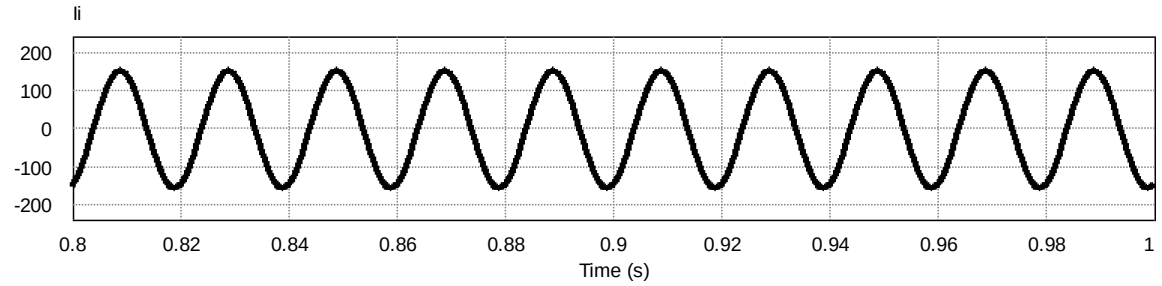


Figure 3.6(a): Input Current waveform of the proposed Buck-Boost converter

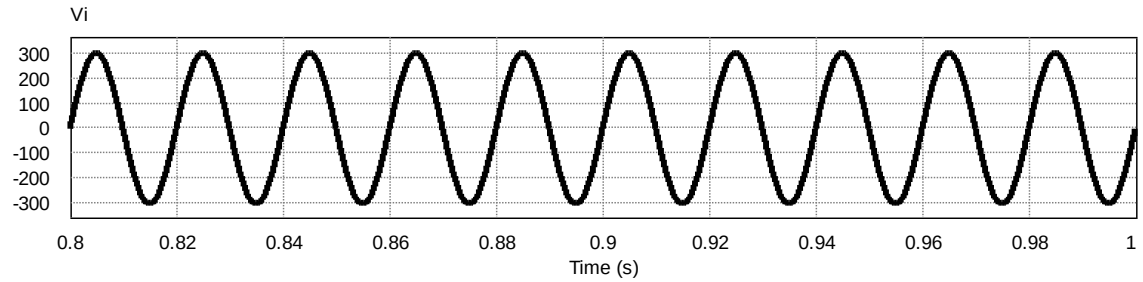


Figure 3.6(b): Input Voltage waveform of the proposed Buck-Boost converter

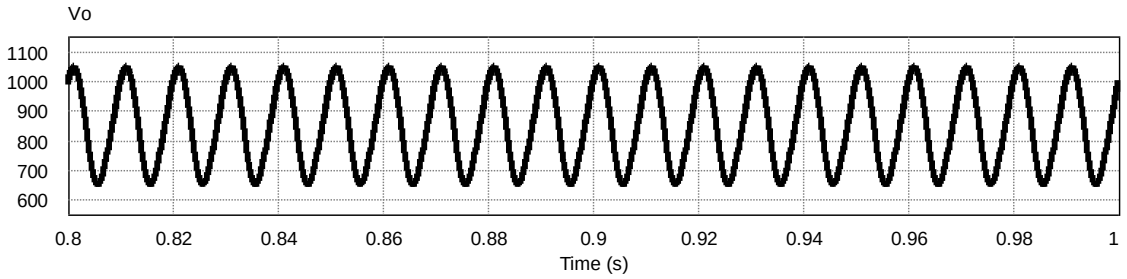


Figure 3.6(c): Output Voltage waveform of the proposed Buck-Boost converter

From figures 3.4(b),3.5(b) and 3.6(b) it is seen that, the input voltage of the proposed converter is a sinusoidal voltage with a peak value of 300 V. The peak to peak value is 600 V. From figure 3.4(a), we see the input current varies from 0.4 A to -0.4 A for duty cycle of 0.1. For the other two duty ratio's as seen from figure 3.5(a) and 3.6(a), it is observed that the input current varies from 40 A to -40 A and from 150A to -150 A respectively. The output voltage waveforms for duty

ratio of 0.1,0.6 and 0.9 are provided in figure 3.4(c),3.5(c) and 3.6(c) respectively. The average value of output voltages for these duty ratios are 50 V,640V and 852 V respectively.

3.6 Simulation results of Proposed Single-Phase Non-isolated AC-DC Buck Boost Converter under Load variation (for duty ratio of 0.2)

Performance analysis of proposed single-phase non-isolated AC-DC Buck-Boost converter under load variation (for duty ratio of 0.2) was given in table 3.3. In this section, the simulation results are provided for load of 50Ω and 110Ω (for duty ratio of 0.2). For these loads the figures of input current waveform, input voltage waveform and output voltage waveform are provided.

For load of 50Ω:

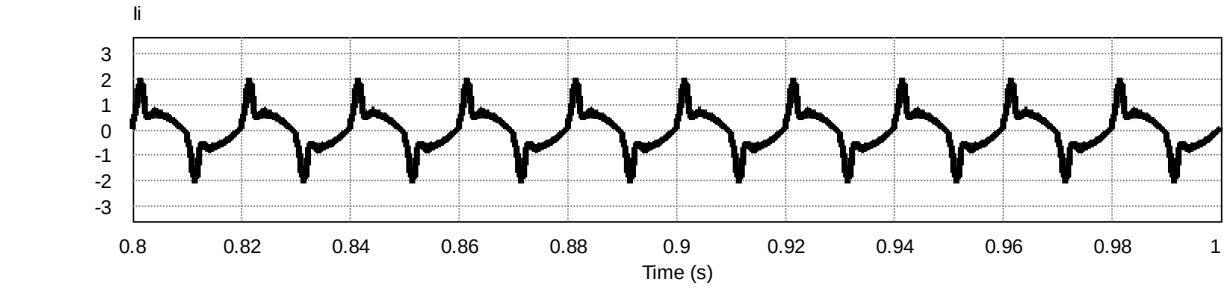


Figure 3.7(a): Input Current waveform of the proposed Buck-Boost converter

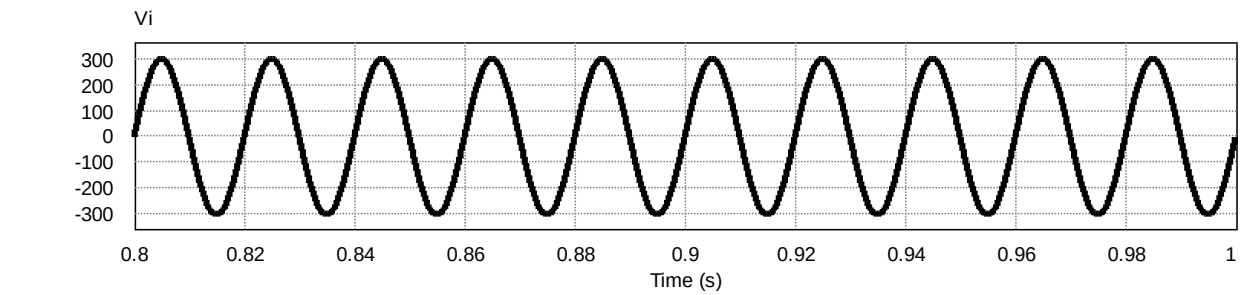


Figure 3.7(b): Input Voltage waveform of the proposed Buck-Boost converter

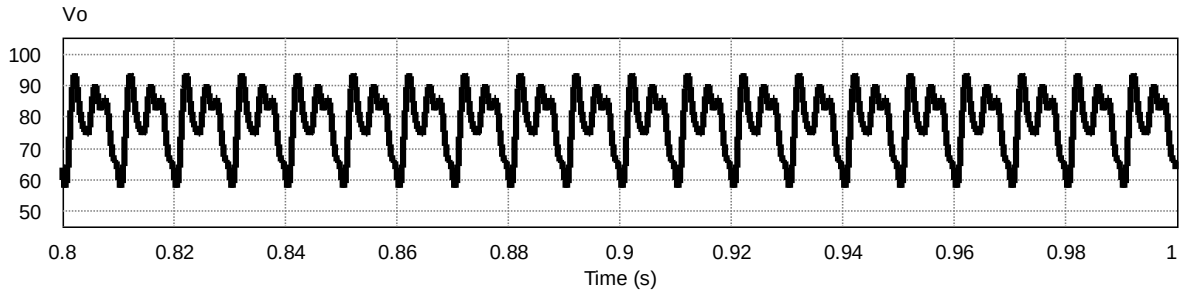


Figure 3.7(c): Output Voltage waveform of the proposed Buck-Boost converter

For load of 110Ω:

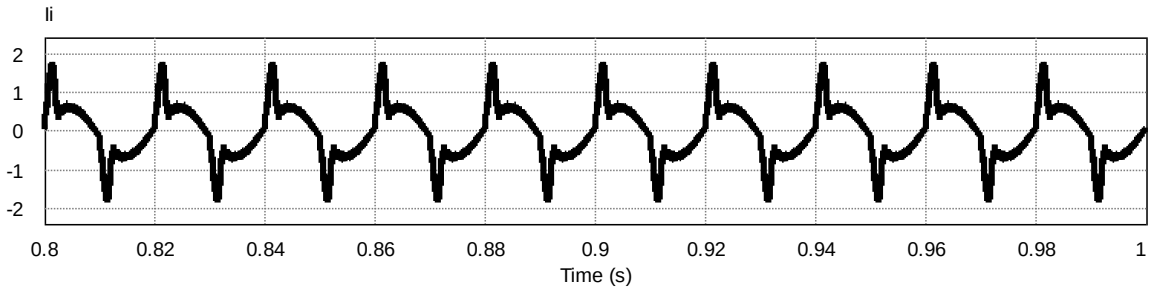


Figure 3.8(a): Input Current waveform of the proposed Buck-Boost converter

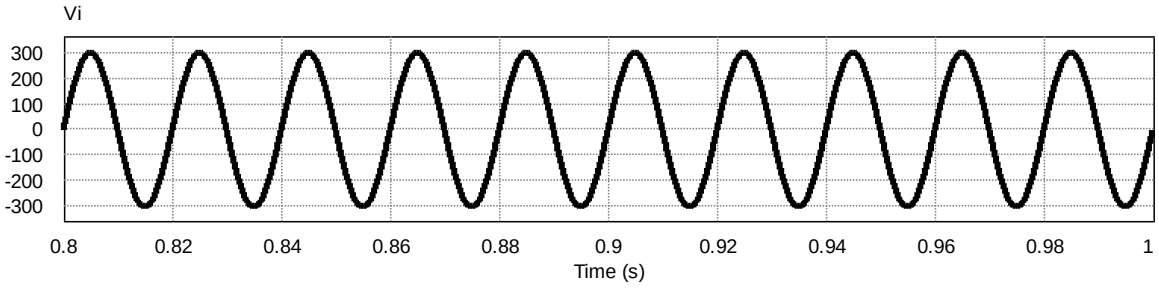


Figure 3.8(b): Input Voltage waveform of the proposed Buck-Boost converter

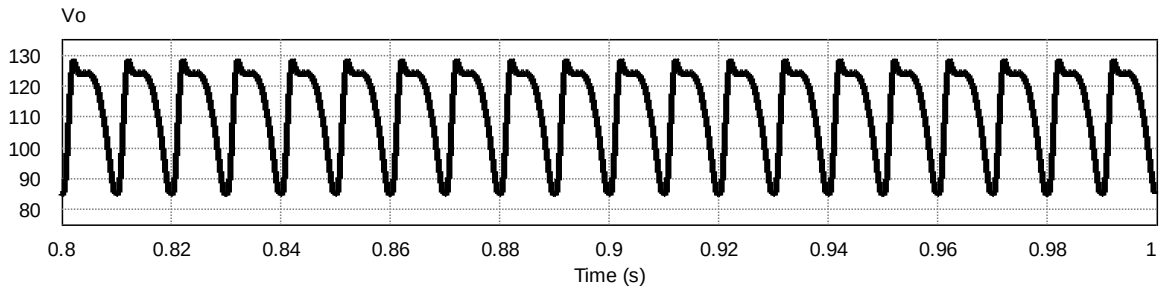


Figure 3.8(c): Output Voltage waveform of the proposed Buck-Boost converter

From figures 3.7(b) and 3.8(b) it is seen that, the input voltage of the proposed converter is a sinusoidal voltage with a peak value of 300 V. The peak to peak value is 600 V. From figure 3.7(a) and 3.8(a), we see the input current varies from 2 A to -2 A for load of 50Ω and 110Ω (under duty ratio of 0.2). The output voltage waveforms for these two loads (under duty ratio of 0.2) are provided in figure 3.7(c) and 3.8(c). The average value of output voltages for these loads are 78 V and 111 V respectively.

3.7 Simulation results of Proposed Single-Phase Non-isolated AC-DC Buck Boost Converter under Load variation (for duty ratio of 0.6)

Performance analysis of proposed single-phase non-isolated AC-DC Buck-Boost converter under load variation (for duty ratio of 0.6) was given in table 3.4. In this section, the simulation results are provided for load of 50Ω,90Ω and 110Ω (for duty ratio of 0.6). For these loads the figures of input current waveform, input voltage waveform and output voltage waveform are provided.

For load of 50Ω:

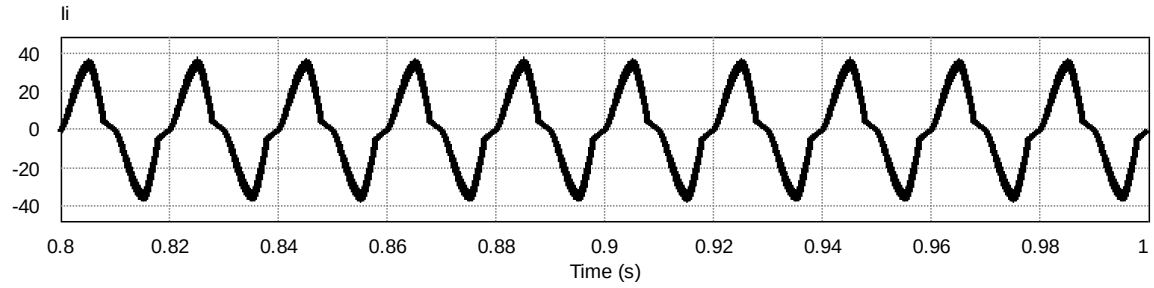


Figure 3.9(a): Input Current waveform of the proposed Buck-Boost converter

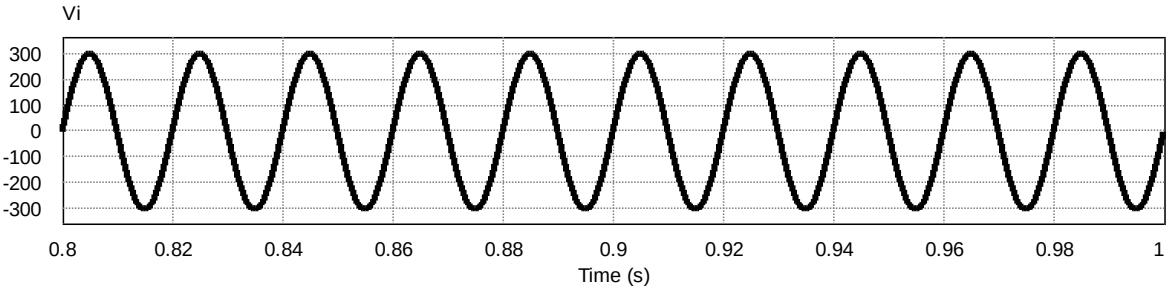


Figure 3.9(b): Input Voltage waveform of the proposed Buck-Boost converter

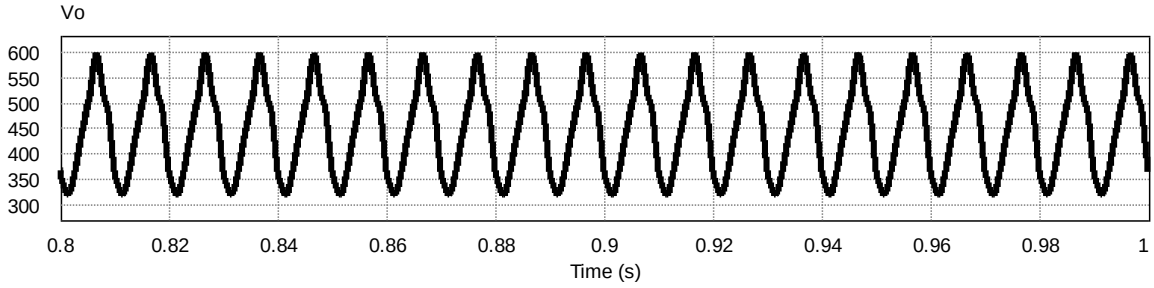


Figure 3.9(c): Output Voltage waveform of the proposed Buck-Boost converter

For load of 90Ω:

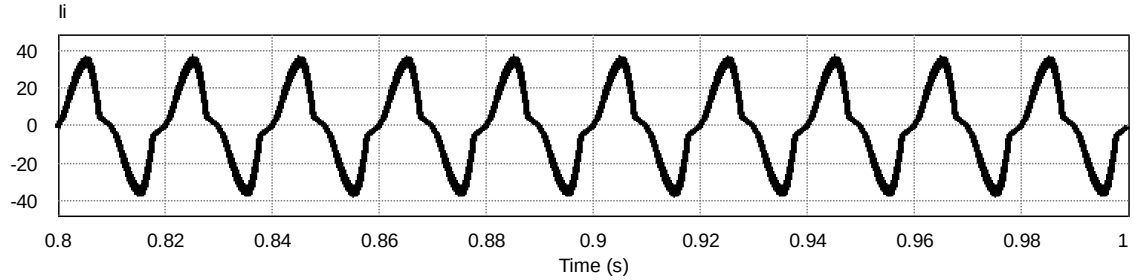


Figure 3.10 (a): Input Current waveform of the proposed Buck-Boost converter

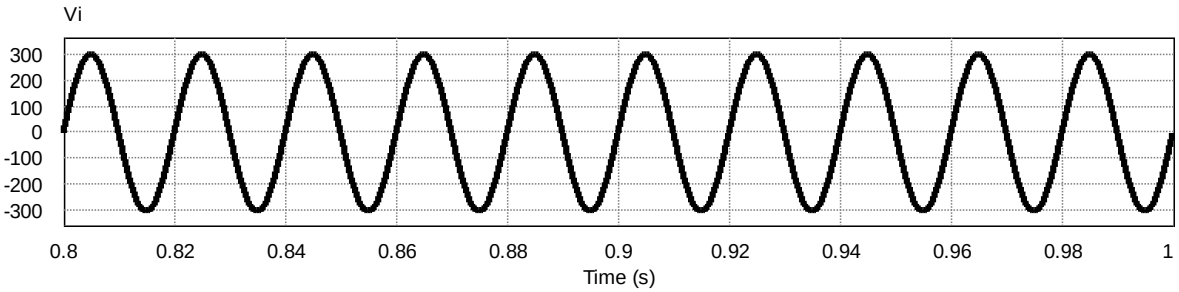


Figure 3.10(b): Input Voltage waveform of the proposed Buck-Boost converter

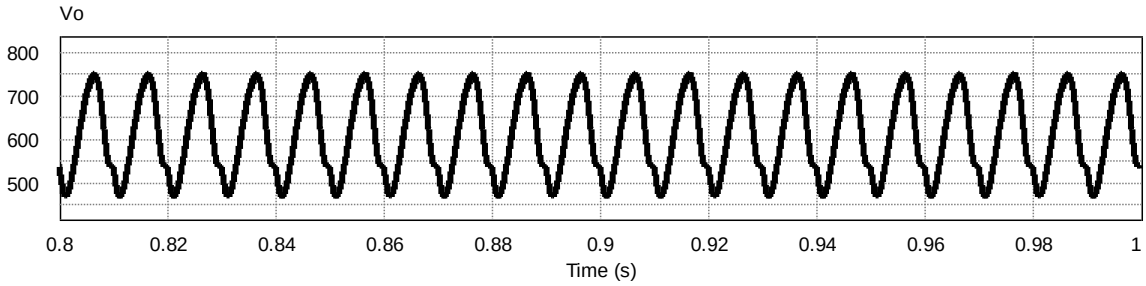


Figure 3.10(c): Output Voltage waveform of the proposed Buck-Boost converter

For load of 110Ω:

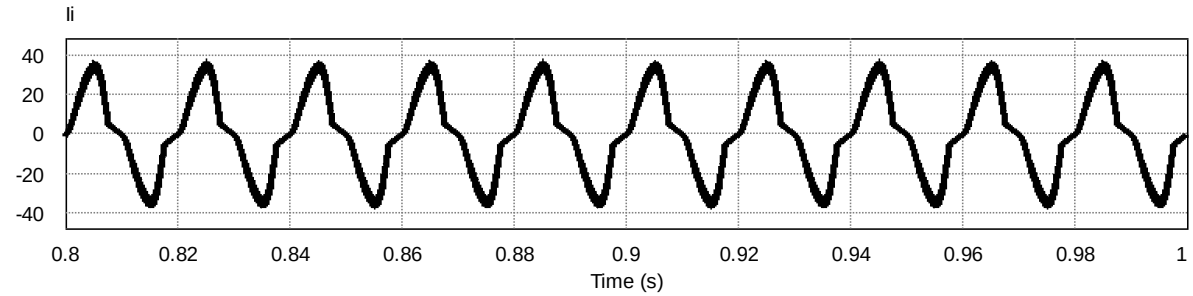


Figure 3.11(a): Input Current waveform of the proposed Buck-Boost converter

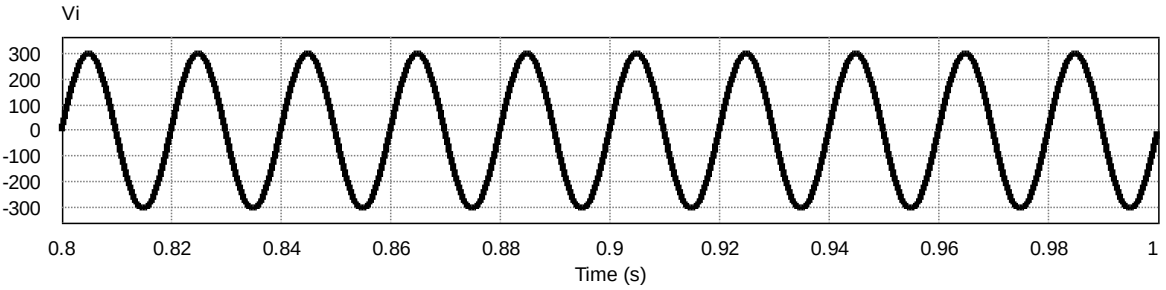


Figure 3.11(b): Input Voltage waveform of the proposed Buck-Boost converter

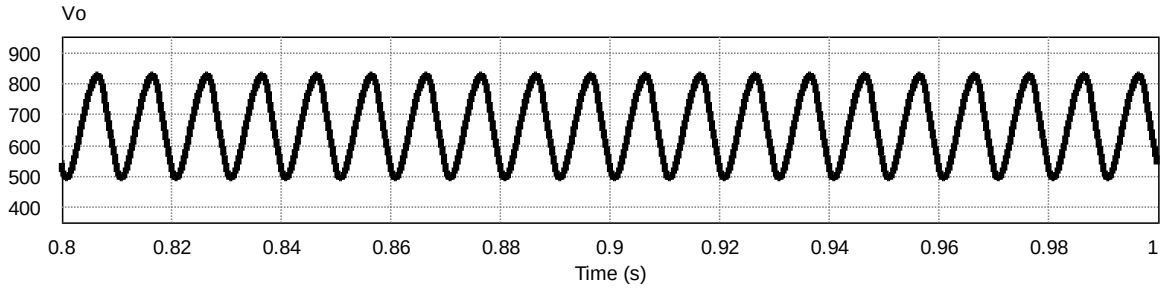


Figure 3.11(c): Output Voltage waveform of the proposed Buck-Boost converter

From figures 3.9(b),3.10(b) and 3.11(b) it is seen that, the input voltage of the proposed converter is a sinusoidal voltage with a peak value of 300 V. The peak to peak value is 600 V. From figure 3.9(a),3.10(a) and 3.11(a), we see the input current varies from 40 A to -40 A for load of 50Ω,90Ω and 110Ω (under duty ratio of 0.6). The output voltage waveforms for these loads (under duty ratio of 0.6) are provided in figure 3.9(c),3.10(c) and 3.11(c). The average value of output voltages for these loads are 448 V,608 V and 663 V respectively.

3.8 Simulation results of Proposed Single-Phase Non-isolated AC-DC Buck Boost Converter under frequency variation (for duty ratio of 0.2)

Performance analysis of proposed single-phase non-isolated AC-DC Buck-Boost converter under frequency variation (for duty ratio of 0.2) was given in table 3.5. In this section, the simulation results are provided for switching frequency of 30 kHz and 80 kHz (for duty ratio of 0.2). For these frequencies the figures of input current waveform, input voltage waveform and output voltage waveform are provided.

For frequency of 30 kHz:

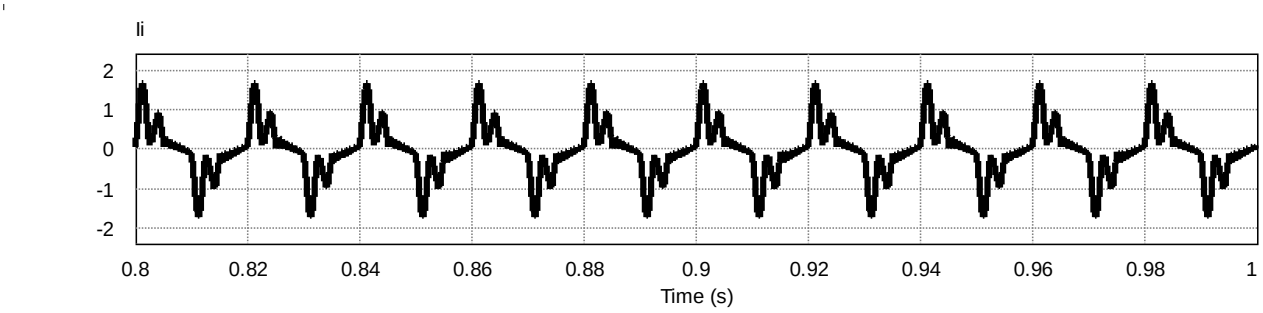


Figure 3.12(a): Input Current waveform of the proposed Buck-Boost converter

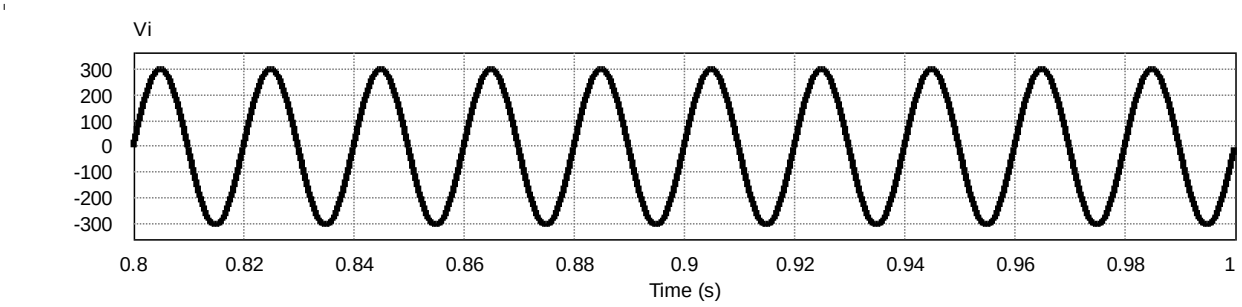


Figure 3.12(b): Input Voltage waveform of the proposed Buck-Boost converter

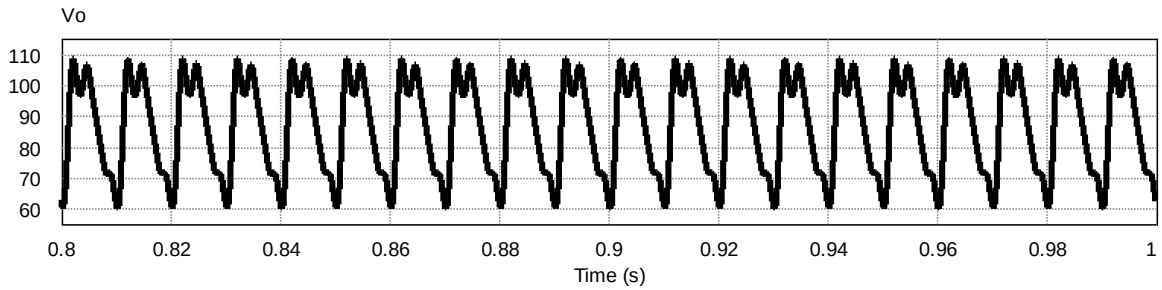


Figure 3.12(c): Output Voltage waveform of the proposed Buck-Boost converter

For frequency of 80 kHz:

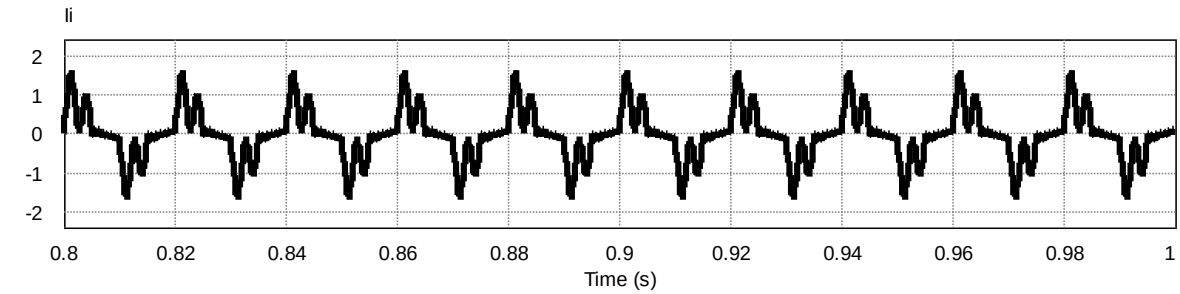


Figure 3.13(a): Input Current waveform of the proposed Buck-Boost converter

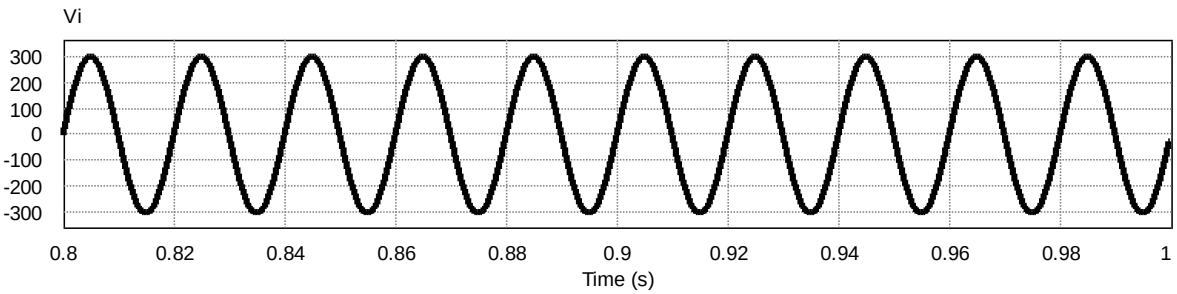


Figure 3.13(b): Input Voltage waveform of the proposed Buck-Boost converter

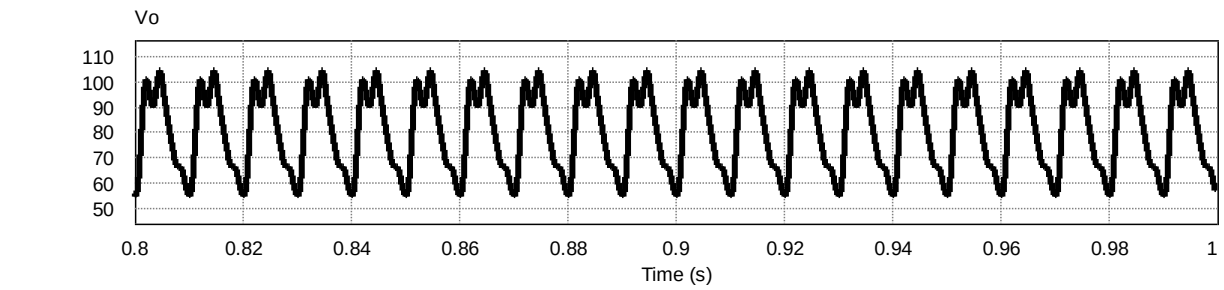


Figure 3.13(c): Output Voltage waveform of the proposed Buck-Boost converter

From figures 3.12(b) and 3.13(b) it is seen that, the input voltage of the proposed converter is a sinusoidal voltage with a peak value of 300 V. The peak to peak value is 600 V. From figure 3.12(a) and 3.13(a), we see the input current varies from 1.9 A to -1.9 A for frequency of 30 kHz and 80kHz (under duty ratio of 0.2). The output voltage waveforms for these two frequencies (under duty ratio of 0.2) are provided in figure 3.12(c) and 3.13(c). The average value of output voltages for these frequencies are 86 V and 80 V respectively.

3.9 Simulation results of Proposed Single-Phase Non-isolated AC-DC Buck Boost Converter under frequency variation (for duty ratio of 0.6)

Performance analysis of proposed single-phase non-isolated AC-DC Buck-Boost converter under frequency variation (for duty ratio of 0.6) was given in table 3.6. In this section, the simulation results are provided for switching frequency of 30 kHz and 80 kHz (for duty ratio of 0.6). For these frequencies the figures of input current waveform, input voltage waveform and output voltage waveform are provided.

For frequency of 30 kHz:

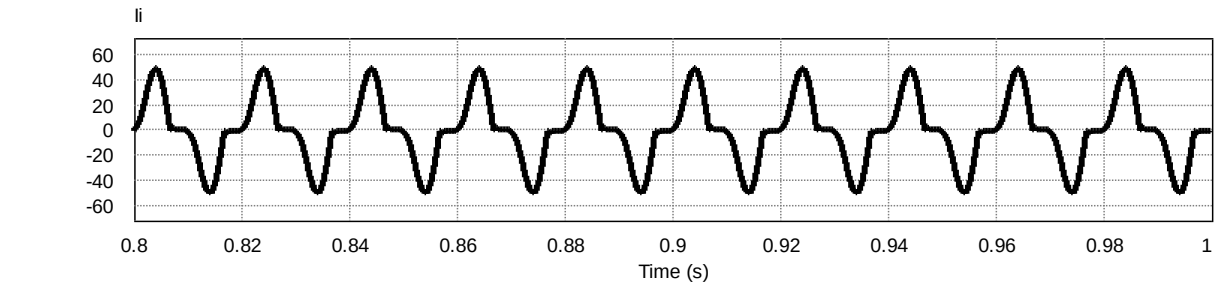


Figure 3.14(a): Input Current waveform of the proposed Buck-Boost converter

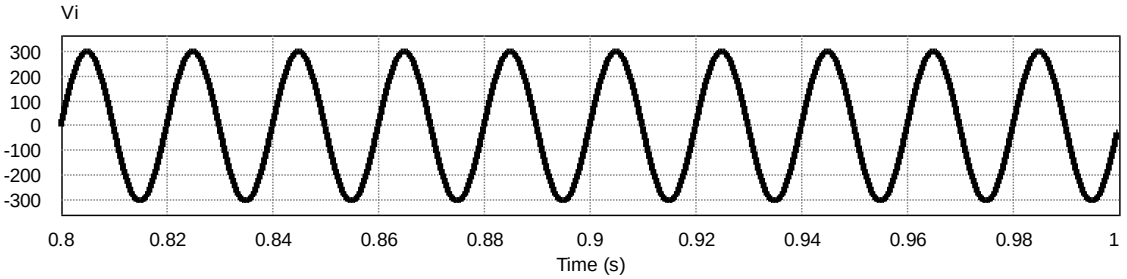


Figure 3.14(b): Input Voltage waveform of the proposed Buck-Boost converter

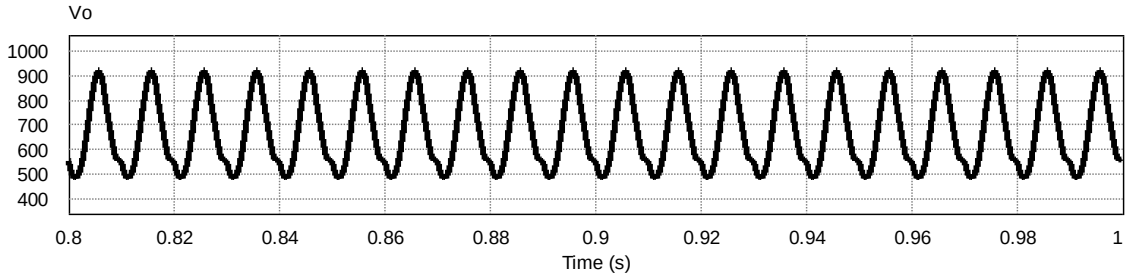


Figure 3.14(c): Output Voltage waveform of the proposed Buck-Boost converter

For frequency of 80 kHz:

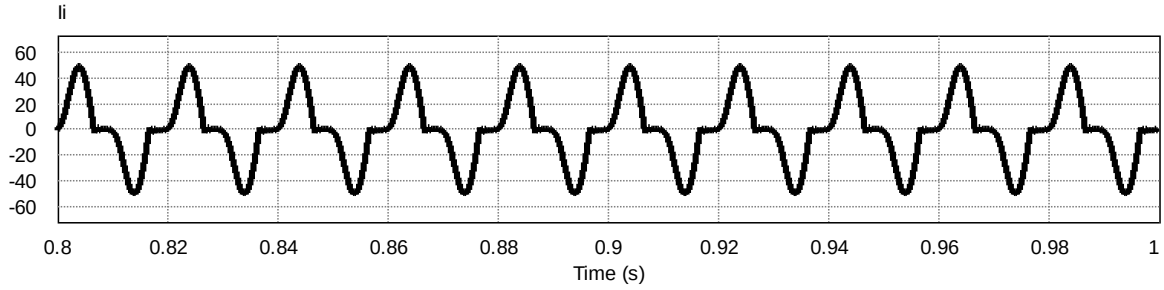


Figure 3.15(a): Input Current waveform of the proposed Buck-Boost converter

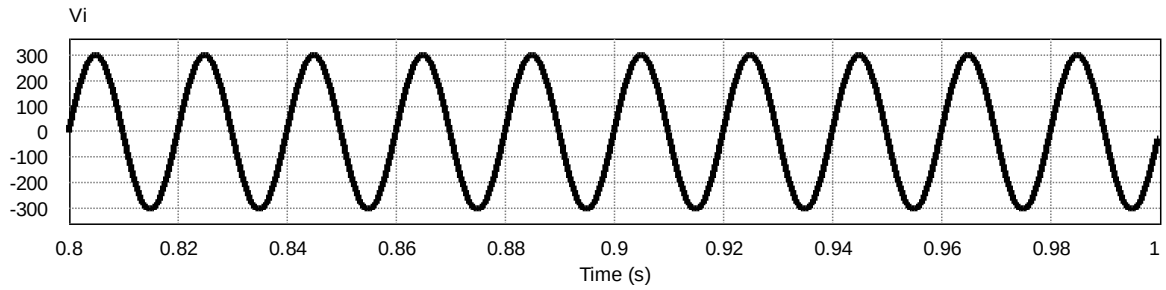


Figure 3.15(b): Input Voltage waveform of the proposed Buck-Boost converter

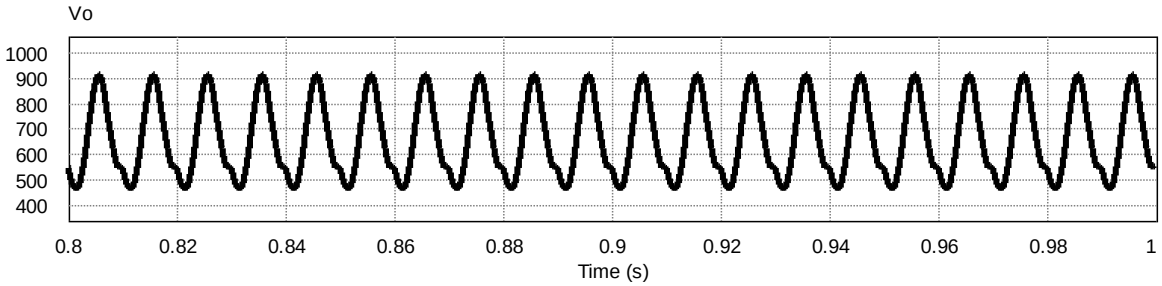


Figure 3.15(c): Output Voltage waveform of the proposed Buck-Boost converter

From figures 3.14(b) and 3.15(b) it is seen that, the input voltage of the proposed converter is a sinusoidal voltage with a peak value of 300 V. The peak to peak value is 600 V. From figure 3.14(a) and 3.15(a), we see the input current varies from 50 A to -50 A for frequency of 30 kHz and 80kHz (under duty ratio of 0.6). The output voltage waveforms for these two frequencies (under duty ratio of 0.6) are provided in figure 3.14(c) and 3.15(c). The average value of output voltages for these frequencies are 673 V and 665 V respectively.

Chapter 4

Performance Analysis of Proposed Single-Phase Non- isolated AC-DC Buck-Boost Converter

4.1 Introduction

Open-loop performance analysis is an important aspect to judge the performance of a specific converter in comparison with other existing converters. It gives us an idea about how much development is obtained in terms of conversion efficiency, power factor, input current THD (%) and voltage gain. A discussion about power factor and harmonic distortion is presented in section 4.2. Performance analysis of proposed converter in comparison with the conventional converter is done under duty cycle, load and frequency variation and presented in section 4.3,4.4 and 4.5 respectively. Performance analysis of proposed converter with recent Converter (Topology 1) under duty cycle variation is given in section 4.6. Performance analysis of proposed converter with recent Converter (Topology 2) under duty cycle variation is provided in section 4.7.

4.2 Power Factor and Harmonic distortion

The input power factor of an AC-DC converter plays a vital role in converter design because it determines how efficiently the converter utilizes the input AC power. Power factor is the ratio of real power to the apparent power [59] and can be showed as [60]

$$\text{PF} = \frac{real\ power(load\ power)}{apparent\ power} = \frac{\sum I_{sn,rms}V_{sn,ms}Cos\theta_n}{I_{s,rms}V_{s,rms}} \quad (4.1)$$

Where, $I_{sn,rms}\ and\ V_{sn,ms}$ denote the rms values of the nth harmonic of input current and input voltage and θ_n is the phase shift between them. The input AC voltage can be assumed to be a pure sinusoid, the product of current harmonic terms and voltage harmonic terms are zero except for the product of fundamental current and voltage harmonics so that eq. (1.1) can be written to be

$$\text{PF} = \frac{I_{s1,rms}}{I_{s,rms}} Cos\theta_1 \quad (4.2)$$

Where , $I_{s1,rms}$ is the rms value of the primary component of the input current. We observe from eq. (1.2) that, the power factor can be expressed as the cosine of the

phase angle between the input voltage and current waveforms. The power factor ranges from zero to one. When power factor is one, it indicates that the input current is in phase with the input voltage.

Total Harmonic Distortion (THD) is another essential term to determine the power quality of electrical power systems. THD is defined as the ratio of the square root of the summation of the square of all non-fundamental harmonics of a waveform to a fundamental component of the same waveform. For a current waveform, particularly the input current of a power electronic converter, it can be expressed as,

$$THD_i = \frac{\sqrt{I_2^2,rms+I_3^2,rms+\cdots+I_n^2,rms}}{I_1,rms} \quad (4.3)$$

Where, I_n, rms is the rms value of the nth harmonic of input current [61].

4.3 Analysis of Proposed Converter under Duty Cycle Variation

The performance analysis of the proposed converter is done in comparison with the conventional converter under the variation of the duty cycle. Here, by conventional converter we meant the Buck-Boost converter discussed in section 2.1.3. The data of comparison is provided in table 4.1. For a better understanding of the comparison column chart and line chart are provided. The proposed converter shows better efficiency over the conventional one, as seen from figure 4.2 except for duty ratio of 0.8 and 0.9. The conventional converter provides a slightly better power factor for lower duty cycles. Still, the proposed converter has a better power factor for the duty ratio of 0.6 and 0.7, which is almost close to unity (figure 4.1). The proposed converter presents a higher voltage gain than the conventional one throughout the variation of duty cycle except for the duty ratio of 0.9, as illustrated in figure 4.3. The total harmonic distortion(THD) of input current shows better performance in the case of the proposed converter for higher duty cycles.

Table 4.1 Performance Comparison of Prosed Buck-Boost converter under duty cycle variation

Duty Cycle	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
0.1	97.587	40.295	0.712	0.238	96.601	6.595	0.847	0.22
0.2	99.061	57.147	0.767	0.548	98.206	7.317	0.969	0.45
0.3	99.288	61.188	0.748	0.854	98.509	6.921	0.976	0.708
0.4	99.276	50.792	0.812	1.35	98.617	10.933	0.981	1.006
0.5	99.158	37.724	0.901	2.08	98.642	29.656	0.953	1.49
0.6	99.045	25.646	0.967	3.009	98.629	25.751	0.961	1.98
0.7	98.719	15.753	0.969	4.147	98.565	24.266	0.953	2.59
0.8	98.025	7.332	0.823	5.322	98.358	20.724	0.898	3.59
0.9	95.292	1.535	0.342	4.02	97.507	6.103	0.627	4.74

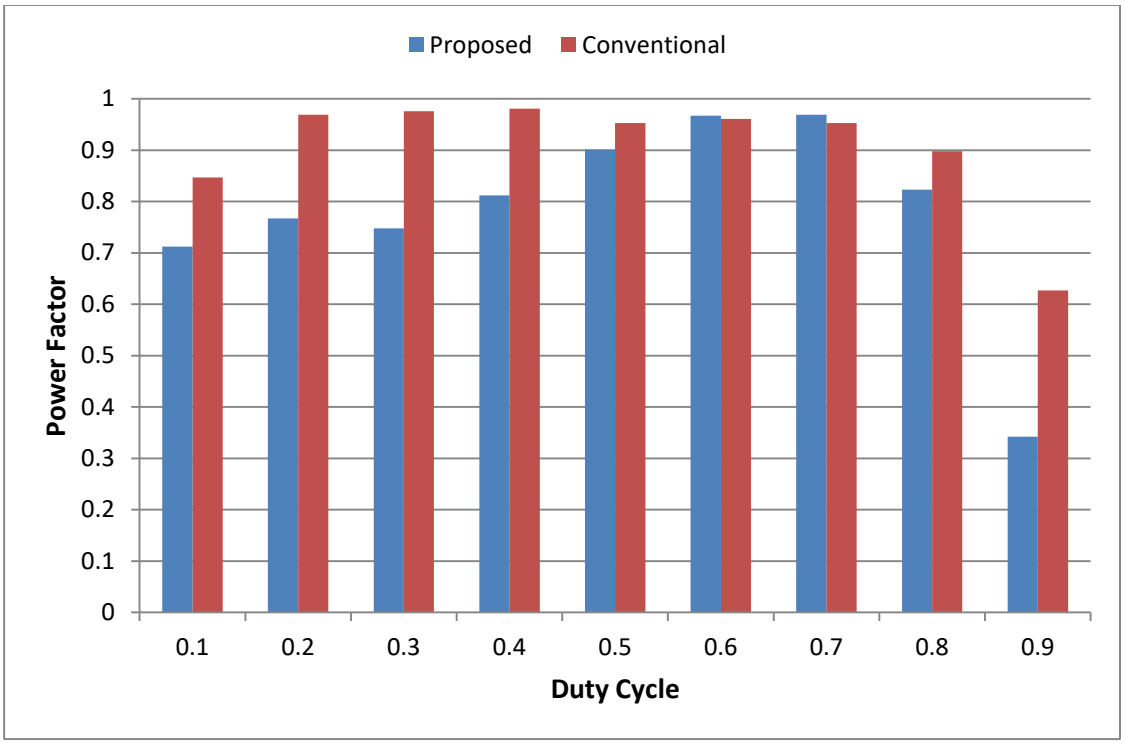


Figure 4.1: Graphical comparison of Power Factor between proposed and conventional converter under Duty Cycle Variation

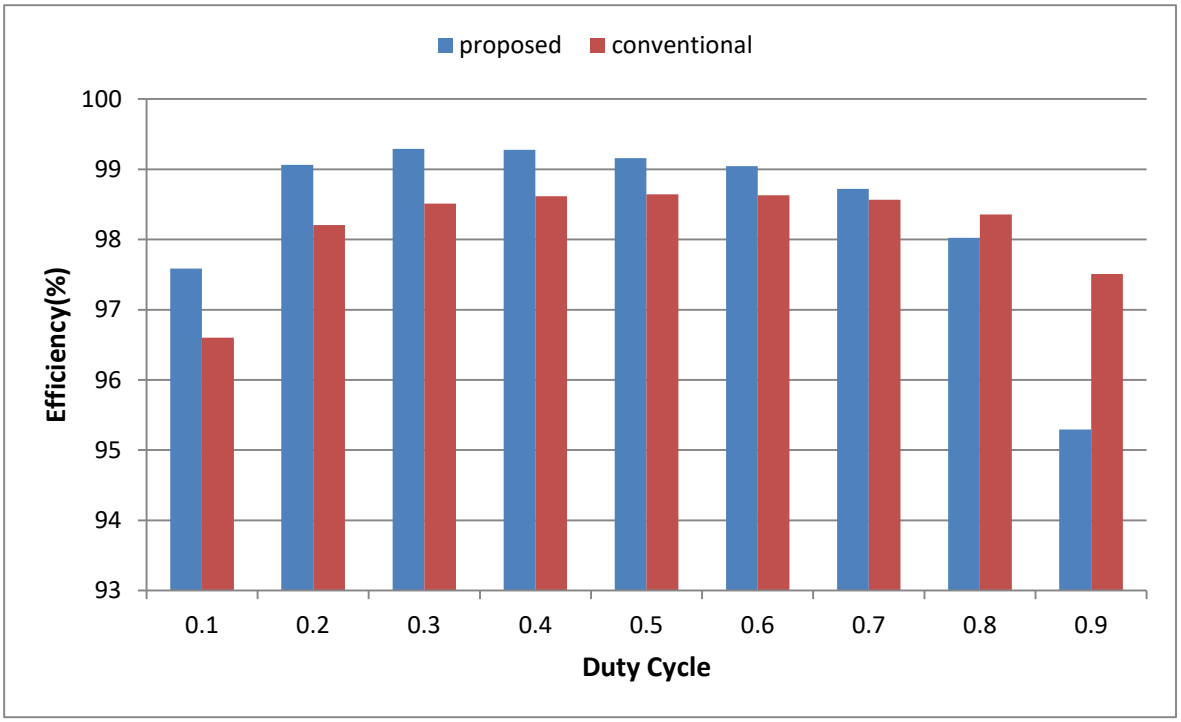


Figure 4.2: Graphical comparison of Efficiency between proposed and conventional converter under Duty Cycle Variation

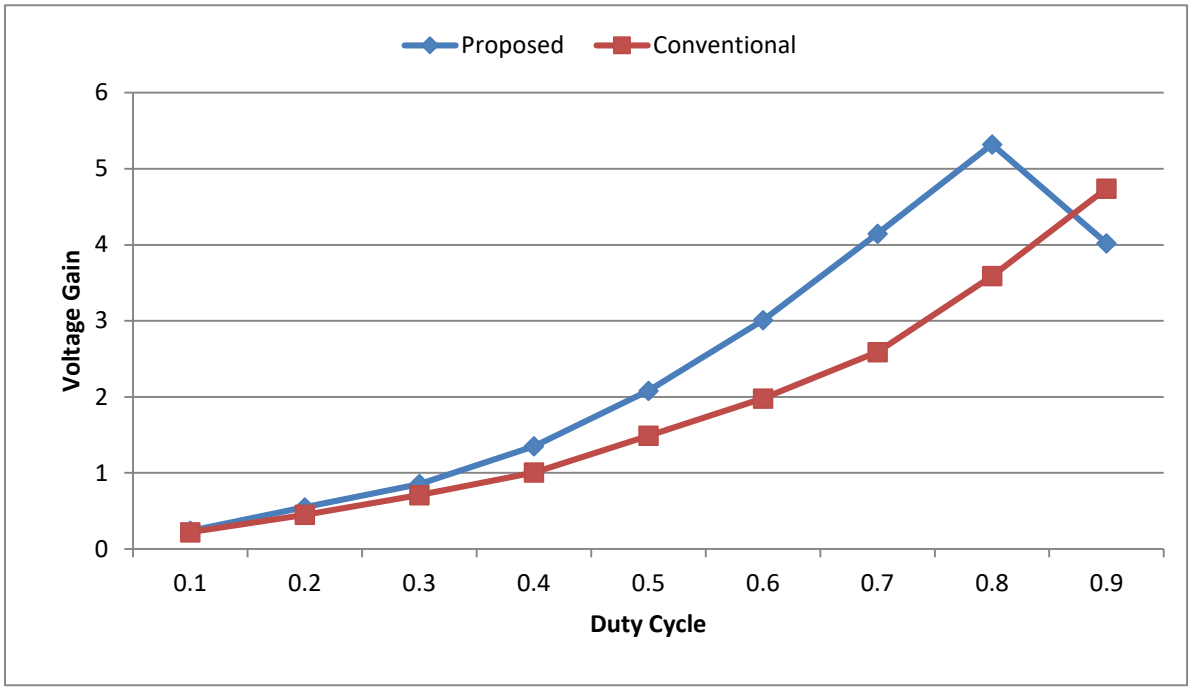


Figure 4.3: Graphical comparison of Voltage Gain between proposed and conventional converter under Duty Cycle Variation

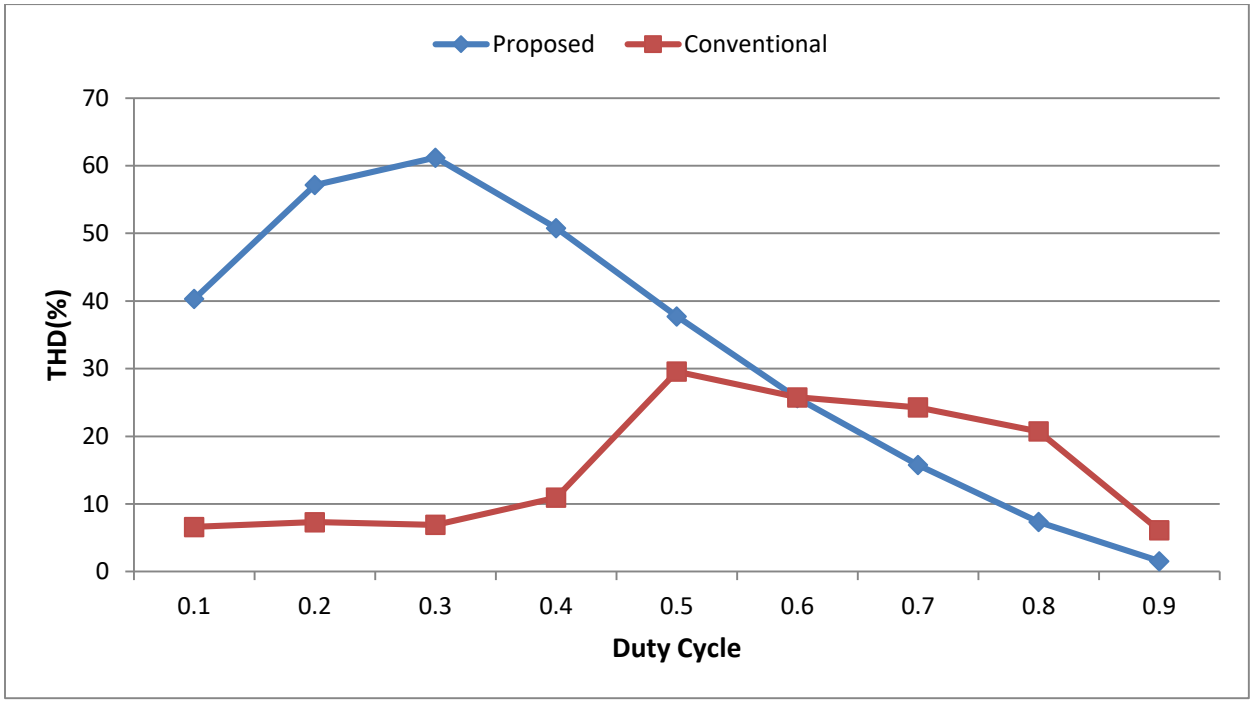


Figure 4.4: Graphical comparison of THD between proposed and conventional converter under Duty Cycle Variation

4.4 Analysis of Proposed Converter under Load Variation

The performance analysis of the proposed converter is done with the variation of load and for the duty cycle of 0.2 and 0.6. The data is provided in table 4.2 and table 4.3. For a better understanding of the comparison column chart and line chart are provided.

For duty ratio of 0.2:

The conventional converter shows a higher power factor over the proposed one throughout the variation of load. The efficiency of the conventional converter is slightly higher than the proposed one. The voltage gain is almost the same for both converters and within the buck mode. The total harmonic distortion (THD) of input current shows better performance in the case of the conventional converter.

For duty ratio of 0.6:

The proposed converter shows a higher power factor over the conventional one throughout the variation of load. The power factor of the proposed converter remains almost close to unity. The proposed converter has much higher efficiency than the conventional one over the variation of load. The efficiency of the proposed converter is as high as 99%. The proposed converter presents a higher voltage gain than the conventional one throughout the variation of load. The total harmonic distortion (THD) of input current shows better performance in the case of the proposed converter for lower loads.

Table 4.2 Performance Comparison of Proposed Buck-Boost converter under Load variation (for duty ratio of 0.2)

Load (Ω)	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
50	94.61	54.63	0.77	0.36	98.24	24	0.95	0.35
70	94.44	59.95	0.76	0.42	98.54	7.3	0.96	0.38
90	94.30	59.06	0.76	0.47	97.51	7.9	0.96	0.43
110	94.16	53	0.79	0.51	97.51	7.3	0.97	0.47
130	94.26	57.04	0.79	0.57	97.61	7.5	0.96	0.51
150	94.26	50.62	0.83	0.61	97.51	7.3	0.97	0.55

Table 4.3 Performance Comparison of Proposed Buck-Boost converter under Load variation (for duty ratio of 0.6)

Load (Ω)	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
50	99.21	23.78	0.97	2.10	99.15	23.55	0.96	1.60
70	99.08	23.94	0.97	2.56	98.99	25.14	0.96	1.78
90	99.98	25.23	0.96	2.86	98.72	25.73	0.96	1.91
110	99.01	26.78	0.96	3.12	98.49	25.53	0.96	2.03
130	98.97	28.14	0.96	3.37	98.24	24.66	0.96	2.12
150	99.05	30.04	0.95	3.59	98.04	23.38	0.96	2.19

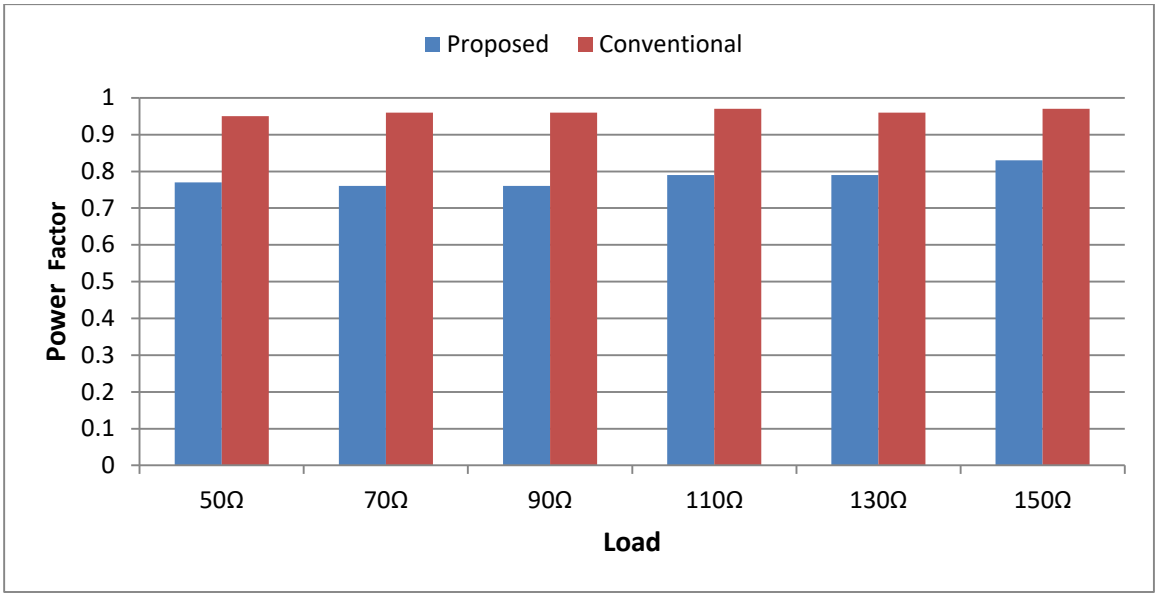


Figure 4.5: Graphical comparison of Power Factor between proposed and conventional converter under Load Variation (for duty ratio 0.2)

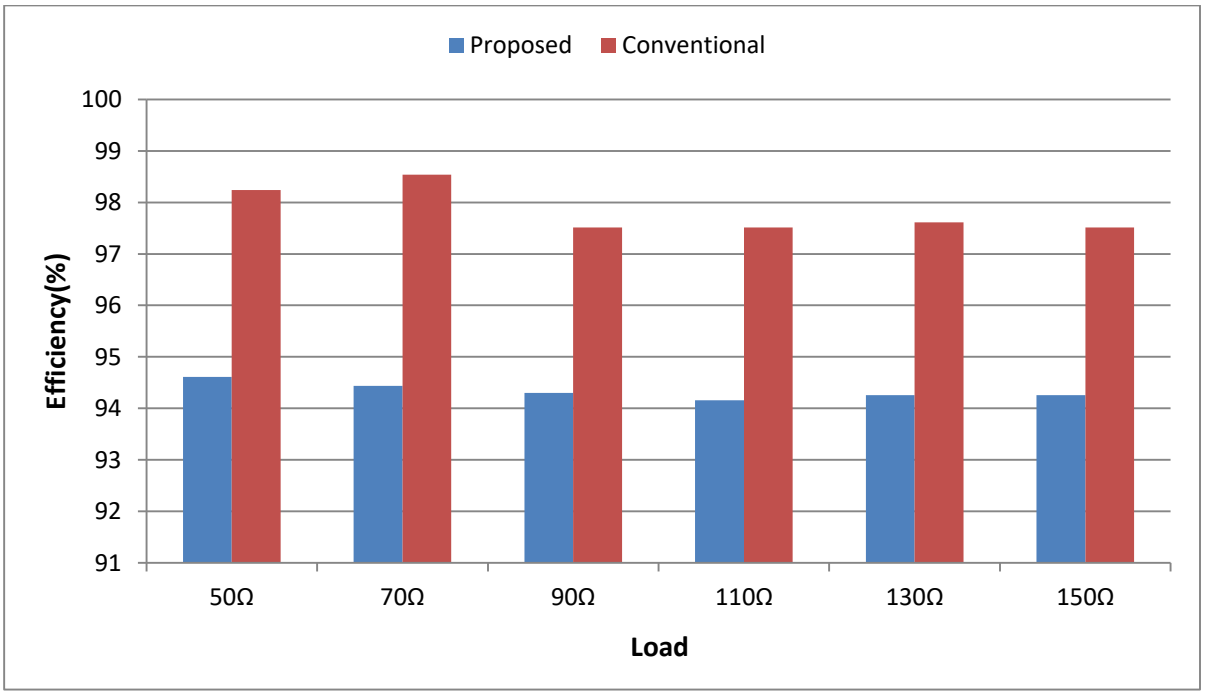


Figure 4.6: Graphical comparison of Efficiency between proposed and conventional converter under Load Variation (for duty ratio 0.2)

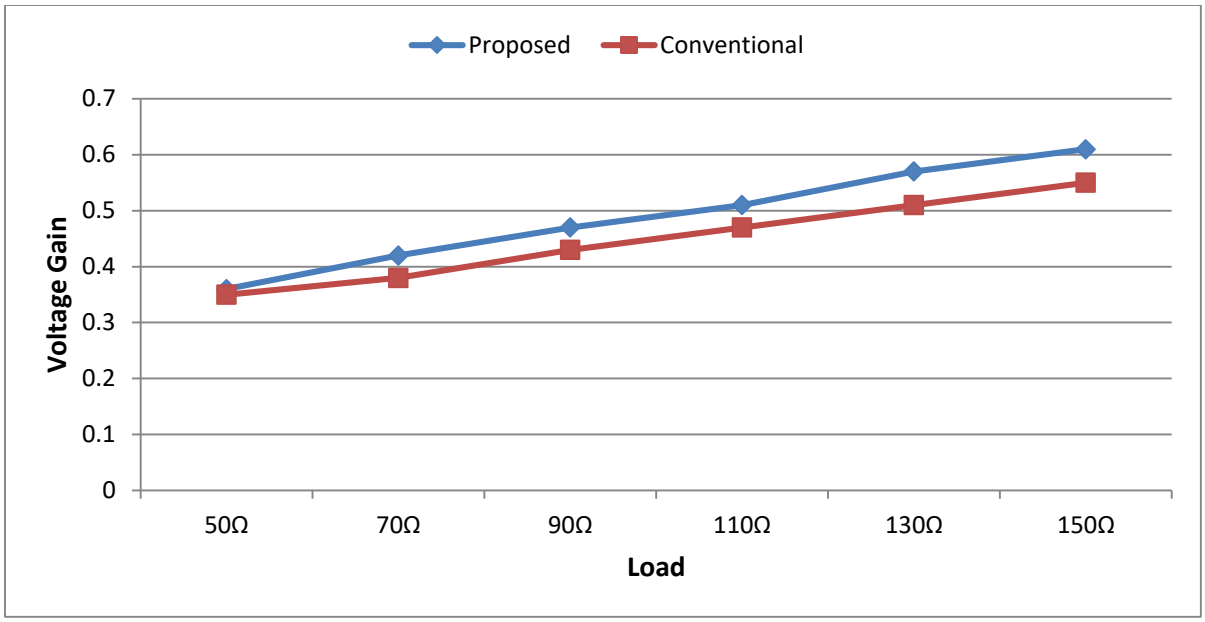


Figure 4.7: Graphical comparison of Voltage Gain between proposed and conventional converter under Load Variation (for duty ratio 0.2)

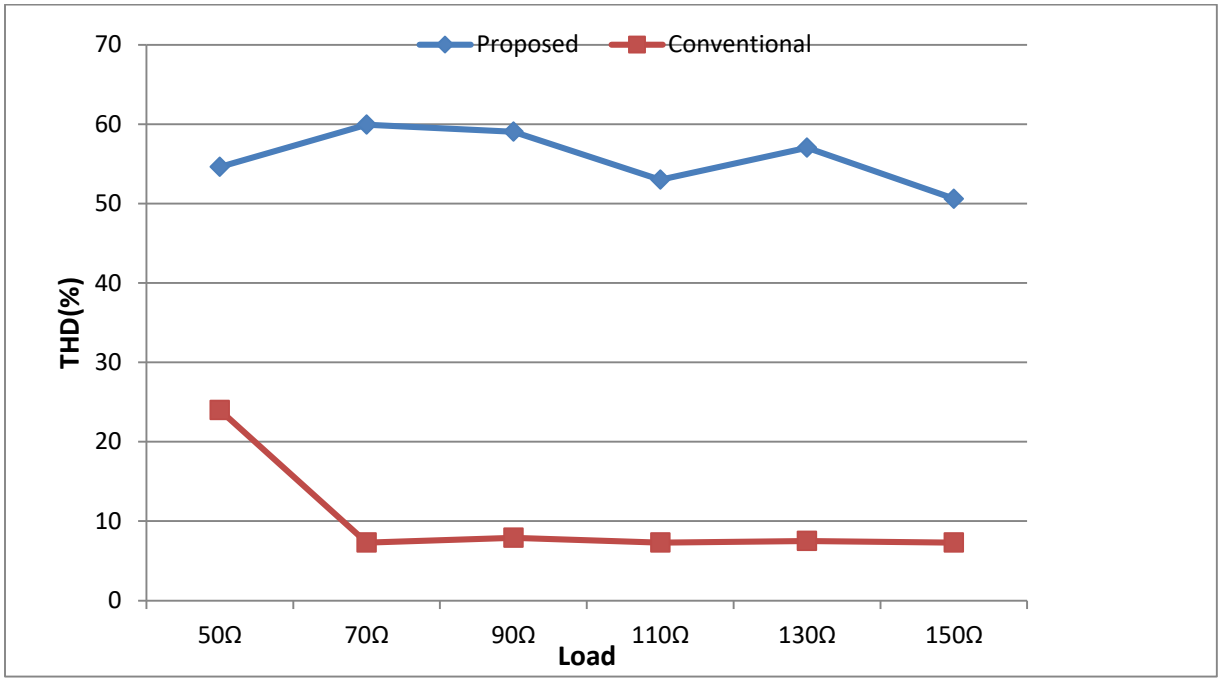


Figure 4.8: Graphical comparison of THD between proposed and conventional converter under Load Variation (for duty ratio 0.2)

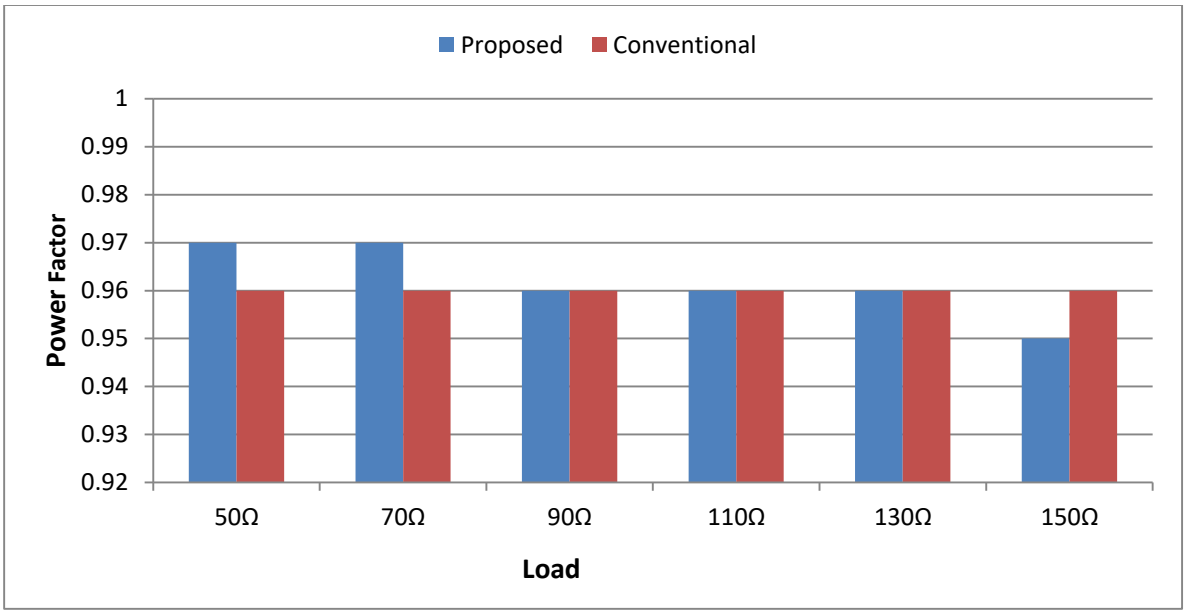


Figure 4.9: Graphical comparison of Power Factor between proposed and conventional converter under Load Variation (for duty ratio 0.6)

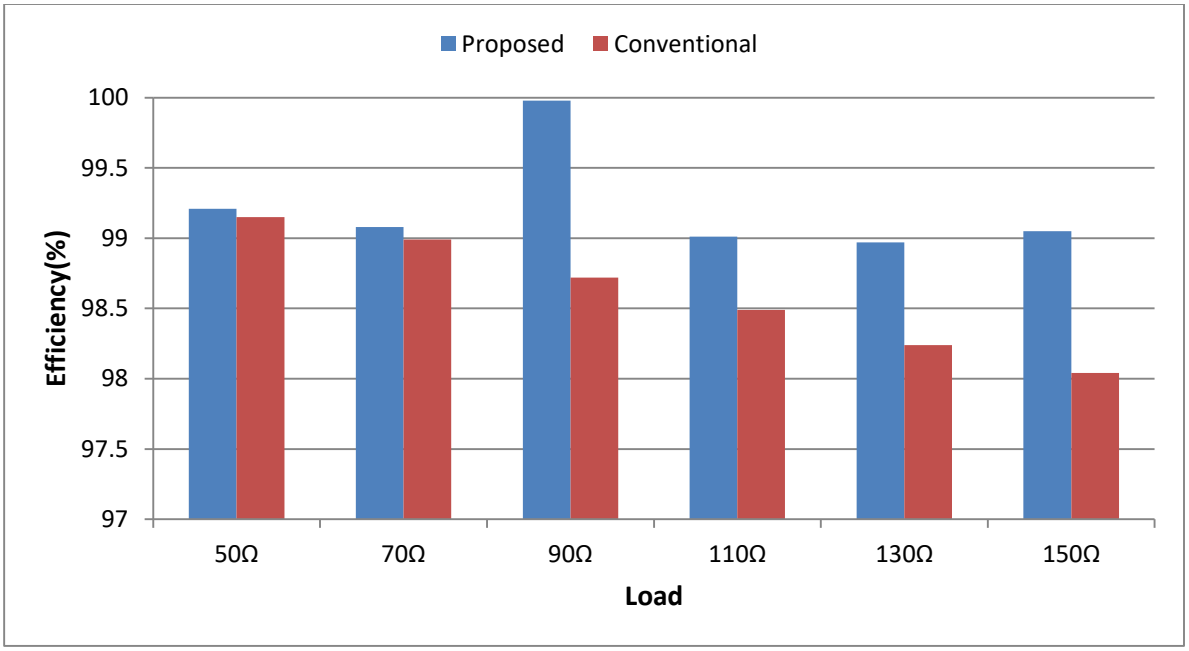


Figure 4.10: Graphical comparison of Efficiency between proposed and conventional converter under Load Variation (for duty ratio 0.6)

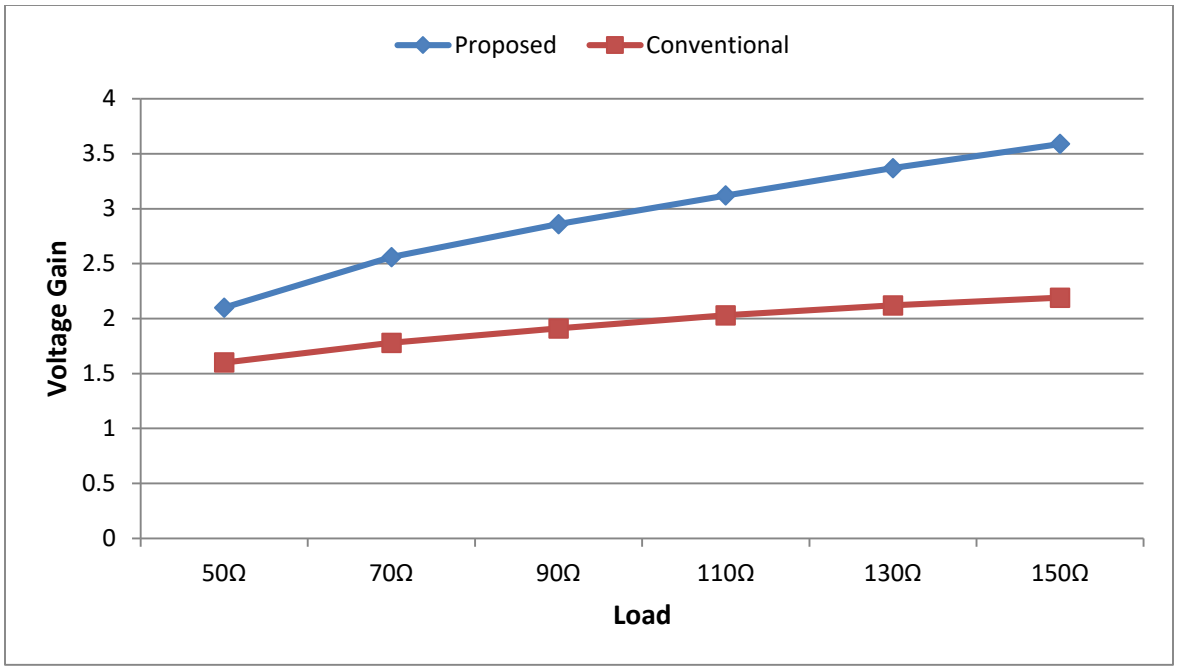


Figure 4.11: Graphical comparison of Voltage Gain between proposed and conventional converter under Load Variation (for duty ratio 0.6)

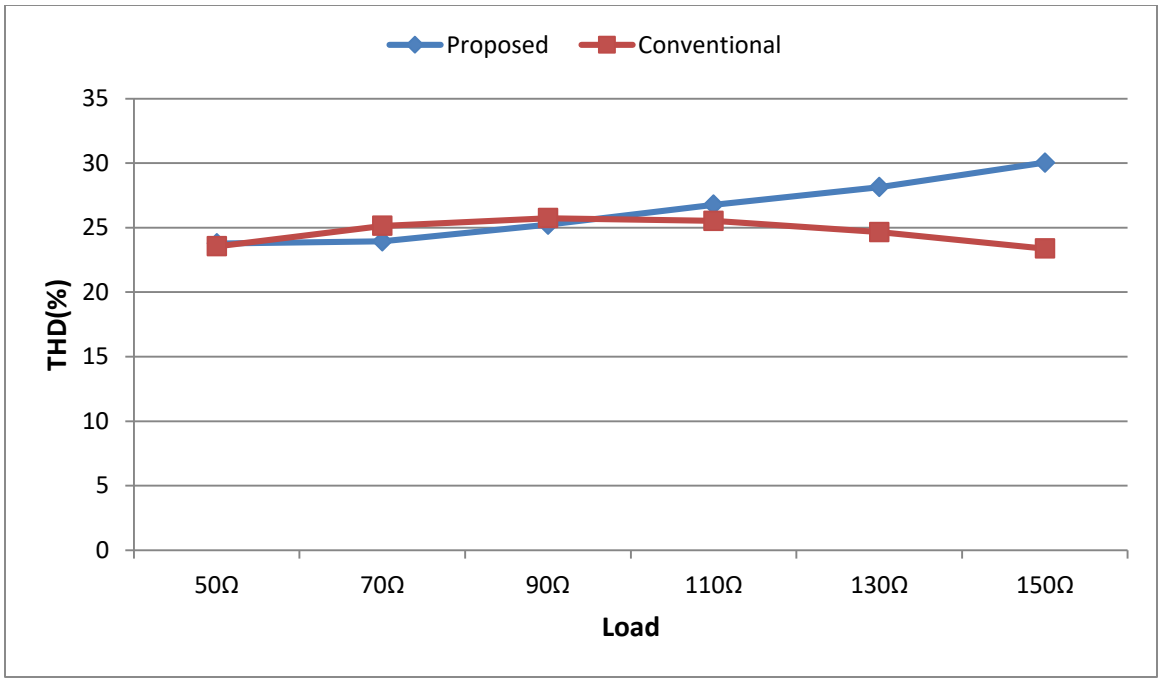


Figure 4.12: Graphical comparison of THD between proposed and conventional converter under Load Variation (for duty ratio 0.6)

4.5 Analysis of Proposed Converter under Frequency Variation

The performance analysis of the proposed converter is done with the variation of switching frequency and for the duty cycle of 0.2 and 0.6. The data is provided in table 4.4 and 4.5. For a better understanding of the comparison column chart and line chart are provided.

For duty ratio of 0.2:

The conventional converter has a better power factor than the proposed one throughout the variation of switching frequency. The proposed converter has much higher efficiency than the conventional one over the variation of switching frequency. The voltage gain remains almost safe for both types of converters over the variation of switching frequency. The total harmonic distortion (THD) of the input current is much lower in the case of the proposed converter than the conventional one for a higher order of switching frequency.

For duty ratio of 0.6:

The proposed converter has a better power factor than the conventional one throughout the variation of switching frequency. The efficiency of the conventional converter is slightly higher than the proposed one. The proposed converter presents a much higher voltage gain than the conventional one throughout the variation of frequency. The total harmonic distortion (THD) of the input current is much lower in the case of the proposed converter than the conventional one over the variation of frequency.

Table 4.4 Performance Comparison of Proposed Buck-Boost converter under frequency variation (for duty ratio 0.2)

Frequency	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
10k	99.49	56.49	0.76	0.509	98.64	7.3	0.96	0.45
20k	99.19	68.74	0.62	0.43	98.04	26.5	0.89	0.34
30k	98.73	70.32	0.58	0.41	97.66	58.4	0.79	0.34
40k	98.54	71.95	0.56	0.40	97.47	73.7	0.74	0.34
50k	98.23	70.28	0.54	0.39	97.11	81.3	0.71	0.34
60k	97.65	71.65	0.54	0.38	98.20	86.4	0.69	0.34
70k	97.34	71.42	0.53	0.38	96.05	90.7	0.68	0.34
80k	96.88	71.34	0.53	0.38	95.70	93.6	0.67	0.34
90k	96.70	73.33	0.52	0.38	95.27	98.8	0.66	0.34
100k	96.54	73.95	0.52	0.37	95.52	102	0.65	0.34

Table 4.5 Performance Comparison of Proposed Buck-Boost converter under frequency variation (for duty ratio 0.6)

Frequency	Proposed Converter				Conventional Converter			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
10k	98.71	25.64	0.96	3.00	98.61	25.75	0.96	1.97
20k	97.99	41.27	0.88	3.15	98.36	52.12	0.84	1.92
30k	97.71	44.36	0.86	3.16	98.24	56.58	0.81	1.88
40k	97.42	45.30	0.85	3.15	97.92	58.61	0.79	1.87
50k	96.94	45.64	0.85	3.13	97.73	59.91	0.78	1.86
60k	96.91	46.05	0.84	3.13	97.66	60.60	0.77	1.86
70k	96.72	46.15	0.84	3.12	97.53	61.08	0.77	1.86
80k	96.49	46.17	0.84	3.10	97.15	61.54	0.77	1.85
90k	96.18	46.24	0.84	3.10	97.15	61.72	0.77	1.85
100k	95.35	46.20	0.84	3.08	96.72	61.82	0.77	1.85

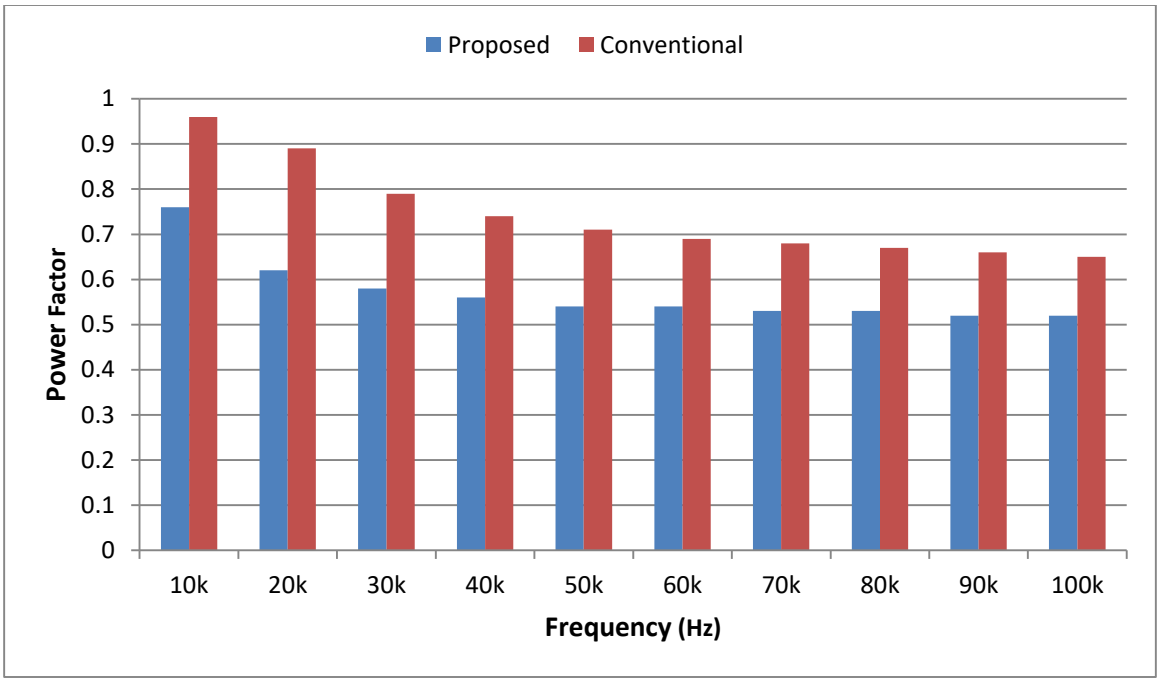


Figure 4.13: Graphical comparison of Power Factor between proposed and conventional converter under frequency Variation (for duty ratio of 0.2)

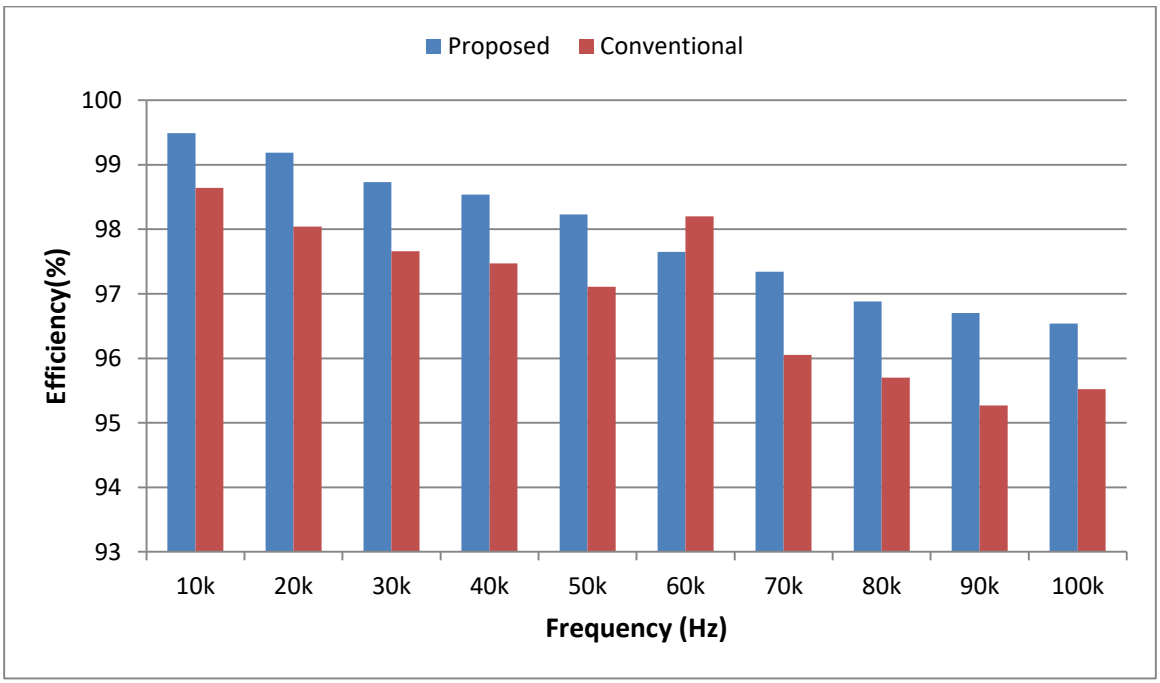


Figure 4.14: Graphical comparison of Efficiency between proposed and conventional converter under frequency Variation (for duty ratio of 0.2)

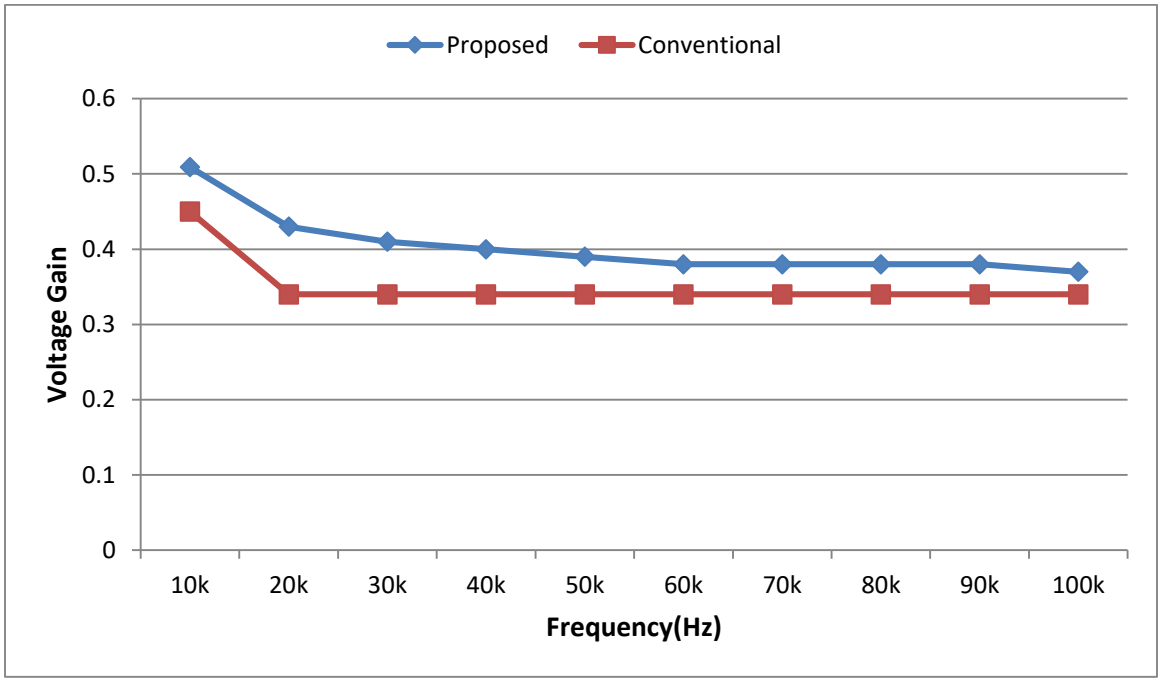


Figure 4.15: Graphical comparison of Voltage Gain between proposed and conventional converter under frequency Variation (for duty ratio 0.2)

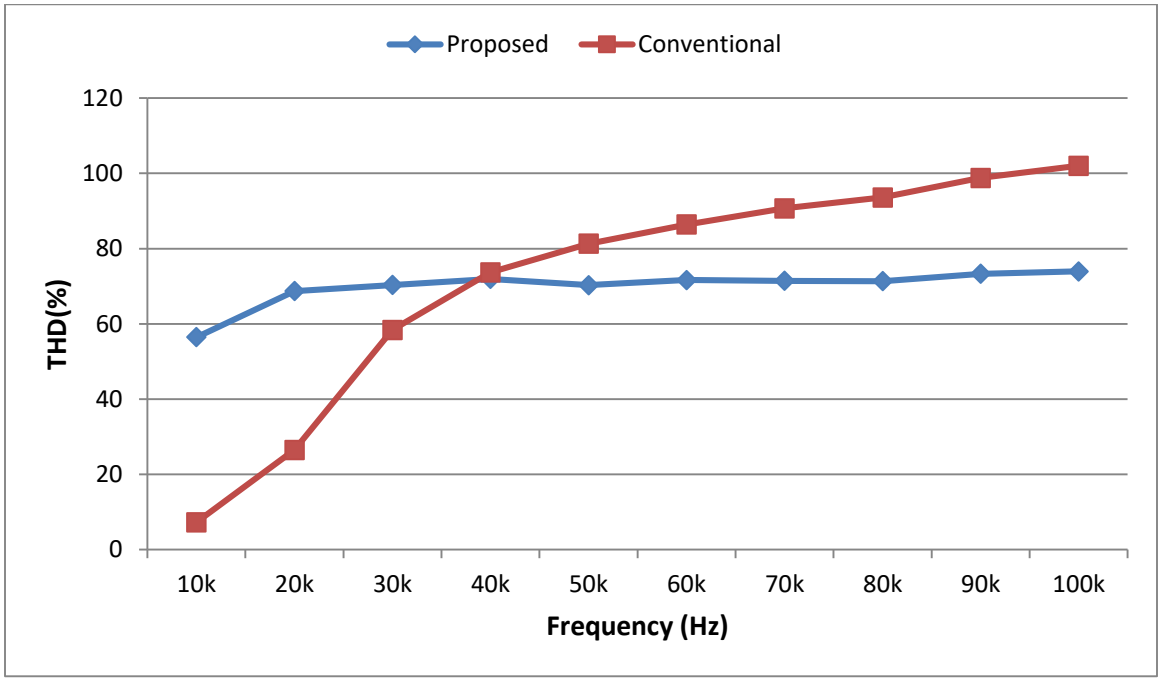


Figure 4.16: Graphical comparison of THD between proposed and conventional converter under frequency Variation (for duty ratio 0.2)

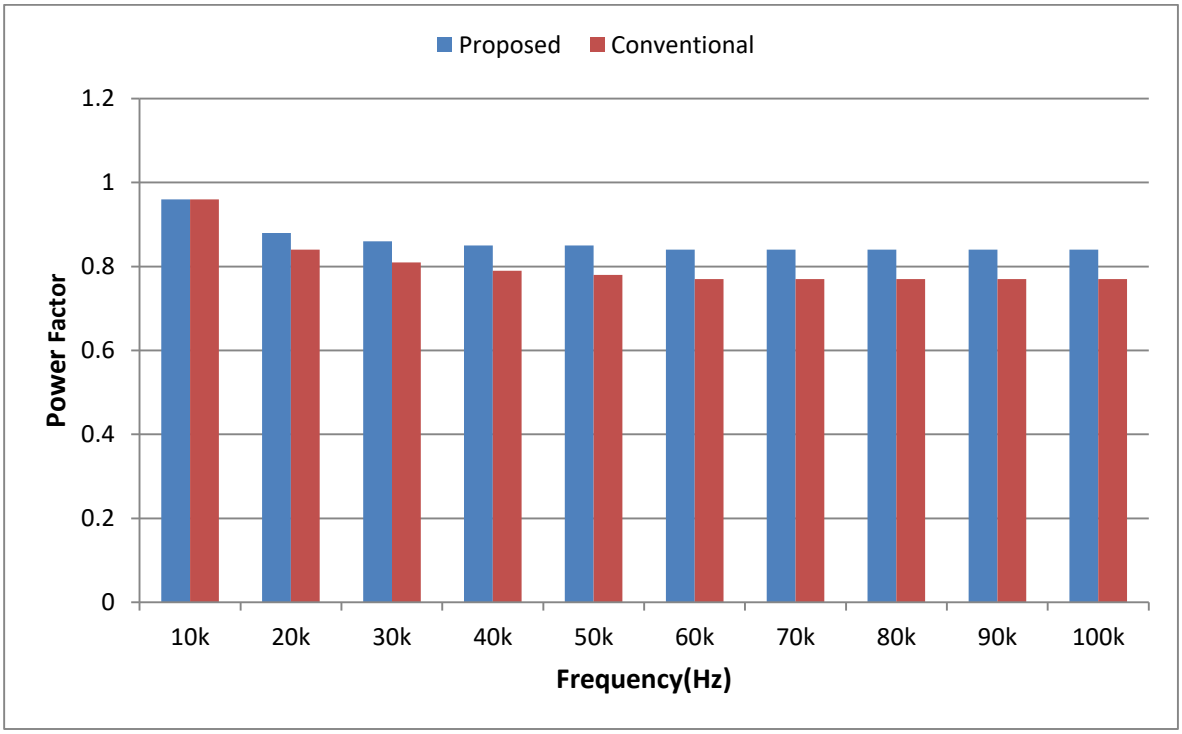


Figure 4.17: Graphical comparison of Power Factor between proposed and conventional converter under frequency Variation (for duty ratio of 0.6)

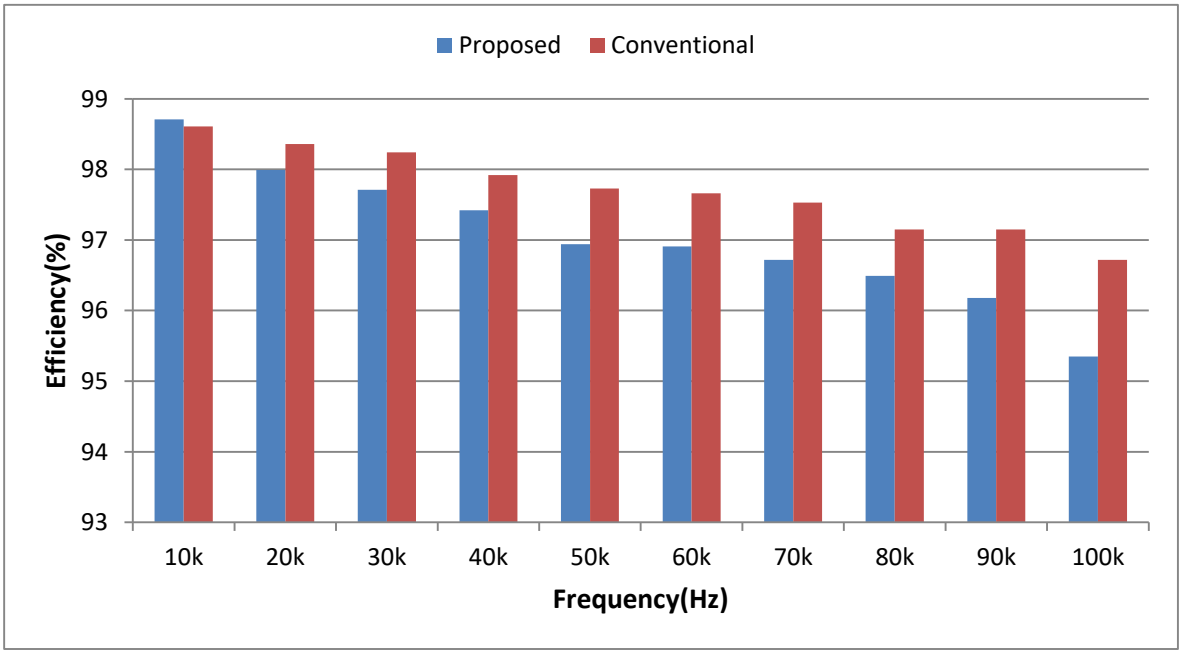


Figure 4.18: Graphical comparison of Efficiency between proposed and conventional converter under frequency Variation (for duty ratio of 0.6)

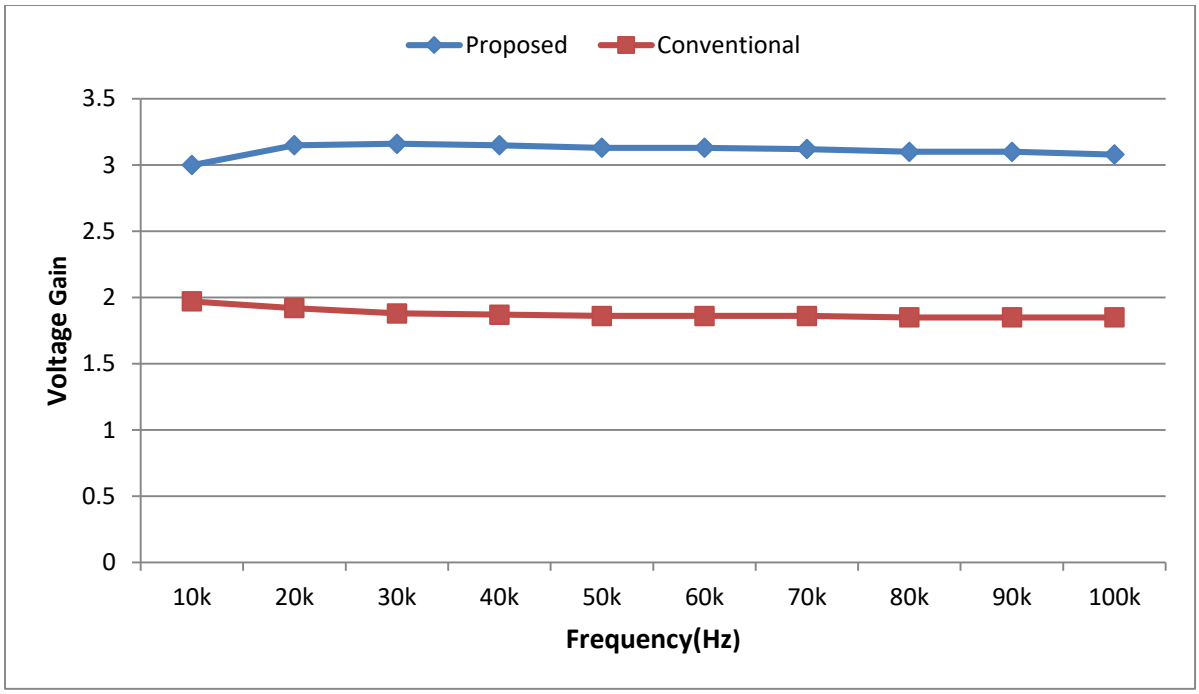


Figure 4.19: Graphical comparison of Voltage Gain between proposed and conventional converter under frequency Variation (for duty ratio 0.6)

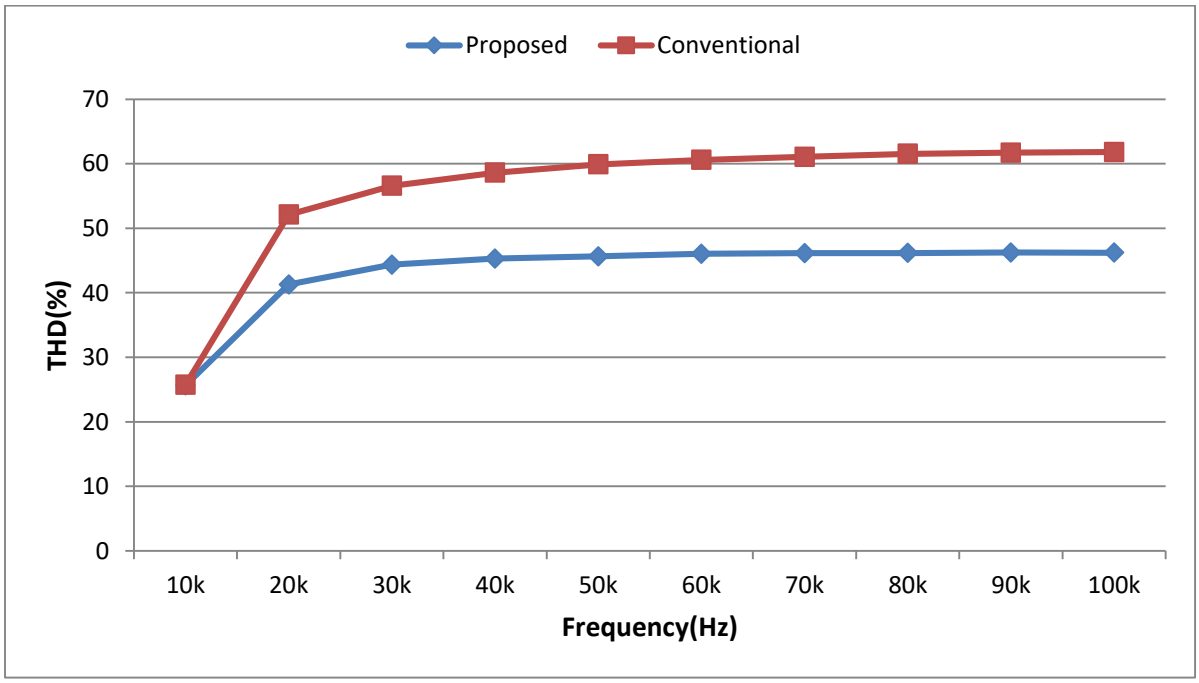


Figure 4.20: Graphical comparison of THD between proposed and conventional converter under frequency Variation (for duty ratio 0.6)

4.6 Analysis of Proposed Converter with Recent Converter (Topology 1) under duty cycle variation

In chapter 2, we have shown the open-loop analysis of various recent converter topologies. Here, we have provided a performance analysis of the proposed converter with recent converter topologies. Firstly, we have given a performance analysis scenario of the proposed converter with the recent converter topology 1 under duty cycle variation. Topology 1 is the input switched single phase Buck-Boost AC-DC converter [56]. The data is provided in table 4.6. For a better understanding of the comparison column chart and line chart are provided. Topology 1 converter offers an improved power factor than the proposed converter throughout the variation of the duty cycle. The proposed converter has better efficiency than the topology 1 converter over the variation of the duty cycle. The proposed converter can perform better step-up, step-down operation than the topology 1 converter. The total harmonic distortion (THD) of input current shows better performance in the case of topology 1 converter.

Table 4.6 Performance Comparison of the Proposed converter with recent converter (topology 1) under duty cycle variation

Duty Cycle	Proposed Converter				Recent Converter (topology 1)			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
0.1	97.587	40.295	0.712	0.238	74%	3%	0.94	0.64
0.2	99.061	57.147	0.767	0.548	81.28%	2.7%	0.97	0.73
0.3	99.288	61.188	0.748	0.854	87.34%	3.15%	0.97	0.79
0.4	99.276	50.792	0.812	1.35	92.54%	3.28%	0.97	0.84
0.5	99.158	37.724	0.901	2.08	97.16%	2.7%	0.98	0.89
0.6	99.045	25.646	0.967	3.009	98.62%	2%	0.99	1.33
0.7	98.719	15.753	0.969	4.147	98.35%	1.7%	0.99	2.06
0.8	98.025	7.332	0.823	5.322	96.98%	1%	0.93	3.28
0.9	95.292	1.535	0.342	4.02	86.40%	0.4%	0.5	3.51

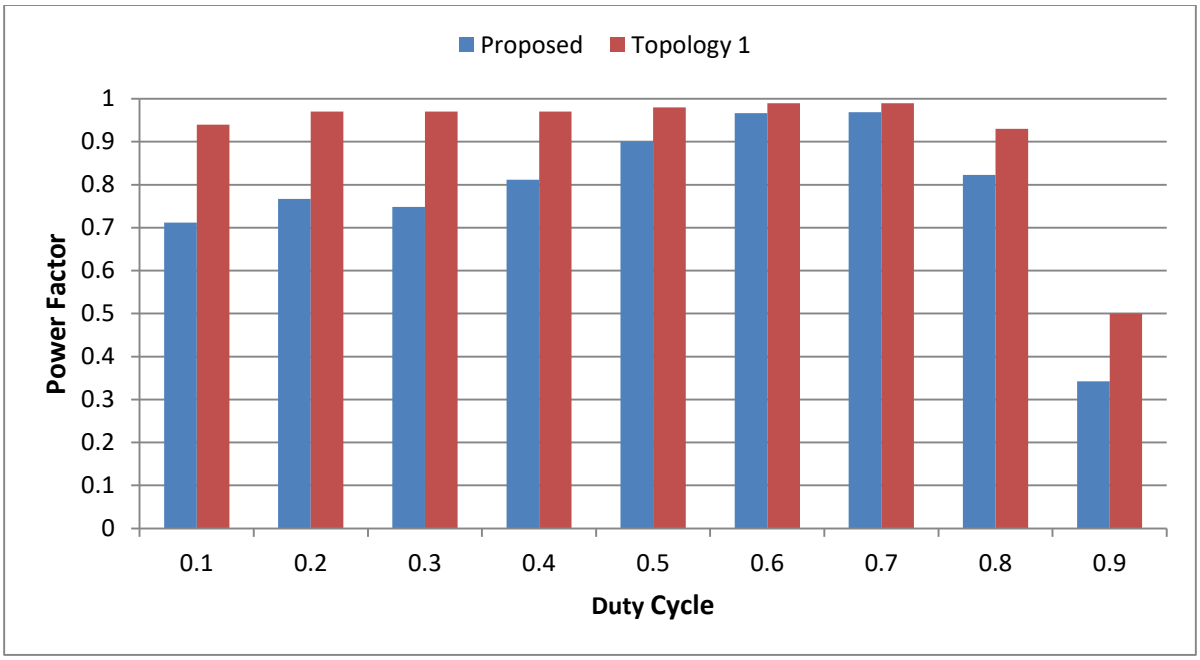


Figure 4.21: Graphical comparison of Power Factor between proposed and recent converter (topology 1) under duty cycle Variation.

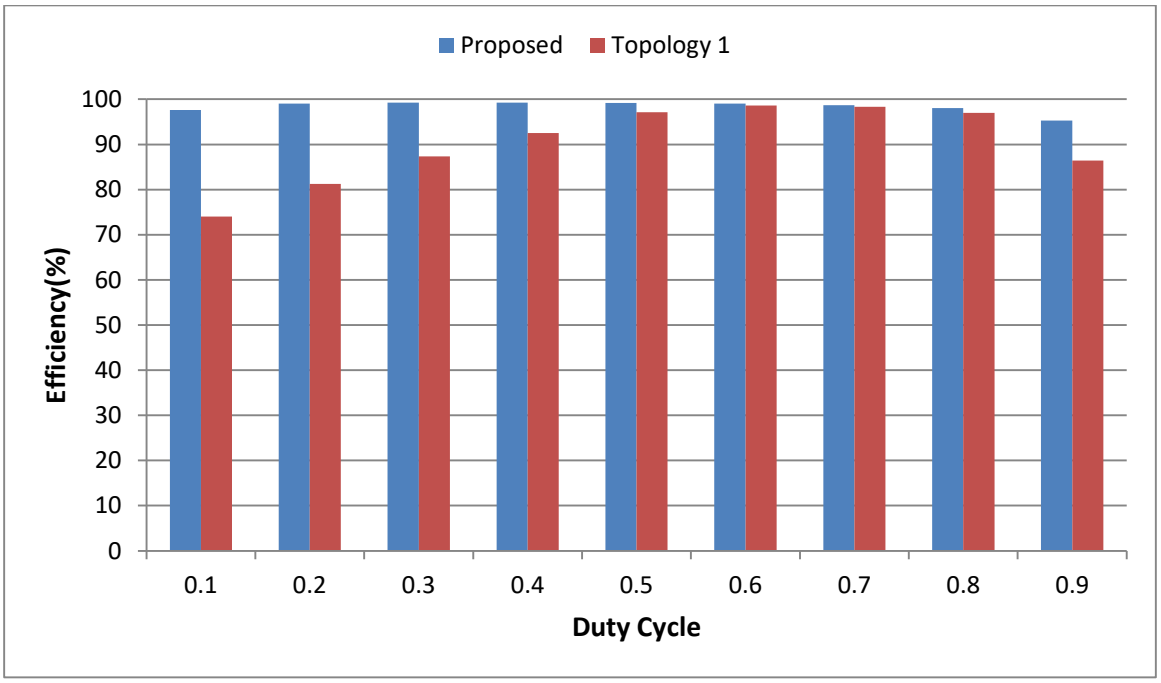


Figure 4.22: Graphical comparison of Efficiency between proposed and recent converter (topology 1) under duty cycle Variation

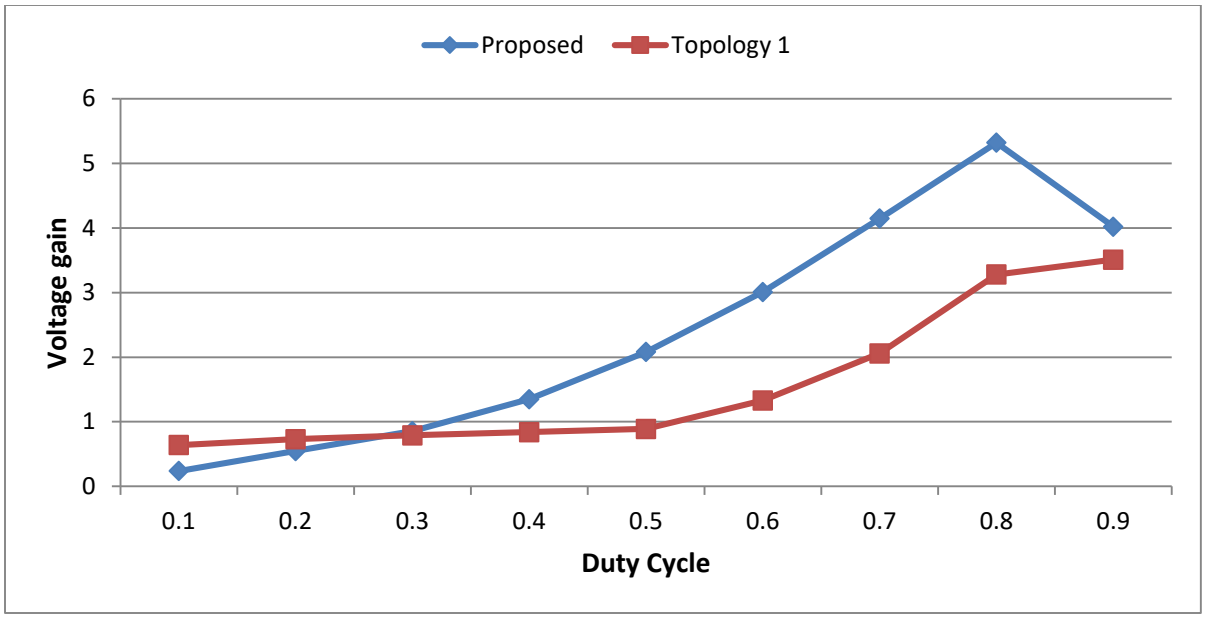


Figure 4.23: Graphical comparison of Voltage gain between proposed and recent converter (topology 1) under duty cycle Variation

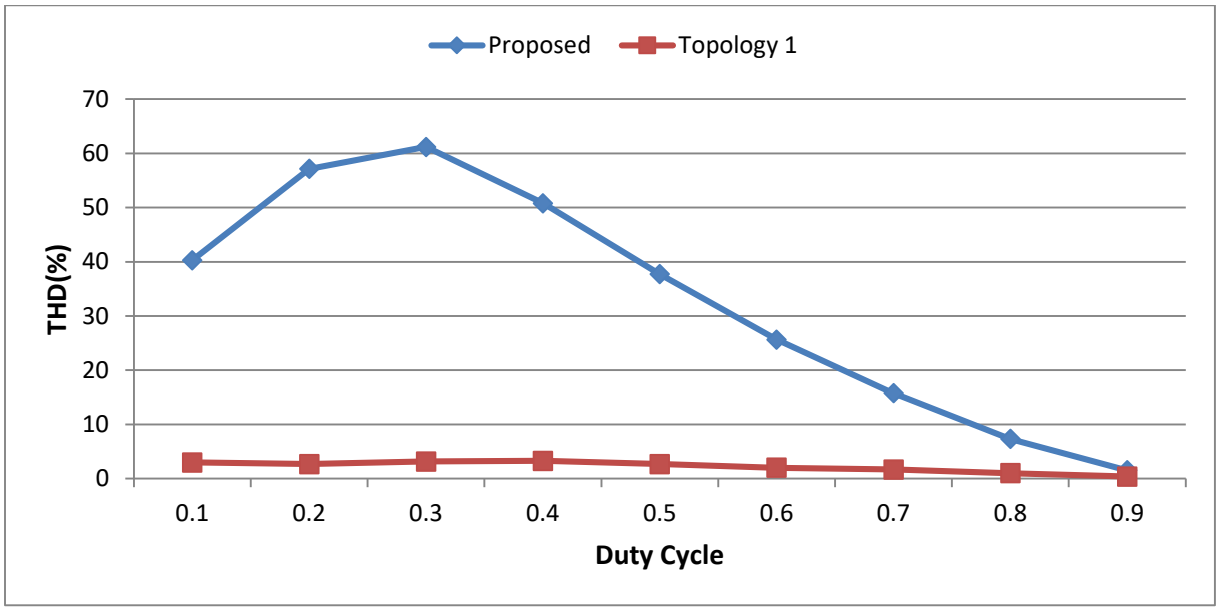


Figure 4.24: Graphical comparison of THD between proposed and recent converter (topology 1) under duty cycle Variation

4.7 Analysis of Proposed Converter with Recent Converter (Topology 2) under duty cycle variation

A performance analysis is done between the proposed converter and the recent converter topology 2 under duty cycle variation. Topology 2 is the high-efficiency single-phase switched capacitor AC to DC converter [57]. The data is provided in table 4.7. For a better understanding of the comparison column chart and line chart are provided. The proposed converter represents a much better power factor than the topology 2 converter throughout the variation of the duty cycle. The proposed converter has better efficiency than the topology 2 converter over the variation of the duty cycle. The proposed converter can perform better step-up, step-down operation than the topology 2 converter. The total harmonic distortion (THD) of input current shows much better performance in the case of topology 2 converter.

Table 4.7 Performance Comparison of the Proposed converter with recent converter (topology 2) under duty cycle variation

Duty Cycle	Proposed Converter				Recent Converter (topology 2)			
	Efficiency (%)	THD (%)	Power Factor	Voltage Gain	Efficiency (%)	THD (%)	Power Factor	Voltage Gain
0.1	97.587	40.295	0.712	0.238	80%	23.3%	0.12	0.42
0.2	99.061	57.147	0.767	0.548	90.88%	0.8%	0.39	0.84
0.3	99.288	61.188	0.748	0.854	93.46%	0.25%	0.73	1.25
0.4	99.276	50.792	0.812	1.35	94.72%	0.20%	0.94	1.62
0.5	99.158	37.724	0.901	2.08	95.25%	0.14%	0.99	1.90
0.6	99.045	25.646	0.967	3.009	95.49%	0.27%	0.95	2.08
0.7	98.719	15.753	0.969	4.147	95.99%	4.5%	0.78	2.20
0.8	98.025	7.332	0.823	5.322	95.95%	3.18%	0.40	1.69
0.9	95.292	1.535	0.342	4.02	93.06%	24.2%	0.10	0.77

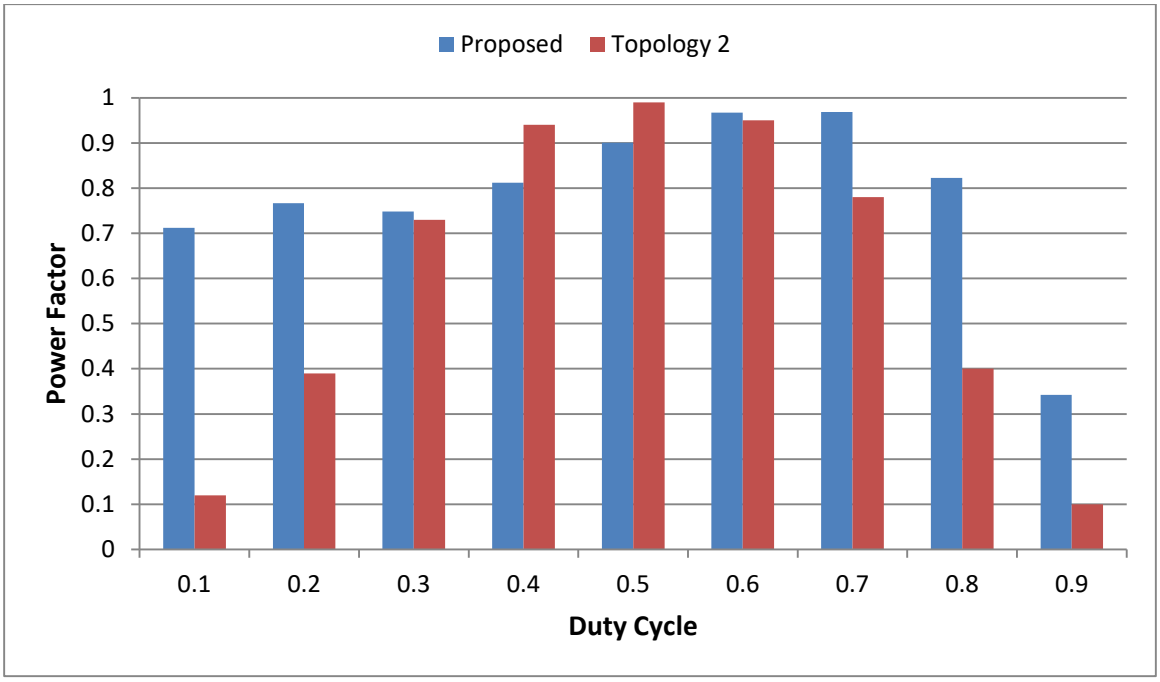


Figure 4.25: Graphical comparison of Power Factor between proposed and recent converter (topology 2) under duty cycle Variation

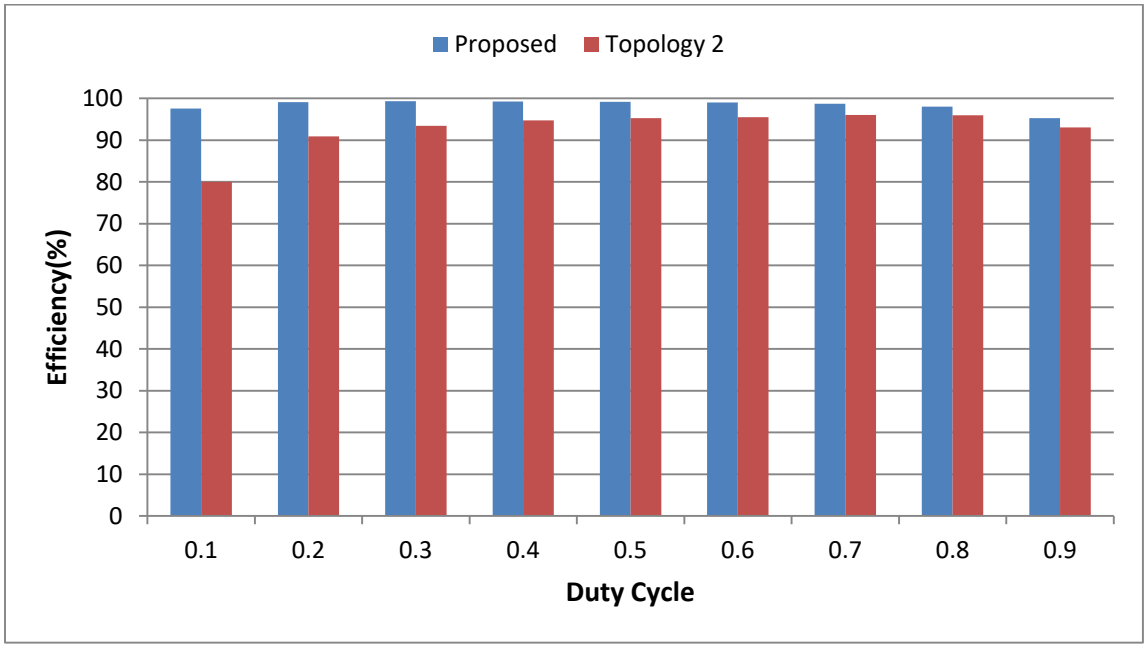


Figure 4.26: Graphical comparison of Efficiency between proposed and recent converter (topology 2) under duty cycle Variation

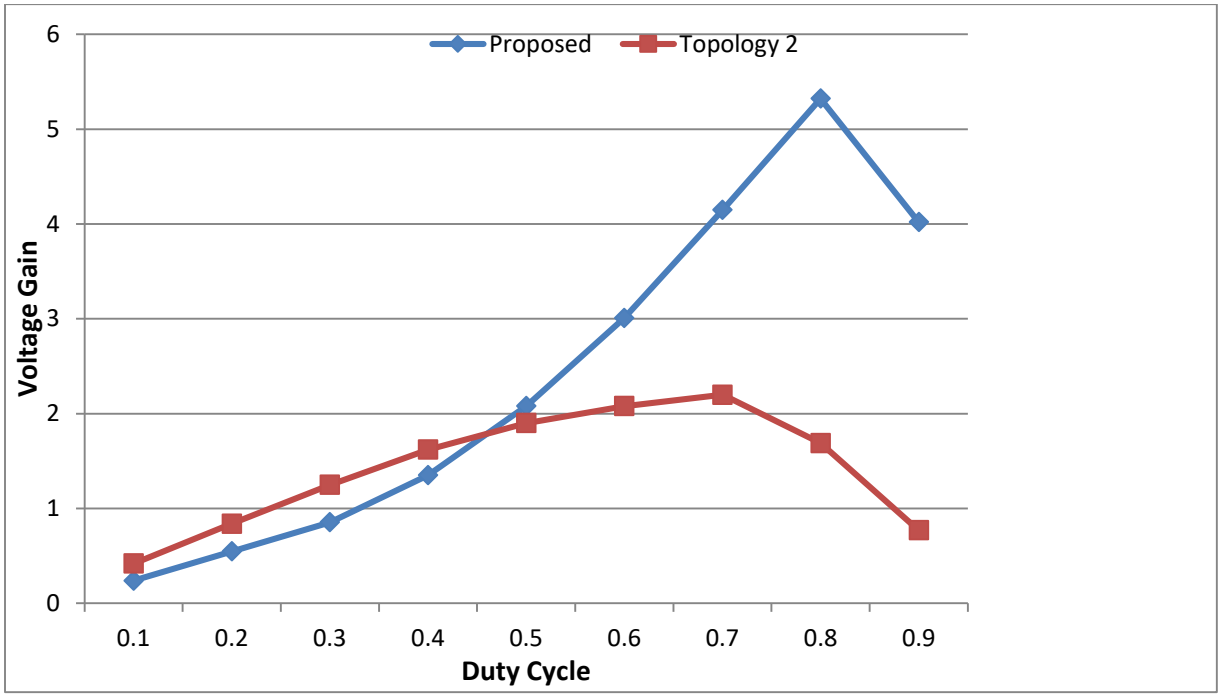


Figure 4.27: Graphical comparison of Voltage gain between proposed and recent converter (topology 2) under duty cycle Variation

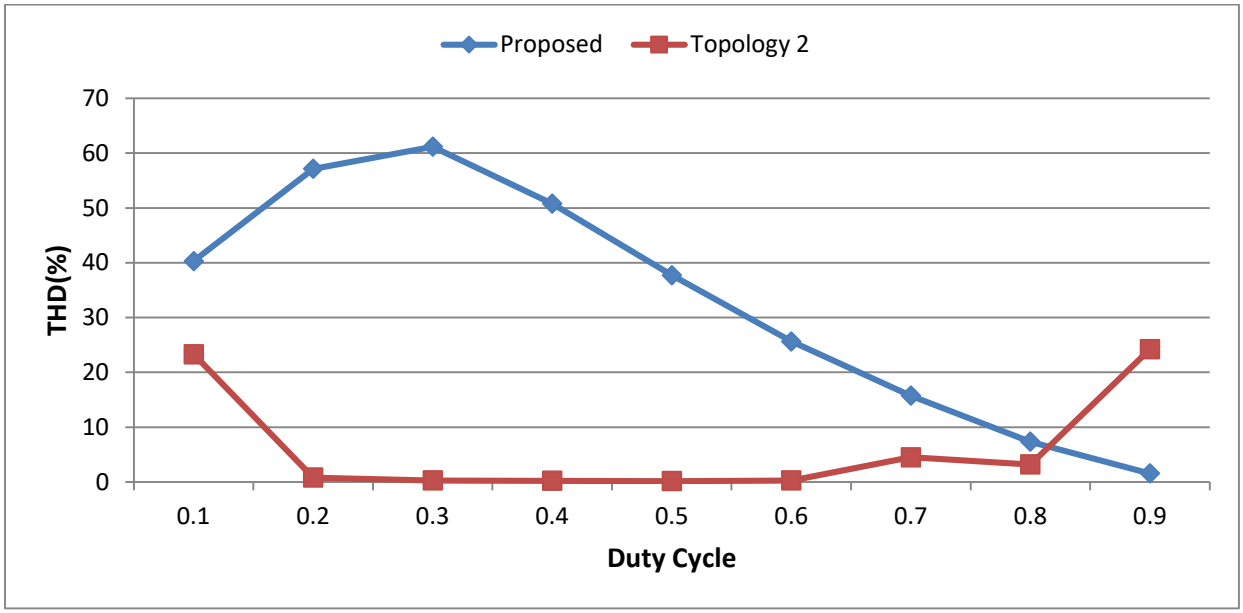


Figure 4.28: Graphical comparison of THD between proposed and recent converter (topology 2) under duty cycle Variation

Chapter 5

Feedback Controller with Proposed Converter and the Observation of Dynamic Response

5.1 Operating Principle of Single-Phase PFC

The power factor plays a vital role in deciding the power quality of electrical systems. There are numerous disadvantages of low power factor like large KVA rating of the equipment, need of greater conductor size, large copper losses, poor voltage regulation, reduced handling capacity of systems, etc. In general, the input power factor of conventional AC-DC converters is very low in open-loop operation. These result in many problems in the overall power system. Proper feedback controller design can overcome such troubles by improving the input power factor of the converters. Generally, PFC control consists of two loops. One is the inner current control loop, and the other is the outer voltage control loop. In this chapter, the feedback controller is designed for the proposed single-phase non-isolated AC-DC Buck-Boost converter, as shown in fig 5.1.

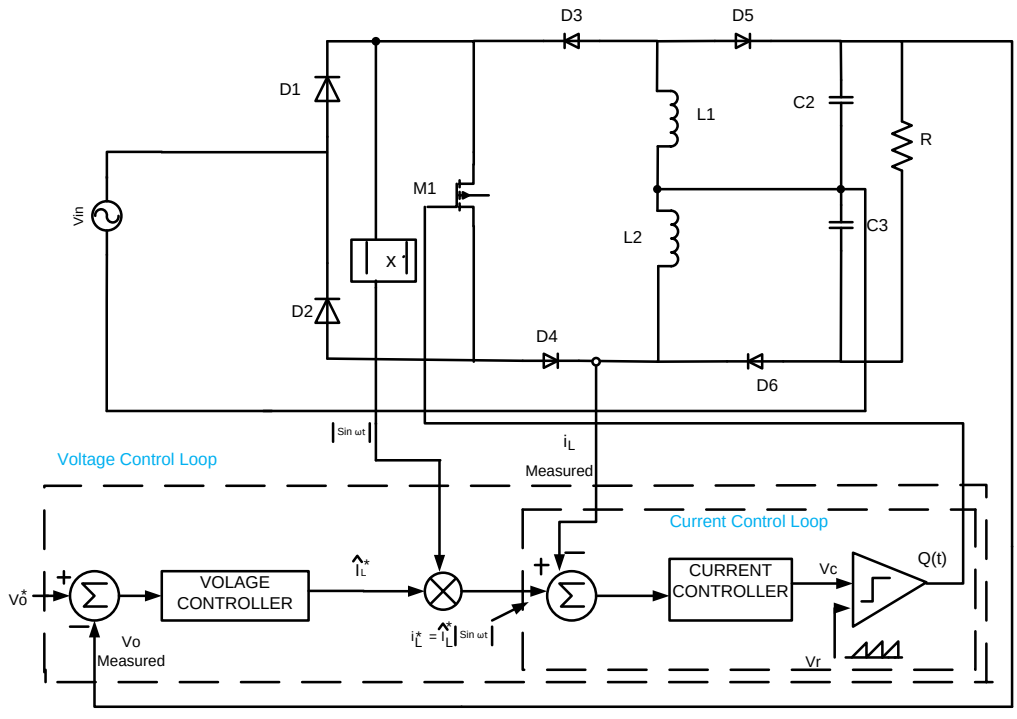


Figure 5.1: Proposed converter with the feedback controller

The proposed Buck-Boost converter consists of a MOSFET, diodes, and inductors L1 and L2. The MOSFET has been pulse width modulated at a constant switching frequency. The resulting current i_L through the inductor L2 is shaped to have the full-wave rectified waveform $\bar{\imath}_L = \hat{I}_L$ |sin ωt| similar to $|v_s(t)|$ as shown in fig 5.2

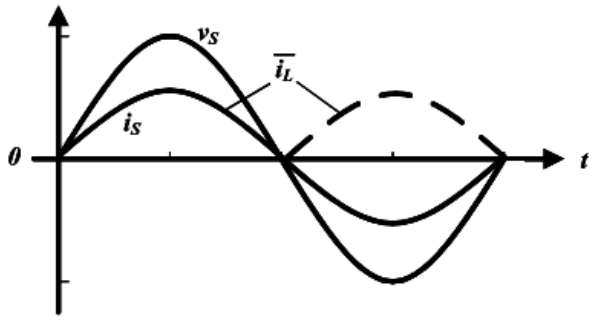


Fig 5.2: PFC waveforms

The DC transformer model of the circuit in figure 5.1 is shown in figure 5.3, where $|v_s|$ represents the absolute value of the supply voltage. In the Buck-Boost converter, the output voltage V_0 of the converter can be higher or less than the peak of supply voltage $\hat{V}_s$ depending on the duty cycle (d). The proposed converter provides an output voltage that is in the same polarity of the input signal.

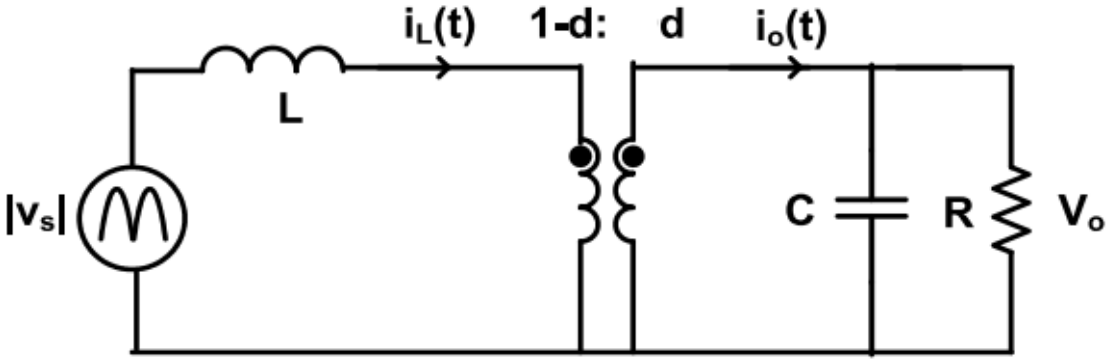


Figure 5.3: The DC Transformer model of the proposed AC-DC Buck-Boost converter

The voltage gain of the converter is given below,

$$\frac{V_O}{|V_s|} = \frac{d(t)}{1- d(t)}$$

Or, $\frac{d(t)}{1- d(t)} = \frac{V_O}{|V_{s|}}$

Or, $\frac{d(t)-1+d(t)}{d(t)+1- d(t)} = \frac{V_O-|V_s|}{V_O+|V_{s|}}$

Or, $2\ d(t) = \frac{V_O-|V_s|}{V_O+|V_{s|}}$

Or, $d(t) = \frac{1}{2}\frac{V_O-|V_s|}{V_O+|V_{s|}}$

Or, $d(t) = \frac{1}{2}\frac{V_O-\hat{V}_s\,|\sin\omega t|}{V_O+\hat{V}_s\,|\sin\omega t|}$ .....(5.1)

Where, $\hat{V}_s$ is the peak input voltage.

According to equation (5.1), a variable duty cycle is needed for keeping the input current in phase with the supply voltage.

5.2 Control of PFC

The PFC circuit for the proposed Buck-Boost converter, together with its control circuit, has been shown in figure 5.4 in block diagram form. In regulating a PFC, the primary intention is to draw a sinusoidal current, in-phase with the utility voltage.

The reference inductor current i_L^* is of the full-wave rectified form, similar to that in figure 5.2. The prerequisites on the form and the amplitude of the inductor current direct to two control loops, as shown in figure 5.4, to pulse-width modulate the switch of the proposed Buck-Boost converter.

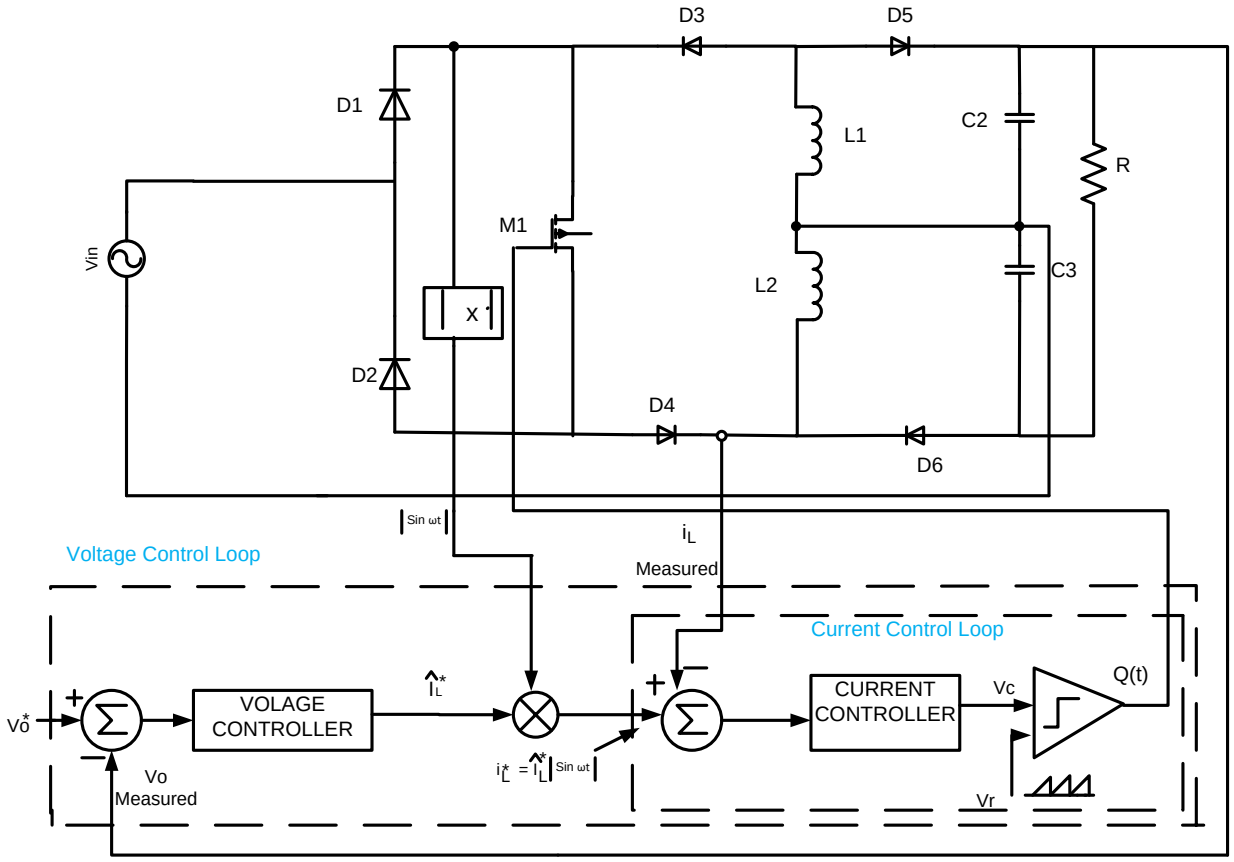


Figure 5.4: PFC Control Loops

The average inner current control loop ensues the form of i_L^* based on the template |sin ωt| provided by assessing the rectifier output voltage $|v_S(t)|$.Based on the output voltage feedback the outer voltage control loop determines the amplitude of $\hat{I}_L$ of i_L^*.The output voltage will drop below its preselected reference value V_o^*, if the inductor current is inadequate for a given load supplied by the PFC. The output voltage is measured and is taken as the feedback signal. By utilizing this feedback signal, the voltage control loop adjusts the inductor current amplitude to fetch the output voltage to its reference value. The voltage feedback control functions to control the output voltage of the PFC to the pre-selected dc voltage.

5.3 Designing the Inner Average-Current Control loop

The inner current control loop is shown within the inner dotted box in fig 5.4. To follow the reference with as little THD as possible, an average–current-mode control is used with high bandwidth, where the error between the reference $i_L^*(t)$ and the measured inductor current $i_L(t)$ is amplified by a current controller to produce the control voltage $V_c(t)$. This control voltage is compared with a ramp signal $V_r(t)$, with a peak of $\hat{V}_r$ at the switching frequency f_s in the PWM controller IC to produce the switching signal Q(t).

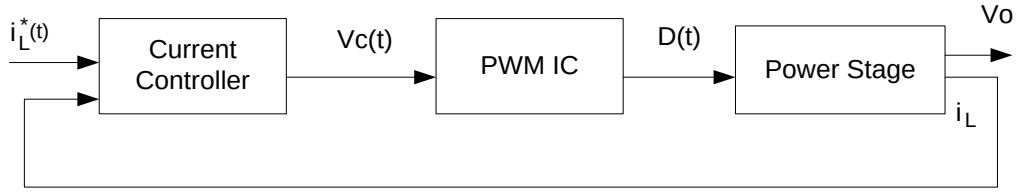


Figure 5.5: PFC Current Loop

5.4 Designing the Outer Voltage Control loop

The outer voltage control loop is needed to determine the peak,$\hat{I}_L$, of the inductor current. In this voltage loop, the bandwidth is limited to approximately 15 Hz. The reason has to do with the fact that the output voltage across the capacitor contains a component V_{oc} at twice the line-frequency. This output voltage ripple must not be corrected by the voltage loop; otherwise, it will lead to a third-harmonic distortion in the input current.

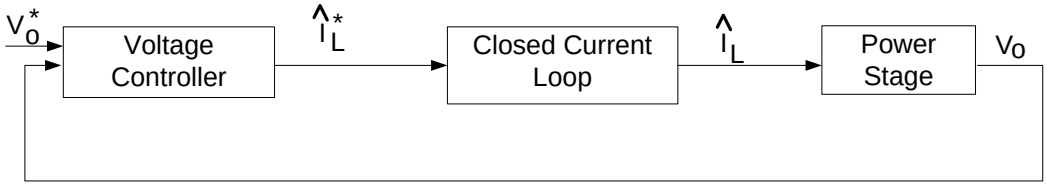


Figure 5.6: PFC Voltage Loop

5.5 Transfer function of the PFC control loops for feedback control

The current controller is realized with a PI controller.

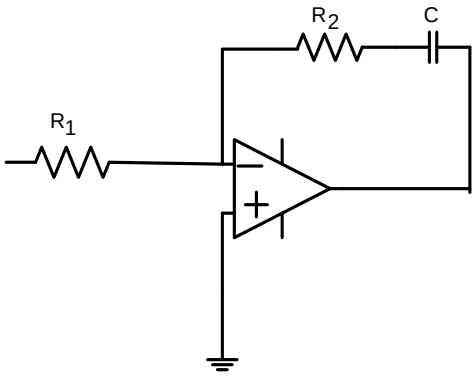


Figure 5.7: PI controller

The transfer function of the PI controller is derived as

$$G_c = -\frac{R_2}{R_1}\,\frac{(s+\frac{1}{R_2C})}{s}$$

Here, the PI controller is tuned with the values of $R_2 = 220k, R_1 = 10k$ and C = 0.022uF.So,

$$G_c = -\frac{220k}{10k}\,\frac{(s+\frac{1}{0.00484})}{s}$$

$$= \frac{-22s-4545.45}{s}$$

$$= -22 - \frac{4545.45}{s} \qquad (5.2)$$

From the above equation we find K_p = -22 and K_i = - 4545.45

The voltage controller yields the transfer function of

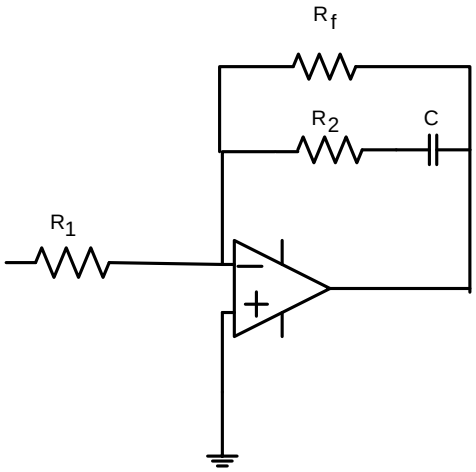


Figure 5.8: Voltage controller for feedback control

$$G_v = -\frac{\left(R_2 + \frac{1}{sC}\right) \parallel R_f}{R_1}$$

$$= -\frac{\frac{R_f R_2 sC + R_f}{R_2 sC + 1 + R_f sC}}{R_1}$$

Here,$R_1 = R_2 = 10k$,$R_f = 12K$ and C = 0.01uF.So,

$$G_v = -\frac{R_f R_1 sC + R_f}{R_1^2 sC + R_{1+} R_f R_1 sC}$$

After putting the values,

$$G_v = -\frac{1.2\ s+12000}{s+10000+1.2s}$$

$$= -\frac{1.2s+12000}{2.2s+10000}$$

5.6 Simulation with Designed Controller

Simulation has been done for the proposed converter with the feedback controller. The parameters of the circuit are given in Table 5.1. The PFC Controller is designed to obtain an average output voltage of 1000Vdc. The simulation results are given in Table 5.2. In table 5.2 the conventional converter stands for the

converter discussed in section 2.1.3. The input-output waveforms are shown in figure 5.9.

Table 5.1 Parameter Table for the feedback controller of the proposed converter

Parameters	**Value**
Input voltage (Vi) Peak	300V
Switching Frequency (S)	10kHz
Line frequency	50 Hz
Inductor (L1)	5mH
Inductor (L2,L3)	1mH
Capacitance (C1)	1uF
Capacitance (C2,C3)	330uF
Load Resistor (R)	100Ω
Gain of Voltage Sensor (V_{SEN1}, V_{SEN2})	0.00333,0.0068
Gain of Current Sensor(I_{SEN1})	0.251

Table 5.2 Results of the Simulation of the Converter with Feedback Controller for 1000 Vdc

Performance Parameters	Conventional Buck-Boost	Proposed Buck-Boost Without Feedback	Proposed Buck-Boost With Feedback
Efficiency	97%	97.5%	98.64%
Input Power Factor	0.627	0.823	0.994
Input Current THD	6.2%	7.3%	10.85%

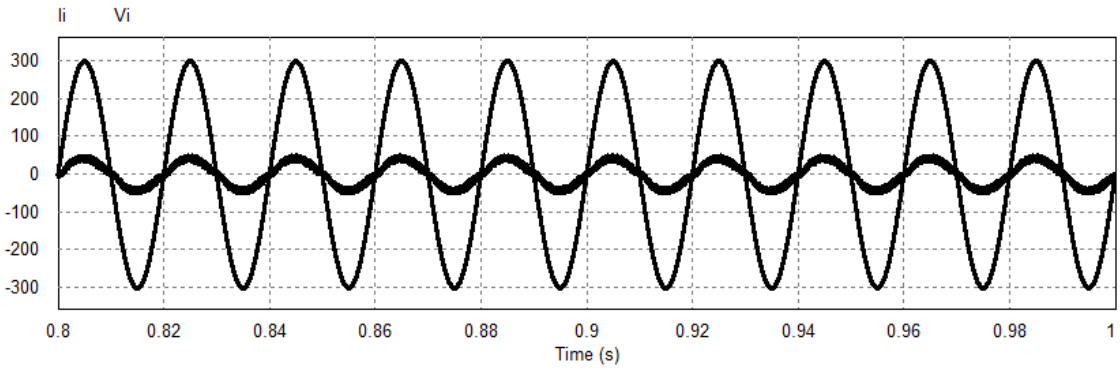


Figure 5.9(a): Waveshape of Input voltage and Input current of proposed converter with feedback

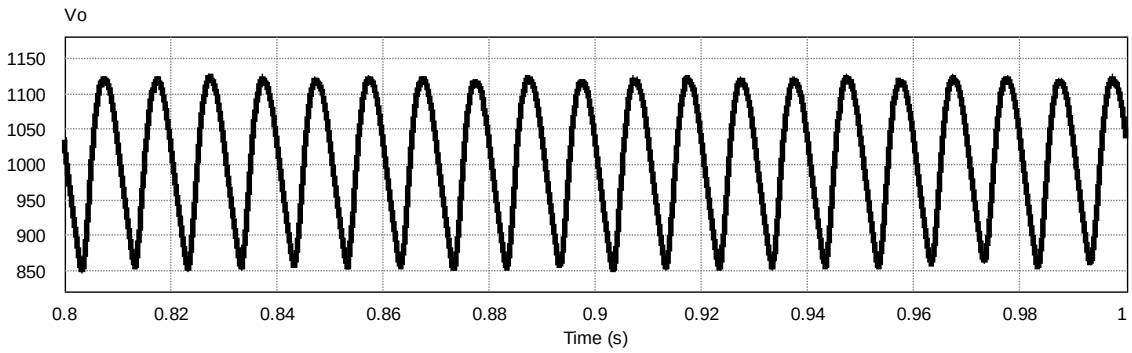


Figure 5.9(b): Waveshape of the Output voltage of the proposed converter with feedback

5.7 Dynamic Response

Dynamic response observation is a very crucial part of the AC-DC converter design. Many converters can't maintain the desired level of voltage with sudden changes in load. Thus it is essential to design such converters that can keep the desired level of output voltage with changes in load. The proposed converter exhibits a dynamically stable voltage level with sudden changes in load. To evaluate the voltage regulation and the dynamic response of the proposed converter with feedback control, the controller was set with the reference voltage to provide 1000 Vdc output with a resistive load of 200Ω. The simulation of the circuit is carried out with sudden load changes, which is given in table 5.3. The simulation result showing the output voltage is given in figure 5.11. It is evident from the

resultant waveform that, due to feedback control, the output voltage of the converter remains almost constant with the change of load.

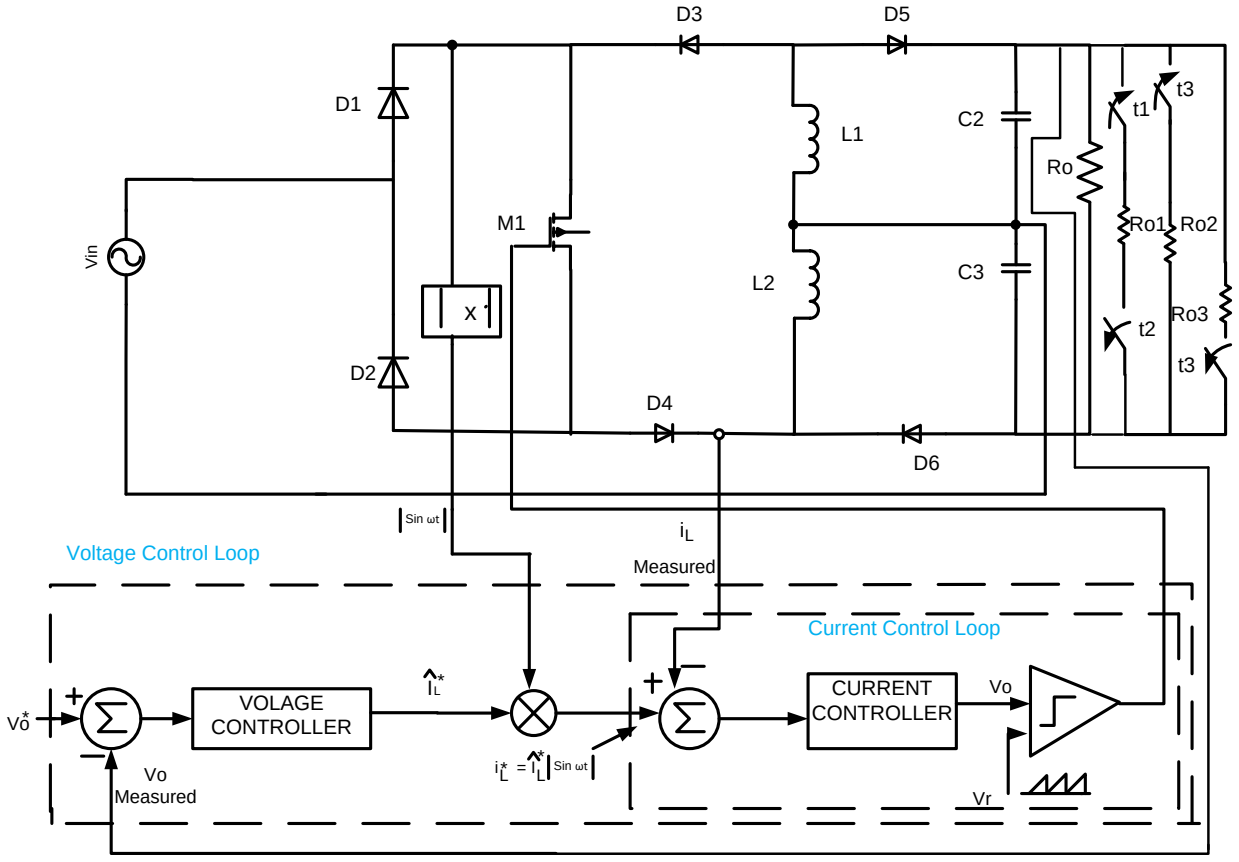


Figure 5.10: Non-isolated Single Phase AC-DC Buck-Boost Converter for Dynamic Analysis

Table 5.3 Changes in load for figure 5.10

Time (ms)	Load(Ω)
0-300	200
300-500	66.6
500-750	100
750-1000	150

Parameters for the circuit in figure 5.10

Parameters	Value
Resistor (Ro,Ro1,Ro2,Ro3)	200Ω,100Ω,600Ω,200Ω
Time (t1,t2,t3)	300 ms,500 ms,750 ms

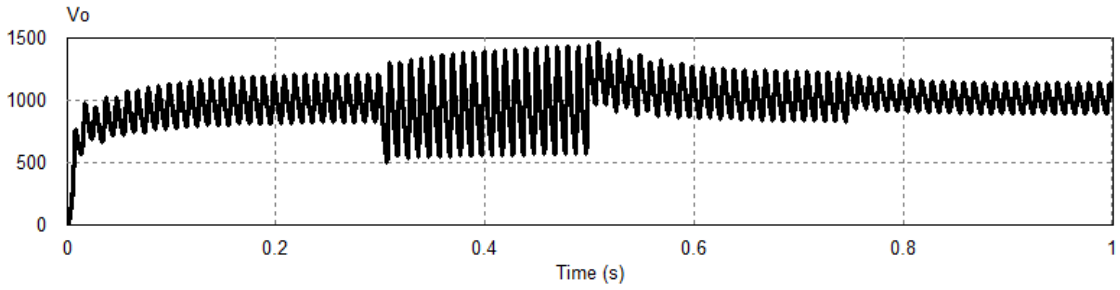


Figure 5.11: Typical waveform of output voltage for load change of the circuit of figure 5.10

5.8 Transfer function of the feedback control loops for Dynamic Response

The voltage controller and the current controller both are realized by the PI controller with separate proportional and integral gains.

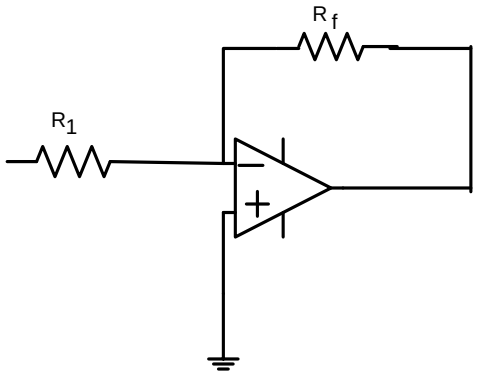


Figure 5.12: Proportional gain

The proportional gain, K_p is found as = $-\frac{R_f}{R_1}$

Here,$R_f = 82k, R_1 = 10k$

So,K_p = -8.2

The transfer function of the integral portion is,

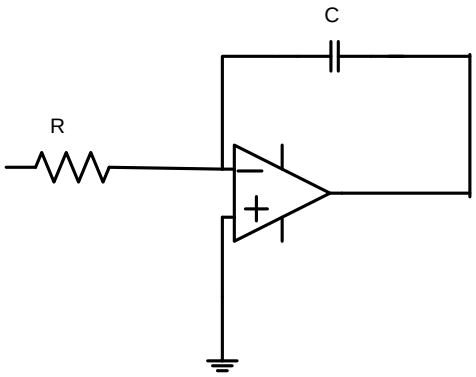


Figure 5.13: Integral gain

$$G_I = -\frac{\frac{1}{RC}}{s}$$

Here, R = 25.3k and C = 0.22uF

So,

$$G_I = -\frac{179.6}{s} \qquad (5.3)$$

From the above equation, we find K_i= -179.6.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

From the open-loop analysis, it is evident that the proposed converter provides better conversion efficiency than the conventional converter throughout the variation of the duty cycle. Input power factor of the proposed converter is less than the conventional converter for lower and higher duty cycles. By using suitable feedback control in the closed-loop system, the problem of low input power factor has been corrected. The proposed converter with the PFC controller provides a very high input power factor (0.994), which is almost close to unity. The proposed converter has lesser total harmonic distortion (THD) of the input current in comparison with the conventional one for higher duty cycles. For lower duty cycles the conventional converter shows better performance. Again, using the feedback controller, the THD of the input current is kept close to IEEE Standards for the proposed converter. In terms of voltage gain, two converters provide similar performance in buck mode, but the proposed converter has a higher boost voltage than the conventional converter. Shortly we can say that, the proposed converter shows low input power factor and higher THD for some duty ratio's in open-loop analysis, but the introduction of the feedback controller has eliminated these shortcomings. The proposed converter with the feedback controller provides higher conversion efficiency, reduced total harmonic distortion (THD) of input current, and quality power factor. The performance analysis of the proposed converter in contrast with some recent converters is done in chapter 4. From the study, it is clearly seen that the proposed converter represents better conversion efficiency than the recent converters. Some of the converters provide much lesser THD, but that comes with reduced efficiency and, in some cases, with lower input power factor. The use of a feedback controller with the proposed converter not only maintains its impressive conversion efficiency but also improves other performance parameters significantly.

6.2 Future Works

With the present state of the work, several future goals can be attained.

- Small signal analysis can be done to determine the AC equivalent circuit modeling.
- Conduction power loss at the diodes and the switching power loss at the switches can be calculated theoretically in detail. Hardware implementation can also be carried out with suitable lab setups to make this work more effective.

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