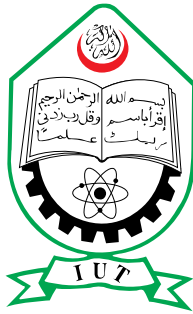


**DOCTOR OF PHILOSOPHY**  
**IN**  
**ELECTRICAL AND ELECTRONIC ENGINEERING**

**Development of Input Switched Hybrid AC to DC Converters**

**Golam Sarowar**



**Department of Electrical and Electronic Engineering**

**Islamic University of Technology (IUT)**

**Board Bazar, Gazipur-1704, Bangladesh.**

**December 30, 2016**

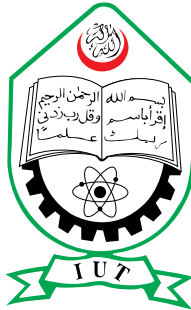
# **Development of Input Switched Hybrid AC to DC Converters**

By

Golam Sarowar

A Thesis Submitted to the Board of Examiners in Partial Fulfilment of the  
Requirements for the Degree of

## **DOCTOR OF PHILOSOPHY IN ELECTRICAL AND ELECTRONIC ENGINEERING**



Department of Electrical and Electronic Engineering

Islamic University of Technology (IUT)

Board Bazar, Gazipur-1704, Bangladesh.

December, 2016


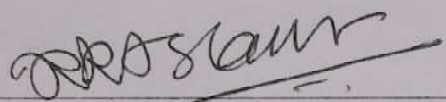
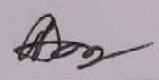
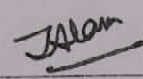
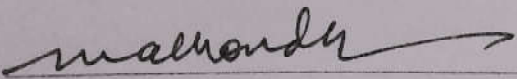
© 2016 Golam Sarowar

All Rights Reserved.

## Certificate of Approval

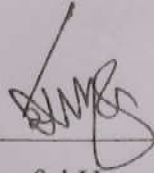
The thesis entitled “**Development of Input Switched Hybrid AC to DC Converters**” submitted by Golam Sarowar, Student No. 102701 of Academic Year 2010-2011 has been found as satisfactory and accepted as partial fulfilment of the requirement for the Degree of Doctor of Philosophy in Electrical and Electronic Engineering on December 30, 2016

### Board of Examiners

1.   
Dr. Md. Ashraful Hoque  
Professor and Head,  
Department of EEE, IUT, Gazipur, Bangladesh  
Chairman  
(Supervisor and  
Ex-officio Member)
2.   
Dr. Kazi Khairul Islam  
Professor  
Department of EEE, IUT, Gazipur, Bangladesh  
Member
3.   
Dr. Md. Ruhul Amin  
Professor  
Department of EEE, IUT, Gazipur, Bangladesh  
Member
4.   
Dr. Mohammad Jahangir Alam  
Professor  
Department of EEE, BUET, Dhaka, Bangladesh  
Member  
(External)
5.   
Dr. Mohammad Ali Choudhury  
Professor  
Department of EEE, BUET, Dhaka, Bangladesh  
Member  
(External)

## Declaration

I hereby declare that I am the sole author of this dissertation and that the work presented in it, unless otherwise referenced, is entirely my own. I also declare that the work has not been submitted, in whole or in part, to any other university as an exercise for a degree or any other qualification.



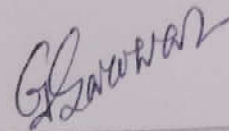
---

Md. Ashraful Hoque

Professor,

Electrical and Electronic Engineering Department,  
Islamic University of Technology (IUT).

Date: December, 2016



---

Golam Sarowar

Student No.: 102701

Academic Year: 2010-2011

Date: December, 2016

Dedicated to my family and friends

## Table of Contents

<b>Certificate of Approval</b>	<b>iii</b>
<b>Declaration</b>	<b>iv</b>
<b>Table of Contents</b>	<b>vi</b>
<b>List of Figures</b>	<b>xii</b>
<b>List of Tables</b>	<b>xx</b>
<b>List of Abbreviations of Technical Terms</b>	<b>xxiv</b>
<b>Acknowledgments</b>	<b>xxv</b>
<b>Abstract</b>	<b>xxvi</b>
<b>Chapter 1 Introduction</b>	<b>1</b>
1.1 AC to DC Converters	1
1.2 Review of AC to DC Converter	2
1.2.1 Review According to Topologies	2
1.2.2 Review According to application	6
1.2.3 Review According to Control Technique	7
1.3 Problem Identification and Research Motivation	11
1.4 Research Objectives	12
1.5 Thesis Outline	12
<b>Chapter 2 Background of the Research</b>	<b>14</b>
2.1 Current Status of the Problem	14
2.2 Performance Parameters of AC to DC Converter	20
2.3 Investigation of DC to DC converters	23
2.3.1 Hybrid Buck Converter	23
2.3.2 Hybrid Boost Converter	27
2.3.3 Hybrid Buck-Boost Converter	31
2.4 Discussions	40
<b>Chapter 3 Conventional and Proposed Single Phase Step-up AC to DC Converters</b>	<b>41</b>
3.1 Conventional Output Switched AC to DC Boost Converter	41
3.1.1 Principle of Operation	42

3.1.2	Open Loop Simulation	43
3.1.3	Ideal Voltage Gain Expression	45
3.2	Diode-Capacitor Assisted Output Switched AC to DC Boost Converter	46
3.2.1	Principle of Operation	47
3.2.2	Open Loop Simulation	48
3.2.3	Ideal Voltage Gain Expression	50
3.3	Input Switched Full-Bridge AC to DC Boost Converter	51
3.3.1	Principle of Operation	52
3.3.2	Open Loop Simulation	53
3.3.3	Ideal Voltage Gain Expression	54
3.4	Diode-Capacitor Assisted Input Switched Full-Bridge AC to DC Boost Converter	58
3.4.1	Principle of Operation	59
3.4.2	Open Loop Simulation	61
3.4.3	Ideal Voltage Gain Expression	62
3.5	Input Switched Half-Bridge AC-DC Boost Converter	63
3.5.1	Principle of Operation	64
3.5.2	Open Loop Simulation	65
3.5.3	Ideal Voltage Gain Expression	66
3.6	Modified Input Switched AC to DC Boost Converter	71
3.6.1	Principle of Operation	71
3.6.2	Open Loop Simulation	73
3.6.3	Ideal Voltage Gain Expression	74
3.7	Input Switched Coupled Capacitor Full-Bridge AC to DC Boost Converter	78
3.7.1	Principle of Operation	79
3.7.2	Open Loop Simulation	80
3.7.3	Ideal Voltage Gain Expression	82
3.8	Input Switched Coupled Capacitor Half-Bridge AC to DC Boost Converter	86



3.8.1	Principle of Operation	87
3.8.2	Open Loop Simulation	89
3.8.3	Ideal Voltage Gain Expression	90
3.9	Comparison of Conversion Efficiency	95
3.10	Discussions	96
<b>Chapter 4</b>	<b>Investigation of Step-Up Converters with Feedback</b>	<b>98</b>
4.1	Modified Input Switched AC to DC Boost Converter	98
4.1.1	Feedback Analysis	98
4.1.2	Dynamic Response	100
4.2	Input Switched Half-Bridge AC to DC Boost Converter	103
4.2.1	Feedback Analysis	103
4.2.2	Dynamic Response	106
4.3	Diode-Capacitor Assisted Output Switched AC to DC Boost Converter	108
4.3.1	Feedback Analysis	108
4.3.2	Dynamic Response	111
4.4	Diode-Capacitor Assisted Input Switched Full-Bridge AC to DC Boost Converter	113
4.4.1	Feedback Analysis	113
4.4.2	Dynamic Response	116
4.5	Input Switched Coupled Capacitor Full-Bridge AC to DC Boost Converter	118
4.5.1	Feedback Analysis	118
4.5.2	Dynamic Response	121
4.6	Input Switched Coupled Capacitor Half-Bridge AC to DC Boost Converter	123
4.6.1	Feedback Analysis	123
4.6.2	Dynamic Response	126
4.7	Discussions	128
<b>Chapter 5</b>	<b>Investigation of AC to DC Step-Down Converters</b>	<b>129</b>
5.1	Output Switched Full-Bridge AC to DC SEPIC Converter	129

5.1.1	Principle of Operation	130
5.1.2	Open Loop Simulation	131
5.1.3	Ideal Voltage Gain Expression	132
5.2	Diode-Capacitor Assisted Output Switched Full-Bridge AC to DC SEPIC Converter	133
5.2.1	Principle of Operation	134
5.2.2	Open Loop Simulation	135
5.2.3	Ideal Voltage Gain Expression	136
5.3	Output Switched Half-Bridge AC to DC SEPIC Converter	138
5.3.1	Principle of Operation	138
5.3.2	Open Loop Simulation	139
5.3.3	Ideal Voltage Gain Expression	141
5.4	Capacitor Assisted Output Switched Half-Bridge AC to DC SEPIC Converter	148
5.4.1	Principle of Operation	148
5.4.2	Open Loop Simulation	150
5.4.3	Ideal Voltage Gain Expression	151
5.5	Input Switched full-Bridge SEPIC AC to DC Converter	158
5.5.1	Principle of Operation	159
5.5.2	Open Loop Simulation	160
5.5.3	Ideal Voltage Gain Expression	161
5.6	Capacitor Assisted Input switched Full-Bridge AC to DC SEPIC Converter	168
5.6.1	Principle of Operation	169
5.6.2	Open Loop Simulation	170
5.6.3	Ideal Voltage Gain Expression	172
5.7	Input Switched Half-Bridge AC to DC SEPIC Converter	179
5.7.1	Principle of Operation	179
5.7.2	Open Loop Simulation	181
5.7.3	Ideal Voltage Gain Expression	182

5.8	Capacitor Assisted Input Switched Half-Bridge AC to DC SEPIC Converter	189
5.8.1	Principle of Operation	190
5.8.2	Open Loop Simulation	191
5.8.3	Ideal Voltage Gain Expression	192
5.9	Modified Input Switched AC to DC SEPIC Converter	200
5.9.1	Principle of Operation	200
5.9.2	Open Loop Simulation	202
5.9.3	Ideal Voltage Gain Expression	203
5.10	Comparison of Conversion Efficiency	211
5.11	Discussions	213
<b>Chapter 6</b>	<b>Investigation of Step-Down Converters with Feedback</b>	<b>214</b>
6.1	Modified input switched AC to DC SEPIC converter	214
6.1.1	Feedback Analysis	214
6.1.2	Dynamic Response	216
6.2	Capacitor Assisted Input switched Full-Bridge AC to DC SEPIC converter	219
6.2.1	Feedback Analysis	219
6.2.2	Dynamic Response	222
6.3	Capacitor Assisted Output Switched Half-Bridge AC to DC SEPIC converter	224
6.3.1	Feedback Analysis	224
6.3.2	Dynamic Response	227
6.4	Capacitor Assisted Input switched Half-Bridge AC to DC SEPIC converter	229
6.4.1	Feedback Analysis	229
6.4.2	Dynamic Response	232
6.5	Diode-Capacitor Assisted Output Switched Full-bridge AC to DC SEPIC converter	234
6.5.1	Feedback Analysis	234
6.5.2	Dynamic Response	237

6.6	Discussions	239
<b>Chapter 7</b>	<b>Design of Feedback Control</b>	<b>240</b>
7.1	The Operating Principle of PFC	240
7.2	Control of PFCs	245
7.3	AC Equivalent Circuit Modelling of Proposed Boost Converter	246
7.3.1	Small-Signal Model of Proposed Boost Converter	246
7.3.2	The Control-to-Output Transfer Function	249
7.3.3	Line-to-Output Transfer Function (Power Stage Transfer Function for Voltage Control Loop)	254
7.3.4	Power Stage Transfer Function for Current Control loop	257
7.4	Design of Inner Average Current Control Loop	258
7.4.1	PWM Controller Transfer Function	259
7.4.2	Transfer Function of the Converter for Current Control Loop	260
7.4.3	Designing the Current Controller	260
7.5	Design of Outer Voltage Control Loop	261
7.6	Controller Design	263
7.2	Simulation with Designed Controller	275
7.3	Discussions	277
<b>Chapter 8</b>	<b>Experimental Results</b>	<b>278</b>
8.1	Experimental Results for Modified Input Switched AC to DC Boost Converter	278
8.2	Experimental Results for Modified Input Switched AC to DC SEPIC Converter	286
8.3	Discussions	294
<b>Chapter 9</b>	<b>Summary and Conclusion</b>	<b>295</b>
9.1	Major Contributions of the Thesis	297
9.2	Conclusion	298
9.3	Future Work	299
	<b>References</b>	<b>300</b>
	<b>Published Works</b>	<b>311</b>

## List of Figures

Figure 1.1	General AC to DC Converter topologies.	5
Figure 2.1	Schematic diagram of single phase bridge rectifier.	14
Figure 2.2	Waveforms of circuit of Figure 2.1. (a) Input voltage-current and (b) output voltage.	15
Figure 2.3	Single phase bridge rectifier with output filter capacitor.	16
Figure 2.4	Waveforms of circuit of Figure 2.3. (a) Input voltage-current and (b) output voltage.	17
Figure 2.5	Bridge rectifier with input and output filter.	17
Figure 2.6	Waveforms of circuit of Figure 2.5. (a) Input voltage-current and (b) output voltage.	18
Figure 2.7	Two-stage AC to DC buck converter.	19
Figure 2.8	Waveforms of circuit of Figure 2.7. (a) Input voltage-current and (b) output voltage.	20
Figure 2.9	Conventional DC to DC buck converter.	23
Figure 2.10	Hybrid DC to DC buck converter.	24
Figure 2.11	Efficiency vs duty cycle of conventional and hybrid buck converter.	25
Figure 2.12	Efficiency vs switching frequency of convention and hybrid buck converter.	26
Figure 2.13	Output voltage of conventional buck converter at $D = 0.3$ .	26
Figure 2.14	Output voltage of hybrid buck converter at $D = 0.3$ .	27
Figure 2.15	Conventional DC to DC boost converter.	27
Figure 2.16	Hybrid DC to DC boost converter.	28
Figure 2.17	Efficiency vs duty cycle of conventional and hybrid boost converter.	29
Figure 2.18	Efficiency vs switching frequency of conventional and hybrid boost converter.	30
Figure 2.19	Output voltage of conventional boost converter at $D = 0.7$ .	30
Figure 2.20	Output voltage of hybrid boost converter at $D = 0.7$ .	31
Figure 2.21	Conventional DC to DC buck-boost converter.	31
Figure 2.22	Hybrid DC to DC buck-boost down converter.	32
Figure 2.23	Hybrid DC to DC buck-boost up converter.	32
Figure 2.24	Efficiency vs duty cycle of conventional and hybrid buck-boost down converter.	33
Figure 2.25	Efficiency vs duty cycle of conventional and hybrid buck-boost up converter.	34
Figure 2.26	Efficiency vs switching frequency of conventional and hybrid buck-boost down converter.	36
Figure 2.27	Output voltage of conventional buck-boost converter at $D = 0.3$ .	36
Figure 2.28	Output voltage of hybrid buck-boost down converter at $D = 0.3$ .	37
Figure 2.29	Efficiency vs switching frequency of conventional and hybrid buck-boost up converter.	38

Figure 2.30	Output voltage of conventional buck-boost converter at $D = 0.7$ .	39
Figure 2.31	Output voltage of hybrid buck-boost up converter at $D = 0.7$ .	39
Figure 3.1	Conventional output switched AC to DC boost converter.	41
Figure 3.2	Four steps of operation of the converter in Figure 3.1, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	43
Figure 3.3	Conventional output switched AC to DC boost converter with voltage labels for positive half cycle of operation.	45
Figure 3.4	Proposed diode-capacitor assisted output switched AC to DC boost converter.	46
Figure 3.5	Four steps of operation of the converter in Figure 3.4, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	48
Figure 3.6	Proposed diode-capacitor assisted output switched AC to DC boost converter with voltage labels for positive half cycle of operation.	50
Figure 3.7	Input switched full-bridge AC to DC boost converter.	51
Figure 3.8	Four steps of operation of the converter in Figure 3.7, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	53
Figure 3.9	Input switched full-bridge AC to DC boost converter with voltage labels for positive half-cycle.	54
Figure 3.10	Proposed diode-capacitor assisted input switched full-bridge AC to DC converter.	59
Figure 3.11	Four steps of operation of the converter in Figure 3.10, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	61
Figure 3.12	Input Switched half-bridge AC to DC boost converter.	63
Figure 3.13	Four steps of operation of the converter in Figure 3.12, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	65

Figure 3.14	Input Switched half-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.	66
Figure 3.15	Proposed modified input switched AC to DC Boost Converter.	71
Figure 3.16	Four steps of operation of the converter in Figure 3.15, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	72
Figure 3.17	Proposed modified input switched AC to DC Boost Converter with voltage labels for positive half cycle of operation.	74
Figure 3.18	Proposed input switched coupled capacitor full-bridge AC to DC boost converter.	78
Figure 3.19	Four steps of operation of the converter in Figure 3.18, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	80
Figure 3.20	Proposed input switched coupled capacitor full-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.	82
Figure 3.21	Proposed input switched coupled capacitor half-bridge AC to DC boost converter.	87
Figure 3.22	Four steps of operation of the converter in Figure 3.21, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	88
Figure 3.23	Proposed input switched coupled capacitor half-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.	90
Figure 3.24	Comparison of AC to DC boost converters in terms of conversion efficiency.	96
Figure 4.1	Modified input switched AC to DC boost converter with feedback control.	98
Figure 4.2	Typical input-output waveforms of the circuit of Figure 4.1.	100
Figure 4.3	Modified input switched AC to DC boost converter for dynamic analysis.	101
Figure 4.4	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.3.	103
Figure 4.5	Input switched half-bridge AC to DC boost converter with feedback control.	104
Figure 4.6	Typical input-output waveforms of the circuit of Figure 4.5.	105

Figure 4.7	Input switched half-bridge AC to DC boost converter for dynamic analysis.	106
Figure 4.8	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.7.	108
Figure 4.9	Diode-capacitor assisted output switched AC to DC boost converter with feedback control.	109
Figure 4.10	Typical input-output waveforms of the circuit of Figure 4.9.	110
Figure 4.11	Diode-capacitor assisted output switched AC to DC boost converter for dynamic analysis.	111
Figure 4.12	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.11.	113
Figure 4.13	Diode-capacitor assisted input switched full-bridge AC to DC boost converter for feedback analysis.	114
Figure 4.14	Typical input-output waveforms of the circuit of Figure 4.13.	115
Figure 4.15	Diode-capacitor assisted input switched full-bridge AC to DC boost converter for dynamic analysis.	116
Figure 4.16	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.15.	118
Figure 4.17	Input switched coupled capacitor full-bridge AC to DC boost converter for feedback analysis.	119
Figure 4.18	Typical input-output waveforms of the circuit of Figure 4.17.	120
Figure 4.19	Input switched coupled capacitor full-bridge AC to DC boost converter for dynamic analysis.	121
Figure 4.20	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.19.	123
Figure 4.21	Input switched coupled capacitor half-bridge AC to DC boost converter for feedback analysis.	124
Figure 4.22	Typical input-output waveforms of the circuit of Figure 4.21.	125
Figure 4.23	Input switched coupled capacitor half-bridge AC to DC boost converter for dynamic analysis.	126
Figure 4.24	Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.23.	128
Figure 5.1	Conventional output switched full-bridge AC to DC SEPIC converter.	129
Figure 5.2	Four steps of operation of the converter in Figure 5.1, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	131
Figure 5.3	Conventional output switched full-bridge AC to DC SEPIC converter with voltage across the components.	132
Figure 5.4	Proposed diode-capacitor assisted output switched full-bridge AC to DC converter.	134
Figure 5.5	Four steps of operation of the converter in Figure 5.4, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle	135



	(c) circuit when the switch is ON during negative half cycle	
	(d) circuit when the switch is OFF during negative half cycle of line frequency.	
Figure 5.6	Proposed diode-capacitor assisted output switched full-bridge AC to DC converter with voltage across the components.	137
Figure 5.7	Output switched half-bridge AC to DC SEPIC Converter.	138
Figure 5.8	Four steps of operation of the converter in Figure 5.7, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	139
Figure 5.9	Output switched half-bridge AC to DC SEPIC Converter for positive half cycle of operation.	141
Figure 5.10	Proposed capacitor assisted output switched half-bridge AC to DC SEPIC converter.	148
Figure 5.11	Four steps of operation of the converter in Figure 5.10, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	149
Figure 5.12	Proposed capacitor assisted output switched half-bridge AC to DC SEPIC converter with voltage across the components.	151
Figure 5.13	Conventional input switched full-bridge AC to DC SEPIC converter.	158
Figure 5.14	Four steps of operation of the converter in Figure 5.13, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	160
Figure 5.15	Conventional input switched full-bridge AC to DC SEPIC converter for positive cycle of operation.	161
Figure 5.16	Proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter.	169
Figure 5.17	Four steps of operation of the converter in Figure 5.16, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	170
Figure 5.18	Proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter with voltage across the components.	172
Figure 5.19	Input switched half-bridge AC to DC SEPIC converter.	179

Figure 5.20	Four steps of operation of the converter in Figure 5.19, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	181
Figure 5.21	Input switched half-bridge AC to DC SEPIC converter.	182
Figure 5.22	Capacitor assisted input switched AC to DC SEPIC converter.	190
Figure 5.23	Four steps of operation of the converter in Figure 5.22, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency	191
Figure 5.24	Capacitor assisted input switched AC to DC SEPIC converter.	193
Figure 5.25	Modified input switched AC to DC SEPIC converter.	200
Figure 5.26	Four steps of operation of the converter in Figure 5.25, (a) circuit when the switch is ON during positive half cycle (b) circuit when the switch is OFF during positive half cycle (c) circuit when the switch is ON during negative half cycle (d) circuit when the switch is OFF during negative half cycle of line frequency.	202
Figure 5.27	Modified input switched AC to DC SEPIC converter with voltage across the components.	203
Figure 5.28	Comparison of AC to DC SEPIC converters in terms of conversion efficiency.	211
Figure 6.1	Modified input switched AC to DC SEPIC converter with feedback control.	214
Figure 6.2	Typical input-output waveforms of the circuit of Figure 6.1.	216
Figure 6.3	Modified input switched AC to DC SEPIC converter for dynamic analysis.	217
Figure 6.4	Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.3.	219
Figure 6.5	Capacitor assisted input switched full-bridge AC to DC SEPIC converter with feedback control.	220
Figure 6.6	Typical input-output waveforms of the circuit of Figure 6.5.	221
Figure 6.7	Capacitor assisted input switched full-bridge AC to DC SEPIC converter for dynamic analysis.	222
Figure 6.8	Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.7.	224
Figure 6.9	Capacitor assisted output switched half-bridge AC to DC SEPIC converter with feedback control.	225
Figure 6.10	Typical input-output waveforms of the circuit of Figure 6.9.	226
Figure 6.11	Capacitor assisted output switched half-bridge AC to DC SEPIC converter for dynamic analysis.	227

Figure 6.12	Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.11.	229
Figure 6.13	Capacitor assisted input switched half-bridge AC to DC SEPIC converter with feedback control.	230
Figure 6.14	Typical input-output waveforms of the circuit of Figure 6.13.	231
Figure 6.15	Capacitor assisted input switched half-bridge AC to DC SEPIC converter for dynamic analysis.	232
Figure 6.16	Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.15.	234
Figure 6.17	Diode-capacitor assisted output switched AC to DC converter with feedback control.	235
Figure 6.18	Typical input-output waveforms of the circuit of Figure 6.17.	236
Figure 6.19	Diode-capacitor assisted output switched AC to DC converter for dynamic analysis.	237
Figure 6.20	Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.19.	239
Figure 7.1	Diode-capacitor assisted output switched AC to DC Boost Converter.	240
Figure 7.2	PFC waveforms.	241
Figure 7.3	The DC transformer model of the diode-capacitor assisted output switched AC to DC Boost Converter.	241
Figure 7.4	Required variable duty cycle for the PFC controller.	242
Figure 7.5	MATLAB code to generate the variable duty cycle of Figure 7.4.	243
Figure 7.6	PFC control loops.	245
Figure 7.7	Linearizing the switching power-pole.	246
Figure 7.8	Derived small signal model of the diode-capacitor assisted output switched AC to DC Boost Converter.	249
Figure 7.9	Reduced small signal model for deriving control to output transfer function.	250
Figure 7.10	Circuit after source transformation.	250
Figure 7.11	Circuit after impedance transformation.	250
Figure 7.12	The equivalent Thevenin's model of the circuit.	253
Figure 7.13	The reduced model to derive line to output transfer function.	254
Figure 7.14	The impedance transformed model.	255
Figure 7.15	The reduced small signal model for current control loop.	257
Figure 7.16	Simplified current control loop for PFC.	259
Figure 7.17	PWM waveforms.	260
Figure 7.18	Voltage control loop for PFC.	262
Figure 7.19	Op-amp circuit to implement current control loop.	266
Figure 7.20	Op-amp circuit to implement voltage control loop.	273
Figure 7.21	Diode capacitor assisted output switched AC to DC boost converter with PFC control.	276
Figure 7.22	Typical input-output waveforms of the PFC controlled converter of Figure 7.21.	277

Figure 8.1	The equivalent circuit of experimental set up done in Laboratory on single phase modified input switched AC to DC boost converter.	278
Figure 8.2	The experimental set up done in laboratory for proposed boost converter.	279
Figure 8.3	Waveforms of Oscilloscope for modified input switched AC to DC converter for 25% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	281
Figure 8.4	Waveforms of Oscilloscope for modified input switched AC to DC converter for 50% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	283
Figure 8.5	Waveforms of Oscilloscope for modified input switched AC to DC converter for 75% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	285
Figure 8.6	The equivalent circuit of experimental set up done in Laboratory on single phase modified input switched AC to DC SEPIC converter.	286
Figure 8.7	The experimental set up done in laboratory for SEPIC converter.	287
Figure 8.8	Waveforms of Oscilloscope for modified input switched AC to DC converter for 25% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	289
Figure 8.9	Waveforms of Oscilloscope for modified input switched AC to DC converter for 50% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	291
Figure 8.10	Waveforms of Oscilloscope for modified input switched AC to DC converter for 75% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input current-voltage.	293

## List of Tables

Table 2.1	Harmonic current distortion. (IEEE 519)	22
Table 2.2	Efficiency vs duty cycle of conventional and hybrid buck converter.	24
Table 2.3	Efficiency vs switching frequency of convention and hybrid buck converter.	25
Table 2.4	Efficiency vs duty cycle of conventional and hybrid boost converter.	28
Table 2.5	Efficiency vs switching frequency of conventional and hybrid boost converter.	29
Table 2.6	Efficiency vs duty cycle of conventional and hybrid buck-boost down converter.	33
Table 2.7	Efficiency vs duty cycle of conventional and hybrid buck-boost up converter.	34
Table 2.8	Efficiency vs switching frequency of conventional and hybrid buck-boost down converter.	35
Table 2.9	Efficiency vs switching frequency of conventional and hybrid buck-boost up converter.	38
Table 3.1	Parameters of the converter of Figure 3.1.	44
Table 3.2	Simulation results of the converter of Figure 3.1.	44
Table 3.3	Average output voltage vs duty cycle of the converter of Figure 3.1.	46
Table 3.4	Parameters of the converter of Figure 3.4.	49
Table 3.5	Simulation results of the converter of Figure 3.4.	49
Table 3.6	Average output voltage vs duty cycle of the converter of Figure 3.4.	51
Table 3.7	Parameters of the converter of Figure 3.7.	53
Table 3.8	Simulation results of the converter of Figure 3.7.	54
Table 3.9	Average output voltage vs duty cycle of the converter of Figure 3.7.	58
Table 3.10	Parameters of the converter of Figure 3.10.	61
Table 3.11	Simulation results of the converter of Figure 3.10.	62
Table 3.12	Average output voltage vs duty cycle of the converter of Figure 3.10.	63
Table 3.13	Parameters of the converter of Figure 3.12.	65
Table 3.14	Simulation results of the converter of Figure 3.12.	66
Table 3.15	Average output voltage vs duty cycle of the converter of Figure 3.12.	70
Table 3.16	Parameters of the converter of Figure 3.15.	73
Table 3.17	Simulation results of the converter of Figure 3.15.	73
Table 3.18	Average output voltage vs duty cycle of the converter of Figure 3.15.	78
Table 3.19	Parameters of the converter of Figure 3.18.	81
Table 3.20	Simulation results of the converter of Figure 3.18.	81
Table 3.21	Average output voltage vs duty cycle of the converter of Figure 3.18.	86

Table 3.22	Parameters of the converter of Figure 3.21.	89
Table 3.23	Simulation results of the converter of Figure 3.21.	89
Table 3.24	Average output voltage vs duty cycle of the converter of Figure 3.21.	94
Table 3.25	Comparison of Single phase AC-DC Boost Converters.	95
Table 4.1	Parameters of the circuit of Figure 4.1.	99
Table 4.2	Simulation results of the circuit of Figure 4.1.	99
Table 4.3	Changes in load for Figure 4.3.	101
Table 4.4	Parameters of the circuit of Figure 4.3.	102
Table 4.5	Parameters of the circuit of Figure 4.5.	104
Table 4.6	Simulation results of the circuit of Figure 4.5.	105
Table 4.7	Changes in load for Figure 4.7.	106
Table 4.8	Parameters of the circuit of Figure 4.7.	107
Table 4.9	Parameters of the circuit of Figure 4.9.	109
Table 4.10	Simulation results of the circuit of Figure 4.9.	110
Table 4.11	Changes in load for Figure 4.11.	111
Table 4.12	Parameters of the circuit of Figure 4.11.	112
Table 4.13	Parameters of the circuit of Figure 4.13	114
Table 4.14	Simulation results of the circuit of Figure 4.13.	115
Table 4.15	Changes in load for Figure 4.15.	116
Table 4.16	Parameters of the circuit of Figure 4.15.	117
Table 4.17	Parameters of the circuit of Figure 4.17.	119
Table 4.18	Simulation results of the circuit of Figure 4.13.	120
Table 4.19	Changes in load for Figure 4.19.	121
Table 4.20	Parameters of the circuit of Figure 4.19.	122
Table 4.21	Parameters of the circuit of Figure 4.21.	124
Table 4.22	Simulation results of the circuit of Figure 4.21.	125
Table 4.23	Changes in load for Figure 4.23.	126
Table 4.24	Parameters of the circuit of Figure 4.23.	127
Table 5.1	Parameters of the converter of Figure 5.1.	131
Table 5.2	Simulation results of the converter of Figure 5.1.	132
Table 5.3	Average output voltage vs duty cycle of the converter of Figure 5.1.	133
Table 5.4	Parameters of the converter of Figure 5.4.	136
Table 5.5	Simulation results of the converter of Figure 5.4.	136
Table 5.6	Average output voltage vs duty cycle of the converter of Figure 5.4.	137
Table 5.7	Parameters of the converter of Figure 5.7.	140
Table 5.8	Simulation results of the converter of Figure 5.7.	140
Table 5.9	Average output voltage vs duty cycle of the converter of Figure 5.7.	148
Table 5.10	Parameters of the converter of Figure 5.10.	150
Table 5.11	Simulation results of the converter of Figure 5.10.	150
Table 5.12	Average output voltage vs duty cycle of the converter of Figure 5.10.	158
Table 5.13	Parameters of the converter of Figure 5.13.	160
Table 5.14	Simulation results of the converter of Figure 5.13.	161

Table 5.15	Average output voltage vs duty cycle of the converter of Figure 5.13.	168
Table 5.16	Parameters of the converter of Figure 5.16.	171
Table 5.17	Simulation results of the converter of Figure 5.16.	171
Table 5.18	Average output voltage vs duty cycle of the converter of Figure 5.16.	179
Table 5.19	Parameters of the converter of Figure 5.19.	181
Table 5.20	Simulation results of the converter of Figure 5.19.	182
Table 5.21	Average output voltage vs duty cycle of the converter of Figure 5.19.	189
Table 5.22	Parameters of the converter of Figure 5.22.	192
Table 5.23	Simulation results of the converter of Figure 5.22.	192
Table 5.24	Average output voltage vs duty cycle of the converter of Figure 5.22.	200
Table 5.25	Parameters of the converter of Figure 5.25.	202
Table 5.26	Simulation results of the converter of Figure 5.25.	203
Table 5.27	Average output voltage vs duty cycle of the converter of Figure 5.25.	210
Table 5.28	Comparison of Single Phase AC-DC SEPIC Converters	212
Table 6.1	Parameters of the circuit of Figure 6.1.	215
Table 6.2	Results of the feedback of the modified input switched AC to DC SEPIC converter.	215
Table 6.3	Changes in load for Figure 6.3.	217
Table 6.4	Parameters of the circuit of Figure 6.3.	218
Table 6.5	Parameters of the circuit of Figure 6.5.	220
Table 6.6	Results of the feedback of the proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter.	221
Table 6.7	Changes in load for Figure 6.7.	222
Table 6.8	Parameters of the circuit of Figure 6.7.	223
Table 6.9	Parameters of the circuit of Figure 6.9.	225
Table 6.10	Results of the feedback of the capacitor assisted output switched half-bridge AC to DC SEPIC converter.	226
Table 6.11	Changes in load for Figure 6.11.	227
Table 6.12	Parameters of the circuit of Figure 6.11.	228
Table 6.13	Parameters of the circuit of Figure 6.13.	230
Table 6.14	Results of the feedback of the capacitor assisted input switched half-bridge AC to DC SEPIC converter.	231
Table 6.15	Changes in load for Figure 6.15.	232
Table 6.16	Parameters of the circuit of Figure 6.15.	233
Table 6.17	Parameters of the circuit of Figure 6.17.	235
Table 6.18	Results of the feedback of the diode-capacitor assisted output switched AC to DC SEPIC converter.	236
Table 6.19	Changes in load for Figure 6.19.	237
Table 6.20	Parameters of the circuit of Figure 6.19.	238
Table 7.1	Parameters of the converter of Figure 7.21.	275
Table 7.2	Results of the simulation of the converter with feedback control.	276

Table 8.1	Parameters of circuit of Figure 8.1 for experimental set up.	279
Table 8.2	Results of the experimentation of the modified input switched AC to DC boost converter.	285
Table 8.3	Comparison of performance parameters of the modified input switched AC to DC boost converter for $D=0.75$ .	286
Table 8.4	Parameters of circuit of Figure 8.6 for experimental set up.	287
Table 8.5	Results of the experimentation of the modified input switched AC to DC SEPIC converter.	293
Table 8.6	Comparison of performance parameters of the modified input switched AC to DC boost converter for $D=0.50$ .	294



## **List of Abbreviations of Technical Terms**

<b>SMPS</b>	Switch Mode Power Supply
<b>IGBT</b>	Insulated Gate Bipolar Transistor
<b>THD</b>	Total Harmonic Distortion
<b>PF</b>	Power Factor
<b>CCM</b>	Continuous Conduction Mode
<b>DCM</b>	Discontinuous Conduction Mode
<b>PWM</b>	Pulse Width Modulation
<b>RMS</b>	Root Mean Square
<b>fs</b>	Switching Frequency
<b>D</b>	Duty Cycle
<b>Ton</b>	Turn on Time
<b>Toff</b>	Turn off Time
<b>SEPIC</b>	Single Ended Primary Inductor Converter
<b>LED</b>	Light Emitting Diode
<b>PFC</b>	Power Factor Correction
<b>IC</b>	Integrated Circuit
<b>DSP</b>	Digital Signal Processor
<b>UPS</b>	Uninterruptable Power Supply
<b>EMI</b>	Electromagnetic Interference
<b>PFi</b>	Input Power Factor

## **Acknowledgments**

I have my sincerest appreciation for the help, assistance and advice that many people have given me on countless occasions during the course of my graduate work. First, I would like to express my profound gratitude to Professor Dr. Md. Ashraful Hoque for his guidance, support and encouragement. He has been a wonderful advisor, who has continuously inspired and motivated me to complete many challenging research assignments. The other members of my doctoral committee, Professor Dr. Md. Shahid Ullah, Professor Dr. Kazi Khairul Islam and Professor Dr. Mohammad Ali Choudhury have given their thoughtful suggestions, and I would like to thank them all for that. Acknowledgement is due to EEE department of Islamic University of Technology for supporting my Ph. D studies and this research work.

I am very thankful to my wife for her patience, understanding and support throughout my entire graduate life. She has always been there when I needed her, helping me in all possible ways through constant inspirations and encouragement. She has never hesitated to sacrifice her weekends and holidays for the cause of my study and research. My parents, brothers and sister, have done so much for me from my very childhood until this point, that they deserve the very best of my appreciation. Were it not for my father's guidance, my mother's hard work and the other members' endurance, it would not be possible for me to come this far. My parent-in-law along with other in-laws have also contributed a great deal by constantly encouraging me and helping me in the pursuit of knowledge. I would like to extend my special thanks to them. I would also like to acknowledge the support from my colleagues who have been a constant source of inspiration all along this work.

Above all, I would like to glorify Almighty ALLAH Subhanahu Wa Ta'la for giving me knowledge and patience to carry out this work.

## Abstract

The thesis presents novel circuit topologies for single phase AC to DC conversion. The converters are used for step up, step down and step up/down applications. AC to DC converter with high conversion efficiency is of critical importance in applications in renewable energy sources or power supplies for modern equipment. Unavoidable system disturbances like parameter variations, effect of sudden load change and other noises are resolved by designing precise feedback control for both step-up and step-down applications. The proposed single phase rectifiers are designed to maintain high conversion efficiency at extremely low and high duty cycles. In order to tackle the deviation from the ideal behavior of the gain and attenuation property of the converter at extreme condition, hybrid diode-capacitor networks are introduced. The network provides voltage step-up or step-down prior to DC to DC or AC to DC conversion. In addition, in order to take the advantage of input switching, new topologies are designed by paralleling the outputs of two AC to DC conversion paths of positive and negative half cycles of input AC to output DC. A common single bi-directional switch is used for both positive and negative half cycle conversion. Direct input current switching ensures the current displacement with input voltage to be nearly unity. This control makes it easy to maintain high input power factor and low input current THD. Since the topologies used for DC to DC conversion cannot be used directly for AC to DC conversion, the topologies are modified before applying in AC to DC conversion. The modification causes high component count and circuit complexity. So attempt is taken to design not only using modified DC to DC topologies but also conventional input switched converter is modified by shifting the switch location and using split capacitors at the output. The investigated new single phase AC to DC converters offer higher conversion efficiency which is validated by simulation. Common two loop feedback control strategy for PFC is used with proposed converters to improve the input power factor and to keep the input current THD within prescribed limits. The proposed input switched boost and SEPIC converters perform better compared to conventional ones. Among the proposed converters modified input switched AC to DC boost and SEPIC converter offered best result.

Converters with best performance in the simulation have been implemented in the laboratory experimentations. The test results validated the performances of the proposed converters with the simulation results.

# Chapter 1

## Introduction

### 1.1 AC to DC Converters

Single phase AC to DC converter are common in modern day power supplies. The converter forms interface between the utility power supply and electronic equipment connected to them. The process of rectification used to be simple, but recently, rectifiers have become sophisticated, and are considered as systems rather than circuits [1]. Conventional Single-phase AC-DC converter in bridge configuration suffer from problems of distorted non-sinusoidal input current and low input power factor [1-12]. Because these converters absorb energy from the AC line only when the rectified line voltage is higher than the DC link voltage. To solve the harmonic pollutions caused by AC-DC converters, various methods have been proposed. One simple method is to use the input filter. But inductor and capacitor required in such solution are large. Though it keeps THD in tolerable limit the power factor remains low. To overcome the problem, a number of power factor correction (PFC) AC-DC converters have been proposed and developed [13-26].

Generally, power factor correction (PFC) techniques are implemented by using two power-processing stages. The input PFC stage improves the power factor as well as maintains a constant DC link voltage. The most common PFC stage employ a Boost converter [16, 18-20]. Buck, Buck-Boost, Ćuk, SEPIC and ZETA converters are also employed for the same purpose with different input/output voltage gain relationships. In output stage, high frequency DC-DC converter [27, 28] acts as high frequency current/voltage chopper which is reflected at the input as high frequency chopped AC current. This input current is then filtered by a small filter to obtain near sinusoidal input current with high power factor [29, 30]. This is possible only when the output is full wave pulsed dc. To obtain quality power, the output is desired to be dc with low ripple. As a result, large output capacitor filter is necessary. This output filter with large capacitance draws pulsed current, and the pulsed ac current is reflected to the input side. Thus additional control is required to maintain sinusoidal shape of the input current.

The unidirectional switch used in the DC-DC converters for boost-regulated AC-DC conversion must operate in critical mode [31, 32] that is, the power switch should be turned ON at the instant of zero current in the boost diode. Thus variable switching frequency operation of the DC-DC converter is required due to load or the input voltage changes. Another approach for boost-regulated rectifier involves controlling to a constant level the average current of the boost diode. In order to keep the average current constant through the boost diode, the duty cycle must be modulated over the line cycle. Bridge-less configurations [13, 32-43] and two-diode, two-switch rectifiers are also reported in literatures for AC-DC conversion having the features of boost-regulated rectifier.

The reported bridgeless single phase ac-dc converters use more than one unidirectional switches or one bidirectional switch composed of two unidirectional switches anti-parallel with two diodes. The efficiency varies with the change in duty cycle [33]. The efficiency tends to reduce at extremely high and extremely low duty cycle.

Most devices today operates in very low DC voltage. Usually a transformer is used to reduce the voltage and then AC-DC converter is used. Efficiency suffers due to the use of the transformer. Transformer-less control techniques suffers from a low input power factor and distorted input current. Therefore the scope is there to design a transformer-less AC-DC converter adopting hybrid circuitry [44] and suitable feedback control technique to achieve improved efficiency, high input power factor and low THD for input current.

## **1.2 Review of AC to DC Converter**

The reported works in AC to DC conversion can be reviewed in accordance to their topologies, applications and control strategies.

### **1.2.1 Review According to Topologies**

In static AC to DC conversion diode rectifiers are used in common. There are two types of diode rectifiers: single and multi-phase. The single phase rectifiers are used in low to medium power conversion. The multi-phase mainly three phase AC to DC converters are used to deal with large power. The pulsating output voltage of the rectifier is harmful

for the devices. The output voltage is regulated using capacitive filters. Due to the filter input current is distorted causing a degradation in power quality. In general, the performance of the rectifiers are evaluated in terms of input power factor and input current THD. Since the rectifier unit forms the interface between the load and the utility, the main focus of the research is to improve the quality of power at the point of coupling. Several PFC topologies have been introduced to improve the power quality. With an emphasis on input PFC and input current THD, major rectifier topologies are reviewed as follows:

There are two types of single phase uncontrolled rectification: half-wave and full-wave. In low power applications the half-wave rectifiers are used. The half wave rectifiers caused magnetic saturations to the equipment that supplies the rectifier due to non-zero average input current. This problem is avoided in full-wave ratification as the average input current is zero. It is also easier to regulate the output voltage in case of full-wave rectification, since the output ripple is less compared to half-wave rectifiers. The unity power factor and near sinusoidal input current can be achieved by using different types filters: passive, hybrid and active.

The passive filter technique is the simple solution for the diode bridge rectifier. The reactive elements (line frequency) are connected both in the source and the load side of the rectifiers [24, 33-37]. The use of the passive filter is common due to the simplicity and reliability. These are also insensitive to noise and surges and at times reduces them. The high frequency electromagnetic interference is also absent in these techniques. The absence of switching devices reduces the loss. The research is focused for innovative solutions instead of passive filter techniques due to their size and poor dynamic response. It is also difficult to tune them and they lack the ability to regulate the voltage. As a result the input power factor is poor and conversion efficiency also suffers.

In hybrid filter techniques, to achieve improved power quality semiconductor switches are introduced with the diode bridge. Integration of the switch is done in three different ways: single stage for low power application, two stage for high power application and direct power transfer for improved efficiency [37-38]. In any of the cases, the DC to DC converter unit can be used either in between the rectifier and load or between the

supply and the rectifier. The converters which use the second approach is known as input switched converters. The DC to DC unit can be used for step-up, step-down or step up/down applications. The most common topology used for the power factor correction is the step-up boost converter [39-42]. For step-down applications buck converters can be used and in order to have the freedom in specifying output voltage buck-boost, SEPIC, Ćuk converters can be used. Though the boost converters are commonly used for PFC, other converters like buck, buck-boost, SEPIC, Ćuk, Zeta, flyback, push-pull etc. can also be used. The preference is given to SEPIC and Ćuk over the buck-boost converter since they offer advantages like isolation, inrush current limitation during start-up and overload conditions, lower input current ripple and low electromagnetic interference in discontinuous conduction mode topologies [23, 42-45]. In applications where the isolation is needed between the input and output side, the flyback and push-pull configurations are used.

For input switched converters bidirectional switch is used. The switch comprises of a diode bridge and a semiconductor switch. To keep the switching in the input side the bidirectional switching unit is placed in between the supply and the rectifier. The input switched topologies can also be used with step-up, step-down and step up/down capabilities. The PFC correction becomes easier with input switched topologies since the input current is chopped at high frequency resulting near sinusoidal high frequency chopped input current. Thus a small filter can be used to shape the input current.

In active filter techniques, controlled switches are used instead of diodes. Pulse Width Modulation (PWM) is used to operate these converters. These converters are used to obtain high power quality. In order to do that, complex control algorithms are used which increase the cost [43]. A general classification of different AC to DC (both single and three phase) topologies is shown in Figure 1.1.



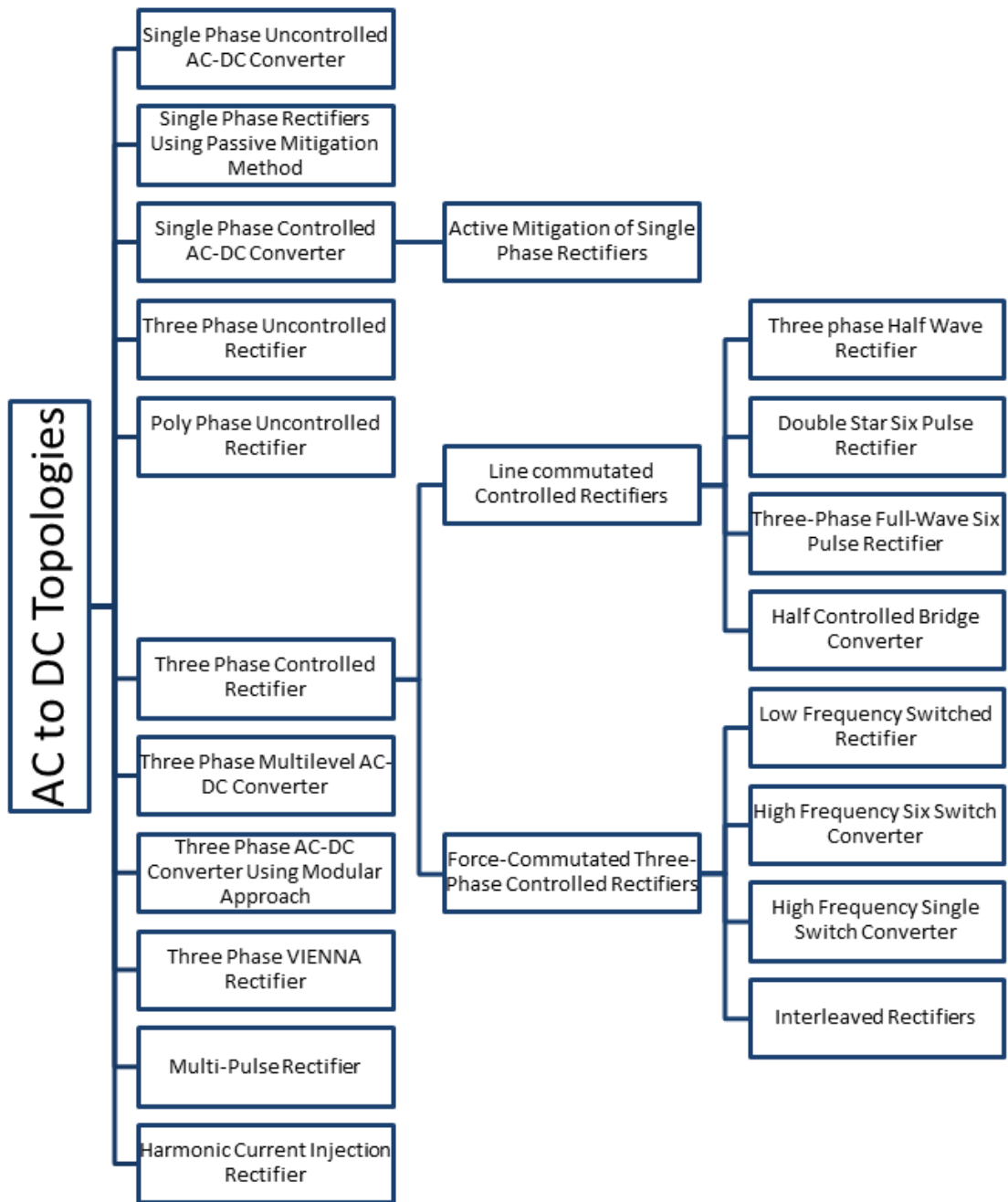


Figure 1.1 General AC to DC Converter topologies.

### 1.2.2 Review According to application

Lighting consumes around 16–20% of the total energy a commercial building uses. To align the lighting levels with human needs, and thus save energy, a dimming technology is used [45-56]. For a fluorescent lamp, the cathode voltage must be maintained while the lamp current is reduced. A dimmable ballast consists essentially of a cascade of power electronics circuits: an EMI filter, an AC–DC conversion circuit that should also assure a high power factor, and an inverter which supplies the lamp. The recent advancement of light-emitting diodes (LEDs) opens a new era of lighting. The LED is an electronic light source [30, 51, 57-60] and its supply has to be electronically controlled current source fed by an AC to DC rectifier

AC-DC converters are used directly in DC motor drives for their smooth control and energy efficient operation. AC motor drives (synchronous and induction) along with special motors generally use AC to DC converters in the front end feeding appropriate inverters [61-76]. AC to DC converters are in use for AC and special type Stepper, brushless DC, switched reluctance and permanent magnet DC motors [65, 77-83].

AC to DC converter used in transportation applications such as electric vehicles [20, 34, 39, 84-89], subways, locomotives and aircraft systems [90-95]. Hybrid electric vehicles have gained popularity as they use less fuel and pollute the environment with less carbon dioxide emission than gas (petrol) driven vehicles.

Application examples of AC-DC converters in Electrical Utilities like HVDC [96, 97], FACTs [98], Static VAR compensation, and harmonic suppression: TCR, TSC, SVG, APF, custom power and power quality control are numerous, where they are used directly or used as the front end converter feeding inverter.

Apart from drives and lighting, other applications that require ac-dc conversion is induction heating, electrochemical processes, plasma torches, electrolysis, electroplating, welding, arc furnaces and ovens etc [99-102].

The AC to DC converter is used for motion control applications in areas such as computer peripherals and industrial robots. The power supply of the computer systems is one of the major application of such converters [103-105].

The AC to DC converter is used in other important applications in residential and home appliances, in the information and telecommunication industry, in renewable energy conversion, in electronic display devices, in high voltage physics experiments and atomic accelerators.

### **1.2.3 Review According to Control Technique**

The primary control objective of the AC to DC converter is to regulate the output voltage. The feedback controller to regulate the output voltage must be designed with the following objectives in mind: zero steady state error, fast response to changes in the input voltage and the output load, low overshoot, and low noise susceptibility. Controls can be classified according to control variables as Voltage Mode Control (VMC) and Current Mode Control (CMC). In the process of regulating the output voltage, a current control loop is embedded inside a voltage control loop [106, 107]. Control circuits are designed for AC to DC converter with an objective to keep the input current in-phase with the supply voltage that is to keep the input power factor unity. Current mode control is the most common control strategy to achieve such objective. In [13-26] the power factor corrector (PFC) circuits force the input current to trace the shape of line voltage. Both VMC and CMC implements two tasks: error compensation and modulation. The performance of the converter system largely depends on the quality of the applied current control strategy to achieve high efficiency, low input current THD, almost sinusoidal input current and high input power factor.

### **Linear and Non-linear Control**

The linear controllers operate with conventional voltage type PWM modulators. In contrast to the nonlinear controllers, linear controller schemes have separated current error compensation and voltage modulation parts. This concept allows exploiting the advantages of open-loop modulators (sinusoidal PWM, space-vector modulator, and optimal PWM) which are of constant switching frequency type. In the linear group, some basic controllers are reported: PI stationary and synchronous, state feedback, and predictive with constant switching frequency. Besides linear control, non-linear control like hard switch converter, soft switched converter, Neural Network(NN) Controller

FLCC controllers are also reported in literature for the control of static power converters [108-110].

### **Current Mode Control Techniques**

Current-mode control is often used in practice due to its desirable features, such as simpler controller design and inherent current limiting. In such a control scheme, an inner current control loop inside the outer voltage-loop is used. In this control arrangement, another state-variable, the inductor current, is utilized as a feedback signal [1, 6].

### Indirect Current Control Techniques

The research in sensorless control has resulted in Direct Power Control and Voltage Oriented Control in the past. One cycle controlled system [111-114] has been reported as another sensorless strategy which does not require ac voltage sensors and phase locked loop (PLL) for synchronization. Reference proposes to eliminate voltage sensors that are required for stable operation of OCC based bidirectional three-phase ac to dc converter. The indirect current control is one of the earliest applications which eliminate current transducers in controlling input current of PWM rectifiers, where, the current control strategy is based on steady-state models of the ac side. In an indirect control strategy is proposed based on a complete dynamical model of the converter resulting linear system of second order, compared with the fourth-order system in the previous ones. This simplifies the stability analysis and greatly facilitates the design of the PI voltage regulator.

### Direct Current Control Techniques

#### *Peak Current Mode Control (PCMC)*

For the current loop, the outer voltage loop produces the reference for the inductor current. This reference current signal is compared with the measured inductor current to turn the switch off when measured inductor current reaches the reference inductor current [6, 115-119]. Disadvantage of PCMC is the presence of sub-harmonic oscillations at duty cycles greater than 50%. In generating reference inductor current

the voltage controller output is modified by a signal called the slope compensation, which is necessary to avoid oscillations at the sub-harmonic frequencies of switching frequency.

#### *Average Current Mode Control (ACMC)*

In order to follow the reference with as little THD as possible, an average-current-mode control is used with a high bandwidth, where the error between the reference inductor current and measured inductor current is amplified by a current controller to produce the control voltage. This control voltage is compared with a ramp in the PWM controller to produce the switching signal [120-124].

#### *Hysteresis Current Mode Control (HCMC)*

In HCMC, inductor current is kept in between the two sinusoidal current references generated corresponding to maximum and minimum boundary limits. To keep the current sinusoidal as possible or to achieve smaller ripple in the input current, a narrow hysteresis band is desired [125-128]. The narrower the hysteresis band, the higher is the switching frequency. According to this control technique, the switch is turned ON when the inductor current decreases below the lower reference and is turned OFF when the inductor current increases above the upper reference, giving rise to a variable frequency control. Simple option for improvement in HMCC is presented in.

#### *Predictive Current Mode Control (PCMC)*

In predictive current control scheme the switch voltage is predicted at the beginning of each modulation/switching period. The prediction is based on the current error, input voltage, switching frequency and input filter inductor and load variables. The predicted switch voltage is compared with double-edge triangular carrier signal to generate PWM pulse to the switches. The carrier signal is chosen for fixed frequency operation but the amplitude of the carrier signal is modulated to accommodate the load voltage/current variation. In every switching/ modulation cycle, the switch voltage reference is predicted and used to generate gate pulses. This technique uses additional information along with error signal that improves converter dynamic performance. The

improvements occur at the expense of cost on sensors and complexity in control circuits [129-133].

#### *Linear Current Control (LCC)*

In LCC the actual current is compared with the reference current to obtain the current error. The error is processed by a proportional-integral controller to provide a modulating signal for a PWM modulator. The modulator produces gate pulses for the converter switches. The pulses are of constant frequency with varying pulse widths, which depend upon the magnitude of the modulating signal produced by the current controller. The controller parameters are tuned to optimize the PWM pulses such that the input current maintains near sinusoidal waveform and the power factor near to unity. The controller requires minimum number of measured signals from converter and hence the implementation using standard integrated circuits becomes simple, cost effective and reliable. The current regulation scheme presented relies on calculation of a duty cycle for each switching state (space vector) of the rectifier. This fundamental concept is extended to a deadbeat, predictive, rectifier current regulator. Direct control of the current space ( $dq$ ) vectors [134] has the advantages of improved harmonic performance, especially at low dc bus voltages (modulation index near unity), and improved dynamic response to a transient in the load power or dc bus voltage at any operating condition in comparison to per-phase PWM techniques.

#### *Nonlinear Carrier Control (NLC)*

The NLC is capable of attaining input resistor emulation in boost and other converters that operate in the continuous conduction mode. Implementation of the controller is quite simple, with no need for sensing of the input voltage or input current. There is no need for a current loop error amplifier. The boost nonlinear-carrier charge controller is inherently stable and is free from the stability problems that require addition of an artificial ramp in current programmed controllers [1].

## **Other Control Techniques**

Apart from the discussed control techniques, there are other control techniques like digital boundary current control [135-137], sliding mode control [138], Lyapunov-based control [139, 140], direct power control, inductor voltage control [106, 107] and digital control [109, 121, 137, 141-143] etc.

## **1.3 Problem Identification and Research Motivation**

Power quality issue is becoming important in areas involving use of power electronic control of AC-DC converters. Research continues to improve the power quality in all fields of electricity use. AC-DC converters with improved power quality are complex, costly, difficult to maintain and unreliable in some cases. Present research work will emphasize to simplify the circuit topology and make cost effective solutions of power quality issues of single phase AC-DC converters. The desirable features of single phase AC-DC converter topologies to be investigated will combine AC-DC and DC-DC conversion in one power conversion stage. Previous works concentrated on two stage solution consisting of diode bridge rectifiers followed by conventional dc-dc converters. One stage solutions by single phase AC to DC conversion will necessitate new single phase topologies. The implementation of new single phase AC-DC conversion by switch mode topologies will convert AC of a single phase supply to produce a combined DC output to the load. Such topologies will switch supply AC at the input in single phase at multiple of supply voltage frequency to regulate the output voltage, and at the same time keep the input current sinusoidal. The input current will then be filtered and controlled by average current control technique to obtain near sinusoidal current with low THD, good converter efficiency and high input power factor. The new single phase AC to DC converter topologies will be investigated by simulation. This will also be implemented practically. The new topologies will be realized by single bidirectional AC switch, passive energy storage components and diodes. It is anticipated that innovations and ideas generated during this research will be of significant contribution to the power quality mitigation of single phase AC to DC conversions.

## **1.4 Research Objectives**

To overcome the problems experienced in switch mode AC to DC converter, the objective of this thesis research is to propose new simple and easy to control topologies to maintain high conversion efficiency at extremely high and low duty cycle. Thus to design and analyse input switched hybrid AC to DC converters with following objectives:

1. To achieve high efficiency at extremely low and high duty cycle of the switching frequency using hybrid diode-capacitor network instead of conventional transformers for voltage step-down or step-up operation.
2. In addition to keep performance parameters satisfactory: high input power factor and low input current THD.
3. Developing small signal model of the converter to design suitable feedback control to regulate output voltage and to shape the input current to a near sinusoidal and keep it in phase with the utility supply voltage.
4. The converter must maintain constant output voltage under load variation. The dynamic response will be studied to verify the desired response pattern being obtained.
5. Hardware implementation of the proposed topologies to validate the outcome.

## **1.5 Thesis Outline**

Chapter 1 provides the introduction and literature review regarding AC to DC converter.

Chapter 2 provides the necessary background of AC to DC converter with performance issues. Section 2.1 gives a brief summary about the current status of the problem. Section 2.2 discusses the performance parameters of AC to DC converter. Section 2.3 provides necessary background of the hybrid DC to DC converter. Hybrid converters are compared with the conventional converter to analyse their improved performance.



In Chapter 3, the working principle of the conventional and proposed boost converters are described in detail. The open loop simulation is carried out to compare the performance of the converters.

In Chapter 4, the proposed boost converters are investigated under feedback condition to improve the input power factor and to keep the input current THD within limits. The feedback control is also studied by simulation for load variation.

In Chapter 5, the conventional and proposed SEPIC converters are investigated for step-down applications without feedback control. The simulation results are analysed.

In Chapter 6, the proposed SEPIC converters are studied with feedback control to improve the shape of the input current. They are also studied by simulation to observe the dynamic response.

In Chapter 7, feedback control is designed in detail for one of the proposed boost converter. The simulation with the designed parameter is also included.

Chapter 9 draws a conclusion of current work. Provides suggestions regarding the future investigation that should be carried out to improve the performances of the proposed converters.

## Chapter 2

### Background of the Research

In this chapter, the necessary background of AC to DC converter with performance issues are discussed in section 2.1 and section 2.2. Investigation of hybrid DC to DC converter is carried out in section 2.3.

#### 2.1 Current Status of the Problem

The input current of the single phase conventional bridge rectifier with resistive load is free from harmonic distortion and ideally in phase with the line voltage. Thus the input current THD is minimum and power factor is near unity. Ideal conversion efficiency is also 100%. The output voltage contains large ripple which is not suitable for the devices to handle. The conventional single phase bridge rectifier with resistive load is shown in Figure 2.1. The corresponding input-output waveforms are shown in the Figure 2.2.

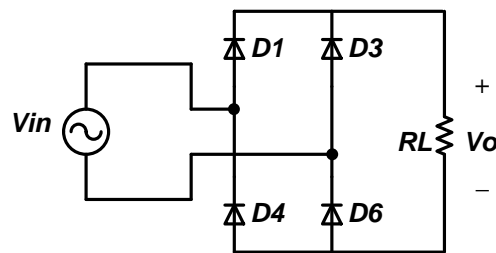
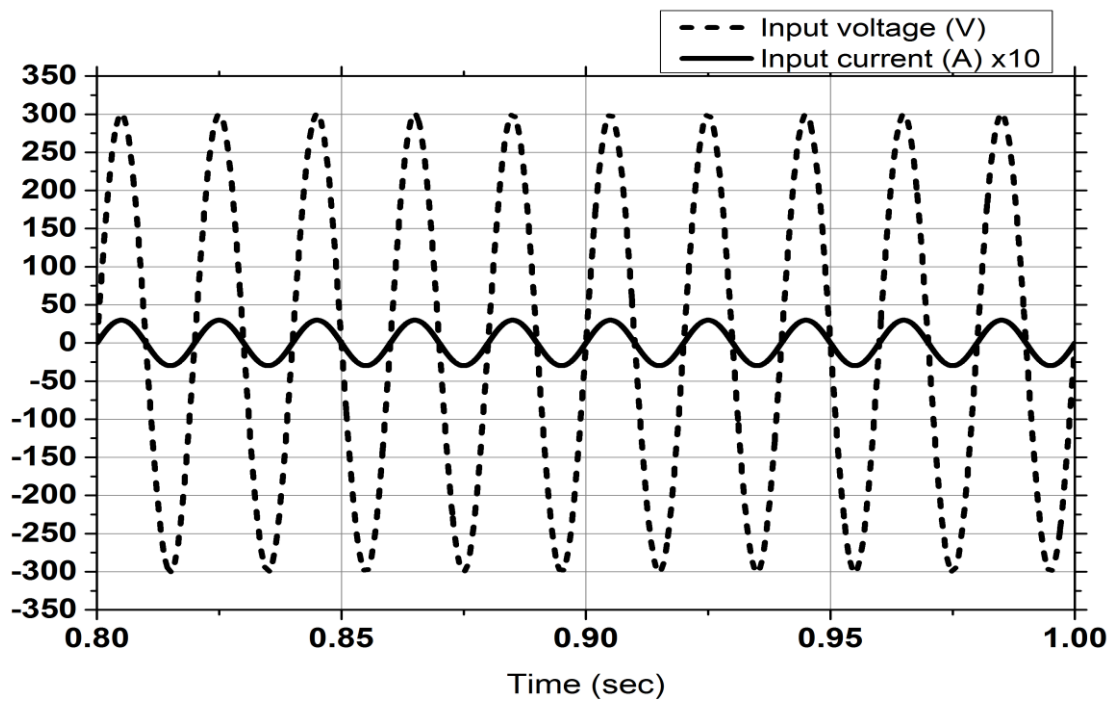
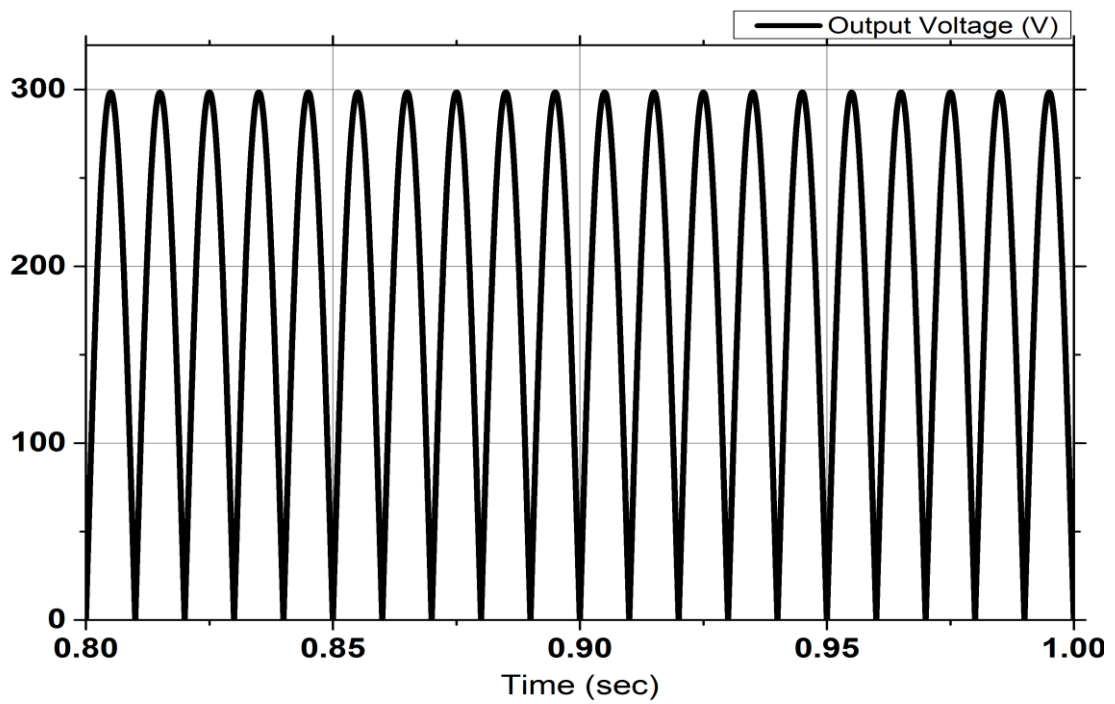


Figure 2.1 Schematic diagram of single phase bridge rectifier.



(a)



(b)

Figure 2.2 Waveforms of circuit of Figure 2.1. (a) Input voltage-current and (b) output voltage.

The pulsating DC output voltage is reduced by introducing large filter capacitor. Due to the capacitor the output voltage is regulated within defined allowed ripple but distorts the input current. The input current is no longer continuous because the load only draws current from the supply only when the supply voltage is higher than the DC-link voltage. The input current is no longer sinusoidal. Discontinuous input current introduces harmonics and as a result input current THD increases. The corresponding circuit is shown in Figure 2.3. The input-output waveforms are shown in Figure 2.4.

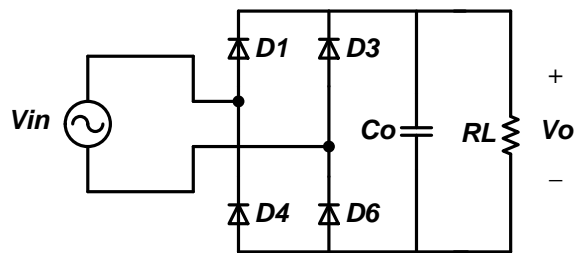
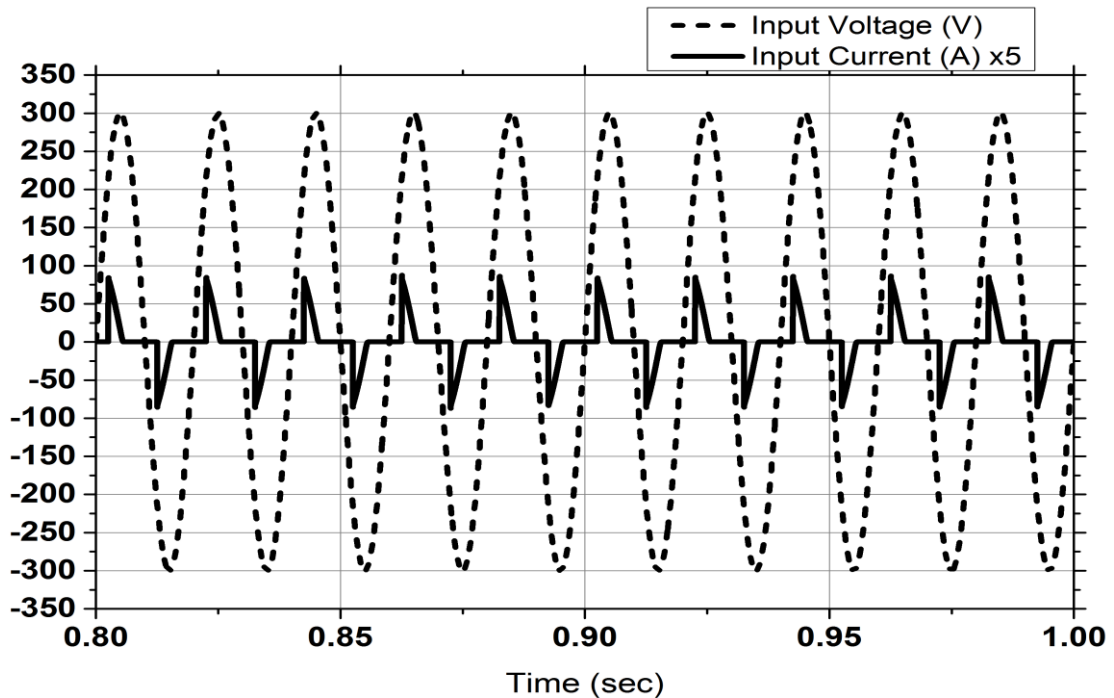
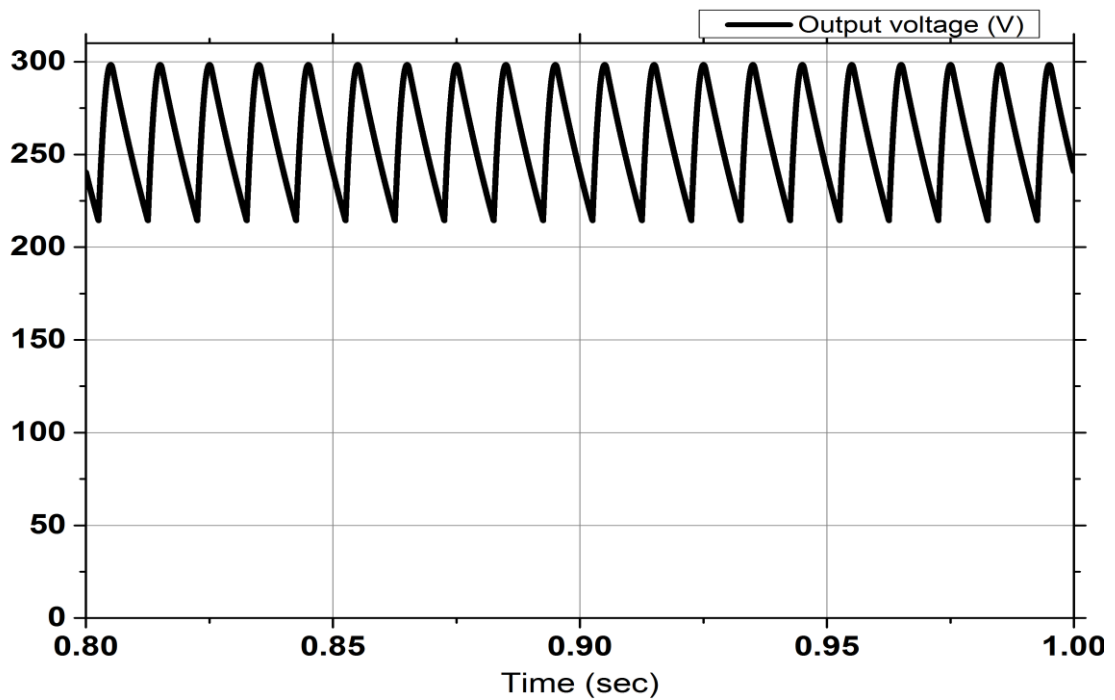


Figure 2.3 Single phase bridge rectifier with output filter capacitor.



(a)



(b)

Figure 2.4 Waveforms of circuit of Figure 2.3. (a) Input voltage-current and (b) output voltage.

Highly distorted input current due to the output capacitor can be made sinusoidal again with the help of large input filter sacrificing efficiency and input power factor. The corresponding circuit and the input-output wave-shapes are shown below.

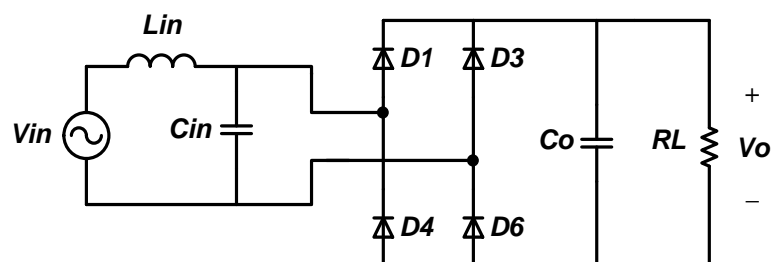
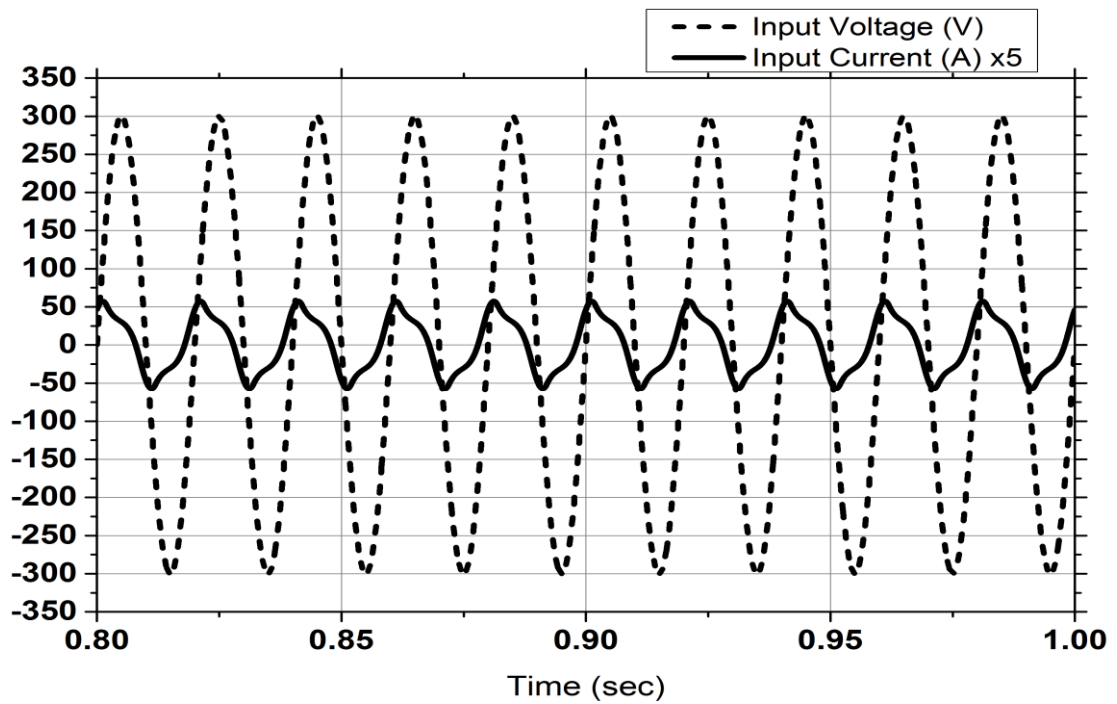
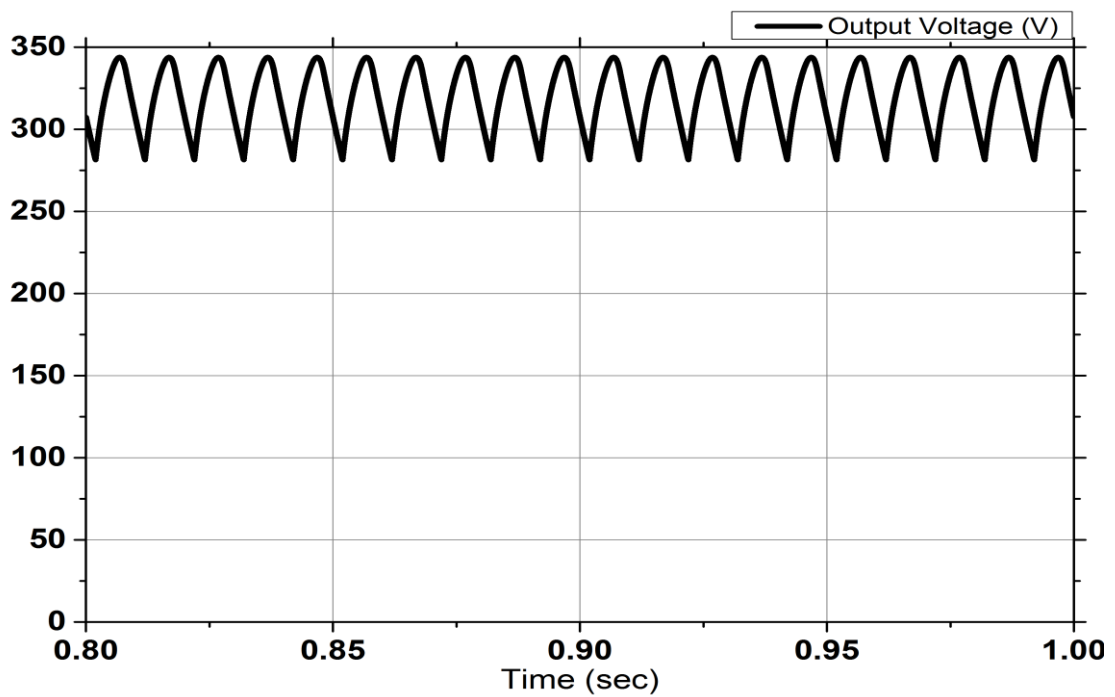


Figure 2.5 Bridge rectifier with input and output filter.



(a)



(b)

Figure 2.6 Waveforms of circuit of Figure 2.5. (a) Input voltage-current and (b) output voltage.

Two stage AC-DC converter topologies are used to reduce the THD and improve the efficiency. The input current will be in phase if feedback control is used or proper L-C filter is used with less efficiency. The first stage is the conventional bridge rectifier and the second stage is the high frequency DC-DC converter. Any conventional topologies can be used in the second stage like buck, boost or buck-boost. Due to the high frequency second stage, a small input filter can keep the input current sinusoidal. The circuit and the wave-shapes of the two stage buck AC-DC converter are shown as example in Figures 2.7-2.8.

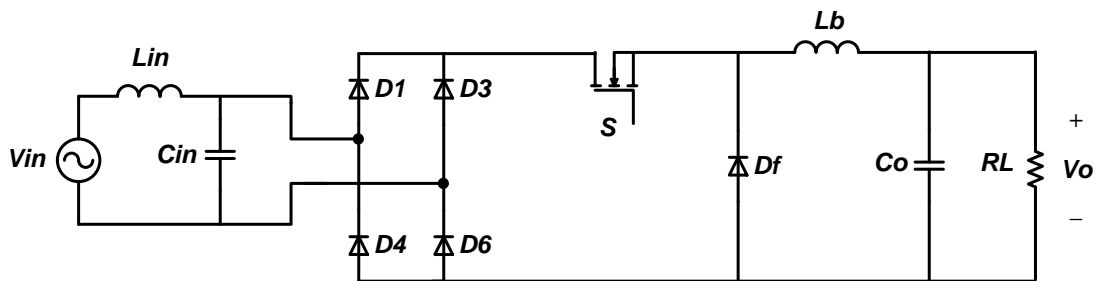
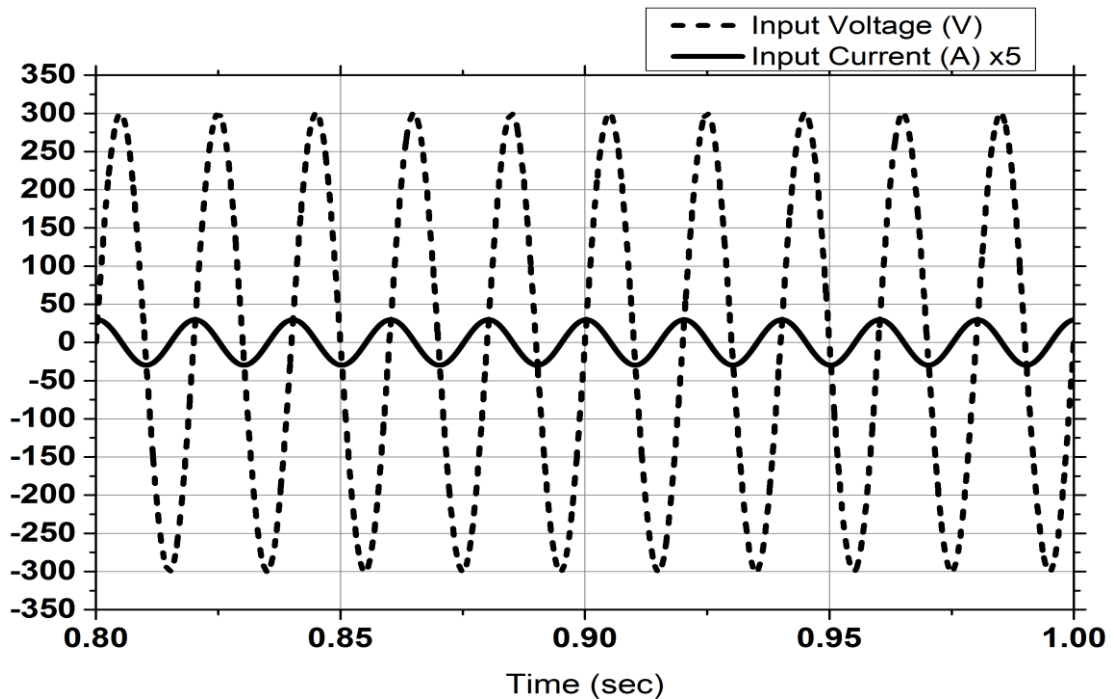
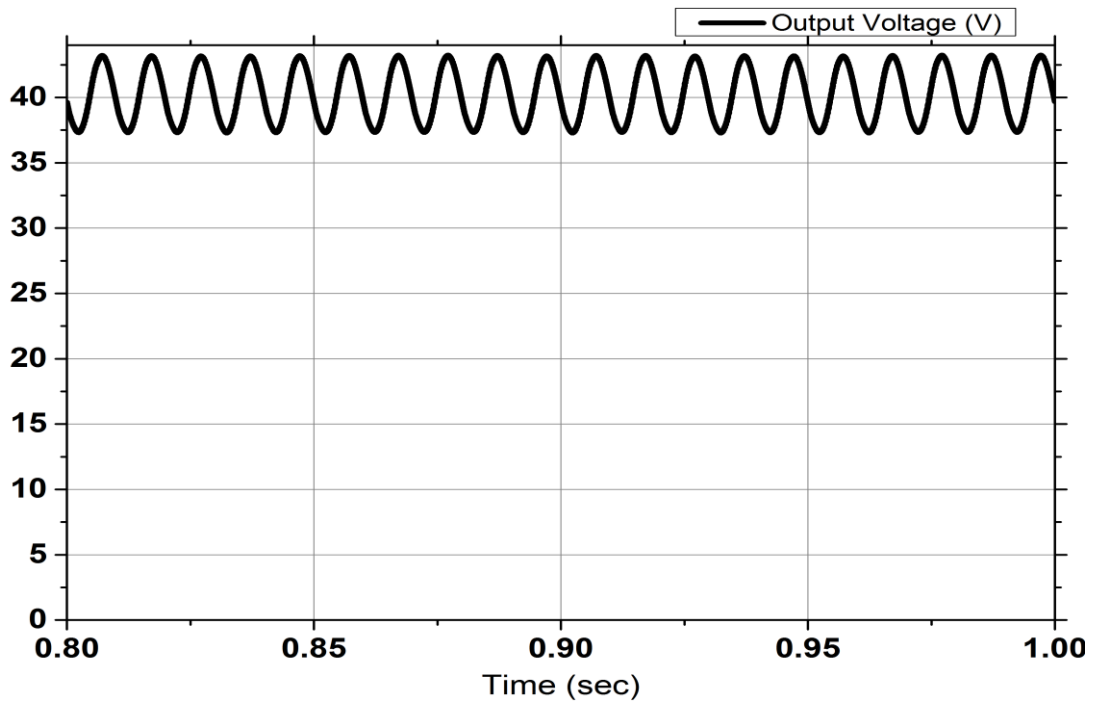


Figure 2.7 Two-stage AC to DC buck converter.



(a)



(b)

Figure 2.8 Waveforms of circuit of Figure 2.7. (a) Input voltage-current and (b) output voltage.

As the number of stage is increased the losses of the system will also increase. Thus the efficiency of the converter suffers. So scope is still there to design new single converter to improve efficiency.

## 2.2 Performance Parameters of AC to DC converter

Input power factor (PF<sub>i</sub>), total harmonic distortion (THD) of the input current, output voltage ripple and the efficiency are the important parameters that determine the quality of the rectifier circuits. Power factor (PF), as applied to voltage and current waveforms is described by the relationship between the apparent power extracted from a driving source and the real power delivered to a receiving load. In mathematical expression of PF is a ratio of the real power delivered to the load and the apparent power supplied by the source

$$PF = \frac{P_R}{P_A} = \cos\theta \quad (2.1)$$



Where  $P_R$  = Real Power and  $P_A$  = Apparent Power. Input current is no longer for modern day appliances load and thus the definition of the power factor also changes:

$$PF = \frac{DPF}{\sqrt{1+THD^2}} \quad (2.2)$$

Where DPF is the displacement power factor and THD is the total harmonic distortion. The definition of DPF is given as,

$$DPF = \cos\theta_1 \quad (2.3)$$

Where  $\theta_1$  is the angle between the fundamental of  $i(t)$  and  $v(t)$ . PF and DPF can be related as,

$$PF = \left(\frac{I_1}{I}\right) DPF \quad (2.4)$$

For undistorted sinusoidal waveforms  $(I_1/I)$  is unity. The total harmonic distortion (THD) of the current  $i(t)$  is defined as the ratio of the rms values of the harmonics over the rms value of the fundamental component.

$$THD = \frac{I_{distortion}}{I_1} = \frac{\left[\sum_{n=2}^{\infty} I_{n\text{rms}}^2\right]^{0.5}}{I_1} \quad (2.5)$$

Where  $I_1$  is the fundamental component of the input current.

There are several deleterious effects of high distortion in the current waveform and the poor power factor that results. These are as follows [6]:

- Power loss in utility equipment such as distribution and transmission lines, transformers, and generators increases, possibly to the point of overloading them.
- Harmonic currents can overload the shunt capacitors used by utilities for voltage support and may cause resonance conditions between the capacitive reactance of these capacitors and the inductive reactance of the distribution and transmission lines.
- The utility voltage waveform will also become distorted, adversely affecting other linear loads, if a significant portion of the load supplied by the utility draws power by means of distorted currents.

In order to prevent degradation in power quality, recommended guidelines (in the form of the IEEE-519) have been suggested by the IEEE (Institute of Electrical and Electronics Engineers). These guidelines place the responsibilities of maintaining power quality on the consumers and the utilities as follows: (1) on the power consumers, such as the users of power electronic systems, to limit the distortion in the current drawn, and (2) on the utilities to ensure that the voltage supply is sinusoidal with less than a specified amount of distortion.

The limits on current distortion placed by the IEEE-519 are shown in Table 2.1 [144], where the limits on harmonic currents, as a ratio of the fundamental component, are specified for various harmonic frequencies. Also, the limits on the THD are specified. These limits are selected to prevent distortion in the voltage waveform of the utility supply.

Table 2.1 Harmonic current distortion. (IEEE 519)

$I_{SC}/I_1$	Odd harmonic order $h$ (in %)					THD (%)
	$h < 11$	$11 \ll h \ll 17$	$17 \ll h \ll 23$	$23 \ll h \ll 35$	$35 \ll h$	
< 20	4.0	2.0	1.5	0,6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-10000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.

Therefore, the limits on distortion in Table 2.1 depend on the “stiffness” of the utility supply. The stiffness is defined by a ratio called the Short-Circuit-Ratio (SCR):

$$SCR = \frac{I_{SC}}{I_1} \quad (2.6)$$

Where,  $I_{SC}$  is the short circuit current calculated by hypothetically placing short-circuit at the supply terminals.

## 2.3 Investigation of DC to DC converters

To derive and design new topologies appropriate for AC to DC converter, it is essential to investigate existing hybrid DC to DC converter. Several hybrid DC to DC converter involving Buck, Boost, Buck-Boost, Ćuk, SEPIC, Zeta configuration are proposed and their operating principle are explained [44]. Conventional DC to DC converter suffers from low efficiency at extremely high and extremely low duty cycle. The hybrid DC to DC topologies suggest to provide improved efficiency in those operating situations because in step down converters output voltage is further reduced with a given duty cycle than conventional converters. Similarly in case of step up converters with a given duty cycle output voltage is further increased than conventional ones. A desired low output voltage is achieved at reasonably high duty cycle than conventional converters. And a desired high output voltage is achieved at reasonably low duty cycle than conventional ones. So extremely high and extremely low duty cycle becomes high and low duty cycle in case of the hybrid DC to DC converters. Buck, boost and buck-boost hybrid DC to DC converter are investigated in this chapter to figure out the efficiency profile of the converters.

### 2.3.1 Hybrid Buck Converter

The diagrams of the conventional and the hybrid buck converter are given below for comparison. The operation principle of the hybrid converter is explained in [44]

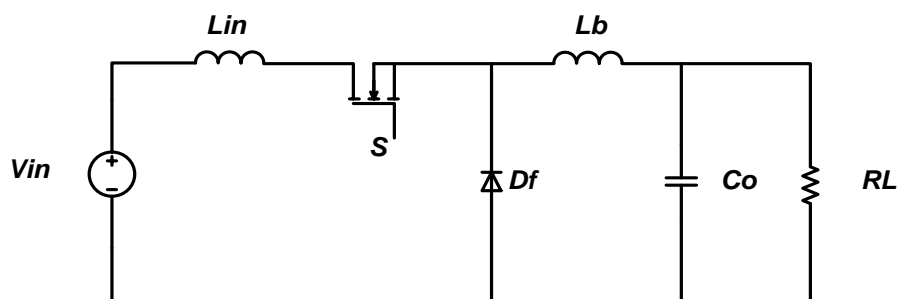


Figure 2.9 Conventional DC to DC buck converter.

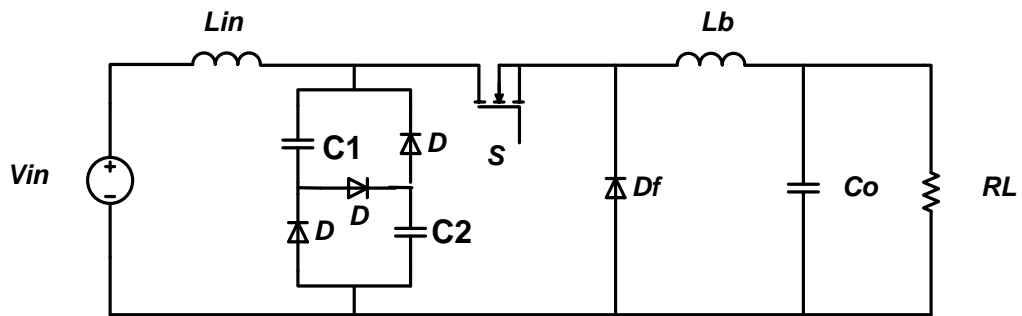


Figure 2.10 Hybrid DC to DC buck converter.

Simulations are carried out in both the conventional and hybrid DC to DC converter under similar conditions. The circuit parameters are:  $V_{in} = 12V$ ,  $L_{in} = L_b = 400\mu H$ ,  $C_1 = C_2 = C_o = 20\mu F$ ,  $R_L = 100\Omega$ . IGBT is taken as switch and an optimum switching frequency of 40 kHz is selected. The efficiency improvements of the hybrid circuit over the conventional buck converter are evident in results of Table 2.2 and graphs of Figure 2.11.

Table 2.2 Efficiency vs duty cycle of conventional and hybrid buck converter.

D	Conv. Buck $\eta$	Hybrid Buck D1 $\eta$
0.1	37	65
0.2	47	85
0.3	54	91
0.4	59	93
0.5	64	94
0.6	67	95
0.7	71	96
0.8	76	98
0.9	80	98

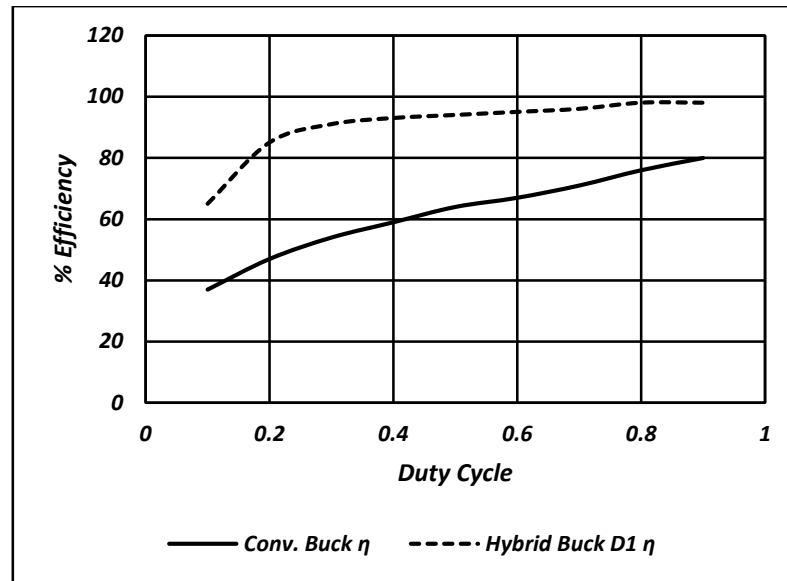


Figure 2.11 Efficiency vs duty cycle of conventional and hybrid buck converter.

Study is also carried out to observe the variation of the efficiency with the change in the switching frequency of the converters. The efficiency improvement of the hybrid circuit over the conventional buck converter for different switching frequency is evident in results of Table 2.3 and graphs of Figure 2.12. Typical output voltage waveforms of the hybrid DC to DC buck converter is shown in Figure 2.13 and 2.14.

Table 2.3 Efficiency vs switching frequency of convention and hybrid buck converter.

D	fsw	Conv. Buck $\eta$	Hybrid Buck D1 $\eta$
0.1	70	41.39	83.70
0.2	60	57.50	94.32
0.3	50	65.00	98.38
0.4	40	63.75	99.64
0.5	30	72.62	99.19
0.6	20	78.67	99.32
0.7	15	85.49	99.62
0.8	10	90.25	99.70
0.9	5	95.49	99.75

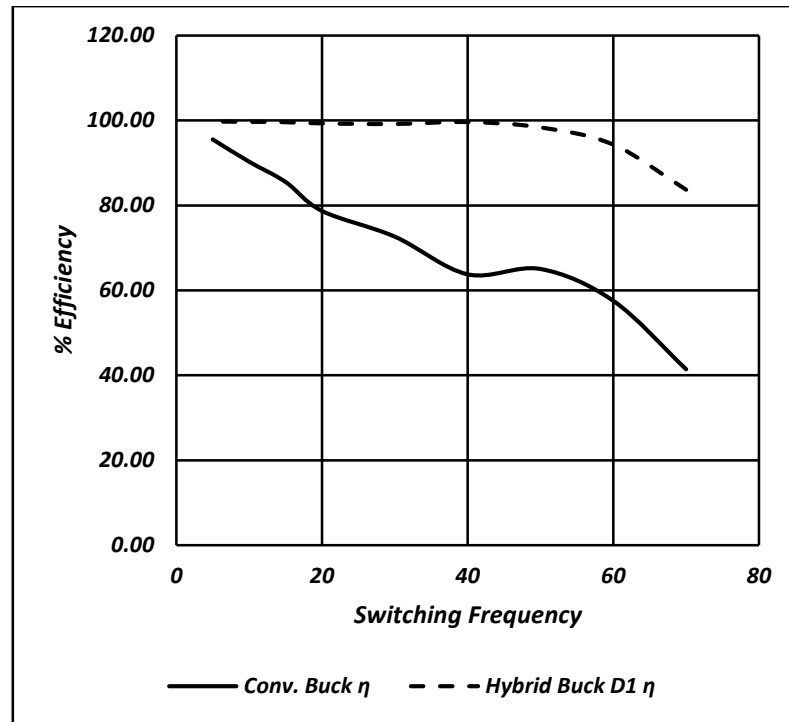


Figure 2.12 Efficiency vs switching frequency of convention and hybrid buck converter.

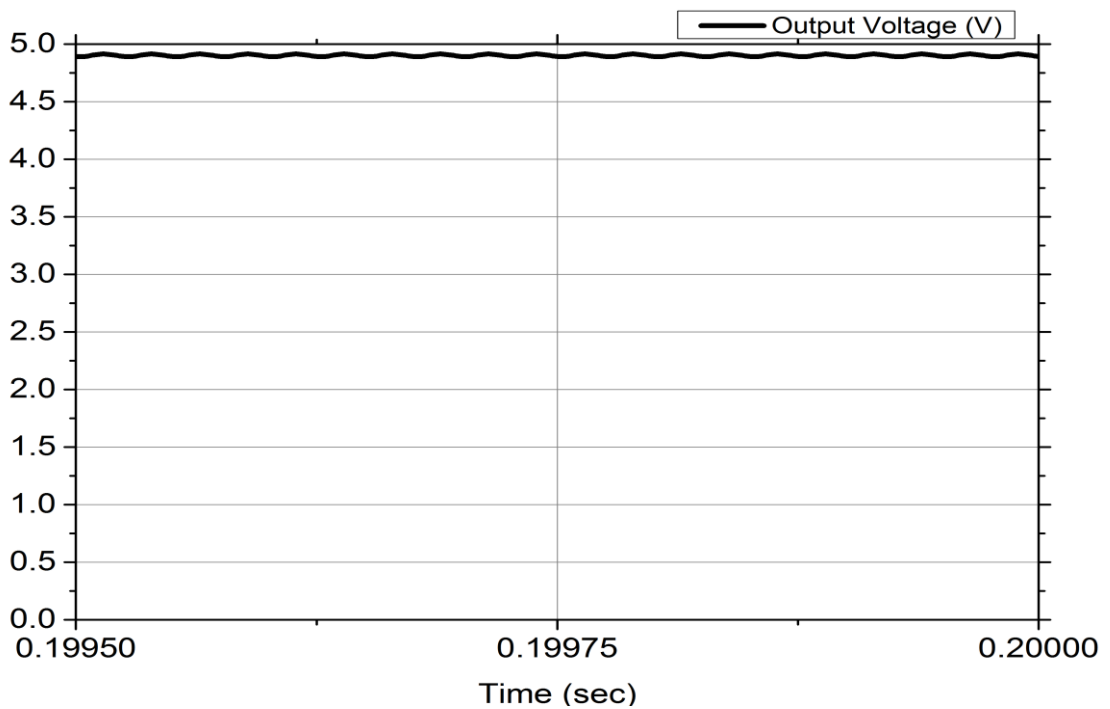


Figure 2.13 Output voltage of conventional buck converter at  $D = 0.3$ .

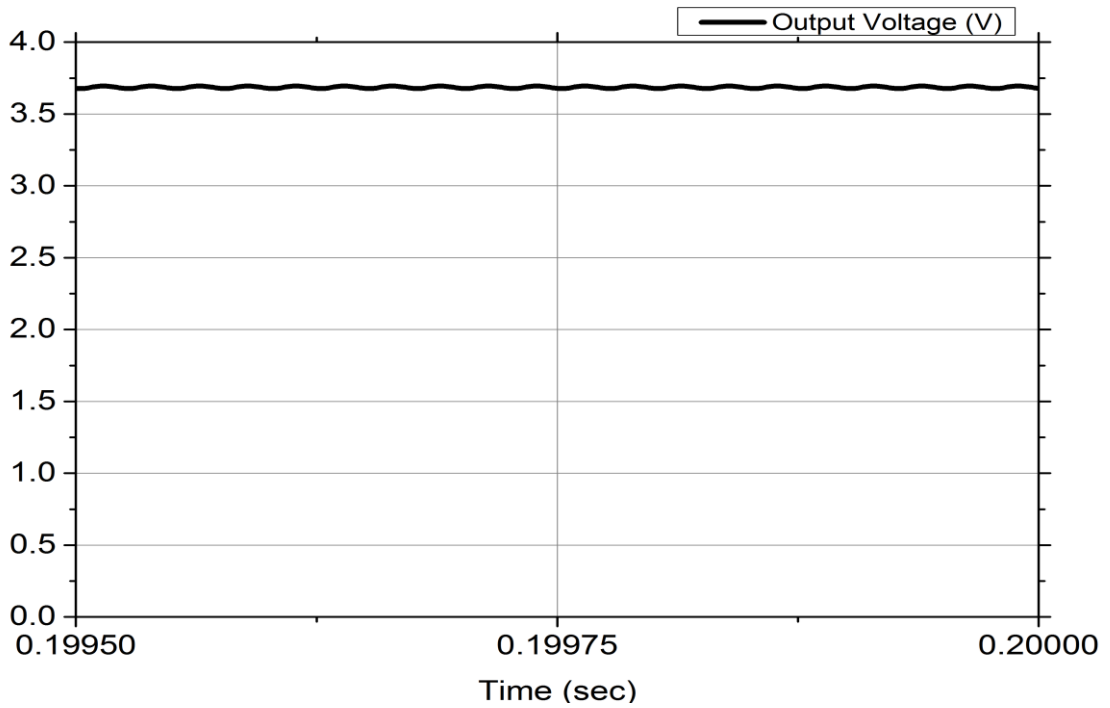


Figure 2.14 Output voltage of hybrid buck converter at  $D = 0.3$ .

### 2.3.2 Hybrid Boost Converter

The diagrams of the conventional boost converter and the hybrid boost converter are given below for comparison.

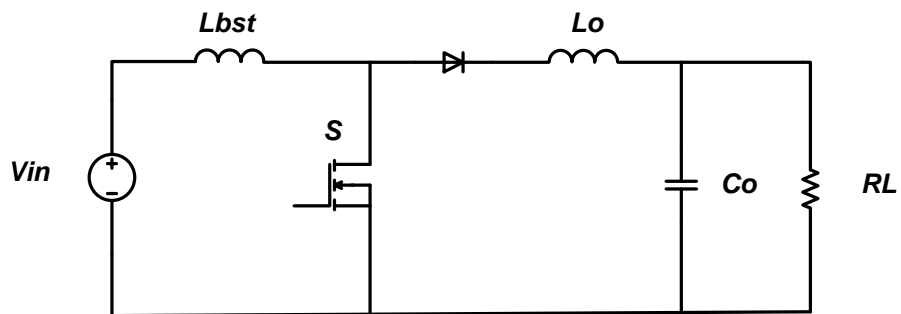


Figure 2.15 Conventional DC to DC boost converter.

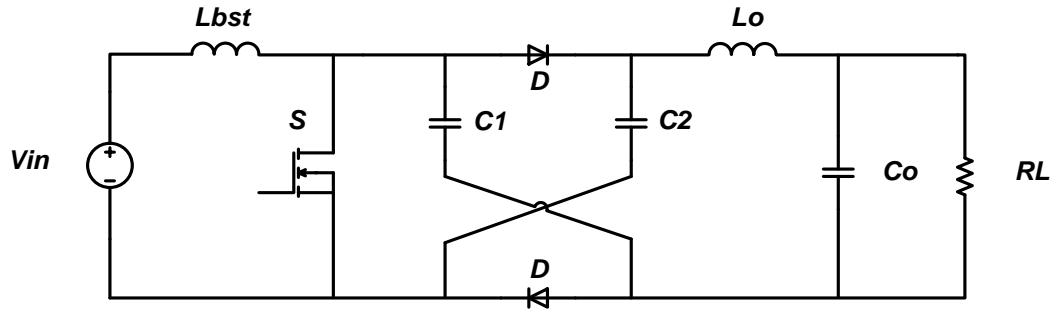


Figure 2.16 Hybrid DC to DC boost converter.

Simulations are carried out for both the conventional and hybrid DC to DC converter under similar conditions. The circuit parameters are:  $V_{in} = 12V$ ,  $L_{in} = L_{bst} = 400\mu H$ ,  $C1 = C2 = C_o = 20\mu F$ ,  $R_L = 100\Omega$ . IGBT is taken as switch and an optimum switching frequency of 40 kHz is selected. The efficiency improvements of the hybrid circuit over the conventional buck converter are evident in results of Table 2.4 and graphs of Figure 2.17.

Table 2.4 Efficiency vs duty cycle of conventional and hybrid boost converter.

D	Conv. Boost $\eta$	Hybrid Boost U1 $\eta$
0.1	92.13	99.40
0.2	79.60	99.54
0.3	73.54	99.58
0.4	67.75	99.62
0.5	62.03	99.69
0.6	56.34	99.75
0.7	50.54	99.63
0.8	44.61	99.57
0.9	38.44	99.37



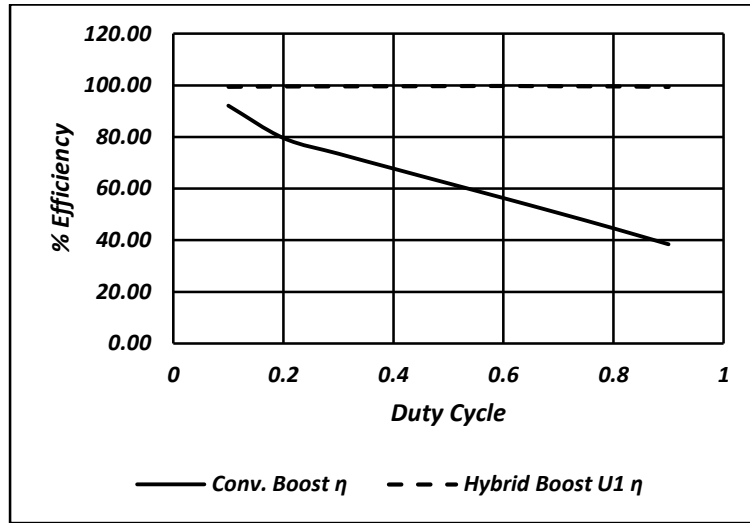


Figure 2.17 Efficiency vs duty cycle of conventional and hybrid boost converter.

Study is also carried out to observe the variation of the efficiency with the change in the switching frequency of the converters. The efficiency improvement of the hybrid circuit over the conventional boost converter for different switching frequency is evident in results of Table 2.5 and graphs of Figure 2.18. Typical output voltage waveforms of the hybrid DC to DC buck converter is shown in Figure 2.19 and 2.20.

Table 2.5 Efficiency vs switching frequency of conventional and hybrid boost converter.

D	fsw (kHz)	Conv. Boost $\eta$	Hybrid Boost U1 $\eta$
0.1	70	96.00	99.63
0.2	60	85.71	99.82
0.3	50	74.92	99.84
0.4	40	69.25	99.80
0.5	30	65.30	99.92
0.6	20	60.86	99.96
0.7	15	56.47	99.95
0.8	10	51.53	99.92
0.9	5	45.58	99.95

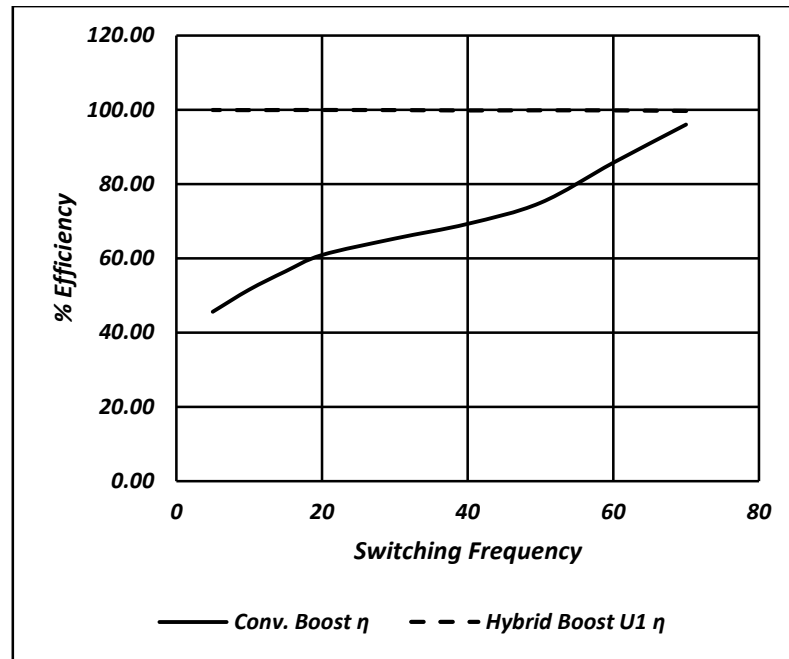


Figure 2.18 Efficiency vs switching frequency of conventional and hybrid boost converter.

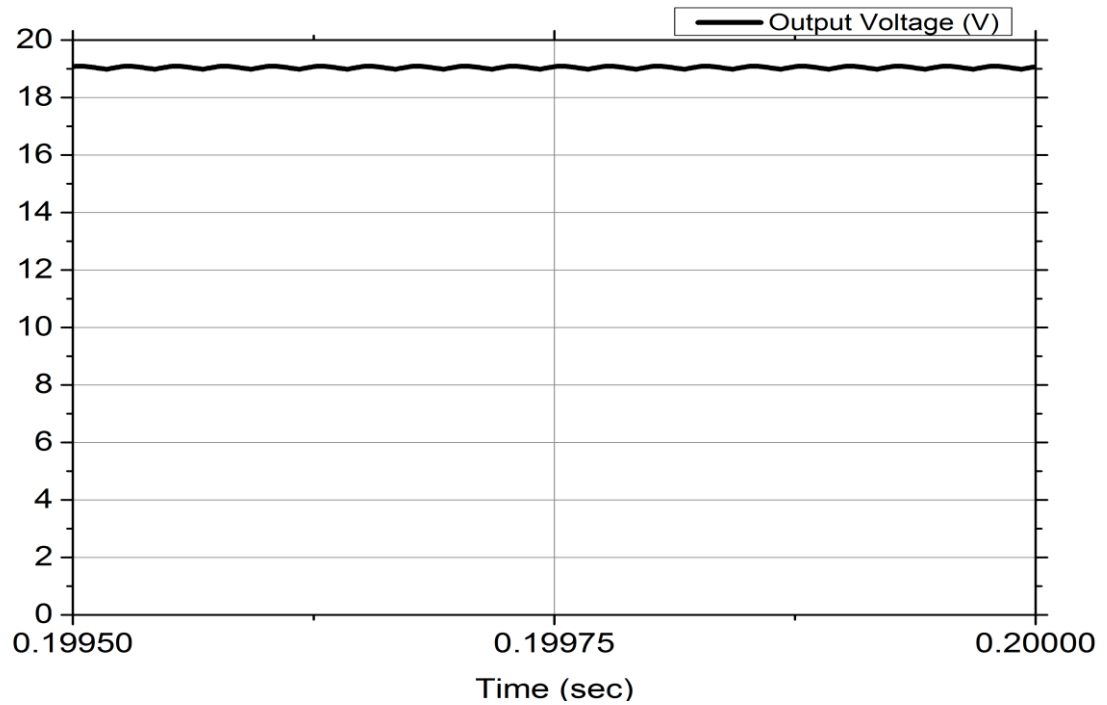


Figure 2.19 Output voltage of conventional boost converter at  $D = 0.7$ .

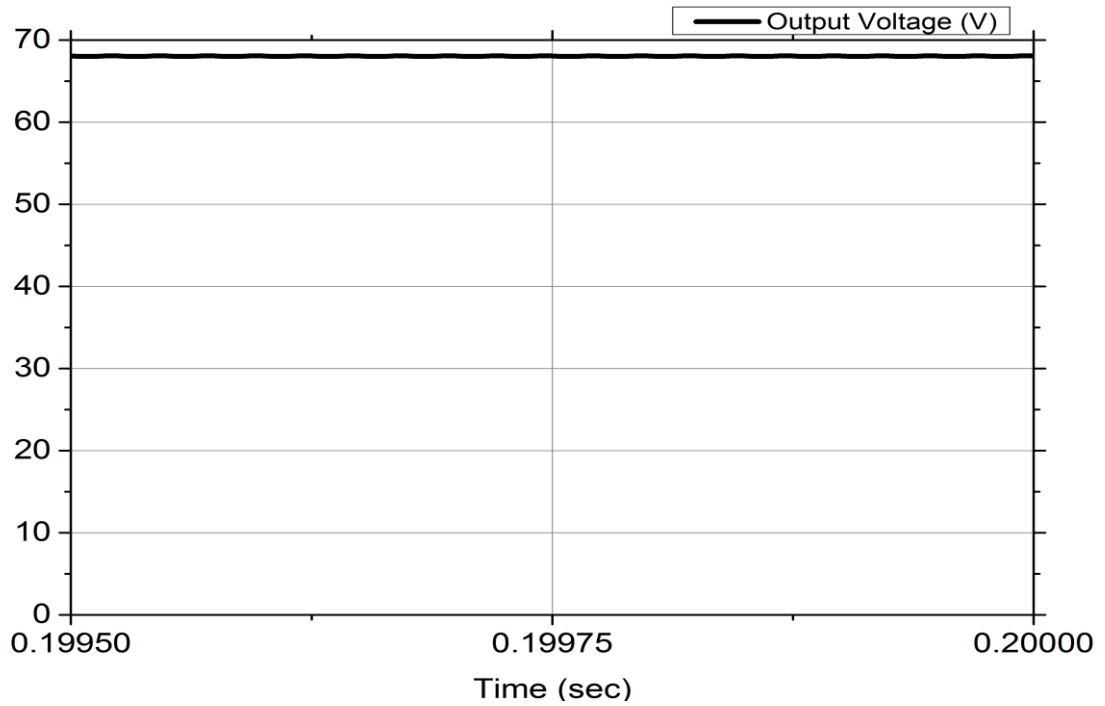


Figure 2.20 Output voltage of hybrid boost converter at  $D = 0.7$ .

### 2.3.3 Hybrid Buck-Boost Converter

The diagrams of the conventional buck-boost converter and the hybrid buck-boost converter for both down and up conversion are given below for comparison.

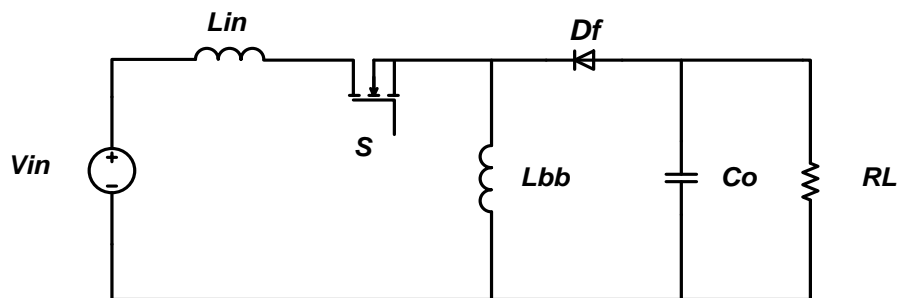


Figure 2.21 Conventional DC to DC buck-boost converter.

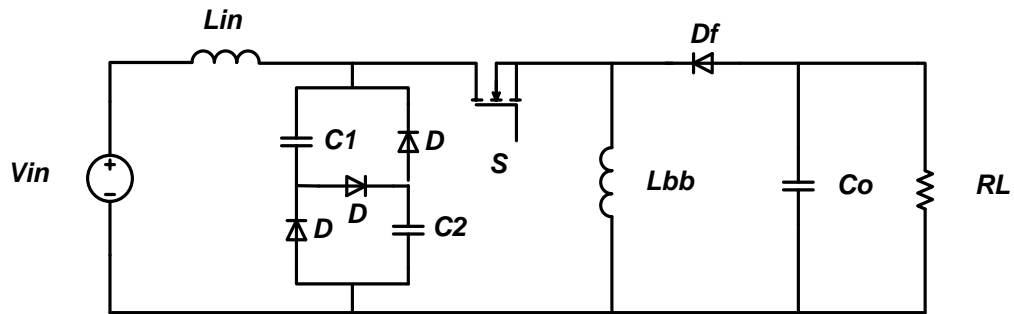


Figure 2.22 Hybrid DC to DC buck-boost down converter.

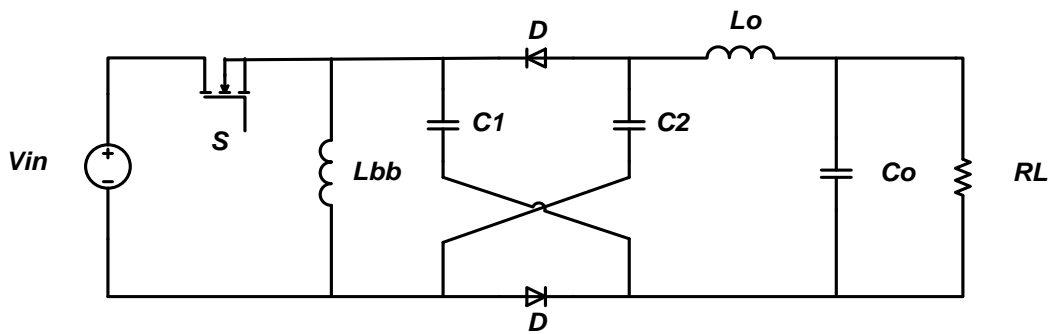


Figure 2.23 Hybrid DC to DC buck-boost up converter.

Simulations are carried out for both the conventional and hybrid DC to DC converter under similar conditions. The circuit parameters are:  $V_{in} = 12\text{V}$ ,  $L_{in} = L_{bb} = 400\mu\text{H}$ ,  $C_1 = C_2 = C_o = 20\mu\text{F}$ ,  $R_L = 100\Omega$ . IGBT is taken as switch and an optimum switching frequency of 40 kHz is selected. The efficiency improvements of the hybrid circuit over the conventional buck-boost down converter are evident in results of Table 2.6 and graphs of Figure 2.24.

Table 2.6 Efficiency vs duty cycle of conventional and hybrid buck-boost down converter.

D	Conv. Buck-Boost $\eta$	Hybrid Buck-Boost D1 $\eta$
0.1	65.93	64.63
0.2	79.11	91.90
0.3	84.87	94.30
0.4	88.02	96.35
0.5	91.67	97.89
0.6	95.28	99.89
0.7	97.27	97.69
0.8	98.71	84.44
0.9	98.89	74.20

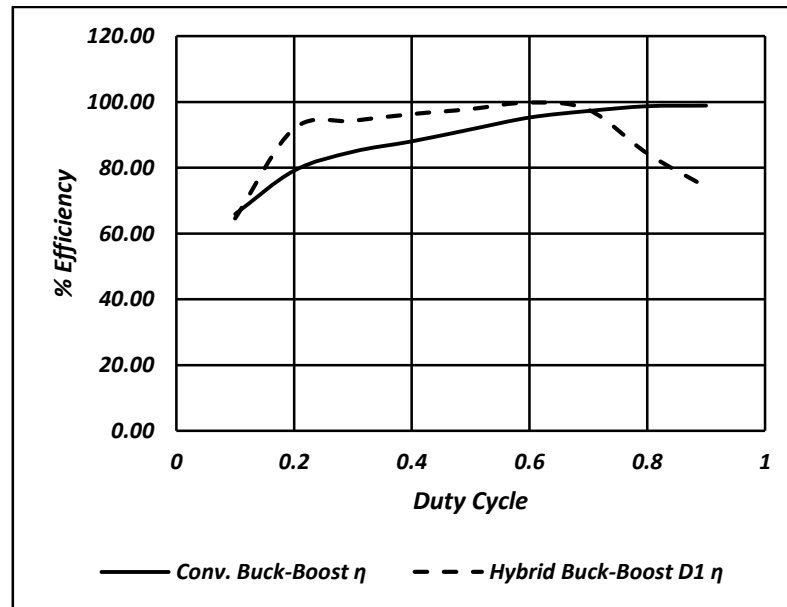


Figure 2.24 Efficiency vs duty cycle of conventional and hybrid buck-boost down converter.

The efficiency improvements of the hybrid circuit over the conventional buck-boost up converter are evident in results of Table 2.7 and graphs of Figure 2.25.

Table 2.7 Efficiency vs duty cycle of conventional and hybrid buck-boost up converter.

D	Conv. Buck-Boost $\eta$	Hybrid Buck-Boost U1 $\eta$
0.1	65.93	66.37
0.2	79.11	79.89
0.3	84.87	88.31
0.4	88.02	93.09
0.5	91.67	95.84
0.6	95.28	97.59
0.7	97.27	98.59
0.8	98.71	99.17
0.9	98.89	99.27

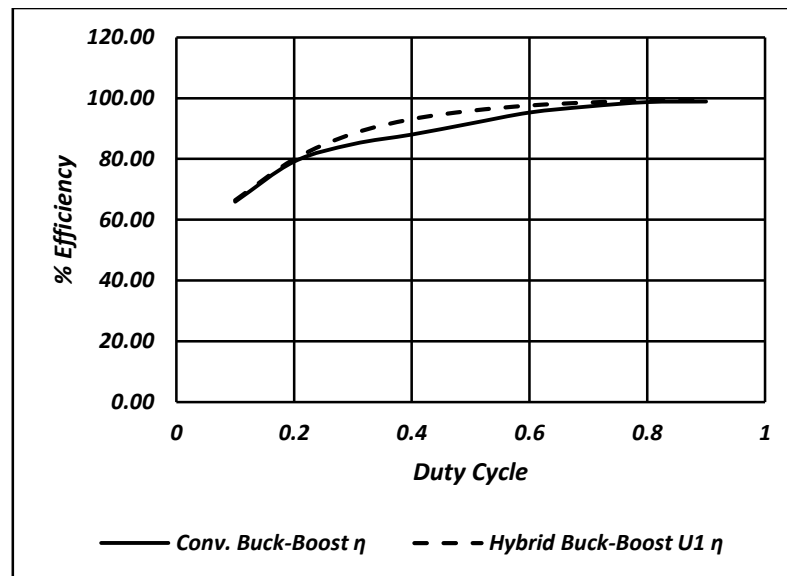


Figure 2.25 Efficiency vs duty cycle of conventional and hybrid buck-boost up converter.

Study is also carried out to observe the variation of the efficiency with the change in the switching frequency of the converters. The efficiency improvement of the hybrid circuit over the conventional buck-boost down converter for different switching frequency is evident in results of Table 2.8 and graphs of Figure 2.26. Typical output voltage waveforms of the hybrid DC to DC buck converter is shown in Figure 2.27 and 2.28.

Table 2.8 Efficiency vs switching frequency of conventional and hybrid buck-boost down converter.

D	fsw (kHz)	Conv. Buck-Boost $\eta$	Hybrid Buck-Boost D1 $\eta$
0.1	70	78.70	82.76
0.2	60	87.85	94.37
0.3	50	87.27	97.21
0.4	40	88.02	98.62
0.5	30	95.55	99.47
0.6	20	95.55	99.40
0.7	15	99.11	99.79
0.8	10	98.70	99.88
0.9	5	99.74	99.93

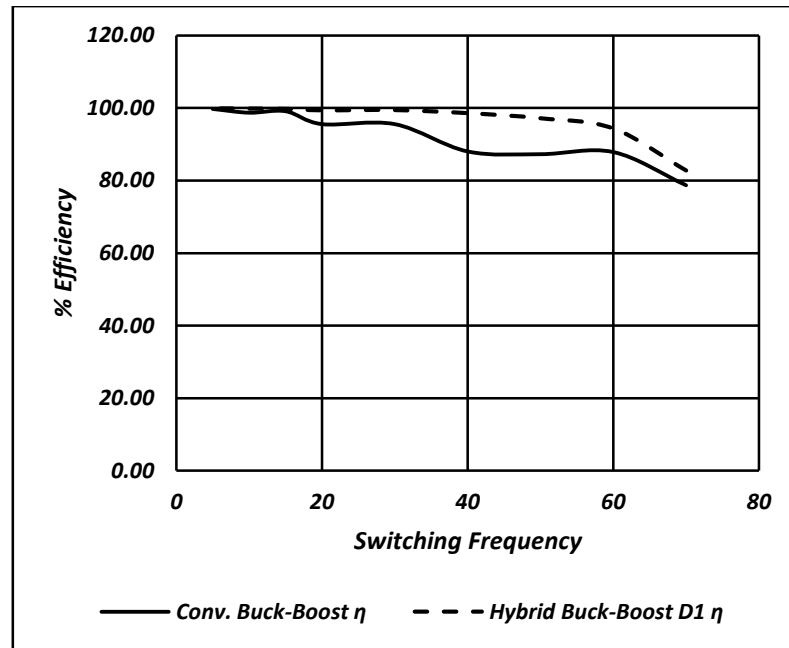


Figure 2.26 Efficiency vs switching frequency of conventional and hybrid buck-boost down converter.

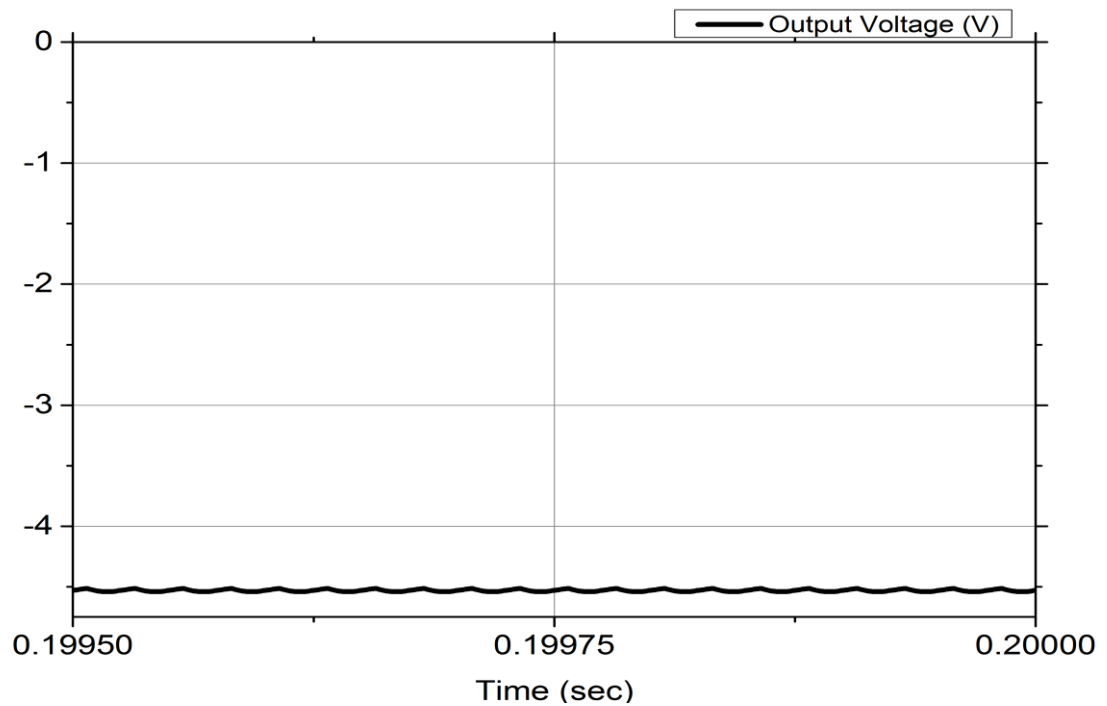


Figure 2.27 Output voltage of conventional buck-boost converter at  $D = 0.3$ .



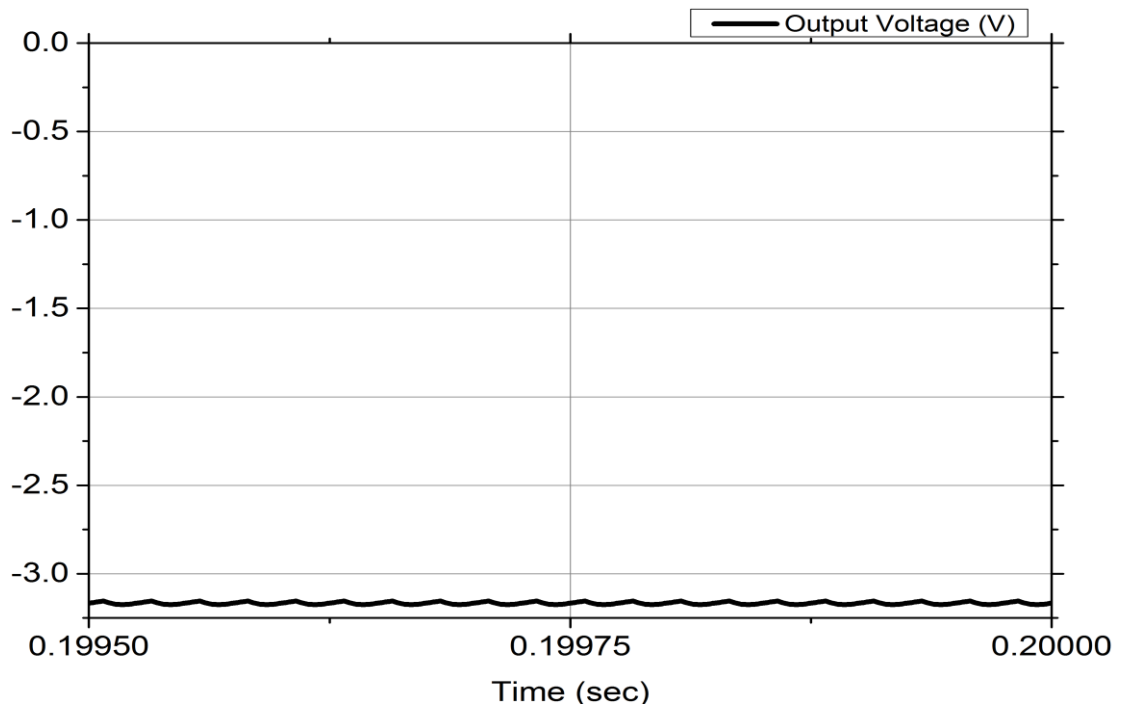


Figure 2.28 Output voltage of hybrid buck-boost down converter at  $D = 0.3$ .

Study is also carried out to observe the variation of the efficiency with the change in the switching frequency of the converters. The efficiency improvement of the hybrid circuit over the conventional buck-boost up converter for different switching frequency is evident in results of Table 2.9 and graphs of Figure 2.29. Typical output voltage waveforms of the hybrid DC to DC buck converter is shown in Figure 2.30 and 2.31.

Table 2.9 Efficiency vs switching frequency of conventional and hybrid buck-boost up converter.

D	fsw (kHz)	Conv. Buck-Boost $\eta$	Hybrid Buck-Boost U1 $\eta$
0.1	70	78.70	82.67
0.2	60	87.85	98.36
0.3	50	87.27	97.22
0.4	40	88.02	97.71
0.5	30	95.55	99.64
0.6	20	95.55	99.24
0.7	15	99.11	99.94
0.8	10	98.70	99.79
0.9	5	99.74	99.81

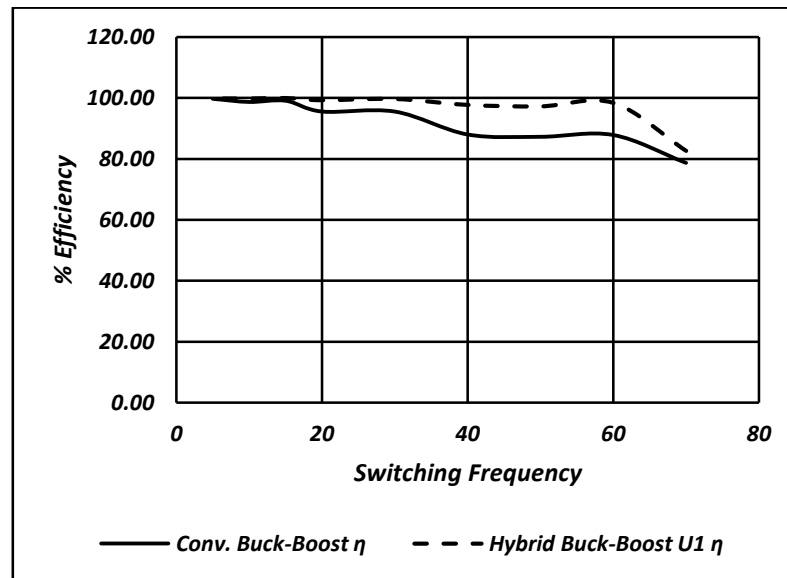


Figure 2.29 Efficiency vs switching frequency of conventional and hybrid buck-boost up converter.

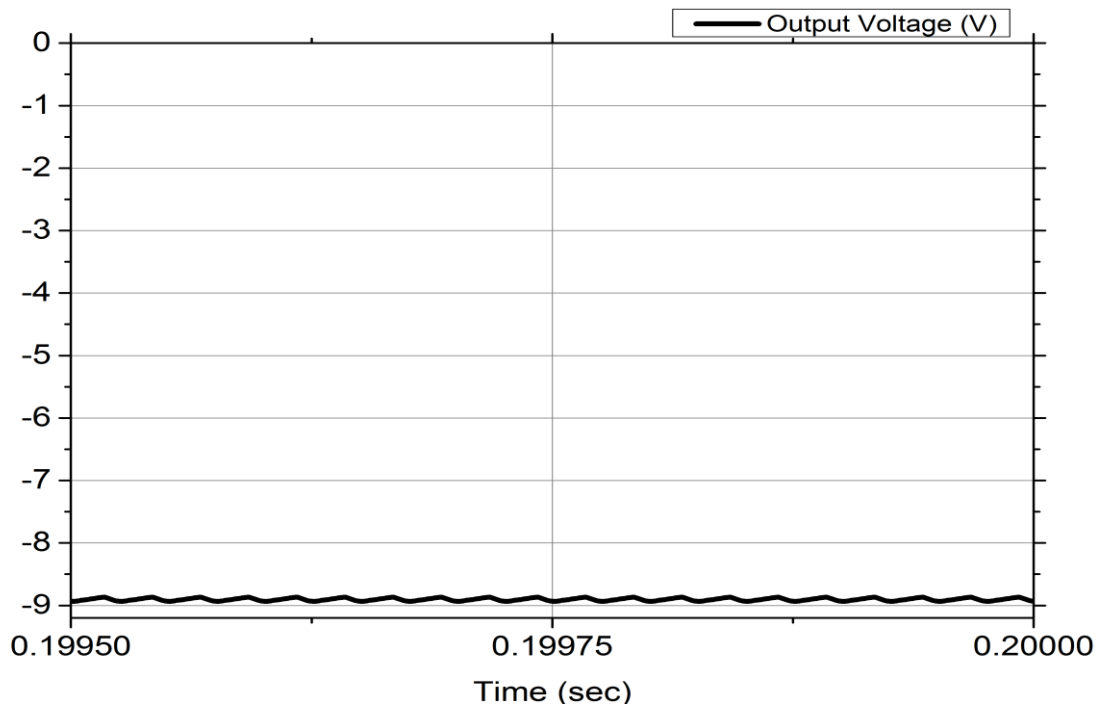


Figure 2.30 Output voltage of conventional buck-boost converter at  $D = 0.7$ .

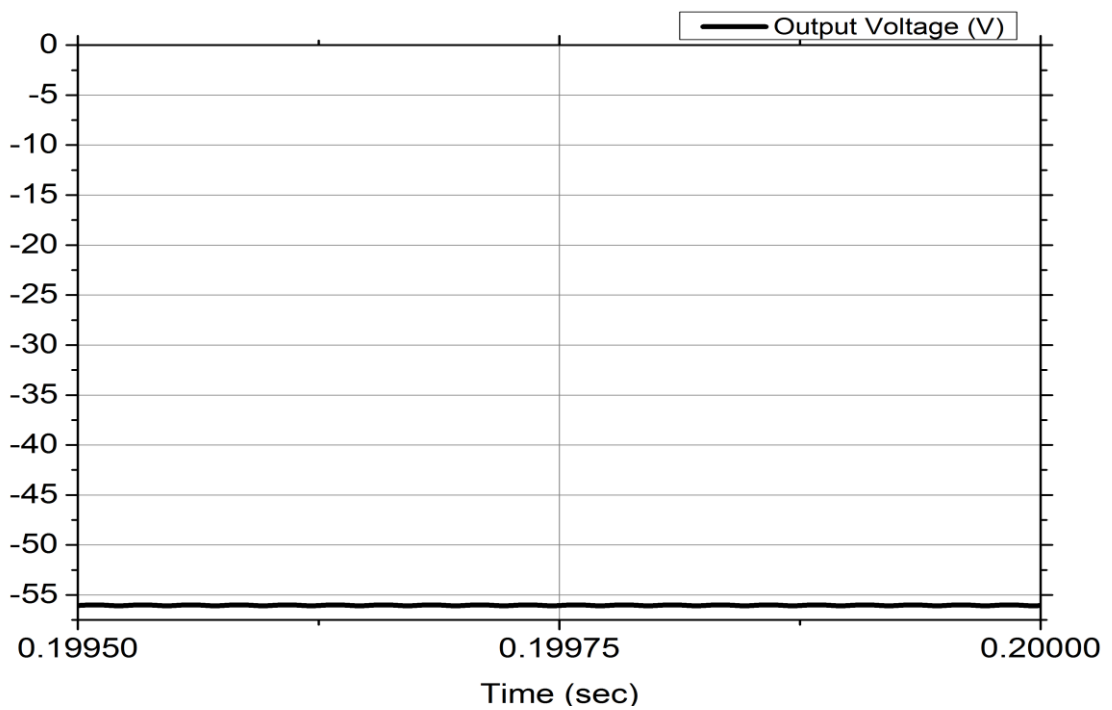


Figure 2.31 Output voltage of hybrid buck-boost up converter at  $D = 0.7$ .

## **2.4 Discussions**

From the simulation of all three types of hybrid DC-DC converter, it is evident that the efficiency is better in the proposed circuits compared to the conventional ones. Thus they can be used for further investigation for the AC-DC converter. Designing AC to DC converter is not as simple as designing DC-DC converter, because it is not only the conversion efficiency that has to be focused. The shape of the input current has to be near sinusoidal reducing harmonics to a prescribed level. Also the input power factor has to be close to unity. Again DC-DC converter can be used in AC-DC converter as an intermediate stage between the bridge rectifier and the load. With increased stage loss will also increase. Alternative to that can be designing single stage converter, which can increase circuit complexity and higher component count due to alternating nature of the source. Therefore topologies incorporating hybrid DC-DC converter and new simpler topologies for single phase AC to DC conversion can be designed and analysed to achieve better performance.

## Chapter 3

# Conventional and Proposed Single Phase Step-up AC to DC Converters

In this chapter, description of the working principle, open loop simulation and voltage gain relation of the conventional and proposed single phase AC to DC step-up converters are provided in section 3.1 through 3.8. The converter works in four stages. Stage I: when the switch is closed during positive half cycle. Stage II: when the switch is open during positive half cycle. Stage III: when the switch is closed during negative half cycle. Stage IV: when the switch is open during negative half cycle. The input/output voltage relationship of the AC to DC converter is tricky to derive because of the alternating nature of the input. The voltage relation has to be derived over line frequency cycle, not just over a switching cycle as it is in the case of DC to DC converters. It is important for understanding to compare the simulated values with the theoretical values. The conventional and proposed converters are compared in terms of conversion efficiency in section 3.9.

### 3.1 Conventional Output Switched AC to DC Boost Converter

The conventional single phase AC to DC boost converter has boost DC-DC converter in between the bridge rectifier and the load. The two stage converter is shown in Figure 3.1.

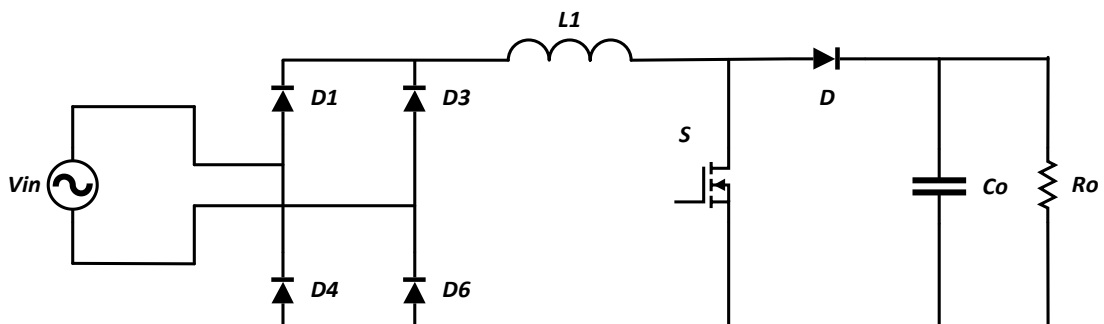
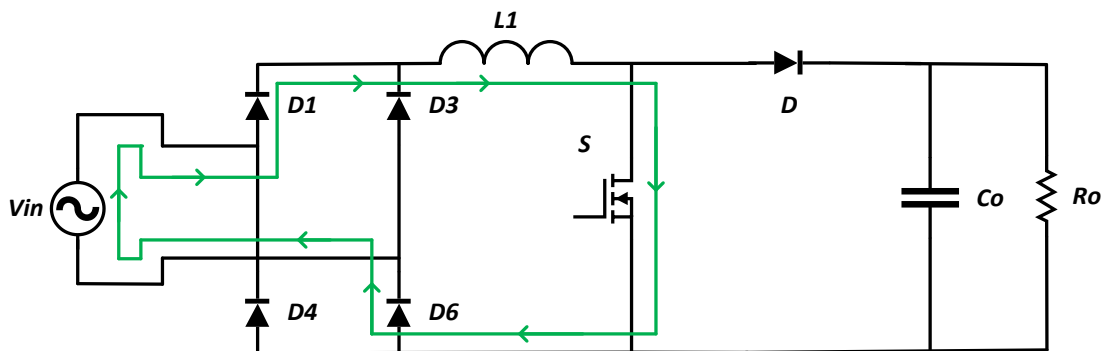


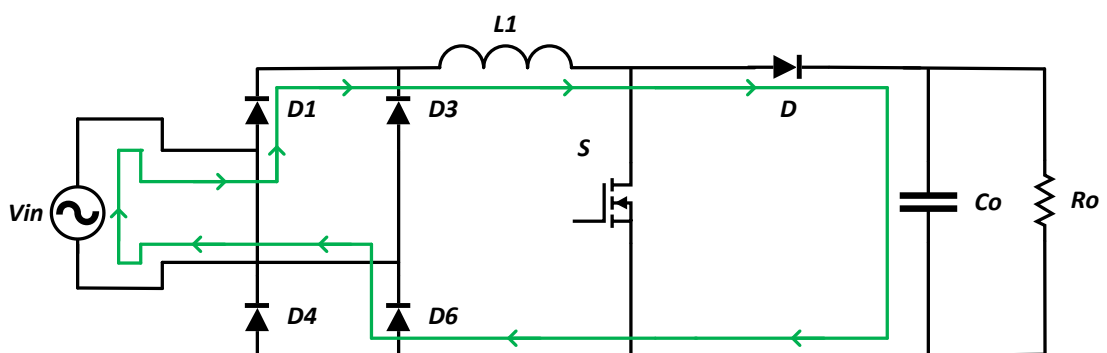
Figure 3.1 Conventional output switched AC to DC boost converter.

### 3.1.1 Principle of Operation

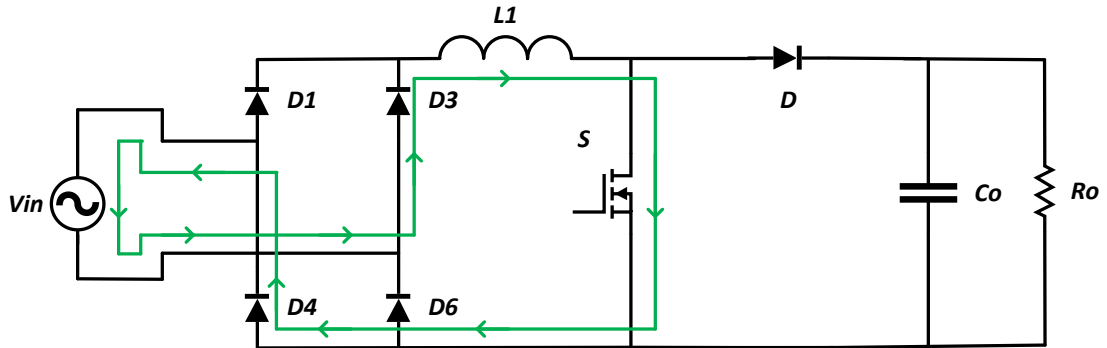
The four working stages of the conventional converter is illustrated in Figure 3.2, where Figure 3.2 (a) and (b) are for switch ON and OFF condition during positive supply cycle and Figure 3.2 (c) and (d) are for switch ON and OFF during negative cycle. When the switch is ON during positive half cycle the boost inductor charges from the source through the short circuit of the source. As the switch turns OFF, the source and the inductor voltage forward biases the output diode and charges the output capacitor. Same phenomenon takes place during the negative supply cycle as the output of the diode rectifier has same polarity.



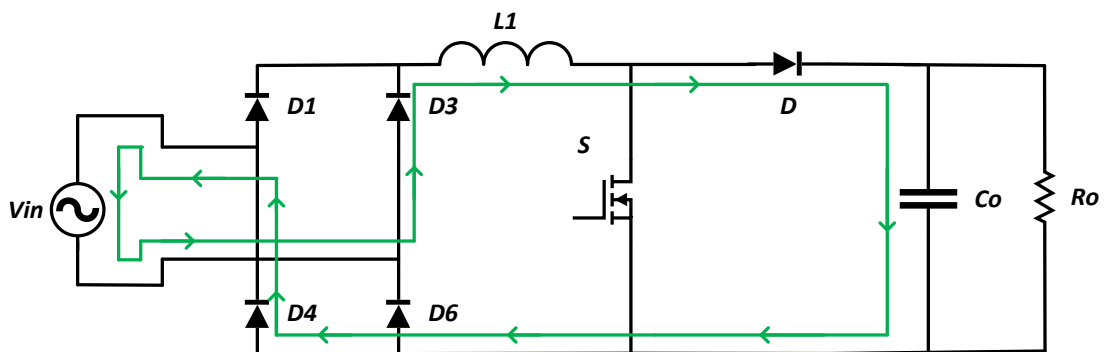
(a)



(b)



(c)



(d)

Figure 3.2 Four steps of operation of the converter in Figure 3.1,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.1.2 Open Loop Simulation

The simulation of the circuit of Figure 3.1 with no feedback for PFC and input current THD improvement is carried out with the parameters of Table 3.1. The results of the simulation is given in Table 3.2.

Table 3.1 Parameters of the converter of Figure 3.1.

Nominal input ac source voltage, $V_l$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_l$	5 mH
Capacitors, $C_o$	220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.2 Simulation results of the converter of Figure 3.1.

Voltage Gain	$V_o$	Efficiency	THD	PFi
1.111	315.730	98.757	87.795	0.769
1.250	355.941	97.623	83.750	0.789
1.428	403.3	97.453	77.690	0.809
1.667	463.108	97.154	70.809	0.824
2.000	540.541	96.709	62.022	0.833
2.500	649.739	95.931	51.699	0.832
3.333	801.351	94.577	38.826	0.814
5.000	1018.80	91.596	43.325	0.785
10.00	1296.20	58.596	37.576	0.923



### 3.1.3 Ideal Voltage gain Expression

The comparison of the theoretical and simulated voltage gain is shown in Table 3.3 for an AC input voltage of 30V<sub>P</sub>. Circuit diagram with voltage labels is shown in Figure 3.3.

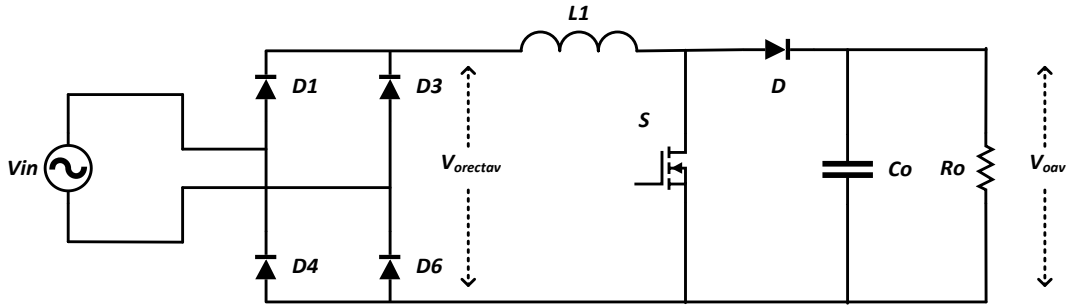


Figure 3.3 Conventional output switched AC to DC boost converter with voltage labels for positive half cycle of operation.

The rectified average voltage after the conventional bridge is,

$$V_{orectav} = \frac{V_{in\max}}{\pi} \int_0^{\pi} \sin \theta d\theta = \frac{2V_{in\max}}{\pi}$$

For DC-DC boost converter,

$$\frac{V_{orectav}}{(1-D)} = V_{oav}$$

Where,  $D = \text{Duty Cycle} = \frac{T_{ON}}{T}$ ,  $(1-D) = \frac{T_{OFF}}{T}$  and  $T = \text{Switching Frequency}$

Therefore the output voltage can be written as,

$$V_{oav} = \frac{2V_{in\max}}{\pi(1-D)} \quad (3.1)$$

Table 3.3 Average output voltage vs duty cycle of the converter of Figure 3.1.

Duty Cycle	$V_{OAV}$ (Theoretical)	$V_{OAV}$ (Simulation)
0.1	21.22	29.578
0.2	23.87	32.789
0.3	27.28	36.759
0.4	31.83	41.761
0.5	38.197	48.224
0.6	47.746	56.822
0.7	63.660	68.557
0.8	95.492	84.872
0.9	190.985	150.096

### 3.2 Diode-Capacitor Assisted Output Switched AC to DC Boost Converter

The single phase hybrid AC to DC boost converter is derived from the idea of hybrid DC to DC boost converter. In this proposed converter, the diode-capacitor network is introduced instead of boost diode. The converter is shown in Figure 3.4. The circuit is the adoption of hybrid DC to DC converter for AC to DC conversion [44].

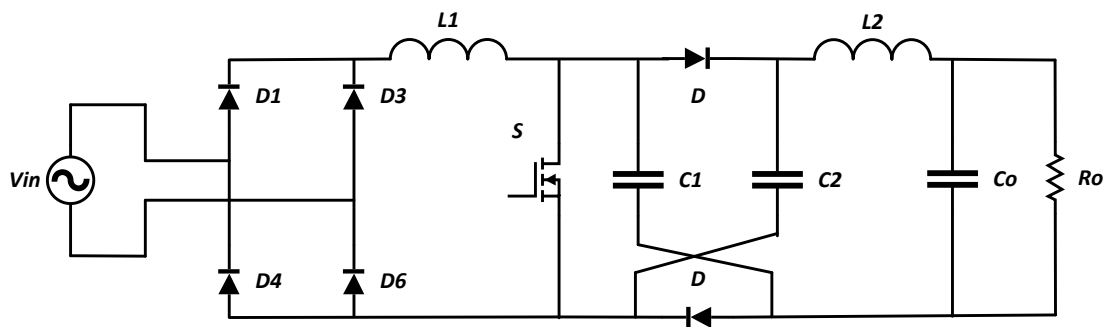
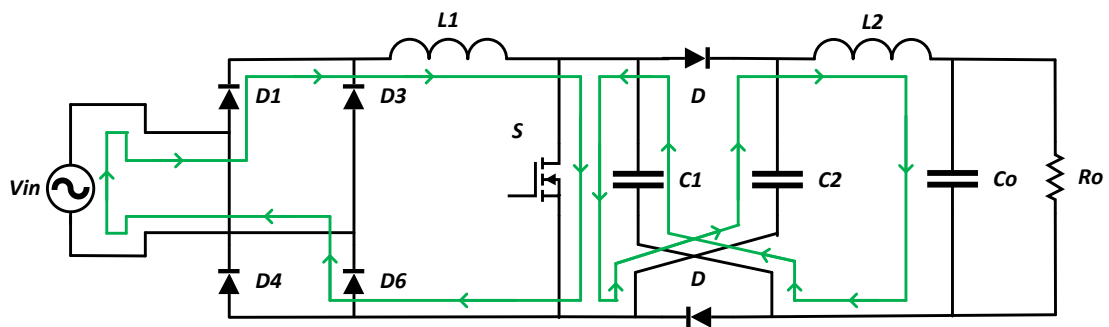


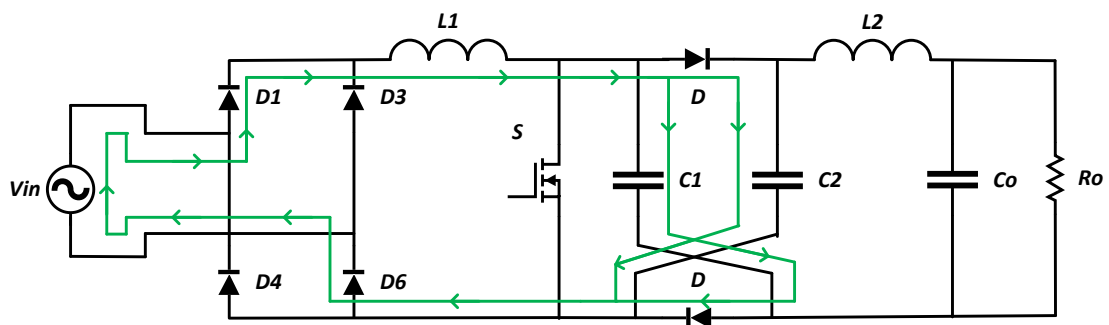
Figure 3.4 Proposed diode-capacitor assisted output switched AC to DC boost converter.

### 3.2.1 Principle of Operation

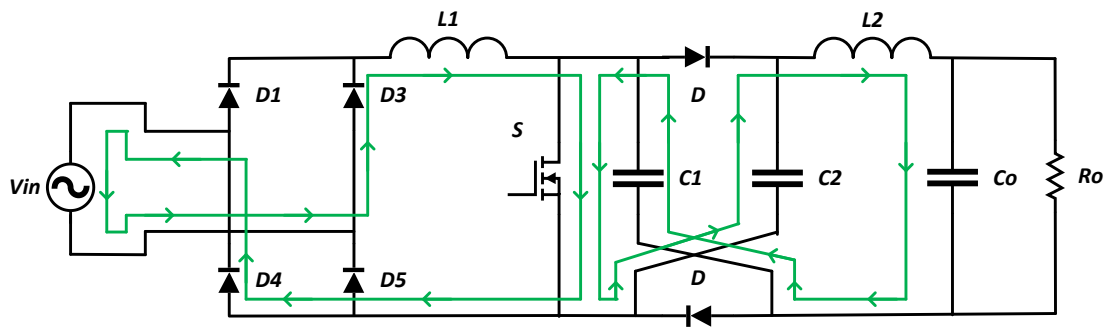
The four working stages of the conventional converter is illustrated in Figure 3.5, where Figure 3.5 (a) and (b) are for switch ON and OFF condition during positive supply cycle and Figure 3.5 (c) and (d) are for switch ON and OFF during negative cycle. When the switch is ON during positive half cycle the boost inductor charges from the source through the short circuit of the source and the output capacitor charges from the hybrid capacitor in series. As the switch turns OFF, the source and the inductor voltage forward biases the output diodes and charges the hybrid capacitors in parallel. Same phenomenon takes place during the negative supply cycle as the output of the diode rectifier has same polarity.



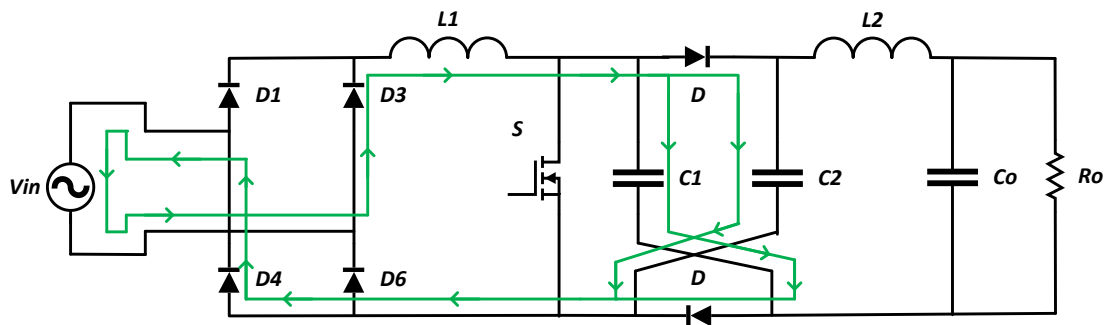
(a)



(b)



(c)



(d)

Figure 3.5 Four steps of operation of the converter in Figure 3.4,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.2.2 Open Loop Simulation

The simulation of the circuit of Figure 3.4 is carried out with the parameters of Table 3.4. The results of the simulation is given in Table 3.5.

Table 3.4 Parameters of the converter of Figure 3.4.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	5 mH, 2 mH
Capacitors, $C_1, C_2$ $C_o$	10 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.5 Simulation results of the converter of Figure 3.4.

Voltage Gain	$V_o$	Efficiency	THD	PFi
1.111	316.824	97.012	77.662	0.787
1.250	354.387	96.983	71.718	0.775
1.428	402.703	96.918	66.545	0.829
1.667	464.752	96.761	60.505	0.845
2.000	545.117	96.398	54.461	0.864
2.500	646.125	95.838	45.553	0.852
3.333	805.638	94.614	35.145	0.827
5.000	1018.90	92.105	44.337	0.791
10.00	1290.80	67.804	36.531	0.921

### 3.2.3 Ideal Voltage gain Expression

The comparison of the theoretical and simulated voltage gain is shown in Table 3.6 for an AC input voltage of 30V<sub>P</sub>. Circuit diagram with voltage labels is shown in Figure 3.6.

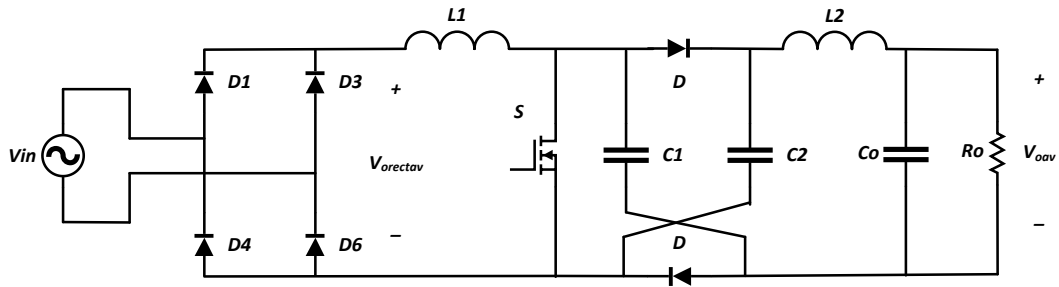


Figure 3.6 Proposed diode-capacitor assisted output switched AC to DC boost converter with voltage labels for positive half cycle of operation.

The rectified average voltage after the conventional bridge is,

$$V_{orectav} = \frac{V_{in\max}}{\pi} \int_0^{\pi} \sin \theta d\theta = \frac{2V_{in\max}}{\pi}$$

For DC-DC boost converter,

$$\frac{(1+D)}{(1-D)} V_{orectav} = V_{oav}$$

Where,  $D = \text{Duty Cycle} = \frac{T_{ON}}{T}$ ,  $(1-D) = \frac{T_{OFF}}{T}$  and  $T = \text{Switching Frequency}$

Therefore the output voltage can be written as,

$$V_{oav} = \frac{2(1+D)V_{in\max}}{\pi(1-D)} \quad (3.2)$$

Table 3.6 Average output voltage vs duty cycle of the converter of Figure 3.4.

Duty Cycle	$V_{OAV}$ (Theoretical)	$V_{OAV}$ (Simulation)
0.1	23.342	30.639
0.2	28.647	36.589
0.3	35.469	43.698
0.4	44.563	52.144
0.5	57.295	62.161
0.6	76.394	73.822
0.7	108.225	90.878
0.8	171.887	134.756
0.9	362.873	217.913

### 3.3 Input Switched Full-Bridge AC to DC Boost Converter

The high frequency switching can be done at the input side of the converter. The converter works as high frequency chopper. The near sinusoidal chopped high frequency current is improved easily by the boost inductor. The converter is shown in Figure 3.7. During the positive half cycle as the switch turns ON and OFF the input inductor is charged by the input voltage when the switch is ON and the output capacitor is charged by the input voltage and inductor charge when switch is OFF. Same process repeats during the negative supply cycle. The operation in four modes of the converter is illustrated in section 3.3.1 (through Figures 3.8 (a) – 3.8(d))

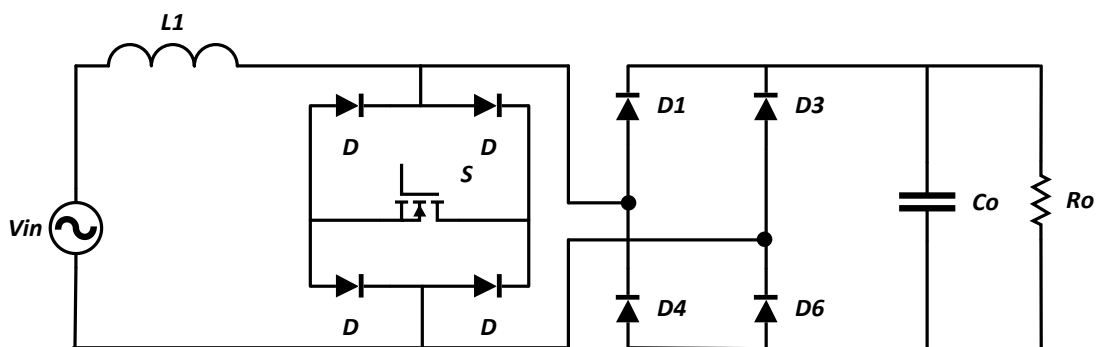
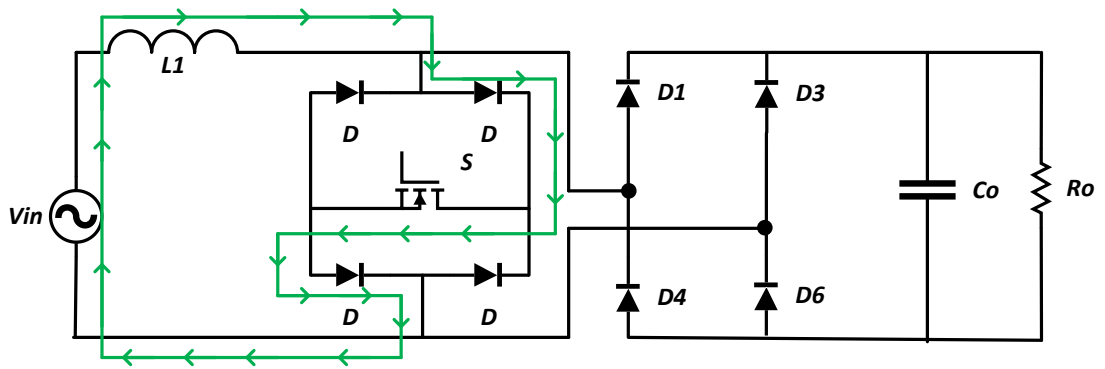


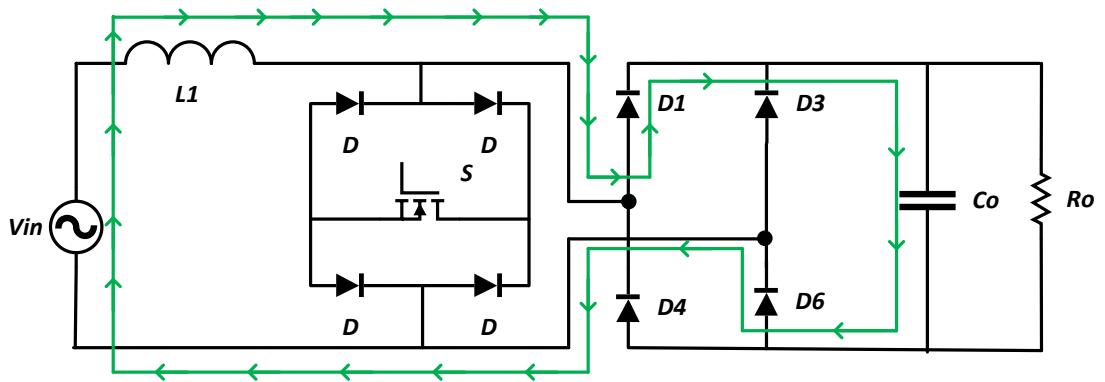
Figure 3.7 Input switched full-bridge AC to DC boost converter.

### 3.3.1 Principle of operation

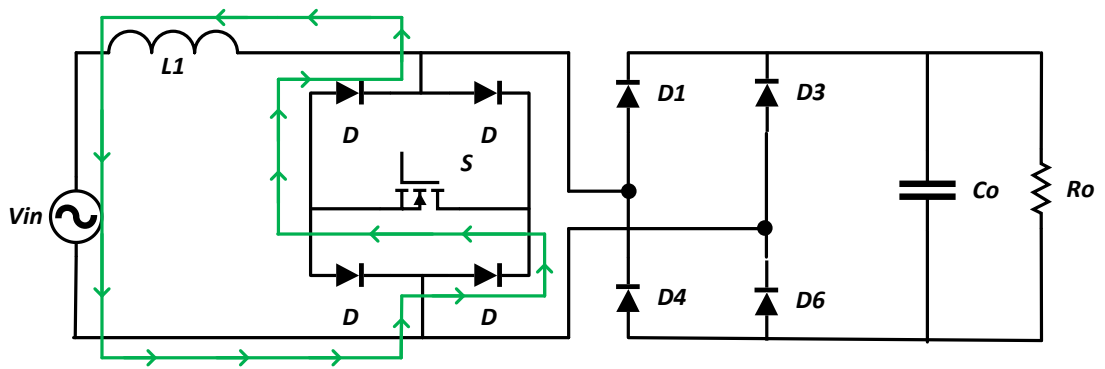
The four working stages of the conventional converter is illustrated in Figure 3.8.



(a)



(b)



(c)



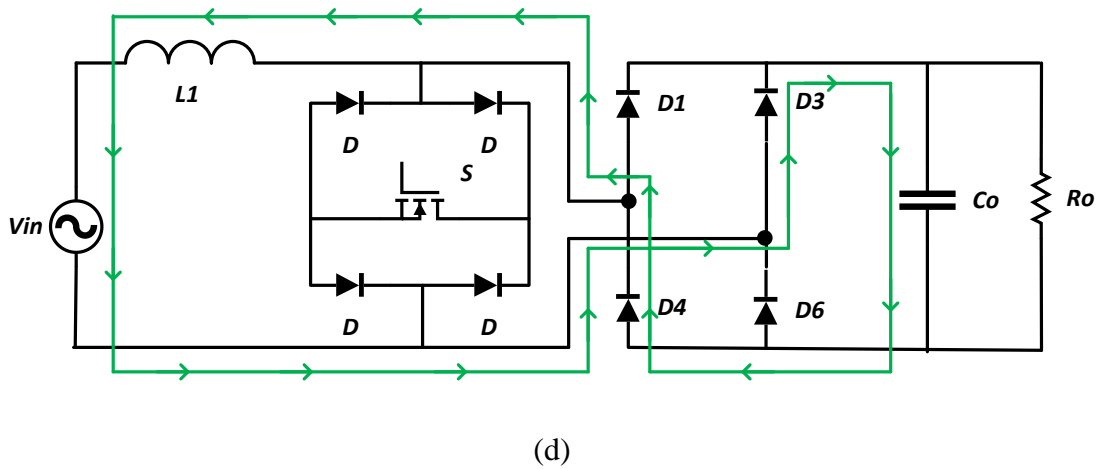


Figure 3.8 Four steps of operation of the converter in Figure 3.7,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.3.2 Open Loop Simulation

The simulation of the circuit of Figure 3.7 is carried out with the parameters of Table 3.7. The results of the simulation is given in Table 3.8.

Table 3.7 Parameters of the converter of Figure 3.7.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_o$	220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.8 Simulation results of the converter of Figure 3.7.

Voltage Gain	Vo	Efficiency	THD	PFi
1.111	320.110	97.806	87.984	0.770
1.250	357.542	97.636	83.750	0.789
1.428	404.278	97.441	77.675	0.810
1.667	463.903	97.115	70.857	0.820
2.000	543.102	96.668	61.970	0.832
2.500	650.634	95.915	51.733	0.831
3.333	804.189	94.571	38.913	0.812
5.000	1008.60	91.407	22.148	0.751
10.00	968.761	68.097	4.049	0.527

### 3.3.3 Ideal Voltage Gain Expression

The expression of ideal voltage gain of the input switched boost single phase AC to DC converter is derived with the help of Figure 3.9

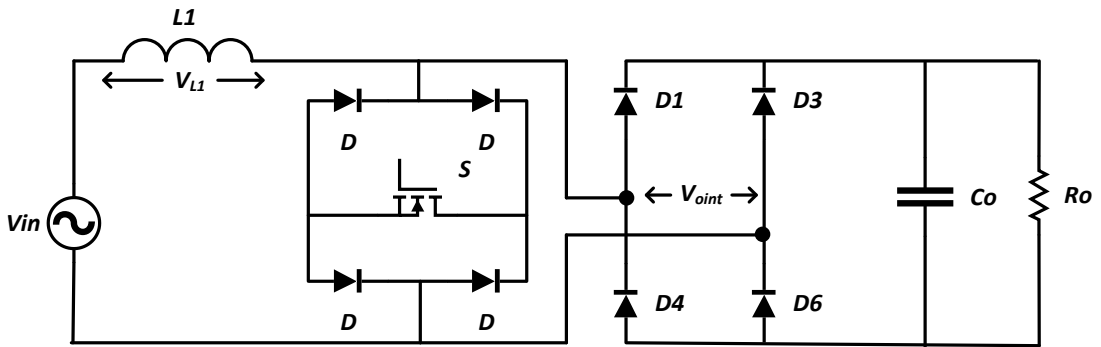


Figure 3.9 Input switched full-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.

When switch is ON,

$$v_L = v_{in}$$

When switch is OFF,

$$v_L = v_{in} - v_{o_{int}}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_L dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{o_{int}}) dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_L dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{o_{int}}) dt \quad (3.3)$$

Suppose,

$$v_{o_{int}} = V_{o_{int\max}} \sin(\omega t - \theta_o)$$

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

From (3.3),

$$\begin{aligned} \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt &= - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{o_{int}}) dt \\ \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{in\max} \sin(\omega t - \theta_{in}) dt &= \\ - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{in\max} \sin(\omega t - \theta_{in}) dt - V_{o_{int\max}} \sin(\omega t - \theta_o)] dt \end{aligned}$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} =$$

$$+ \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{oint\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

Or,

$$- \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right]$$

$$= \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right]$$

$$- \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right]$$

Or,

$$\sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] =$$

$$\sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]$$

Or,

$$\sum_{n=1}^N \frac{V_{in\max}}{\omega} [\cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in})] =$$

$$\sum_{n=1}^N \frac{V_{oint\max}}{\omega} [\cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o)]$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] =$$

Or,

$$\sum_{n=1}^N \frac{V_{oint\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right]$$

$$\text{Or, } \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] =$$

$$\sum_{n=1}^N V_{o\text{int}\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]$$

$$\text{Or, } \frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\sum_{n=1}^N V_{o\text{int}\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or, } \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] = \sum_{n=1}^N V_{o\text{int}\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

$$\text{Or, } \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] = \sum_{n=1}^N V_{o\text{int}\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

$$\text{Or, } \sum_{n=1}^N V_{o\text{int}\max} \left[ \sin(\omega t_i - \theta_o) \right] = \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right]$$

So the average output voltage  $V_{OAV}$  can be derived as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{o\text{int}\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{V_{in\max}}{1-D} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{V_{in\max}}{\pi(1-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{V_{in\max}}{\pi(1-D)} [-\cos\theta]_0^\pi$$

$$\text{Or, } V_{OAV} = \frac{2V_{in\max}}{\pi(1-D)} \quad (3.4)$$

The comparison of the theoretical and simulated voltage gain is shown in Table 3.9 for an AC input voltage of 30V<sub>p</sub>. The simulated gain value deviates the ideal value significantly after duty cycle 0.8. This is due to non-ideal behaviour of components which is not considered in the expression obtained by theoretical methods.

Table 3.9 Average output voltage vs duty cycle of the converter of Figure 3.5.

Duty Cycle	V <sub>OAV</sub> (Theoretical)	V <sub>OAV</sub> (Simulation)
0.1	21.22	30.509
0.2	23.87	33.646
0.3	27.28	38.435
0.4	31.83	42.427
0.5	38.197	48.146
0.6	47.746	57.458
0.7	63.660	69.128
0.8	95.492	84.990
0.9	190.985	87.203

### 3.4 Diode-Capacitor Assisted Input Switched Full-Bridge AC to DC Boost Converter

The input switched full bridge converter is designed by introducing two separate diode-capacitor network, each for individual half cycle of line frequency operation. Though the conduction and switching losses remain same, the circuit complexity of the converter increases. The component count is also high. So the setup cost will also be high. The proposed converter is shown in Figure 3.10.

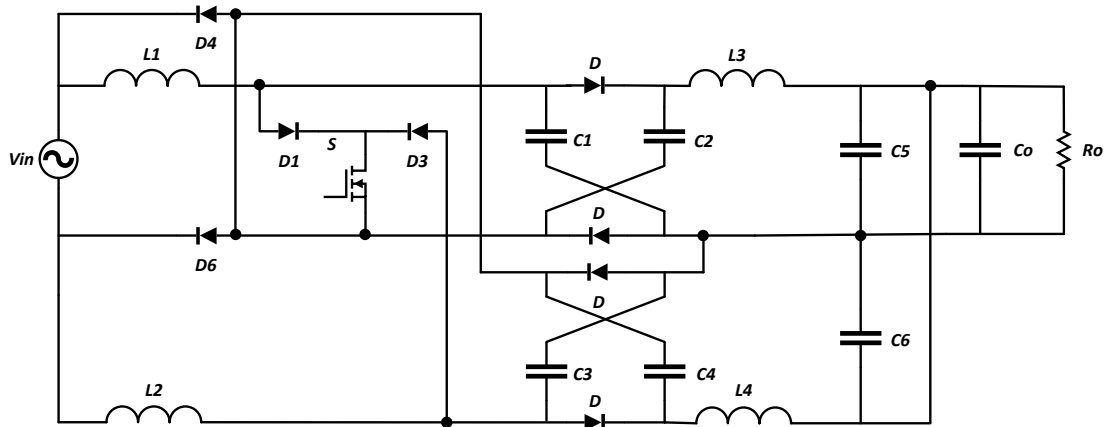
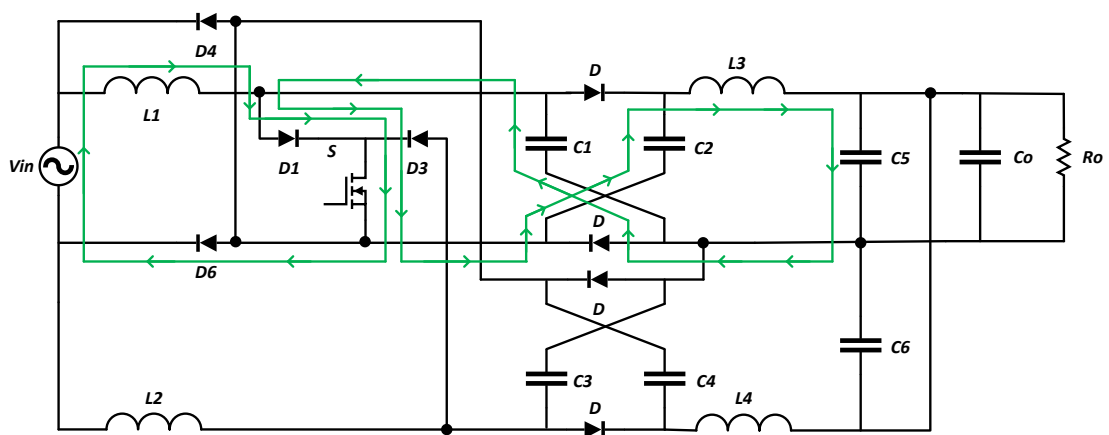


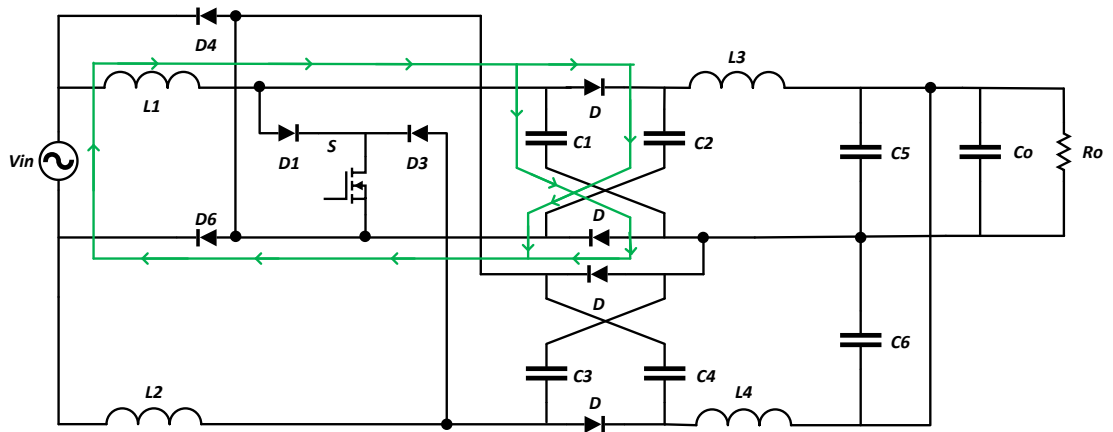
Figure 3.10 Proposed diode-capacitor assisted input switched full-bridge AC to DC converter.

### 3.4.1 Principle of Operation

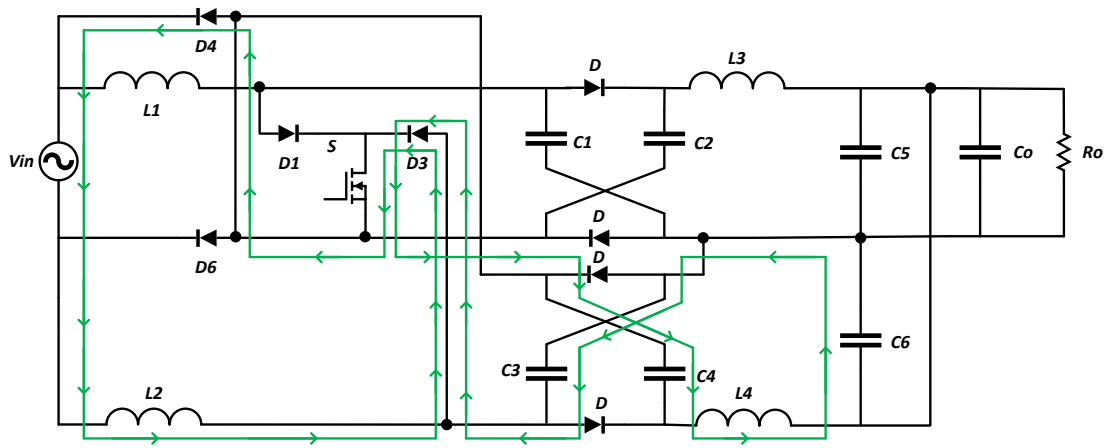
The four working stages of the conventional converter is illustrated in Figure 3.11 (a) to 3.11 (d). When the switch is ON, in the output stage the two intermediate capacitor charges the output capacitor in series at their added voltage. When the switch is OFF, the two intermediate capacitors are charged by the input source and inductor voltage. Similar action takes place during negative half cycle. The intermediate capacitors charging in parallel and the boost voltage has additional voltage boost at the output capacitor as they discharge in series to the output capacitor.



(a)

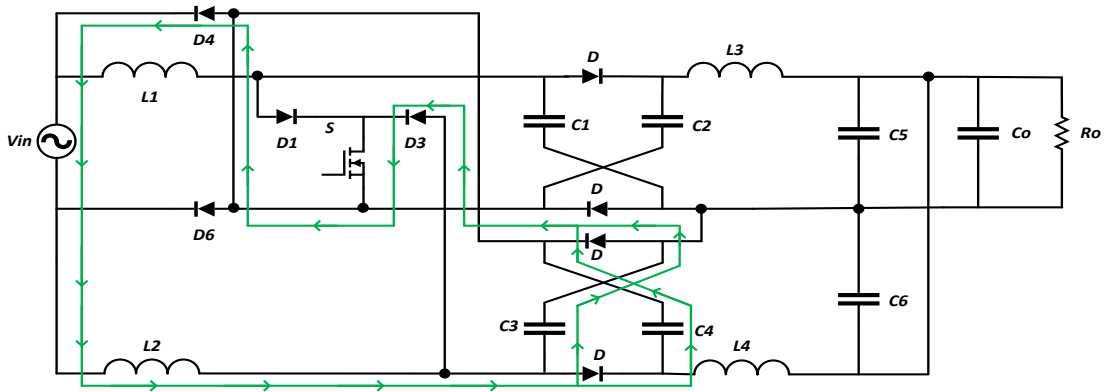


(b)



(c)





(d)

Figure 3.11 Four steps of operation of the converter in Figure 3.10,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.4.2 Open loop Simulation

The simulation of the circuit of Figure 3.10 is carried out with the parameters of Table 3.10. The results of the simulation is given in Table 3.11.

Table 3.10 Parameters of the converter of Figure 3.10.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 0.5 mH
Capacitors, $C_1-C_6$ $C_o$	22 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.11 Simulation results of the converter of Figure 3.10.

Voltage Gain	Vo	Efficiency	THD	PFi
1.111	320.539	97.405	66.864	0.836
1.250	355.822	97.373	40.686	0.923
1.428	403.260	97.301	22.585	0.973
1.667	464.134	97.138	15.479	0.837
2.000	543.825	96.740	10.477	0.987
2.500	651.011	96.208	7.742	0.978
3.333	804.340	94.969	9.6169	0.952
5.000	1007.00	92.147	16.283	0.892
10.00	1105.2	74.044	21.808	0.837

### 3.4.3 Ideal Voltage Gain Expression

The comparison of the theoretical and simulated voltage gain is shown in Table 3.12 for an AC input voltage of 30V<sub>P</sub>. The average output voltage of the converter of Figure 3.10 can be derived according to Section 3.3.3 as,

$$V_{OAV} = \frac{(1+D)}{(1-D)} \frac{2V_{in\max}}{\pi} \quad (3.5)$$

Where,  $D = \text{Duty Cycle} = \frac{T_{ON}}{T}$ ,  $(1-D) = \frac{T_{OFF}}{T}$  and  $T = \text{Switching Frequency}$ .

Table 3.12 Average output voltage vs duty cycle of the converter of Figure 3.10.

Duty Cycle	$V_{OAV}$ (Theoretical)	$V_{OAV}$ (Simulation)
0.1	23.342	31.508
0.2	28.647	37.930
0.3	35.469	44.774
0.4	44.563	52.960
0.5	57.295	63.999
0.6	76.394	75.814
0.7	108.225	90.302
0.8	171.887	100.298
0.9	362.873	96.841

### 3.5 Input Switched Half-Bridge AC-DC Boost Converter

The converter is designed from the conventional input switched converter. Half of the output bridge is replaced by splitting the output capacitor into two. Each of the capacitor is charged in each half cycle. The output voltage is the summation of the two voltages across the two capacitors. The converter is shown in Figure 3.12.

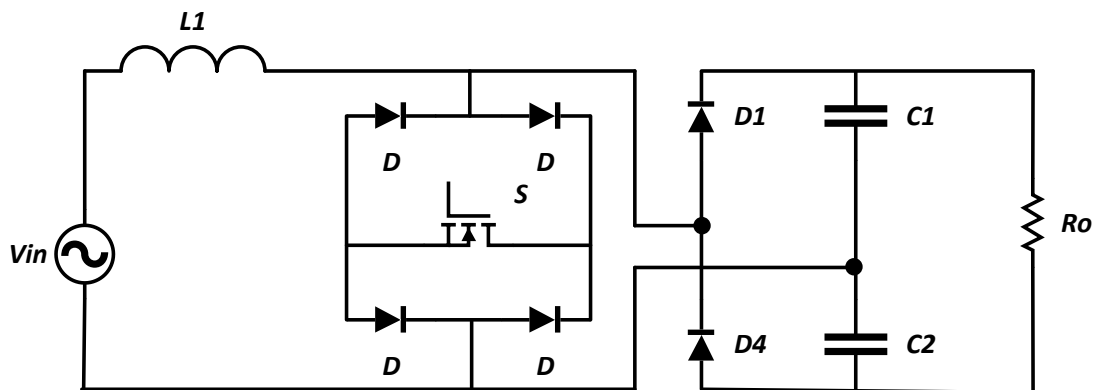
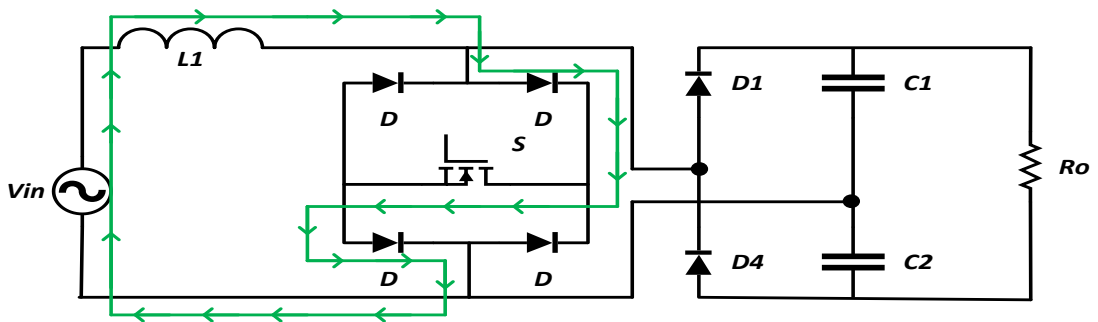


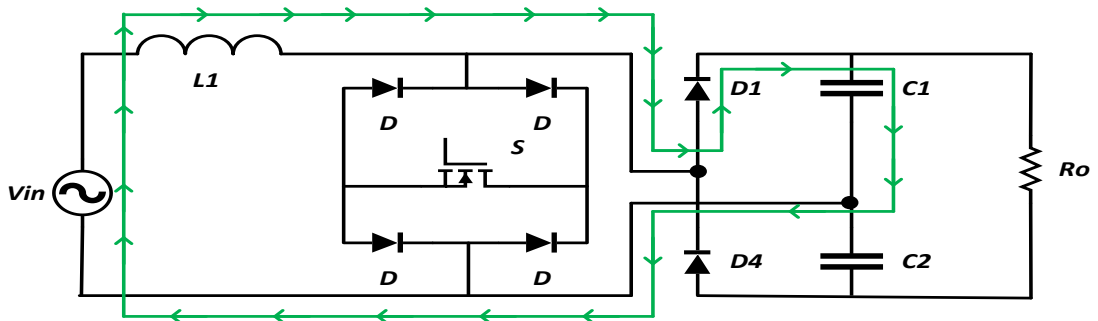
Figure 3.12 Input Switched half-bridge AC to DC boost converter.

### 3.5.1 Principle of Operation

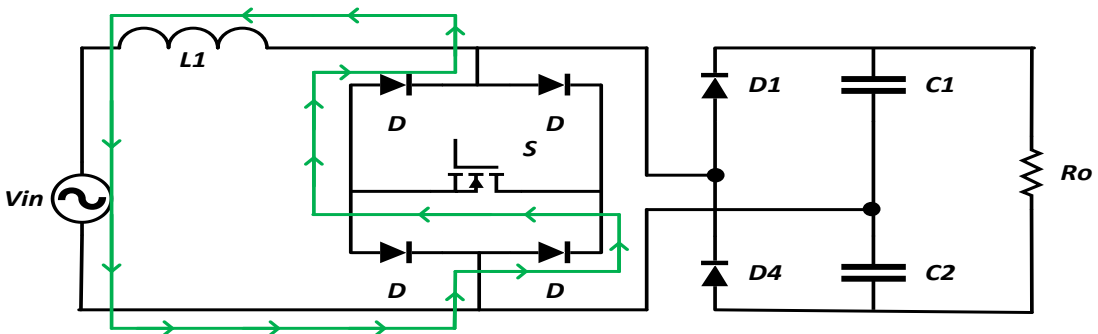
The four working stages of the conventional converter is illustrated Figure 3.13. In these circuits, when switch is ON during positive half cycle, input inductor is charged from the source through shorted switch. And during the OFF period of the switch input source and inductor voltage charges the upper output capacitor at boost voltage. Same actions takes place as the switch turns ON and OFF during negative supply cycle. But this time bottom output capacitor charges to the boost voltage.



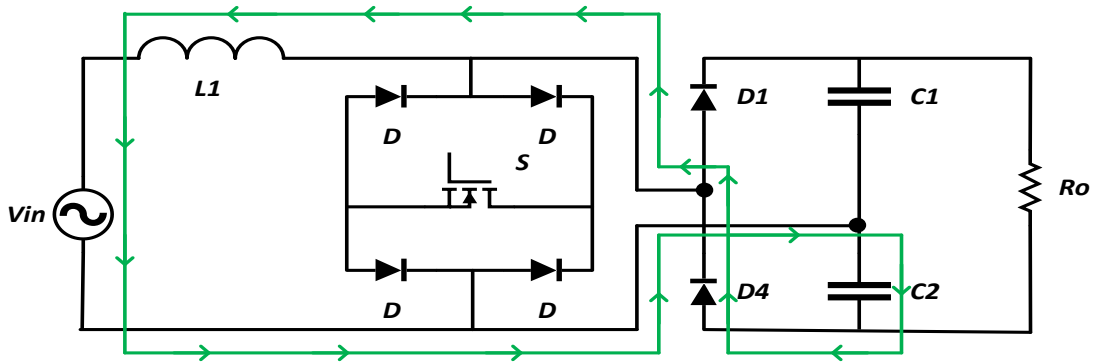
(a)



(b)



(c)



(d)

Figure 3.13 Four steps of operation of the converter in Figure 3.12,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.5.2 Open loop Simulation

The simulation of the circuit of Figure 3.12 is carried out with the parameters of Table 3.13. The results of the simulation is given in Table 3.14.

Table 3.13 Parameters of the converter of Figure 3.12.

Nominal input ac source voltage, $V_l$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_1, C_2$	220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.14 Simulation results of the converter of Figure 3.12.

Voltage Gain	Vo	Efficiency	THD	PFi
1.111	578.147	97.891	66.794	0.800
1.250	661.455	97.584	60.530	0.847
1.428	757.148	97.201	53.435	0.887
1.667	866.622	96.688	45.318	0.913
2.000	987.938	95.883	36.429	0.918
2.500	1115.5	94.451	26.327	0.887
3.333	1228.9	91.216	15.068	0.806
5.000	1059.3	66.078	4.667	0.670
10.00	580.104	30.418	6.7776	0.413

### 3.5.3 Ideal Voltage Gain Expression

Ideal voltage gain expression of the input switched AC to DC converter with split output capacitor is derived with help of Figure 3.14.

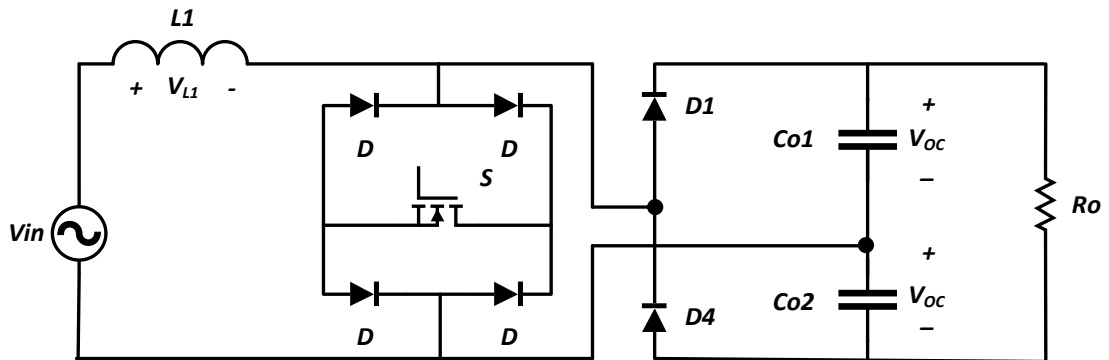


Figure 3.14 Input Switched half-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.

When switch is ON,

$$V_L = V_{in}$$

When switch is OFF,

$$V_L = v_{in} - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_L dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oc}) dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_L dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oc}) dt \quad (3.6)$$

Suppose,

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

From (3.6),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oc}) dt$$

Or,

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{in\max} \sin(\omega t - \theta_{in}) dt - V_{o\max} \sin(\omega t - \theta_o)] dt$$

After Integration,

$$\begin{aligned}
& \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} = \\
& + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\
& - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\
\text{Or,} \quad & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] \\
& - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] \\
\text{Or,} \quad & \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
& \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \\
\text{Or,} \quad & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
& \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\
\text{Or,} \quad & \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \begin{aligned} & 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2} \\ & \sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2} \end{aligned} \right]
\end{aligned}$$



$$\text{Or, } \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]$$

$$\text{Or, } \frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or, } \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] = \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

$$\text{Or, } \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] = \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

$$\text{Or, } \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right] = \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right]$$

Thus the average output voltage can be found as,

$$V_{OAV} = \frac{1}{\pi} \int_0^\pi 2 \times V_{o\max} \sin \theta d\theta \quad ; V_o = V_{oc} + V_{oc}$$

$$\text{Or, } V_{OAV} = \frac{2}{\pi} \int_0^\pi \frac{V_{in\max}}{1-D} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{2V_{in\max}}{\pi(1-D)} \int_0^\pi \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{2V_{in\max}}{\pi(1-D)} [-\cos\theta]_0^\pi$$

$$\text{Or, } V_{OAV} = \frac{4V_{in\max}}{\pi(1-D)} \quad (3.7)$$

The comparison of the theoretical and simulated voltage gain is shown in Table 3.15 for an AC input voltage of 30V<sub>P</sub>.

Table 3.15 Average output voltage vs duty cycle of the converter of Figure 3.12.

Duty Cycle	V <sub>OAV</sub> (Theoretical)	V <sub>OAV</sub> (Simulation)
0.1	42.44	57.080
0.2	47.74	64.803
0.3	54.56	73.510
0.4	63.66	83.286
0.5	76.394	92.788
0.6	95.492	104.528
0.7	127.32	113.285
0.8	190.984	103.933
0.9	381.97	54.311

### 3.6 Modified Input Switched AC to DC Boost Converter

The proposed converter is designed by moving the switch in between the diode bridge. The split output capacitor is used to step the voltage even higher. The proposed circuit is shown in Figure 3.15.

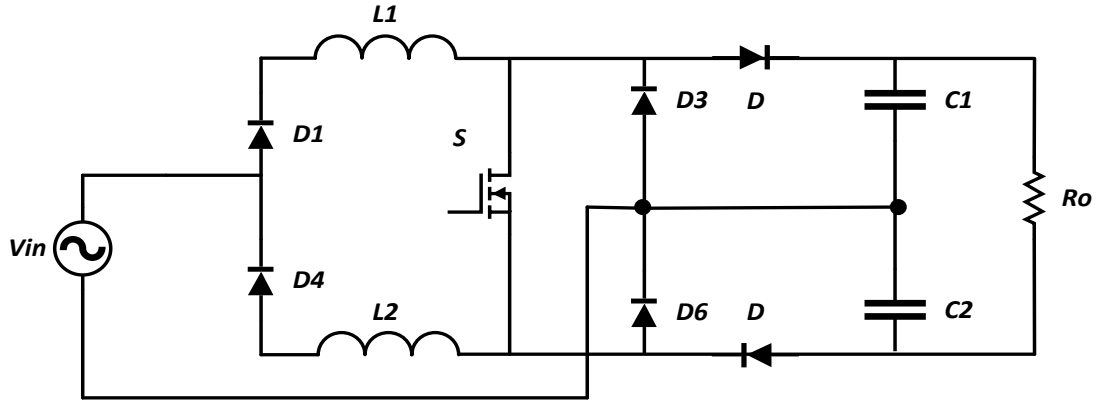
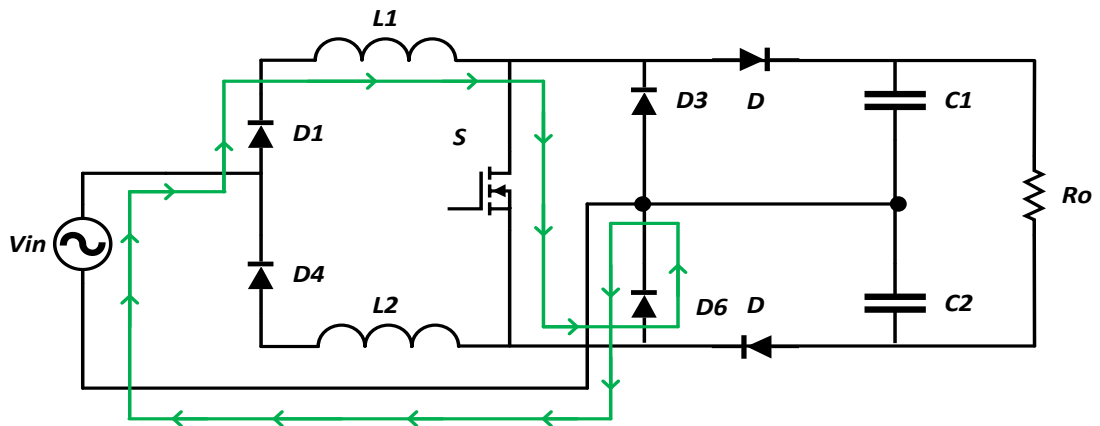


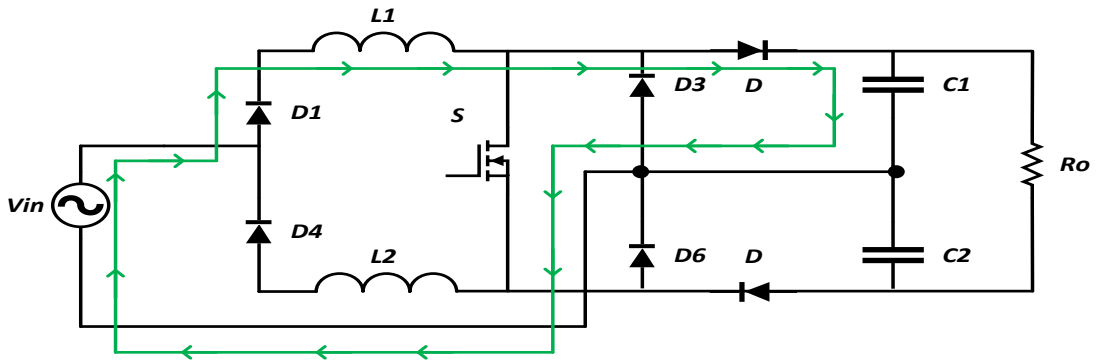
Figure 3.15 Proposed modified input switched AC to DC Boost Converter.

#### 3.6.1 Principle of Operation

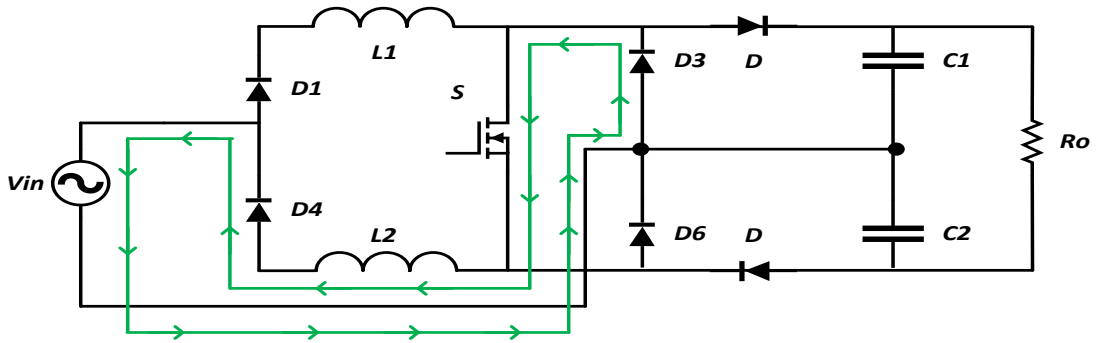
The four working stages of the conventional converter is illustrated in Figure 3.16 (a)-(d). Figures 3.16 (a) and (b) show the charging of upper inductor path when the switch is ON and charging of upper output capacitor when the switch is OFF (at input source and upper inductor voltage). Figure 3.16 (c) and (d) show the charging of lower inductor during switch ON in the negative half cycle and the charging of lower output capacitor by the input source and lower input inductor voltages.



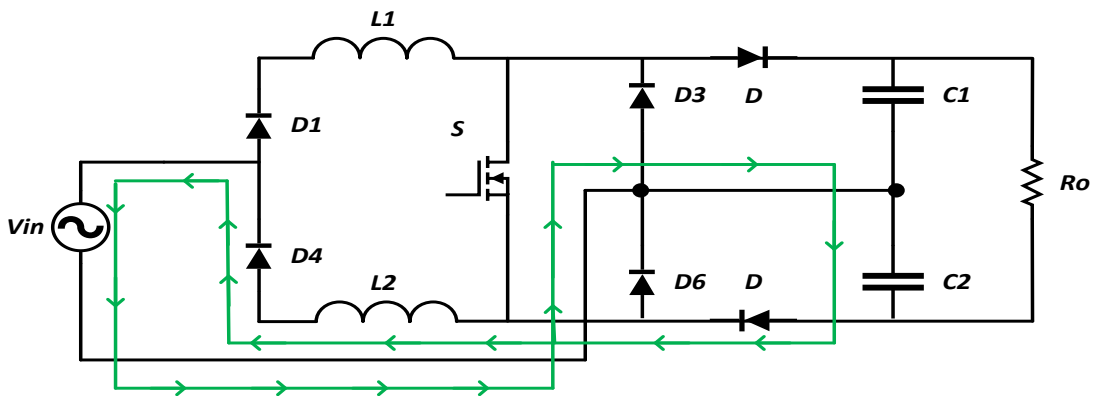
(a)



(b)



(c)



(d)

Figure 3.16 Four steps of operation of the converter in Figure 3.15,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.6.2 Open Loop Simulation

The simulation of the circuit of Figure 3.15 is carried out with the parameters of Table 3.16. The results of the simulation is given in Table 3.17.

Table 3.16 Parameters of the converter of Figure 3.15.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	5 mH
Capacitors, $C_1, C_2$	220 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.17 Simulation results of the converter of Figure 3.15.

Voltage Gain	$V_o$	Efficiency	THD	PFi
1.111	577.410	98.135	66.889	0.806
1.250	660.552	97.853	60.628	0.849
1.428	756.072	97.493	53.514	0.887
1.667	865.358	96.996	45.426	0.913
2.000	986.829	96.232	36.533	0.917
2.500	1114.6	94.803	26.429	0.886
3.333	1228.9	91.590	15.179	0.806
5.000	1128.2	66.341	7.458	0.753
10.00	733.786	27.259	17.216	0.687

### 3.6.3 Ideal Voltage Gain Expression

The comparison of the theoretical and simulated voltage gain is shown in Table 3.18 for an AC input voltage of  $30V_P$ . The proposed converter with voltage labels to derive the average output voltage is shown in Figure 3.17.

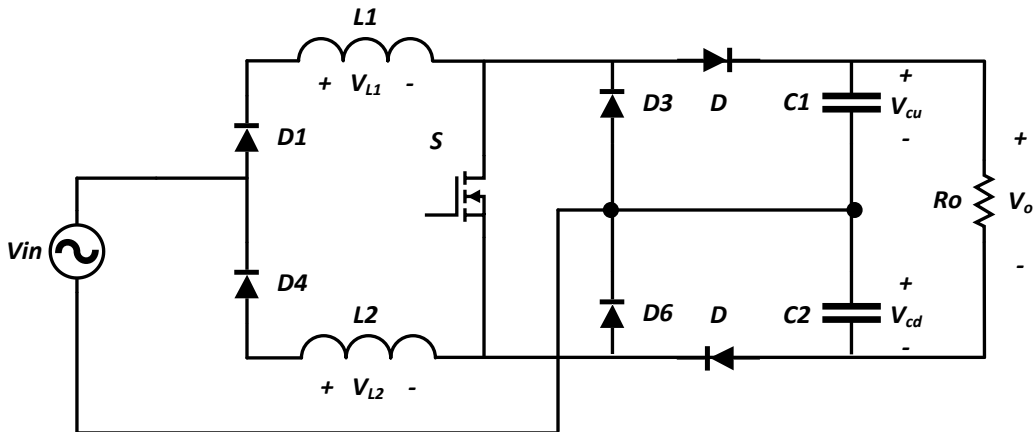


Figure 3.17 Proposed modified input switched AC to DC Boost Converter with voltage labels for positive half cycle of operation.

When switch is ON,

$$V_{L1} = V_{in}$$

When switch is OFF,

$$V_{L1} = V_{in} - V_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} V_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} V_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (V_{in} - V_{oc}) dt$$

Where,  $V_{oc} = V_{cu} = V_{cd}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oc}) dt \quad (3.8)$$

Suppose,

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

From (3.8),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oc}) dt$$

$$\begin{aligned} \text{Or, } & \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{in\max} \sin(\omega t - \theta_{in}) dt = \\ & - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{in\max} \sin(\omega t - \theta_{in}) dt - V_{o\max} \sin(\omega t - \theta_o)] dt \end{aligned}$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{sw}} = \\ & + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} - \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ \text{Or, } & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_o) \right] \end{aligned}$$

$$\text{Or, } \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] =$$

$$\sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]$$

$$\text{Or, } \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] =$$

$$\sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\text{Or, } \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] =$$

$$\sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2} \right]$$

$$\left[ \sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2} \right]$$

$$\text{Or, } \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]$$

$$\text{Or, } \frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$



Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or, } \frac{\frac{\omega T_{SW}}{2}}{(1-D)\frac{\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} [\sin(\omega t_i - \theta_{in})] = \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} [\sin(\omega t_i - \theta_{in})] = \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} [\sin(\omega t_i - \theta_{in})]$$

Thus the average output voltage can be found as,

$$V_{OAV} = \frac{1}{\pi} \int_0^\pi 2 \times V_{o\max} \sin \theta d\theta \quad ; V_o = V_{oc} + V_{oc}$$

$$\text{Or, } V_{OAV} = \frac{2}{\pi} \int_0^\pi \frac{V_{in\max}}{1-D} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{2V_{in\max}}{\pi(1-D)} \int_0^\pi \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{2V_{in\max}}{\pi(1-D)} [-\cos \theta]_0^\pi$$

$$\text{Or, } V_{OAV} = \frac{4V_{in\max}}{\pi(1-D)} \quad (3.9)$$

Table 3.18 Average output voltage vs duty cycle of the converter of Figure 3.15.

Duty Cycle	$V_{OAV}$ (Theoretical)	$V_{OAV}$ (Simulation)
0.1	42.44	55.637
0.2	47.74	62.913
0.3	54.56	70.940
0.4	63.66	79.625
0.5	76.394	88.507
0.6	95.492	96.470
0.7	127.32	100.840
0.8	190.984	96.089
0.9	381.97	65.871

### 3.7 Input Switched Coupled Capacitor Full-Bridge AC to DC Boost Converter

The converter is designed by introducing coupling capacitor to the boost configuration, which provided additional charging to the output capacitor thus maintains high voltage in relatively small duty cycle. The proposed converter also has limited step-down capability. Load isolation is also available due to coupling capacitor. The proposed converter is shown in Figure 3.18.

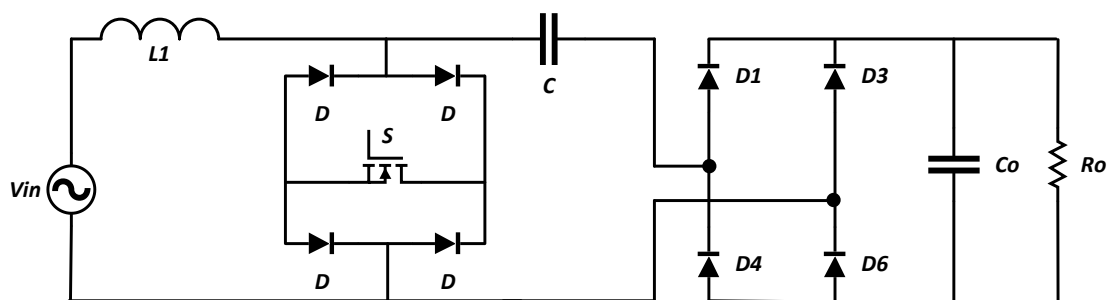
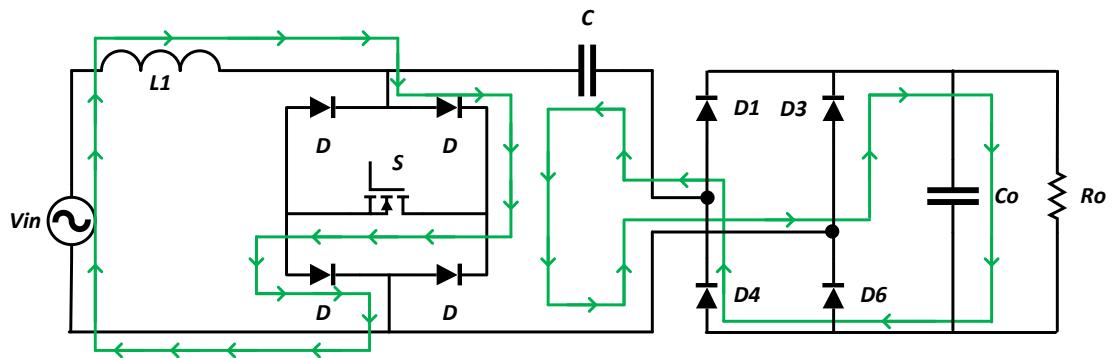


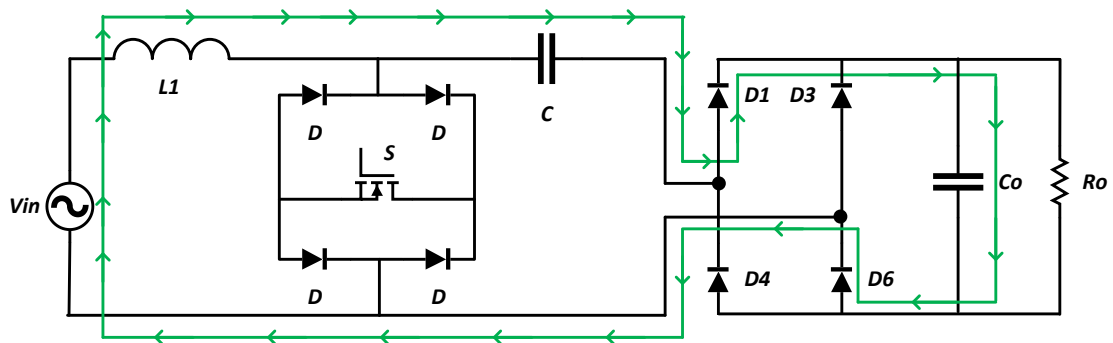
Figure 3.18 Proposed input switched coupled capacitor full-bridge AC to DC boost converter.

### 3.7.1 Principle of Operation

The four working stages of the conventional converter is illustrated in Figure 3.19. When the switch is ON during positive supply cycle, the inductor charges from the supply voltage and the intermediate capacitor charges the output capacitor through the switch and the two forward biased diodes of the output stage. When the switch is OFF, source and the inductor voltage charges the intermediate and output capacitor equally in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)



(b)

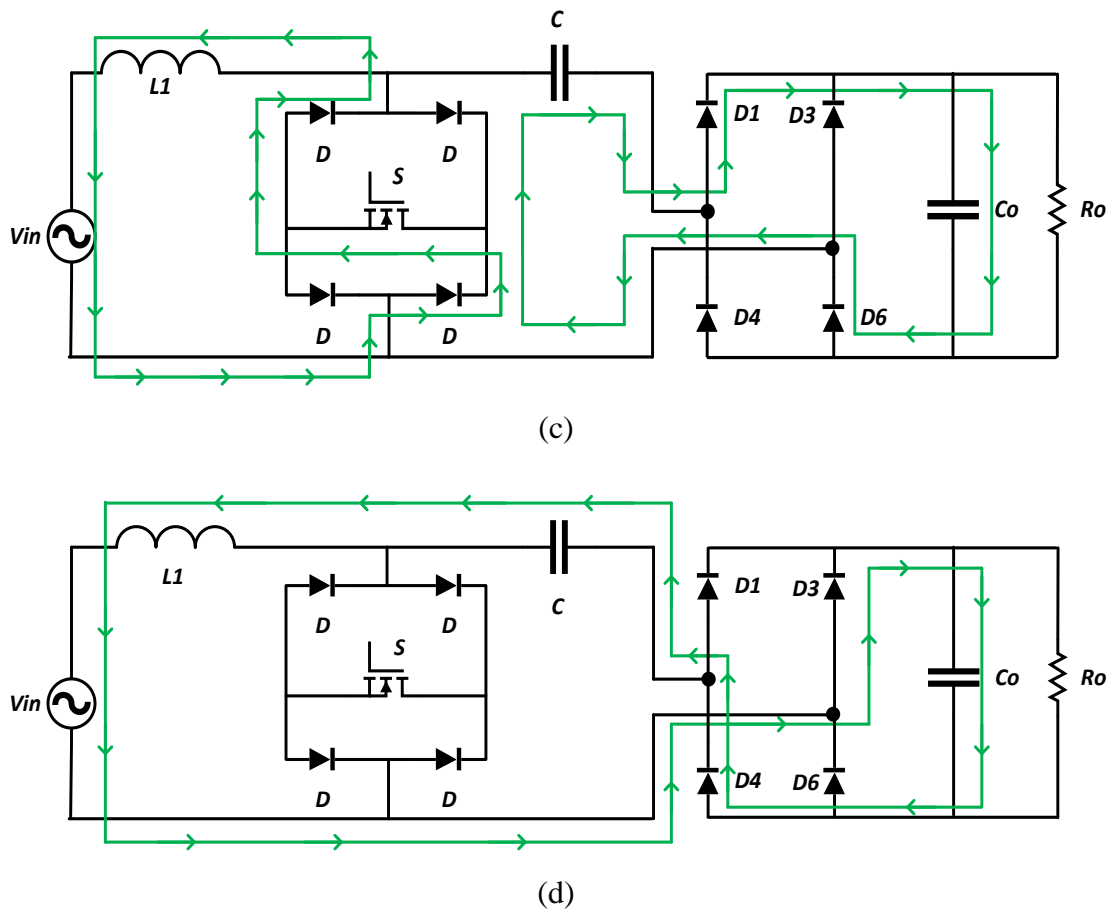


Figure 3.19 Four steps of operation of the converter in Figure 3.18,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.7.2 Open Loop Simulation

The simulation of the circuit of Figure 3.18 is carried out with the parameters of Table 3.19. The results of the simulation is given in Table 3.20.

Table 3.19 Parameters of the converter of Figure 3.18.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_I$	5 mH
Capacitors, $C_o$ $C$	220 $\mu$ F 22 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.20 Simulation results of the converter of Figure 3.18.

Voltage Gain	$V_o$	Efficiency	THD	PFi
1.111	152.690	95.535	92.919	0.635
1.250	175.697	96.395	110.43	0.649
1.428	201.279	96.605	126.69	0.644
1.667	234.544	96.473	119.51	0.639
2.000	280.825	95.508	107.36	0.638
2.500	367.002	93.288	82.174	0.682
3.333	527.742	89.664	57.778	0.790
5.000	809.266	82.668	34.311	0.934
10.00	1087.50	61.012	8.0458	0.922

### 3.7.3 Ideal Voltage Gain Expression

Ideal voltage gain expression of the proposed circuit is derived with help of Figure 3.20.

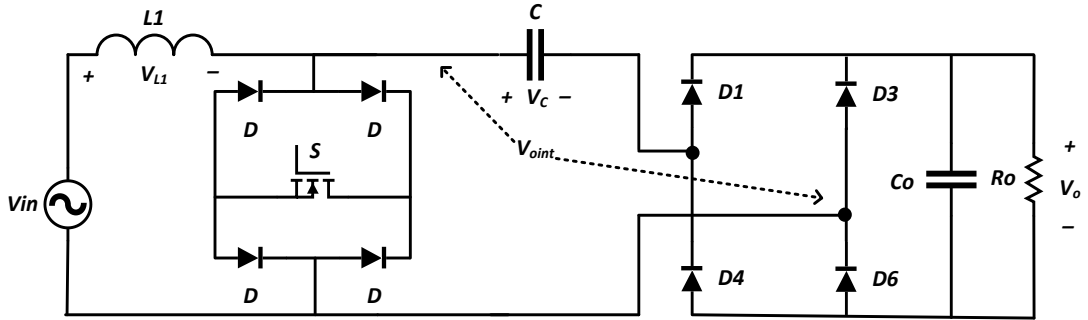


Figure 3.20 Proposed input switched coupled capacitor full-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.

Assume,

$$v_{in} = v_{inmax} \sin \omega t$$

$$v_c = v_{cmax} \sin \omega t$$

$$v_o = v_{omax} \sin \omega t$$

$$v_{int} = v_{intmax} \sin \omega t$$

When switch is ON,

$$v_{L1} = v_{in} - 0$$

$$v_c = v_o$$

When switch is OFF,

$$v_L = v_{in} - v_{oint} \quad ; \text{ Where } v_{oint} = v_c + v_o$$

$$v_c = v_{oint} - v_o$$

For one generalized switching cycle,

$$\int_{t_i}^{t_i+T_{sw}} v_L dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oint}) dt$$

Volt-sec balance over one supply frequency cycle (50Hz or 60Hz) is equal to zero. If  $T_{sup} = NT_{sw}$ , where N is the switching per cycle. Thus over a supply frequency cycle,

$$\int di_L(t) = \frac{1}{L} \int v_L(t) = 0$$

$$\sum_{i=1}^N \int_{t_i}^{t_i+T_{sw}} v_L dt = 0 = \sum_{i=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{i=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oint}) dt$$

$$\sum_{i=1}^N \int_{t_i}^{t_i+T_{sw}} V_{inmax} dt + \sum_{i=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (V_{inmax} \sin \omega t - V_{ointmax} \sin(\omega t - \theta)) dt = 0$$

After integration,

$$\sum_{i=1}^N \left[ -\frac{V_{inmax}}{\omega} \cos \omega t \right]_{t_i}^{t_i+DT_{sw}} + \sum_{i=1}^N \left[ -\frac{V_{inmax}}{\omega} \cos \omega t + \frac{V_{ointmax}}{\omega} \cos(\omega t - \theta) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} = 0$$

Which leads to,

$$\sum_{i=1}^N \left\{ \begin{aligned} & -\frac{V_{inmax}}{\omega} \cos \omega(t_i + DT_{sw}) + \frac{V_{inmax}}{\omega} \cos \omega t_i \\ & -\frac{V_{inmax}}{\omega} \cos \omega(t_i + T_{sw}) + \frac{V_{inmax}}{\omega} \cos \omega(t_i + DT_{sw}) \\ & + \frac{V_{ointmax}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta) - \frac{V_{ointmax}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta) \end{aligned} \right\} = 0$$

Rearranging the following can be obtained,

$$\begin{aligned} & \sum_{i=1}^N -\frac{V_m}{\omega} \{ \cos \omega t_i - \cos \omega(t_i + T_{sw}) \} = \\ & \sum_{i=1}^N -\frac{V_{ointmax}}{\omega} \{ \cos(\omega t_i + \omega DT_s - \theta) - \cos(\omega t_i + \omega T_{sw} - \theta) \} \end{aligned} \quad (3.10)$$

Using following identity

$$\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$$

Equation (3.10) can be written as,

$$\begin{aligned} & \sum_{i=1}^N -V_{inmax} 2 \sin \frac{\omega t_i + \omega t_i + \omega T_{SW}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \omega t_i}{2} = \\ & \sum_{i=1}^N -V_{ointmax} \left\{ \begin{array}{l} 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta + \omega t_i + \omega T_{SW} - \theta}{2} \times \\ \sin \frac{\omega t_i + \omega T_{SW} - \theta - \omega t_i - \omega DT_{SW} + \theta}{2} \end{array} \right\} \end{aligned}$$

Which can be written as,

$$\begin{aligned} & \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) \sin \left( \frac{\omega T_{SW}}{2} \right) = \\ & \sum_{i=1}^N V_{ointmax} \sin \left[ \left( \omega t_i - \theta \right) + \frac{(1+D)\omega T_{SW}}{2} \right] \sin \left[ \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

Which can be written as,

$$\begin{aligned} & \frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) = \\ & \sum_{i=1}^N V_{ointmax} \sin \left[ \left( \omega t_i - \theta \right) + \frac{(1+D)\omega T_{SW}}{2} \right] \end{aligned}$$

Which can be written as,



$$\begin{aligned}
& \sum_{i=1}^N V_{o_{intmax}} \sin \left[ (\omega t_i - \theta) + \frac{(1+DT_{SW})\omega T_{SW}}{2} \right] = \\
& \frac{\frac{\sin \frac{\omega T_{SW}}{2}}{\frac{\omega T_{SW}}{2}} \times \frac{\omega T_{SW}}{2}}{\frac{\sin \frac{(1-D)\omega T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \frac{(1-D)\omega T_{SW}}{2}}{2}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) \quad (3.11)
\end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\begin{aligned}
& \sum_{i=1}^N V_{o_{intmax}} \sin \left[ (\omega t_i - \theta) + \frac{(1+DT_{SW})\omega \times 0}{2} \right] = \\
& \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega \times 0}{2} \right)
\end{aligned}$$

$$\text{Or, } \sum_{i=1}^N V_{o_{intmax}} \sin [(\omega t_i - \theta)] = \frac{1}{(1-D)} \sum_{i=1}^N V_{inmax} \sin(\omega t_i)$$

Which is an expression of boost voltage gain when maximum voltages of input/output sine waves are related by-

$$v_{o_{intmax}} = \frac{1}{1-D} v_{inmax}$$

$V_{o_{int}}$  is divided between C and the output capacitor (during OFF times of positive half cycle) equally due to high frequency switching and/or assumed equal small capacitors.

Therefore,

$$V_{o_{max}} = \frac{1}{2} \cdot V_{o_{intmax}} = \frac{1}{2} \cdot \frac{1}{1-D} V_{inmax}$$

So,

$$V_{OAV} = \frac{2}{\pi} \cdot \frac{1}{2(1-D)} V_{inmax} = \frac{1}{\pi} \cdot \frac{V_{inmax}}{1-D} \quad (3.12)$$

The comparison of the theoretical and simulated voltage gain is shown in Table 3.21 for an AC input voltage of 30V<sub>P</sub>.

Table 3.21 Average output voltage vs duty cycle of the converter of Figure 3.18.

Duty Cycle	V <sub>OAV</sub> (Theoretical)	V <sub>OAV</sub> (Simulation)
0.1	15.915	13.691
0.2	17.904	15.912
0.3	20.463	18.429
0.4	23.873	21.623
0.5	28.648	26.143
0.6	35.810	34.452
0.7	47.746	49.783
0.8	71.620	75.767
0.9	143.239	101.690

### 3.8 Input Switched Coupled Capacitor Half-Bridge AC to DC Boost Converter

The proposed converter is designed by introducing coupling capacitor in between the input switch and output half-bridge. The output capacitors get addition charge during T<sub>on</sub> of the switching period and thus have additional step-up capability. The converter is shown in Figure 3.21.

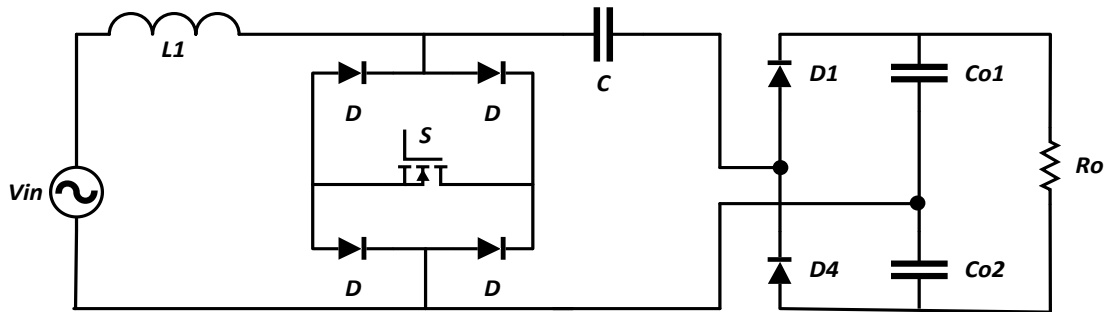
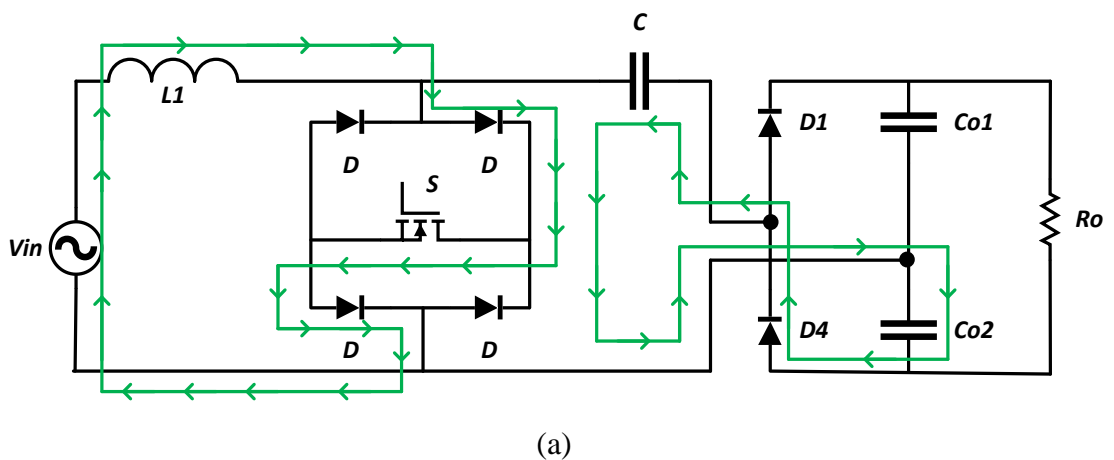


Figure 3.21 Proposed input switched coupled capacitor half-bridge AC to DC boost converter.

### 3.8.1 Principle of Operation

The four working stages of the conventional converter is illustrated in Figure 3.22. When the switch is ON during positive supply cycle, the inductor charges from the supply voltage and the intermediate capacitor charges the lower output capacitor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the intermediate and upper output capacitor equally in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



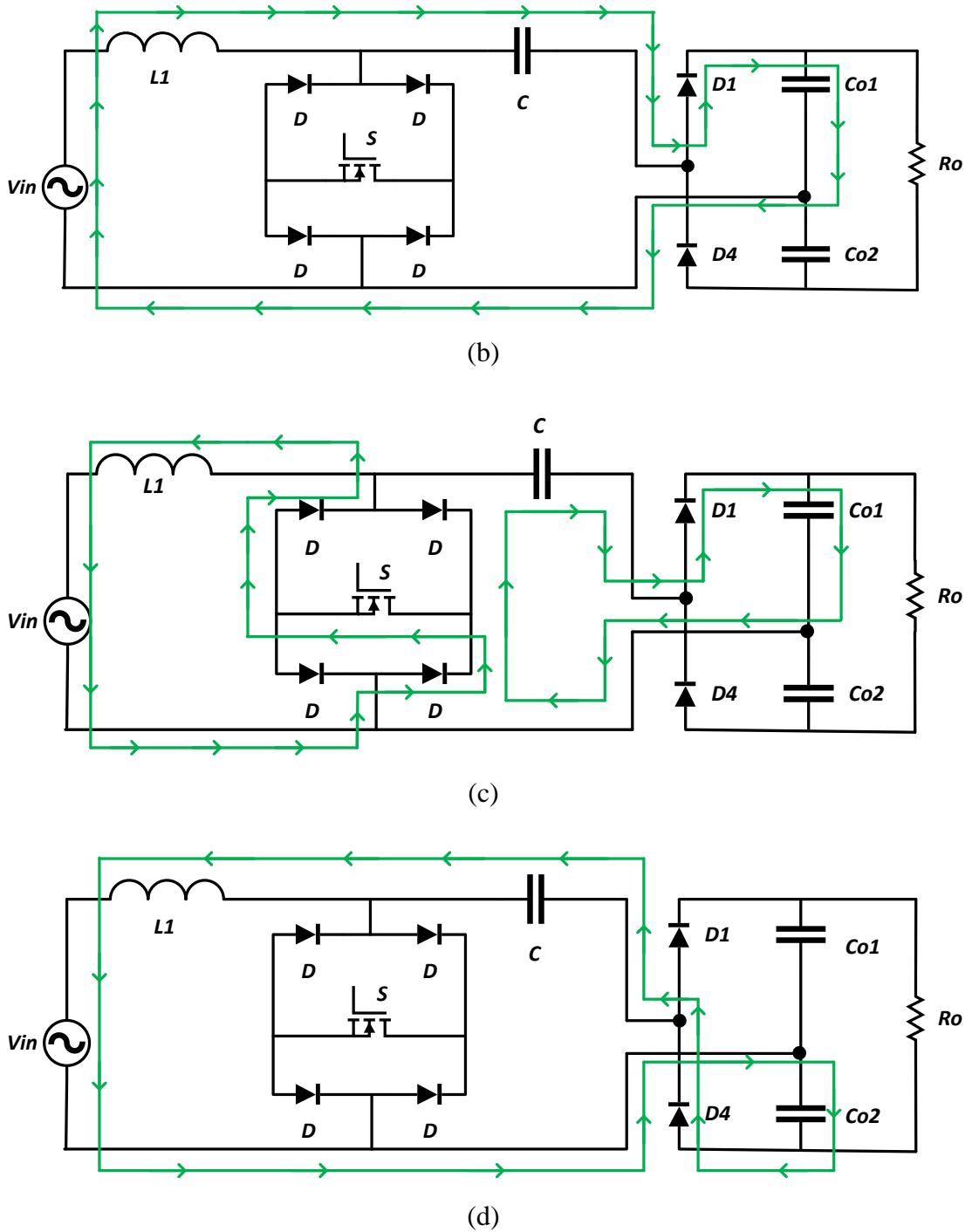


Figure 3.22 Four steps of operation of the converter in Figure 3.21,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 3.8.2 Open Loop Simulation

The simulation of the circuit of Figure 3.21 is carried out with the parameters of Table 3.19. The results of the simulation is given in Table 3.20.

Table 3.22 Parameters of the converter of Figure 3.21.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_{o1}, C_{o2}$ $C$	220 $\mu$ F 22 $\mu$ F
Resistor, $R_o$	100 $\Omega$

Table 3.23 Simulation results of the converter of Figure 3.21.

Voltage Gain	$V_o$	Efficiency	THD	PFi
1.111	251.888	81.172	64.747	0.816
1.250	296.276	84.312	67.249	0.833
1.428	341.113	85.628	58.344	0.871
1.667	396.912	86.065	44.195	0.912
2.000	473.365	85.387	31.231	0.944
2.500	583.010	83.119	22.425	0.969
3.333	741.282	78.684	15.651	0.989
5.000	934.680	69.120	8.1249	0.970
10.00	819.164	40.082	1.9483	0.714

### 3.8.3 Ideal Voltage Gain Expression

Ideal voltage gain expression of the proposed circuit is derived with help of Figure 3.23.

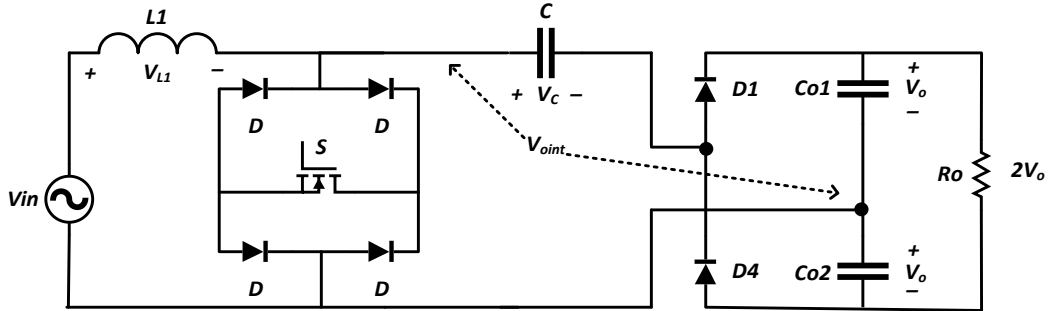


Figure 3.23 Proposed input switched coupled capacitor half-bridge AC to DC boost converter with voltage labels for positive half cycle of operation.

Assume,

$$v_{in} = v_{inmax} \sin \omega t$$

$$v_c = v_{cmax} \sin \omega t$$

$$v_o = v_{omax} \sin \omega t$$

$$v_{int} = v_{intmax} \sin \omega t$$

When switch is ON,

$$v_{L1} = v_{in} - 0$$

$$v_c = v_o$$

When switch is OFF,

$$v_L = v_{in} - v_{oint} \quad ; \text{ Where } v_{oint} = v_c + v_o$$

$$v_c = v_{oint} - v_o$$

For one generalized switching cycle,

$$\int_{t_i}^{t_i+T_{sw}} v_L dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oint}) dt$$

Volt-sec balance over one supply frequency cycle (50Hz or 60Hz) is equal to zero. If

$T_{Sup} = NT_{sw}$ , where N is the switching per cycle. Thus over a supply frequency cycle,

$$\int di_L(t) = \frac{1}{L} \int v_L(t) = 0$$

$$\sum_{i=1}^N \int_{t_i}^{t_i+T_{sw}} v_L dt = 0 = \sum_{i=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{i=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_{oint}) dt$$

$$\sum_{i=1}^N \int_{t_i}^{t_i+T_{sw}} V_{inmax} dt + \sum_{i=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (V_{inmax} \sin \omega t - V_{ointmax} \sin(\omega t - \theta)) dt = 0$$

After integration,

$$\sum_{i=1}^N \left[ -\frac{V_{inmax}}{\omega} \cos \omega t \right]_{t_i}^{t_i+DT_{sw}} + \sum_{i=1}^N \left[ -\frac{V_{inmax}}{\omega} \cos \omega t + \frac{V_{ointmax}}{\omega} \cos(\omega t - \theta) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} = 0$$

Which leads to,

$$\sum_{i=1}^N \left\{ \begin{array}{l} -\frac{V_{inmax}}{\omega} \cos \omega(t_i + DT_{sw}) + \frac{V_{inmax}}{\omega} \cos \omega t_i \\ -\frac{V_{inmax}}{\omega} \cos \omega(t_i + T_{sw}) + \frac{V_{inmax}}{\omega} \cos \omega(t_i + DT_{sw}) \\ + \frac{V_{ointmax}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta) - \frac{V_{ointmax}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta) \end{array} \right\} = 0$$

Rearranging the following can be obtained,

$$\begin{aligned} \sum_{i=1}^N -\frac{V_m}{\omega} \{ \cos \omega t_i - \cos \omega(t_i + T_{sw}) \} = \\ \sum_{i=1}^N -\frac{V_{ointmax}}{\omega} \{ \cos(\omega t_i + \omega DT_s - \theta) - \cos(\omega t_i + \omega T_{sw} - \theta) \} \end{aligned} \quad (3.13)$$

Using following identity

$$\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$$

Equation (3.13) can be written as,

$$\begin{aligned} & \sum_{i=1}^N -V_{inmax} 2 \sin \frac{\omega t_i + \omega t_i + \omega T_{SW}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \omega t_i}{2} = \\ & \sum_{i=1}^N -V_{ointmax} 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta + \omega t_i + \omega T_{SW} - \theta}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta - \omega t_i - \omega DT_{SW} + \theta}{2} \end{aligned}$$

Which can be written as,

$$\begin{aligned} & \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) \sin \left( \frac{\omega T_{SW}}{2} \right) = \\ & \sum_{i=1}^N V_{ointmax} \sin \left[ (\omega t_i - \theta) + \frac{(1+D)\omega T_{SW}}{2} \right] \sin \left[ \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

Which can be written as,

$$\begin{aligned} & \frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) = \\ & \sum_{i=1}^N V_{ointmax} \sin \left[ (\omega t_i - \theta) + \frac{(1+D)\omega T_{SW}}{2} \right] \end{aligned}$$

Which can be written as,

$$\begin{aligned} & \sum_{i=1}^N V_{ointmax} \sin \left[ (\omega t_i - \theta) + \frac{(1+DT_{SW})\omega T_{SW}}{2} \right] = \\ & \frac{\frac{\sin \frac{\omega T_{SW}}{2}}{\omega T_{SW}} \times \frac{\omega T_{SW}}{2}}{\frac{\sin \frac{(1-D)\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times \frac{(1-D)\omega T_{SW}}{2}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega T_{SW}}{2} \right) \end{aligned} \quad (3.14)$$



Using  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and as  $T_{SW} \rightarrow 0$  equation (3.14) reduces to,

$$\sum_{i=1}^N V_{o_{intmax}} \sin \left[ (\omega t_i - \theta) + \frac{(1 + DT_{SW}) \omega \times 0}{2} \right] = \frac{\frac{\omega T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \sum_{i=1}^N V_{inmax} \sin \left( \omega t_i + \frac{\omega \times 0}{2} \right)$$

$$\text{Or, } \sum_{i=1}^N V_{o_{intmax}} \sin [(\omega t_i - \theta)] = \frac{1}{(1-D)} \sum_{i=1}^N V_{inmax} \sin(\omega t_i)$$

Which is an expression of boost voltage gain when maximum voltages of input/output sine waves are related by-

$$v_{o_{intmax}} = \frac{1}{1-D} v_{inmax}$$

$V_{o_{int}}$  divides between C and upper output capacitor during OFF times (of positive half cycle) equally due to switching /and assumed equal small capacitors

$$\therefore v_{upper} \text{ during positive half cycle charges to maximum peak} = \frac{1}{2} \cdot \frac{1}{1-D} V_{inmax}$$

Mean-while lower capacitor charges at  $= \frac{1}{2} \cdot \frac{1}{2} \cdot \frac{1}{1-D} V_{inmax}$  also during OFF time at

$$v_c = \frac{1}{4} \cdot \frac{1}{1-D} v_{inmax}$$

Combined capacitor voltage across load is therefore full wave rectified wave of having

$$\text{maximum of } \frac{1}{2} \cdot \frac{1}{1-D} V_{inmax} + \frac{1}{4} \cdot \frac{1}{1-D} V_{inmax} = \frac{3}{4} \cdot \frac{1}{1-D} V_{inmax}$$

$$V_{OAV} = \frac{3}{4} \cdot \frac{2}{\pi} \cdot \frac{1}{1-D} V_{inmax} = \frac{3}{2\pi} \cdot \frac{V_{inmax}}{1-D} \quad (3.14)$$

The comparison of the theoretical and simulated voltage gain is shown in Table 3.24 for an AC input voltage of 30V<sub>P</sub>.

Table 3.24 Average output voltage vs duty cycle of the converter of Figure 3.13.

Duty Cycle	$V_{OAV}$ (Theoretical)	$V_{OAV}$ (Simulation)
0.1	21.221	23.044
0.2	23.873	27.275
0.3	27.284	31.607
0.4	31.831	36.962
0.5	38.197	44.167
0.6	47.746	54.552
0.7	63.661	69.489
0.8	95.493	87.586
0.9	190.985	77.068

### 3.9 Comparison of Conversion Efficiency

The comparison among the conventional and the proposed converters in terms of conversion efficiency are shown in Table 3.25. The corresponding curves are shown in Figure 3.24.

Table 3.25 Comparison of Single phase AC-DC Boost Converters.

Average Output Voltage $V_{OAV}$	Conventional Output Switched	Diode-Capacitor Assisted Output Switched	Input Switched Full-Bridge	Diode-Capacitor Assisted Input Switched Full-Bridge	Input Switched Half-Bridge	Modified Input Switched	Input Switched CC FB	Input Switched CC HF
350	97.978	97.159	97.651	97.487	-	-	93.824	85.688
400	97.487	96.995	97.487	97.323	-	-	92.616	86.049
450	97.159	96.804	97.159	97.159	-	-	91.339	85.493
500	96.995	96.64	96.995	96.995	-	-	90.144	84.767
550	96.64	96.476	96.476	96.804	-	-	89.076	83.840
600	96.312	96.148	96.149	96.476	97.815	98.143	87.686	82.354
650	95.984	95.821	95.984	96.149	97.651	97.979	86.452	81.272
700	95.493	95.493	95.493	95.821	97.487	97.815	84.967	79.904
750	94.974	95.137	94.974	95.329	97.323	97.651	83.051	78.341
800	94.482	94.646	94.482	94.81	96.995	97.323	80.636	75.863
850	93.827	94.154	93.827	94.318	96.64	96.995	78.012	73.384
900	92.816	93.307	92.652	93.307	96.476	96.804	74.959	70.905
950	90.986	91.969	90.658	91.641	96.148	96.476	71.627	67.510
1000	88.473	89.975	86.971	88.801	95.657	95.984	67.739	58.886

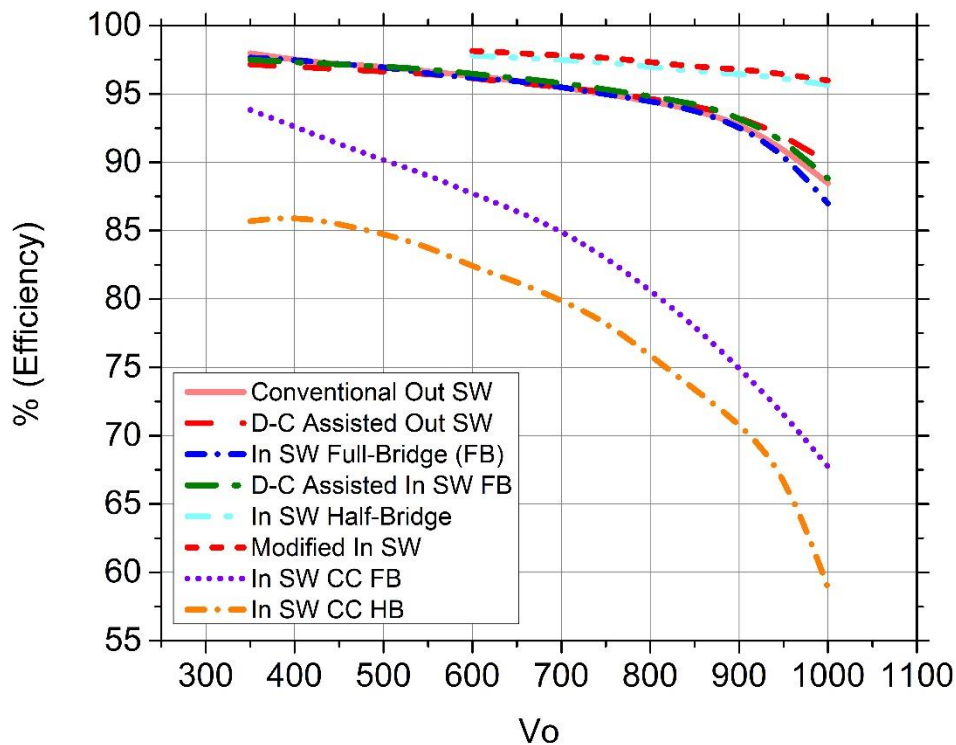


Figure 3.24 Comparison of AC to DC boost converters in terms of conversion efficiency.

### 3.10 Discussions

The simulated values of the voltage gain of all the converters are observed to deviate from the theoretical values at high duty cycles, this is due to inductors internal resistance and non-ideal behaviour of the switching components of the circuit.

All three proposed converters show better conversion efficiency compared to corresponding conventional ones at extreme high voltage gain which is the major objective of the research. The THD of the conventional output switched and diode-capacitor assisted output switched converter is high and they offer moderate PF. For input switched full-bridge converter THD is high and PF is low. Diode-capacitor assisted input switched full-bridge offer satisfactory THD and PF in the mid-range of duty cycle. Input switched half bridge converter shows high THD and satisfactory PF

(in the mid-range of duty cycle). Modified input switched converter shows high THD and satisfactory PF.

All the converters (conventional and proposed) to have better conversion efficiency will be investigated incorporating PFC feedback control. The feedback will keep the input current THD within limits (under 20%). The converters also need to have regulated output voltages. Investigation of all the proposed single phase AC to DC converters are presented in chapter 4.

## Chapter 4

### Investigation of Step-Up Converters with Feedback

The proposed single phase AC to DC step-up converters are subjected to study with feedback control. Both voltage and current control are considered for the simulation. The objective of the investigation is to improve input power factor and reduce total harmonic distortion of the input current. The study is also done for sudden change in load to see the dynamic response of the converter.

#### 4.1 Modified Input Switched AC to DC Boost Converter

##### 4.1.1 Feedback Analysis

The proposed modified input switched AC-DC converter with feedback control is shown in Figure 4.1. The parameters used for the simulation of the converter is given in Table 4.1. The results of the simulation with reference voltage variation is given in Table 4.2. Typical waveform of the circuit is shown in Figure 4.2. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

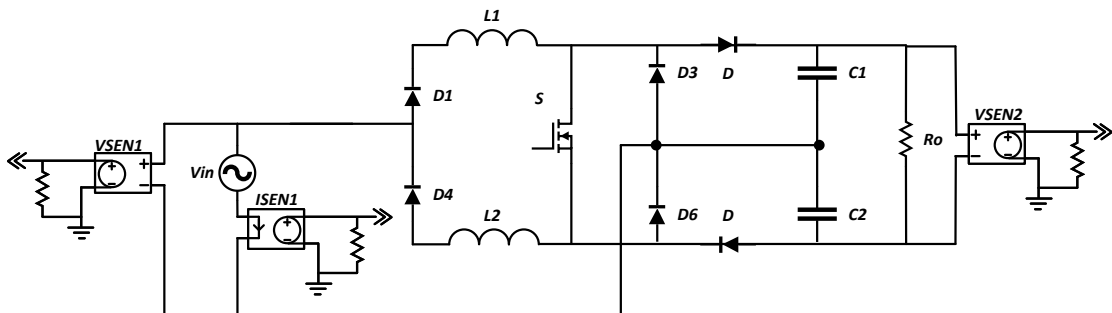


Figure 4.1 Modified input switched AC to DC boost converter with feedback control.

Table 4.1 Parameters of the circuit of Figure 4.1.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	5 mH
Capacitors, $C_1, C_2$	330 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.002
Gain of Current Sensor $I_{SEN1}$	0.25

Table 4.2 Simulation results of the circuit of Figure 4.1.

Ref	$V_{in}$ (peak)	$I_{in}$ (RMS)	$V_o$ (Avg)	Input Current THD	Power Factor	Input Power
4.5	300	23.118	663.040	12.098	0.991	4.8600k
6.0	300	31.987	791.825	9.561	0.995	6.7529k
7.5	300	40.307	872.186	16.639	0.984	8.4161k
9.0	300	48.459	939.960	18.388	0.977	10.043k

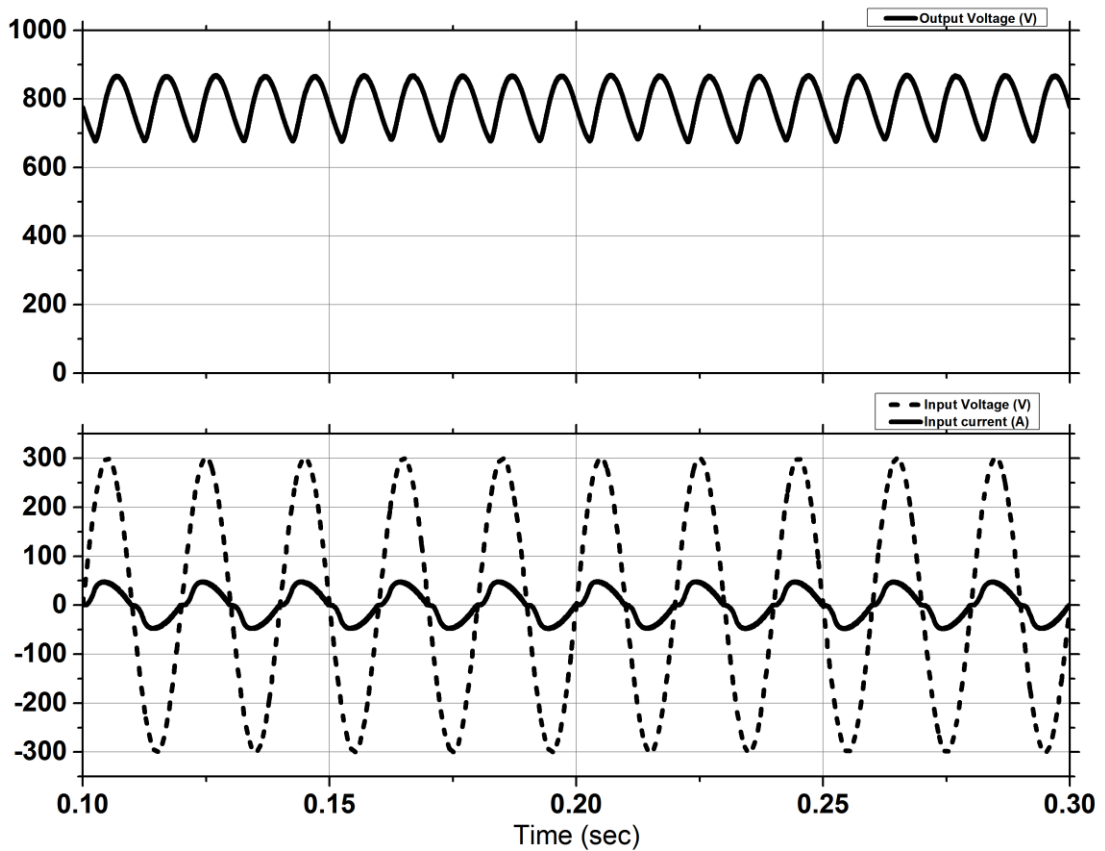


Figure 4.2 Typical input-output waveforms of the circuit of Figure 4.1.

#### 4.1.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 935 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 200  $\Omega$  at 650ms of the simulation time, which is given in Table 4.3. The circuit parameters are given in Table 4.4. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.3 is shown in Figure 4.4. It is evident from the waveforms that due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.



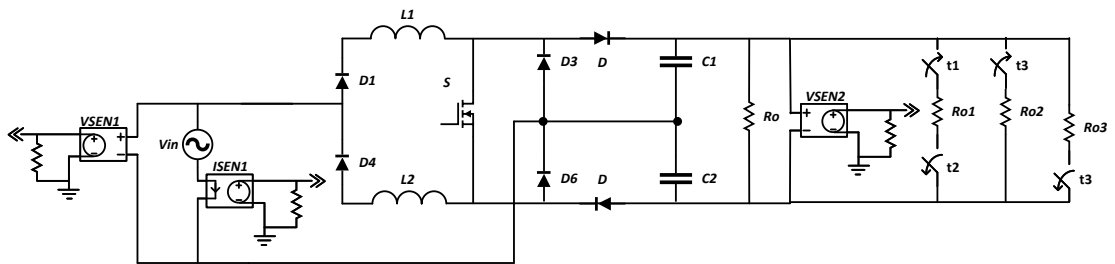


Figure 4.3 Modified input switched AC to DC boost converter for dynamic analysis.

Table 4.3 Changes in load for Figure 4.3.

Time (ms)	Load ( $\Omega$ )
0-250	150
250-450	100
450-650	120
650-900	200

Table 4.4 Parameters of the circuit of Figure 4.3.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	10 mH
Capacitors, $C_1, C_2$	330 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	300 $\Omega$ 300 $\Omega$ , 600 $\Omega$ , 300 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	0.133
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

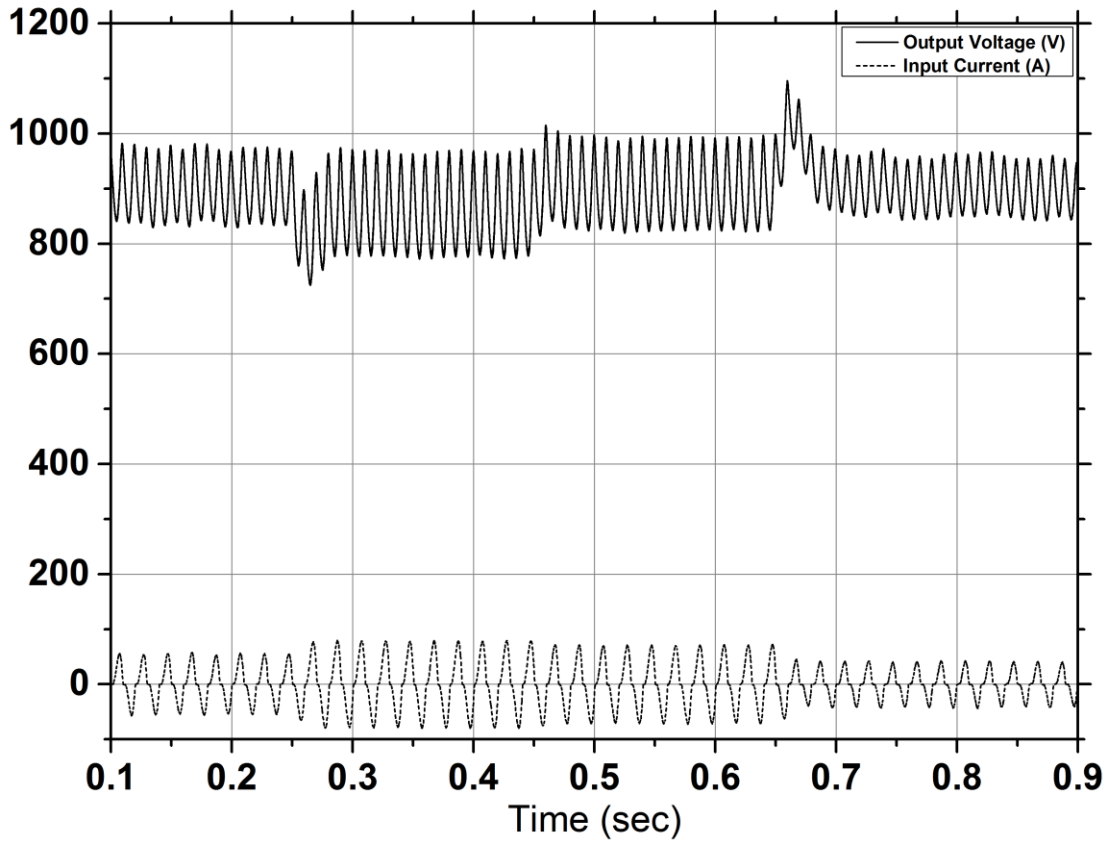


Figure 4.4 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.3.

## 4.2 Input Switched Half-Bridge AC to DC Boost Converter

### 4.2.1 Feedback Analysis

The input switched half-bridge AC-DC converter with feedback control is shown in Figure 4.5. The parameters used for the simulation of the converter is given in Table 4.5. The results of the simulation with reference voltage variation is given in Table 4.6. Typical waveform of the circuit is shown in Figure 4.6. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

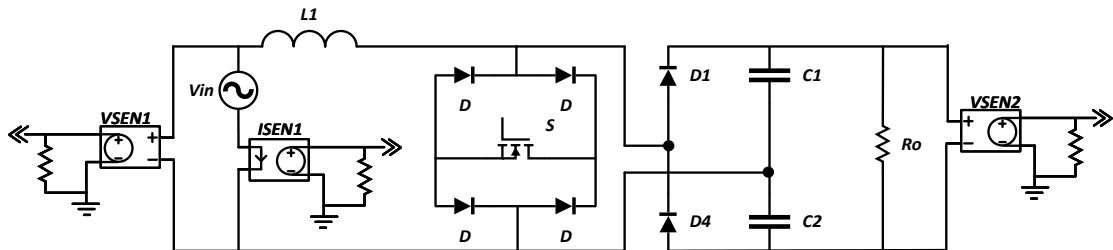


Figure 4.5 Input switched half-bridge AC to DC boost converter with feedback control.

Table 4.5 Parameters of the circuit of Figure 4.5.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_1, C_2$	220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$	0.0033
$V_{SEN2}$	0.002
Gain of Current Sensor $I_{SEN1}$	0.25

Table 4.6 Simulation results of the circuit of Figure 4.5.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
3.0	300	16.362	477.193	42.191	0.862	3.0723k
5.0	300	25.718	655.337	14.870	0.988	5.3925k
7.0	300	37.365	795.890	14.477	0.989	7.4831k
9.0	300	48.664	913.165	16.133	0.983	10.156k

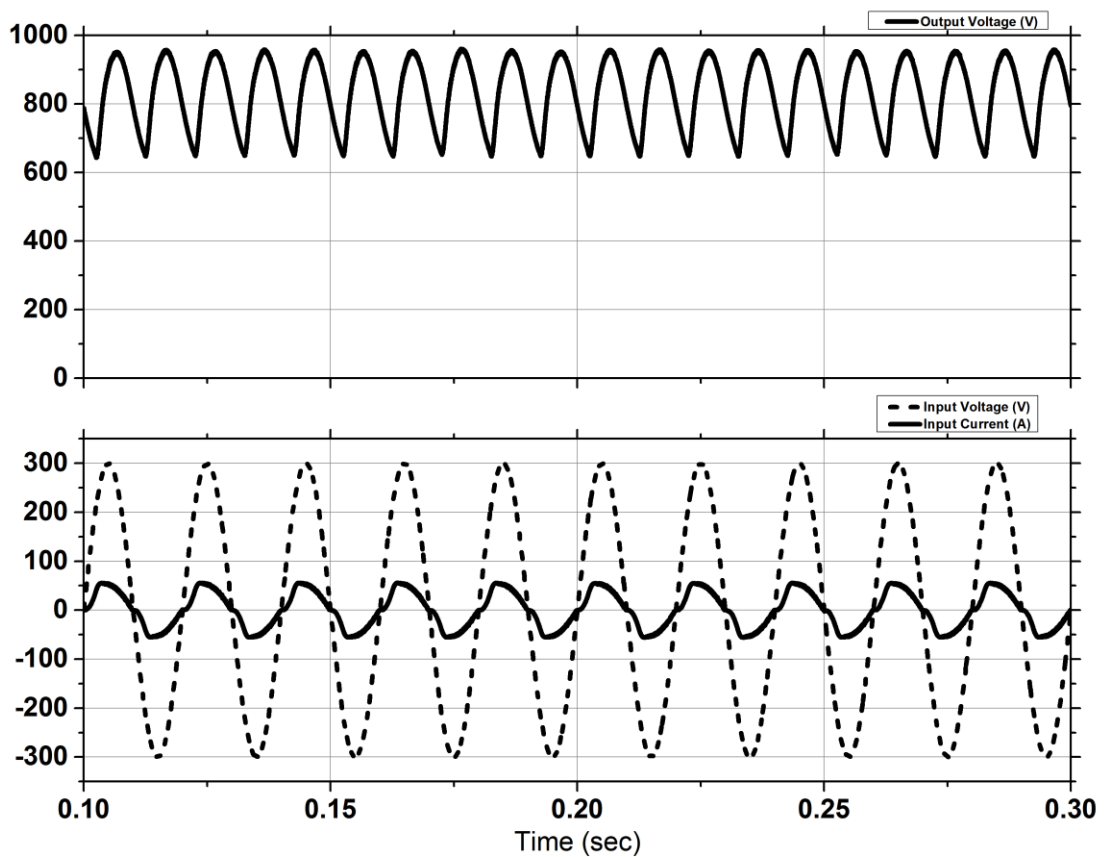


Figure 4.6 Typical input-output waveforms of the circuit of Figure 4.5.

### 4.2.2 Dynamic Response

To test the voltage regulation and the dynamic response of the circuit with feedback control, the controller was set with the reference voltage to provide 1200 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 200  $\Omega$  at 650ms of the simulation time, which is given in Table 4.7. The circuit parameters are given in Table 4.8. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.7 is shown in Figure 4.8. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

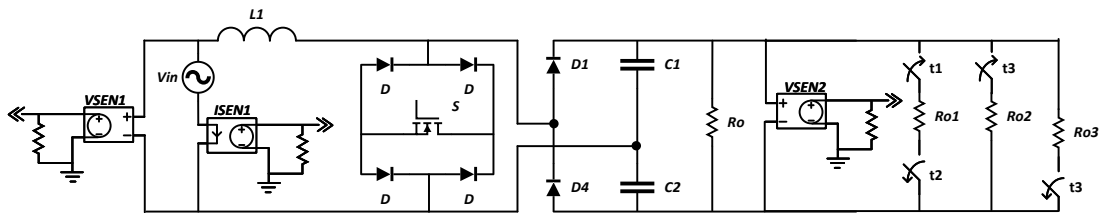


Figure 4.7 Input switched half-bridge AC to DC boost converter for dynamic analysis.

Table 4.7 Changes in load for Figure 4.7.

Time (ms)	Load ( $\Omega$ )
0-250	150
250-450	100
450-650	120
650-900	200

Table 4.8 Parameters of the circuit of Figure 4.7.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_1, C_2$	220 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	300 $\Omega$ 300 $\Omega$ , 600 $\Omega$ , 300 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.001
Gain of Current Sensor $I_{SEN1}$	0.067
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

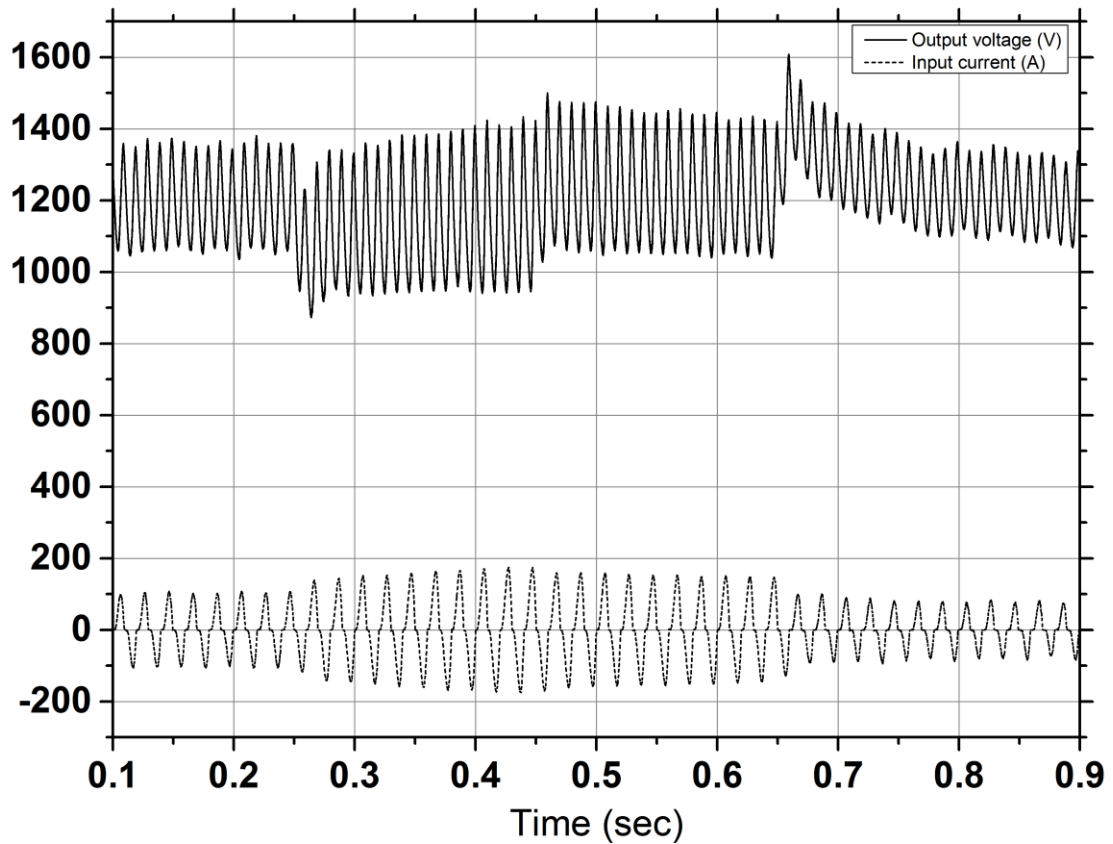


Figure 4.8 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.7.

### 4.3 Diode-Capacitor Assisted Output Switched AC to DC Boost Converter

#### 4.3.1 Feedback Analysis

The proposed diode-capacitor assisted output switched AC-DC converter with feedback control is shown in Figure 4.9. The parameters used for the simulation of the converter is given in Table 4.9. The results of the simulation with reference voltage variation is given in Table 4.10. Typical waveform of the circuit is shown in Figure 4.10. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit with almost unity power factor.



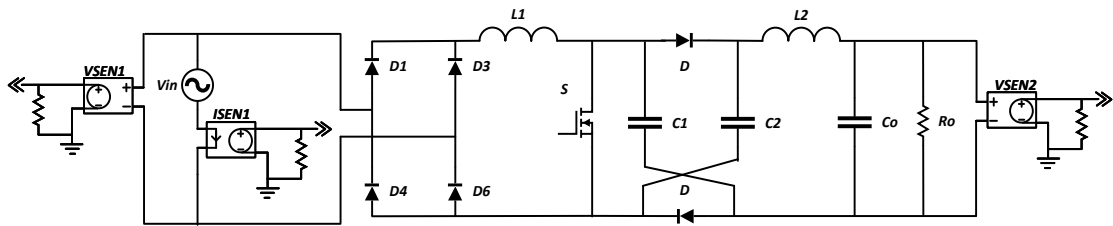


Figure 4.9 Diode-capacitor assisted output switched AC to DC boost converter with feedback control.

Table 4.9 Parameters of the circuit of Figure 4.9.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	5 mH
Capacitors, $C_1, C_2$ $C_o$	10 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.002
Gain of Current Sensor $I_{SEN1}$	0.25

Table 4.10 Simulation results of the circuit of Figure 4.9.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
1.5	300	6.2563	349.993	15.413	0.962	1.2765k
3.0	300	15.161	534.587	24.146	0.941	3.0285k
4.2	300	22.091	643.03	16.44	0.959	4.4969k
6.0	300	32.721	776.753	12.05	0.975	6.7977k

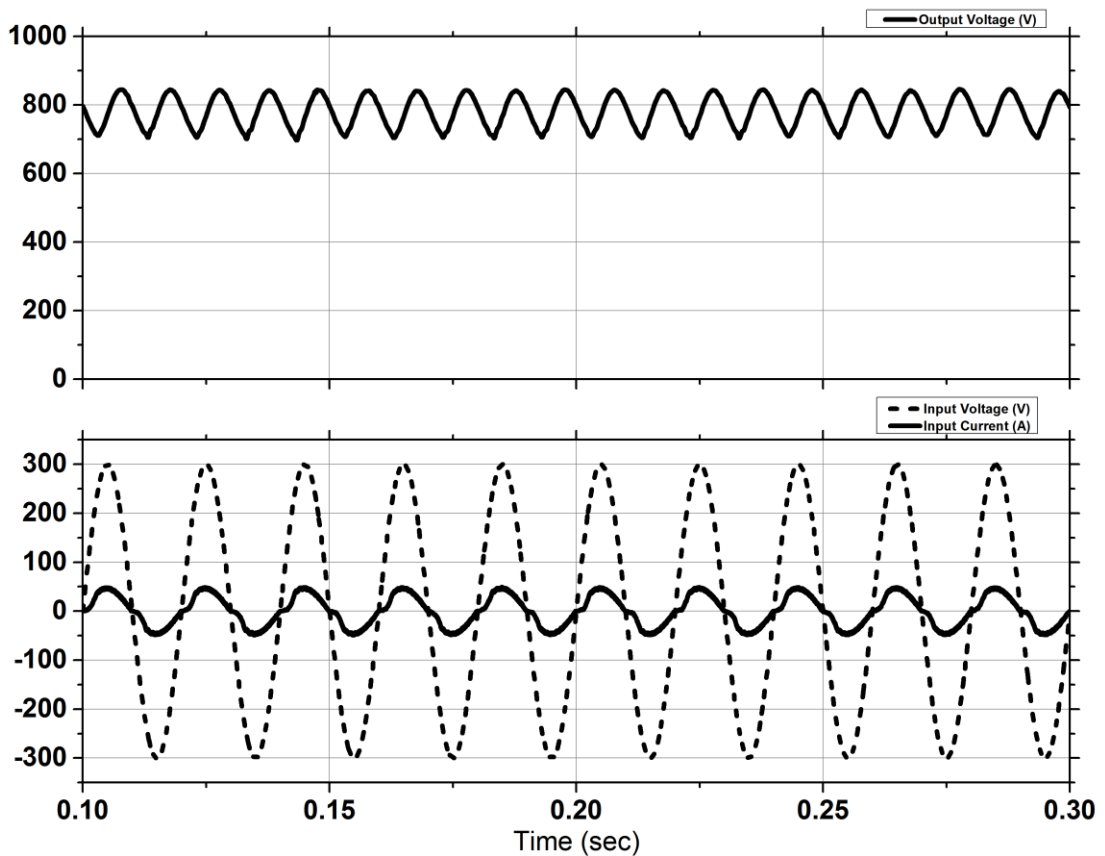


Figure 4.10 Typical input-output waveforms of the circuit of Figure 4.9.

### 4.3.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 930 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 200  $\Omega$  at 650ms of the simulation time, which is given in Table 4.11. The circuit parameters are given in Table 4.12. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.11 is shown in Figure 4.12. It is evident from the waveforms that, with feedback control the output voltage of the converter cannot be kept constant with the change of load. Due to increased circuit complexity it is not that always easy to design the feedback control.

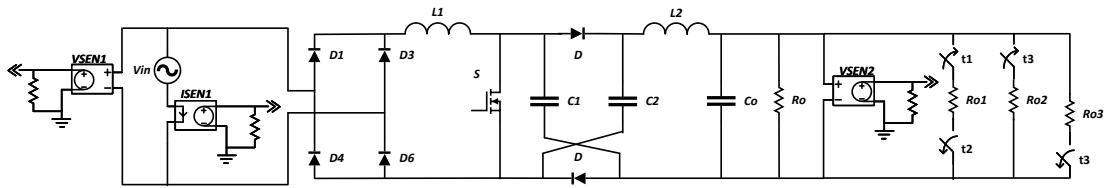


Figure 4.11 Diode-capacitor assisted output switched AC to DC boost converter for dynamic analysis.

Table 4.11 Changes in load for Figure 4.11.

Time (ms)	Load ( $\Omega$ )
0-250	100
250-450	80
450-650	100
650-900	120

Table 4.12 Parameters of the circuit of Figure 4.11.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	5 mH
Capacitors, $C_1, C_2$ $C_o$	10 $\mu$ F 220 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.067
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

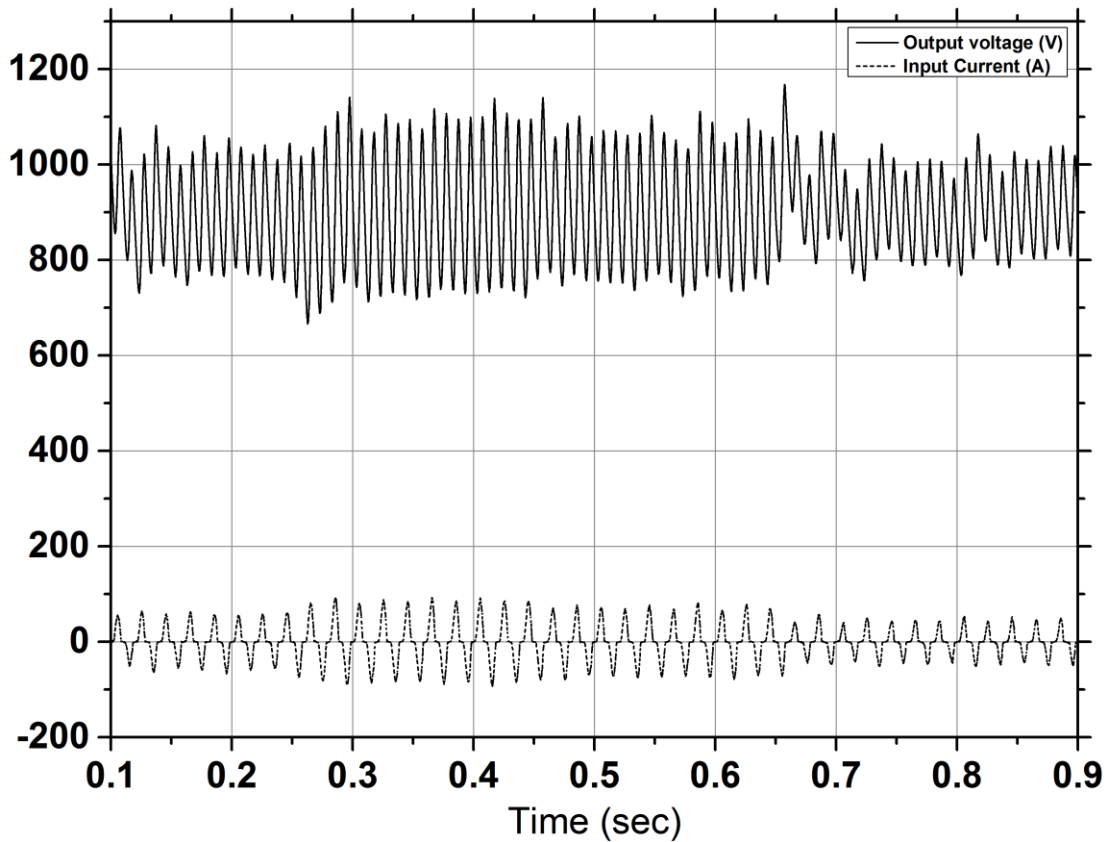


Figure 4.12 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.11.

## 4.4 Diode-Capacitor Assisted Input Switched Full-Bridge AC to DC Boost Converter

### 4.4.1 Feedback Analysis

The proposed diode-capacitor assisted input switched full-bridge AC to DC converter with feedback control is shown in Figure 4.13. The parameters used for the simulation of the converter is given in Table 4.13. The results of the simulation with reference voltage variation is given in Table 4.14. Typical waveform of the circuit is shown in Figure 4.14. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

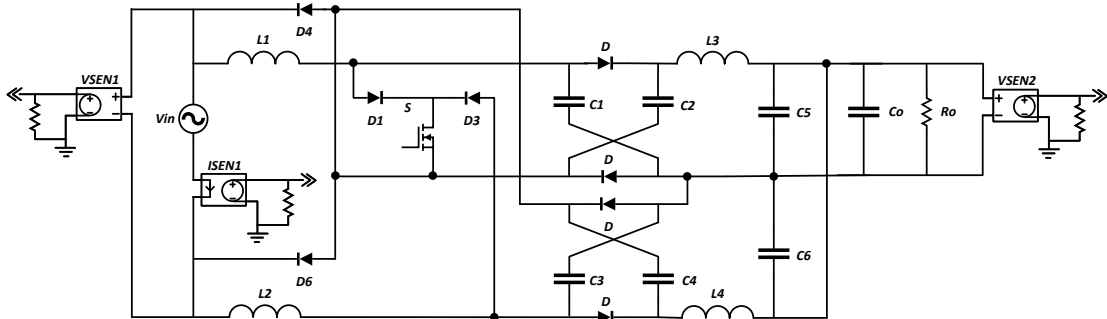


Figure 4.13 Diode-capacitor assisted input switched full-bridge AC to DC boost converter for feedback analysis.

Table 4.13 Parameters of the circuit of Figure 4.13.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 1 mH
Capacitors, $C_1, C_2, C_3, C_4, C_5, C_6$ $C_o$	22 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.25

Table 4.14 Simulation results of the circuit of Figure 4.13.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
1.5	300	11.046	450.994	7.837	0.996	2.3350k
3.0	300	22.406	579.855	6.604	0.998	4.7807k
4.5	300	34.503	654.001	9.247	0.995	7.2865k
6.0	300	45.747	692.405	12.761	0.987	9.5780k

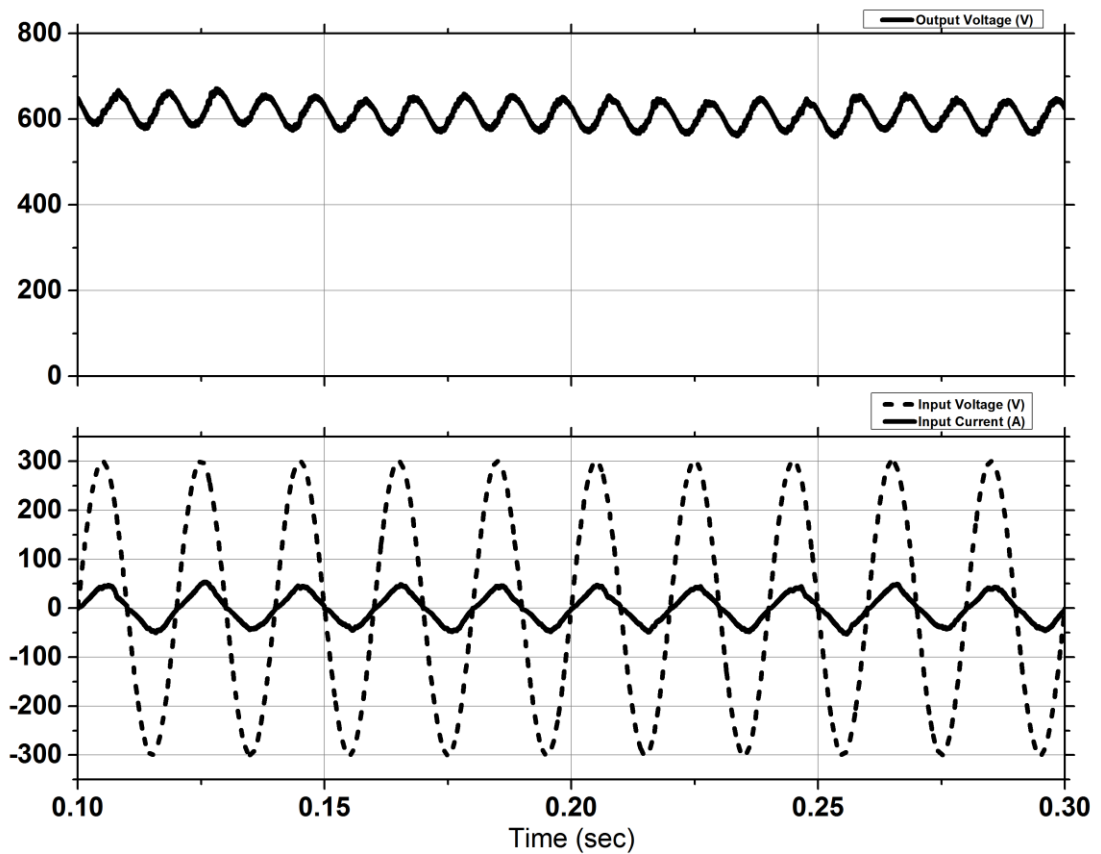


Figure 4.14 Typical input-output waveforms of the circuit of Figure 4.13.

#### 4.4.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 627 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 2000  $\Omega$  at 650ms of the simulation time, which is given in Table 4.15. The circuit parameters are given in Table 4.16. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.15 is shown in Figure 4.16. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

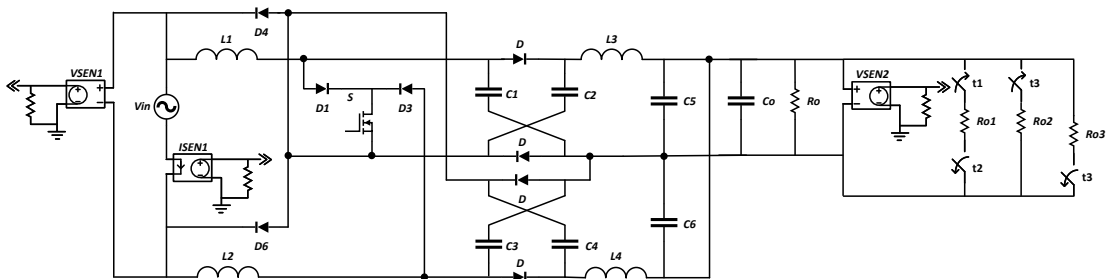


Figure 4.15 Diode-capacitor assisted input switched full-bridge AC to DC boost converter dynamic analysis.

Table 4.15 Changes in load for Figure 4.15.

Time (ms)	Load ( $\Omega$ )
0-400	150
250-450	100
450-650	120
650-800	200



Table 4.16 Parameters of the circuit of Figure 4.15.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 1 mH
Capacitors, $C_1, C_2, C_3, C_4, C_5, C_6$ $C_o$	22 $\mu$ F 220 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	0.067
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

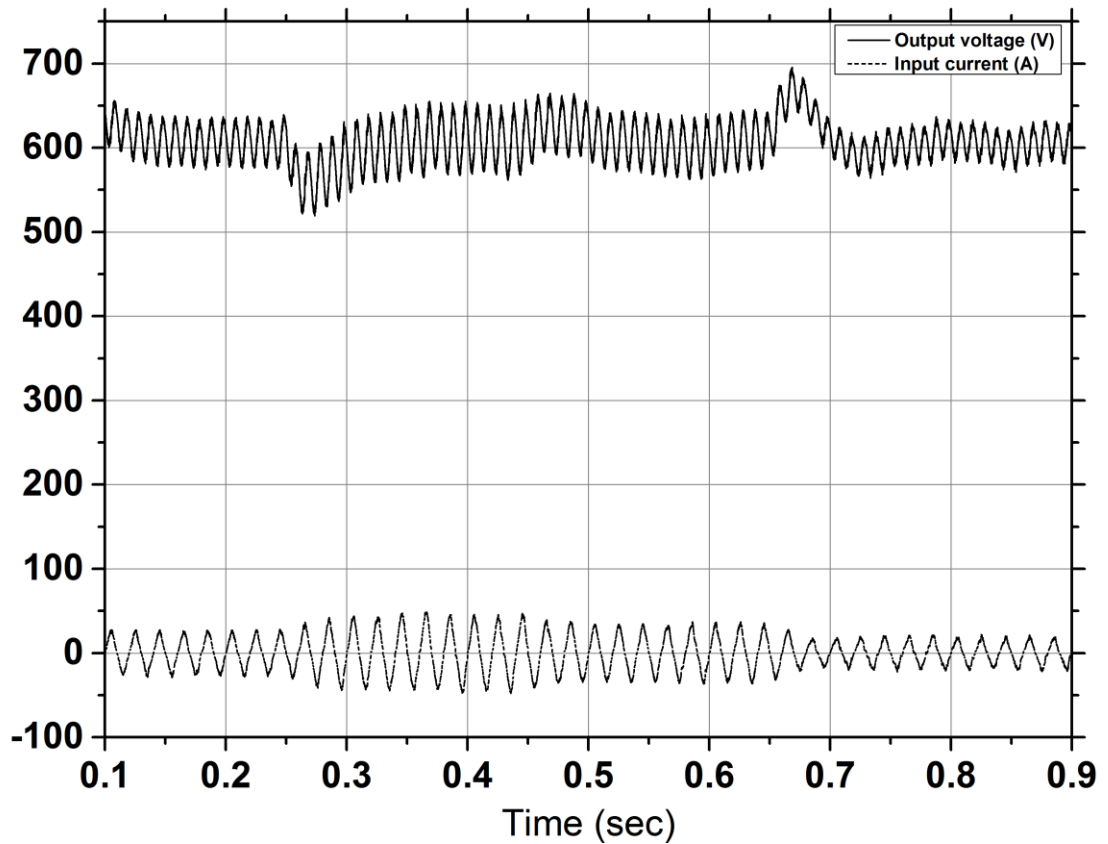


Figure 4.16 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.15.

## 4.5 Input Switched Coupled Capacitor Full-Bridge AC to DC Boost Converter

### 4.5.1 Feedback Analysis

The proposed input switched coupled capacitor full-bridge AC to DC converter with feedback control is shown in Figure 4.17. The parameters used for the simulation of the converter is given in Table 4.17. The results of the simulation with reference voltage variation is given in Table 4.18. Typical waveform of the circuit is shown in Figure 4.18. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

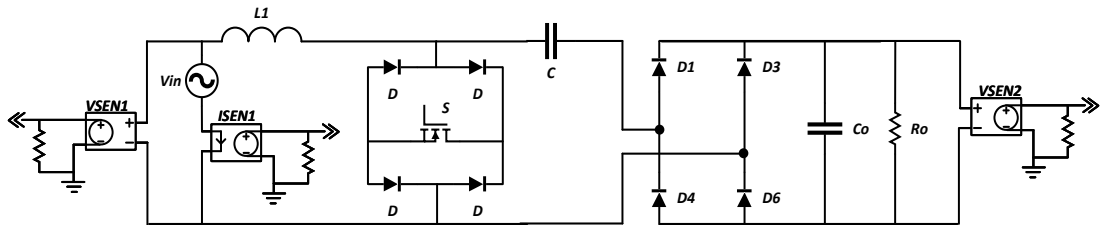


Figure 4.17 Input switched coupled capacitor full-bridge AC to DC boost converter for feedback analysis.

Table 4.17 Parameters of the circuit of Figure 4.17.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_1$ $C_o$	22 $\mu$ F 330 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.85

Table 4.18 Simulation results of the circuit of Figure 4.13.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
1.0	300	5.7719	303.143	5.814	0.973	1.1921k
1.5	300	14.143	454.773	2.745	0.995	2.9850k
2.0	300	20.961	544.058	3.078	0.997	4.4348k
2.5	300	23.684	576.077	3.398	0.998	5.0125k
3.0	300	26.481	605.393	3.825	0.998	5.6053k

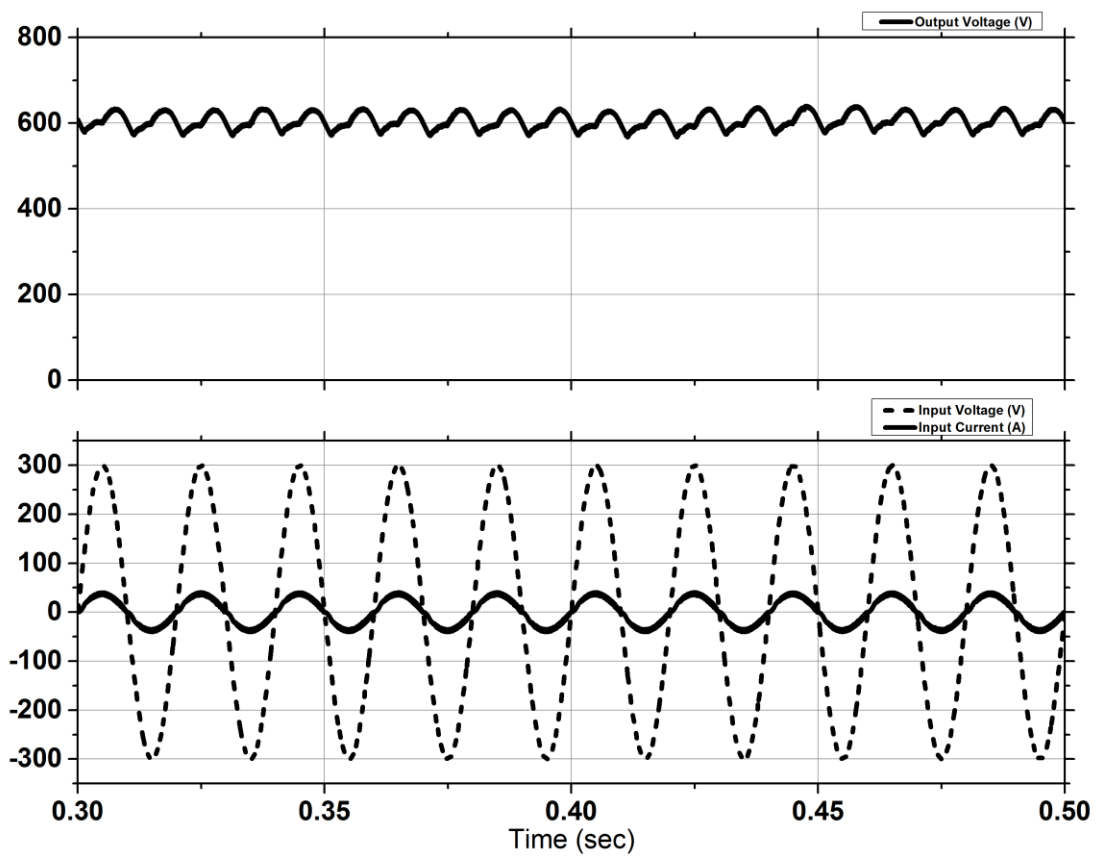


Figure 4.18 Typical input-output waveforms of the circuit of Figure 4.17.

#### 4.5.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 900 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 200  $\Omega$  at 650ms of the simulation time, which is given in Table 4.15. The circuit parameters are given in Table 4.16. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.15 is shown in Figure 4.16. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

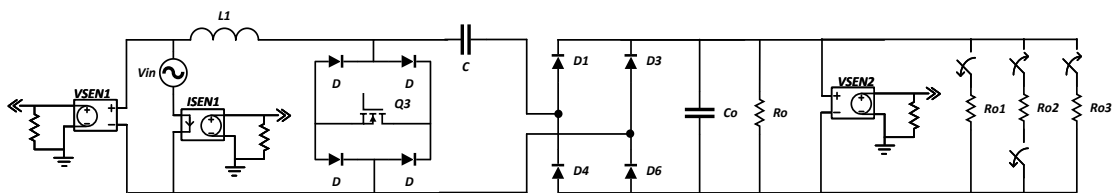


Figure 4.19 Input switched coupled capacitor full-bridge AC to DC boost converter for dynamic analysis.

Table 4.19 Changes in load for Figure 4.19.

Time (ms)	Load ( $\Omega$ )
0-400	150
250-450	100
450-650	120
650-800	200

Table 4.20 Parameters of the circuit of Figure 4.19.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C$ $C_o$	22 $\mu$ F 330 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	300 $\Omega$ 300 $\Omega$ , 600 $\Omega$ , 300 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	0.133
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

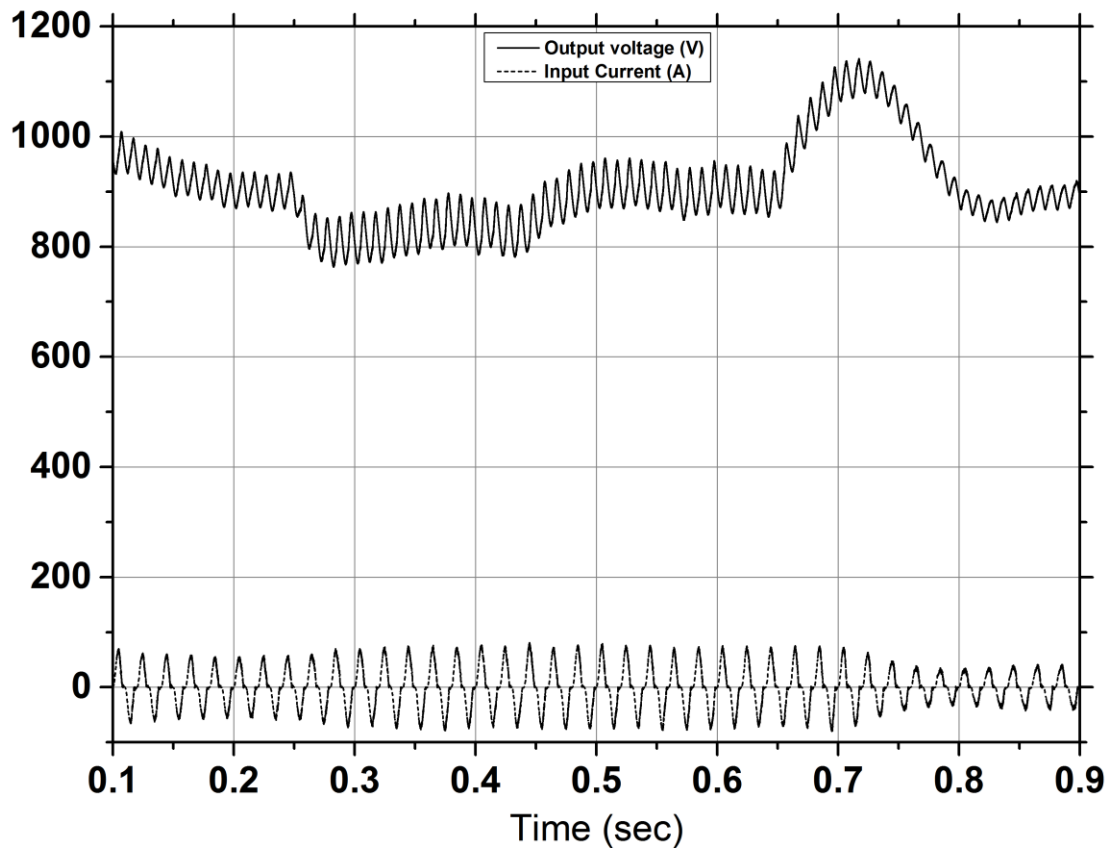


Figure 4.20 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.19.

## 4.6 Input Switched Coupled Capacitor Half-Bridge AC to DC Boost Converter

### 4.6.1 Feedback Analysis

The proposed input switched coupled capacitor half-bridge AC to DC converter with feedback control is shown in Figure 4.21. The parameters used for the simulation of the converter is given in Table 4.21. The results of the simulation with reference voltage variation is given in Table 4.22. Typical waveform of the circuit is shown in Figure 4.22. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

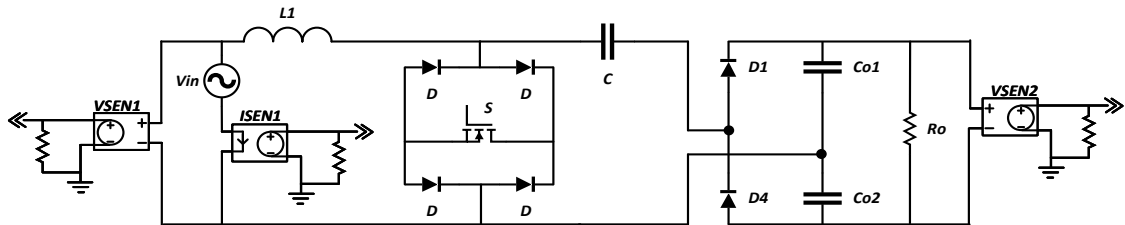


Figure 4.21 Input switched coupled capacitor half-bridge AC to DC boost converter for feedback analysis.

Table 4.21 Parameters of the circuit of Figure 4.21.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C_1$ $C_o$	22 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.85



Table 4.22 Simulation results of the circuit of Figure 4.21.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
1.0	300	5.5419	300.465	7.668	0.978	1.1491k
1.5	300	13.117	441.459	4.901	0.994	2.7650k
2.0	300	20.770	547.361	5.279	0.997	4.3925k
2.5	300	23.611	576.088	5.061	0.997	4.9948k

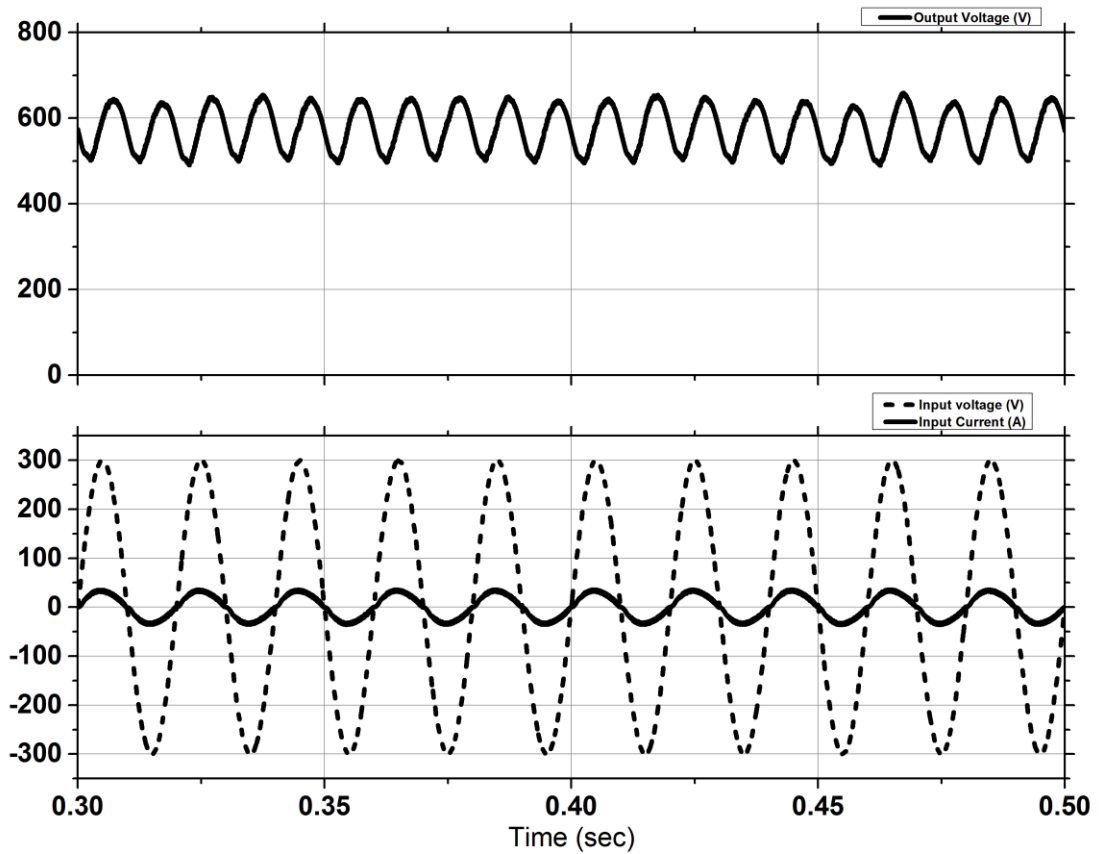


Figure 4.22 Typical input-output waveforms of the circuit of Figure 4.21.

#### 4.6.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 935 Vdc output with a resistive load of 150  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 100  $\Omega$  at 250ms, 120  $\Omega$  at 450ms and 200  $\Omega$  at 650ms of the simulation time, which is given in Table 4.15. The circuit parameters are given in Table 4.16. The simulation result showing the variation of output voltage and input current for the circuit of Figure 4.15 is shown in Figure 4.16. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

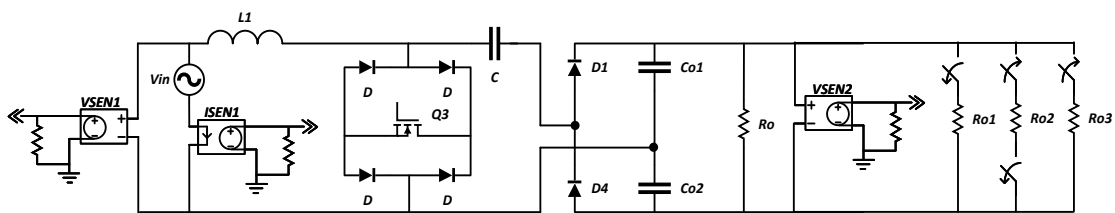


Figure 4.23 Input switched coupled capacitor half-bridge AC to DC boost converter for dynamic analysis.

Table 4.23 Changes in load for Figure 4.23.

Time (ms)	Load ( $\Omega$ )
0-400	150
250-450	100
450-650	120
650-800	200

Table 4.24 Parameters of the circuit of Figure 4.23.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$	5 mH
Capacitors, $C$ $C_o$	22 $\mu$ F 330 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	300 $\Omega$ 300 $\Omega$ , 600 $\Omega$ , 300 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	0.133
Time $t_1, t_2, t_3$	250 ms, 450 ms, 650 ms

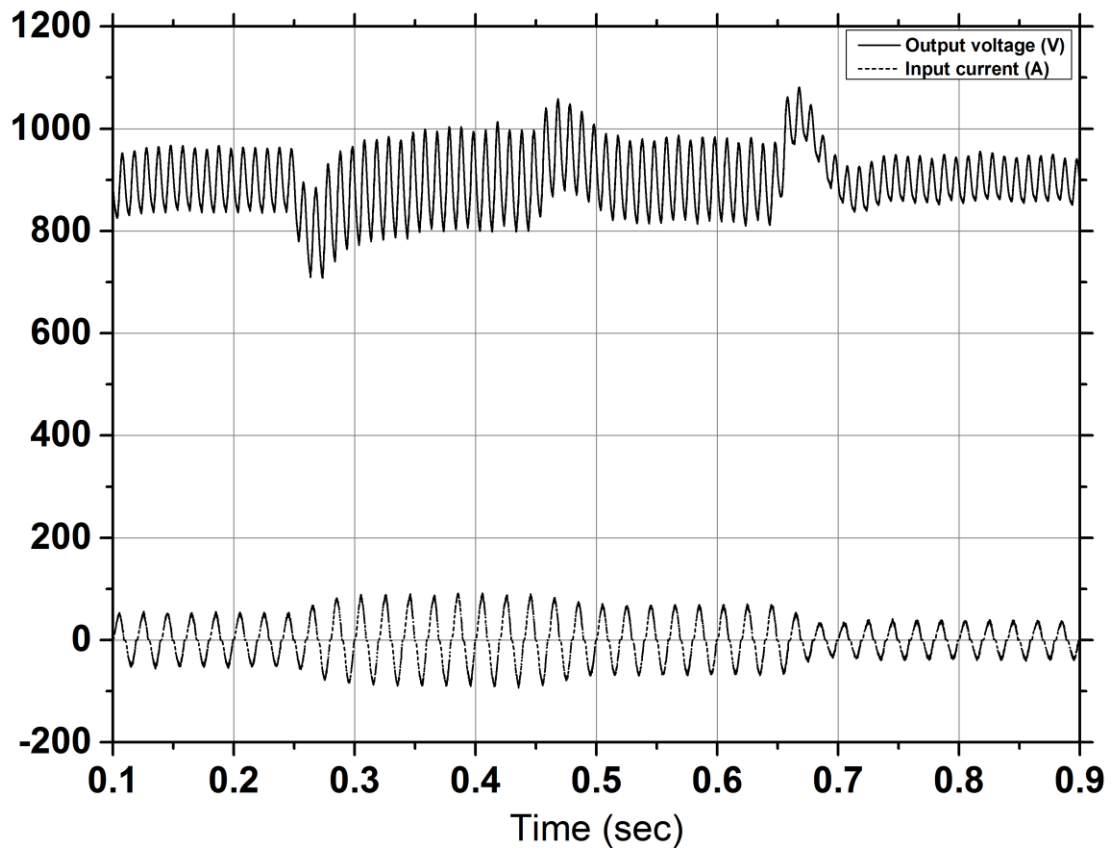


Figure 4.24 Typical waveforms of output voltage and input current for load change of the circuit of Figure 4.23.

#### 4.7 Discussions

The input power factor of the proposed converters have improved with the feedback control. The input current THD is also within prescribed limits for high voltage gains. Most of the converters maintained constant output voltage under variable load condition. Typical results of proposed converters in very low step-down gain are discussed in the next chapter (chapter 5).

## Chapter 5

### Investigation of AC to DC Step-Down Converters

In this chapter, description of the working principle and the open loop simulation of the conventional and proposed SEPIC converters in step-down mode are provided in section 5.1 through 5.9. The converter works in four switching stage. Stage I: when the switch is closed during positive half cycle. Stage II: when the switch is open during positive half cycle. Stage III: when the switch is closed during negative half cycle. Stage IV: when the switch is open during negative half cycle. The simulated voltage gain values are given and not compared with the theoretical values. Since the converter is used for stepping the voltage down, the simulated output voltage is given up to 0.5 duty cycle. The conventional and proposed converters are compared in terms of conversion efficiency in section 5.10.

#### 5.1 Output Switched Full-Bridge AC to DC SEPIC Converter

In conventional two stage AC to DC SEPIC converter, the DC-DC SEPIC converter was placed in between the bridge rectifier and the load. The converter shown in Figure 5.1 is a modified version of the conventional AC to DC SEPIC converter. A diode bridge is introduced at the load side to keep the input current waveform identical in both half cycle, which is one of the major disadvantage of the conventional converter.

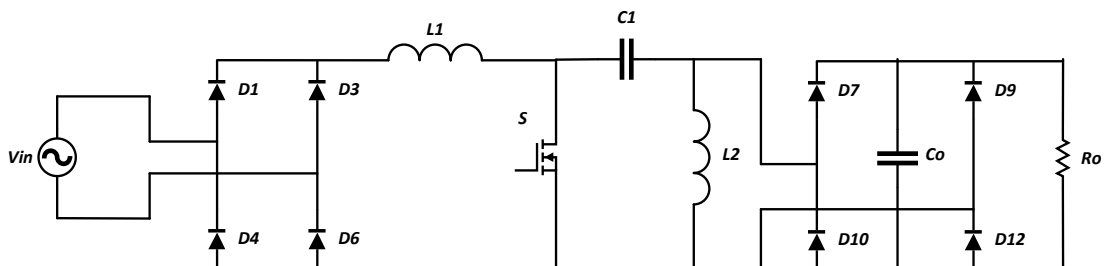
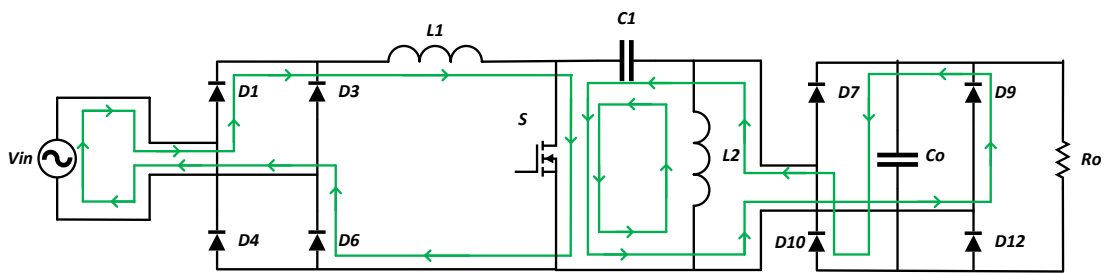


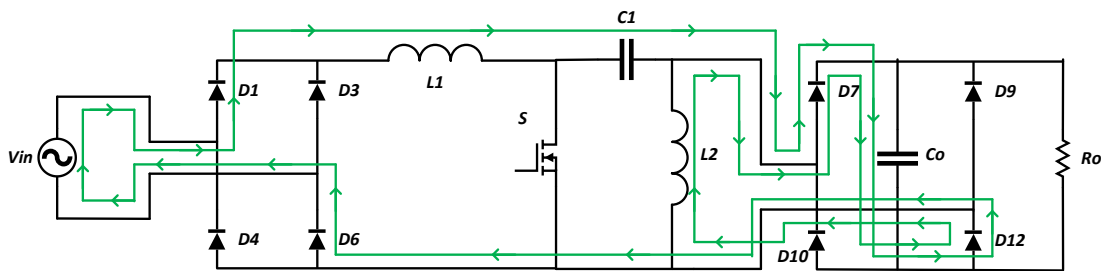
Figure 5.1 Conventional output switched full-bridge AC to DC SEPIC converter.

### 5.1.1 Principle of Operation

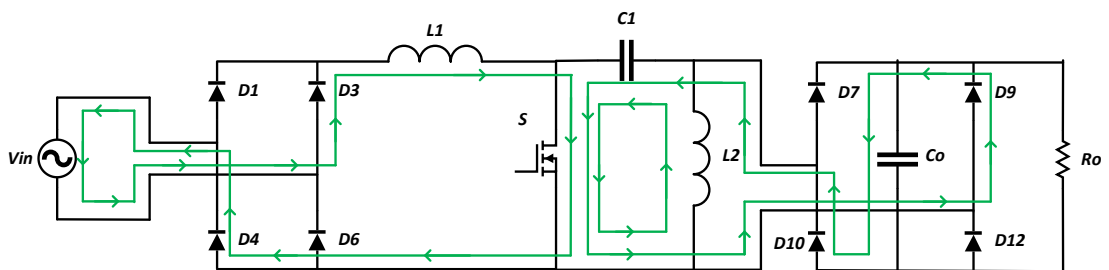
The four working stages of the converter is illustrated in Figure 5.2. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the SEPIC capacitor charges the output inductor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the input inductor voltage charges the intermediate and output capacitor. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)



(b)



(c)

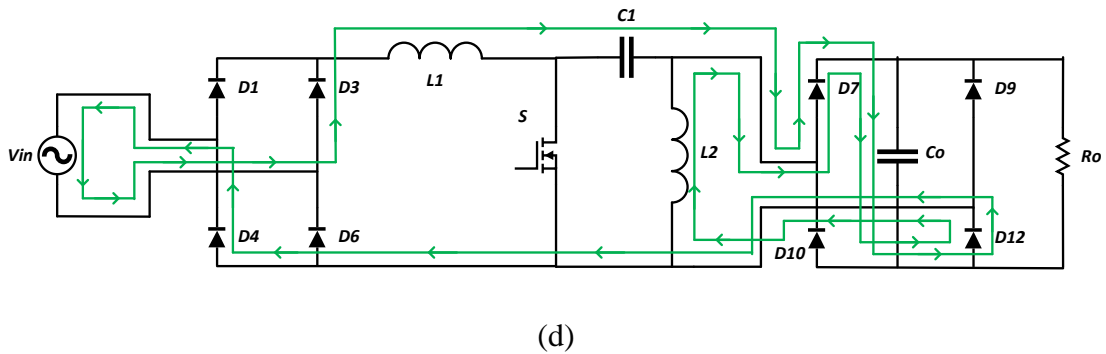


Figure 5.2 Four steps of operation of the converter in Figure 5.1,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.1.2 Open Loop Simulation

The simulation of the circuit of Figure 5.1 is carried out with the parameters of Table 5.1. The results of the simulation is given in Table 5.2.

Table 5.1 Parameters of the converter of Figure 5.1.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.2 Simulation results of the converter of Figure 5.1.

Voltage Gain	Vo	Efficiency	THD	PFi
0.05	148.108	53.138	34.621	0.938
0.10	157.634	58.781	33.200	0.945
0.15	173.116	65.407	29.714	0.954
0.20	193.165	72.840	23.655	0.961
0.25	220.751	80.566	16.885	0.967
0.30	257.019	87.491	11.522	0.973
0.35	302.139	92.764	7.7965	0.979
0.40	345.694	95.849	3.5487	0.983
0.45	389.830	96.892	5.2104	0.986

### 5.1.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.1 with an applied input voltage of  $30V_P$  is given in Table 5.3. Circuit diagram with voltage labels is shown in Figure 5.3.

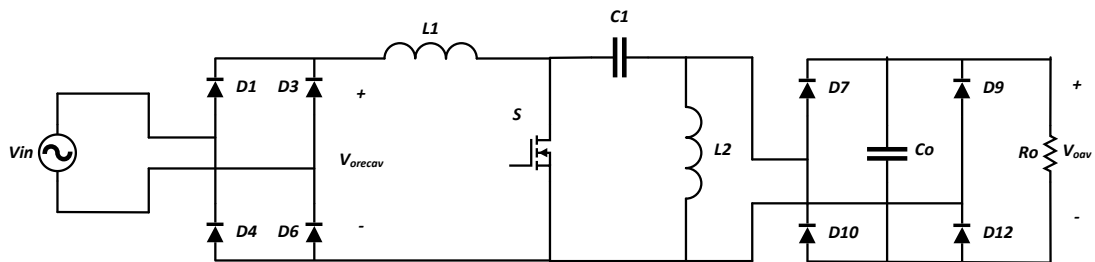


Figure 5.3 Conventional output switched full-bridge AC to DC SEPIC converter with voltage across the components.

The rectified average voltage after the conventional bridge is,

$$V_{orectav} = \frac{V_{inmax}}{\pi} \int_0^{\pi} \sin \theta d\theta = \frac{2V_{inmax}}{\pi}$$



For DC-DC boost converter,

$$\frac{D}{(1-D)} V_{rectav} = V_{oav}$$

Where,  $D = \text{Duty Cycle} = \frac{T_{ON}}{T}$ ,  $(1-D) = \frac{T_{OFF}}{T}$  and  $T = \text{Switching Frequency}$

Therefore the output voltage can be written as,

$$V_{oav} = \frac{2DV_{inmax}}{\pi(1-D)} \quad (5.1)$$

Table 5.3 Average output voltage vs duty cycle of the converter of Figure 5.1.

Duty Cycle	Vo (Simulation)
0.1	12.424
0.2	19.453
0.3	28.752
0.4	37.514
0.5	44.113

## 5.2 Diode-Capacitor Assisted Output Switched Full-Bridge AC to DC SEPIC Converter

The proposed converter is designed by introducing diode-capacitor network instead of SEPIC coupling capacitor. The capacitors in the network are charged in series when the switch is open. When the switch is closed the inductor L2 will be charged by the network capacitors in parallel with half voltage.

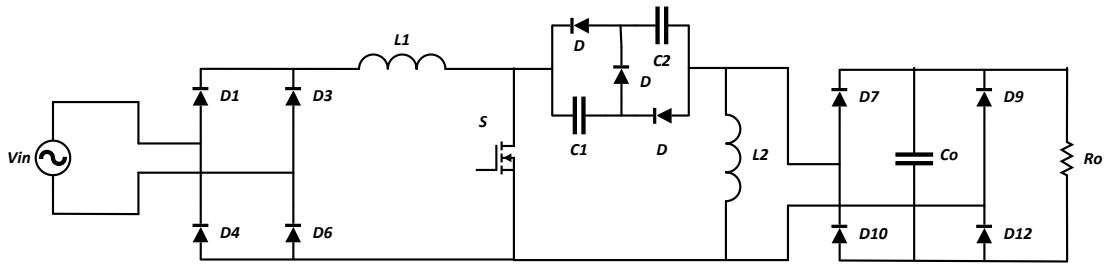
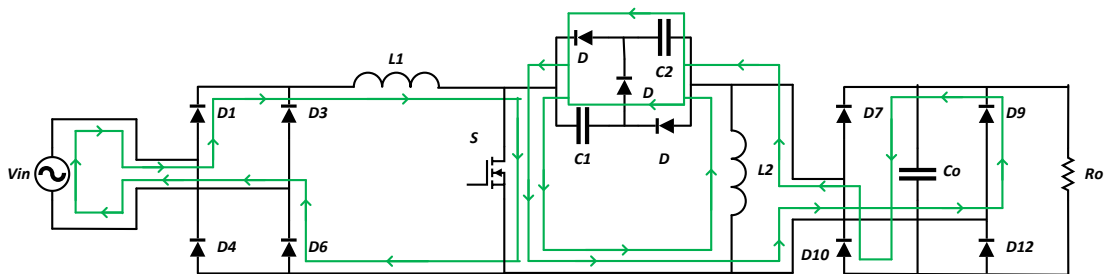


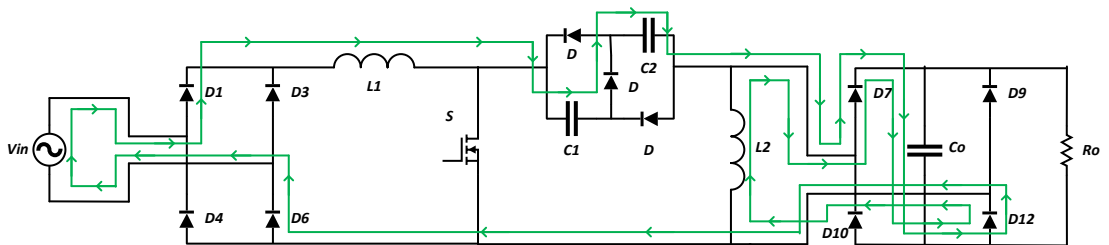
Figure 5.4 Proposed diode-capacitor assisted output switched full-bridge AC to DC converter.

### 5.2.1 Principle of Operation

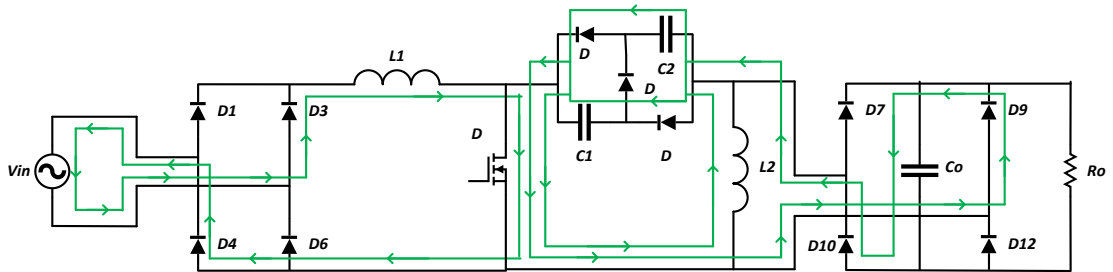
The four working stages of the converter is illustrated in Figure 5.5. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the intermediate capacitors in parallel charges the output inductor through the switch. When the switch is OFF, source and the inductor voltage charges the intermediate capacitors in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



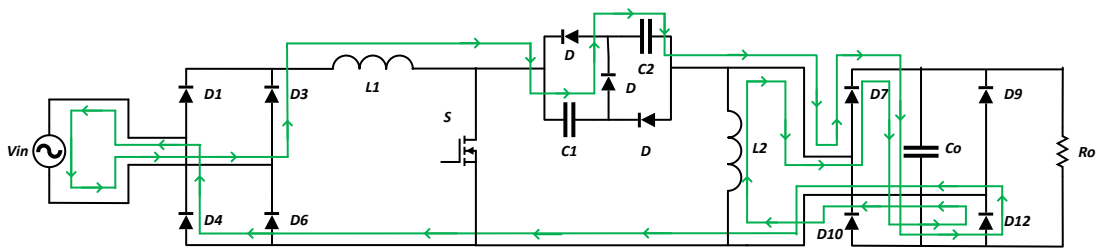
(a)



(b)



(c)



(d)

Figure 5.5 Four steps of operation of the converter in Figure 5.4,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.2.2 Open Loop Simulation

The simulation of the circuit of Figure 5.4 is carried out with the parameters of Table 5.4. The results of the simulation is given in Table 5.5.

Table 5.4 Parameters of the converter of Figure 5.4.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.5 Simulation results of the converter of Figure 5.4.

Voltage Gain	$V_o$	Efficiency	THD	Pfi
0.05	90.308	60.949	63.024	0.878
0.10	97.692	66.751	73.681	0.874
0.15	107.791	74.385	84.564	0.858
0.20	121.188	82.239	98.074	0.839
0.25	138.708	89.772	92.777	0.833
0.30	160.805	96.242	68.143	0.846
0.35	188.375	99.315	37.171	0.873
0.40	216.911	99.931	19.507	0.902
0.45	249.189	99.609	21.191	0.925

### 5.2.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.4 with an applied input voltage of 30V<sub>P</sub> is given in Table 5.6. Circuit diagram with voltage labels is shown in Figure 5.6.

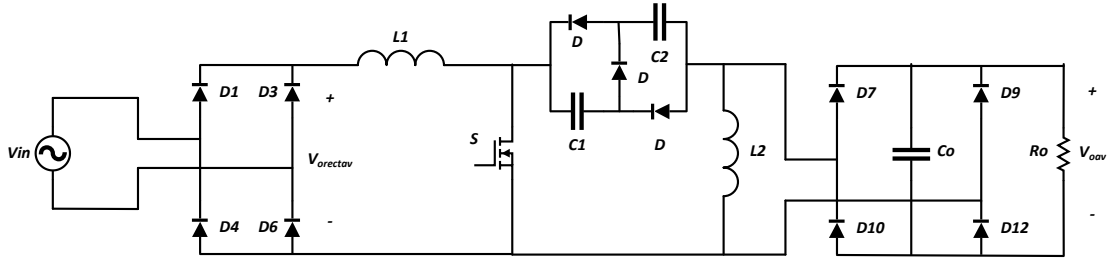


Figure 5.6 Proposed diode-capacitor assisted output switched full-bridge AC to DC converter with voltage across the components.

The rectified average voltage after the conventional bridge is,

$$V_{orectav} = \frac{V_{in\max}}{\pi} \int_0^{\pi} \sin \theta d\theta = \frac{2V_{in\max}}{\pi}$$

For DC-DC boost converter [44],

$$\frac{D}{(1-D)(2-D)} V_{orectav} = V_{oav}$$

Where,  $D = \text{Duty Cycle} = \frac{T_{ON}}{T}$ ,  $(1-D) = \frac{T_{OFF}}{T}$  and  $T = \text{Switching Frequency}$

Therefore the output voltage can be written as,

$$V_{oav} = \frac{2DV_{in\max}}{\pi(1-D)(2-D)} \quad (5.2)$$

Table 5.6 Average output voltage vs duty cycle of the converter of Figure 5.4.

Duty Cycle	Vo (Simulation)
0.1	9.268
0.2	15.692
0.3	22.900
0.4	29.791
0.5	34.626

### 5.3 Output Switched Half-Bridge AC to DC SEPIC Converter

The converter is designed by modifying the output switched full-bridge by introducing split capacitors at the load side. The converter is shown in Figure 5.7.

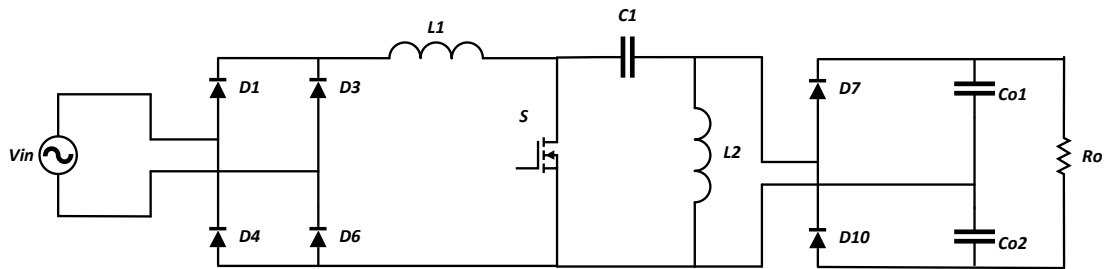
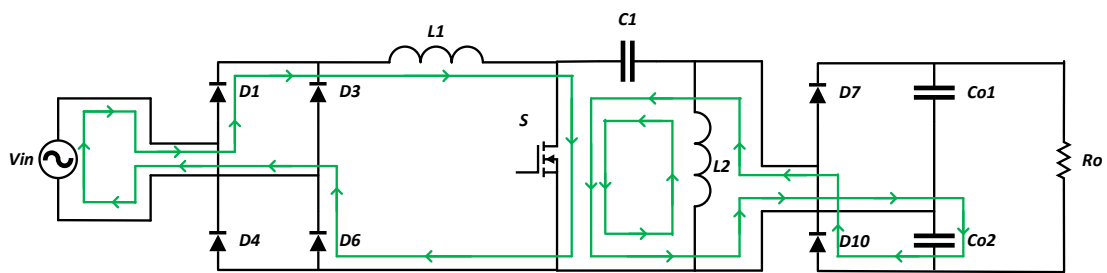


Figure 5.7 Output switched half-bridge AC to DC SEPIC Converter.

#### 5.3.1 Principle of Operation

The four working stages of the converter is illustrated in Figure 5.8. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the SEPIC capacitor charges the output inductor and lower output capacitor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the SEPIC and upper output capacitor in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)

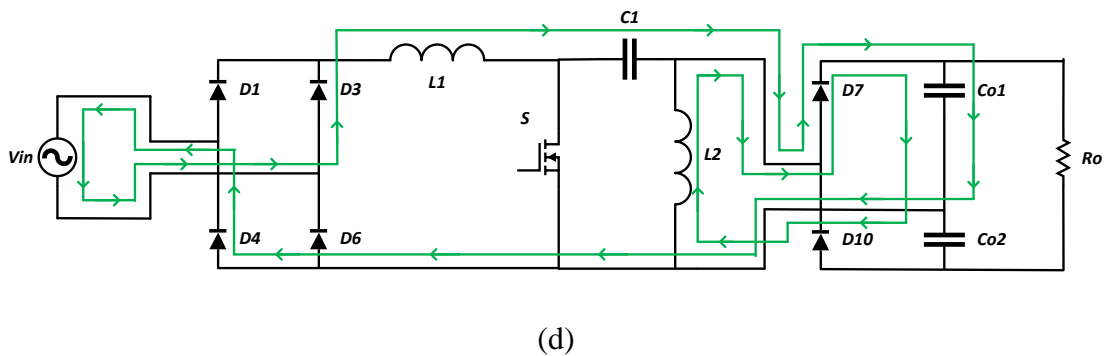
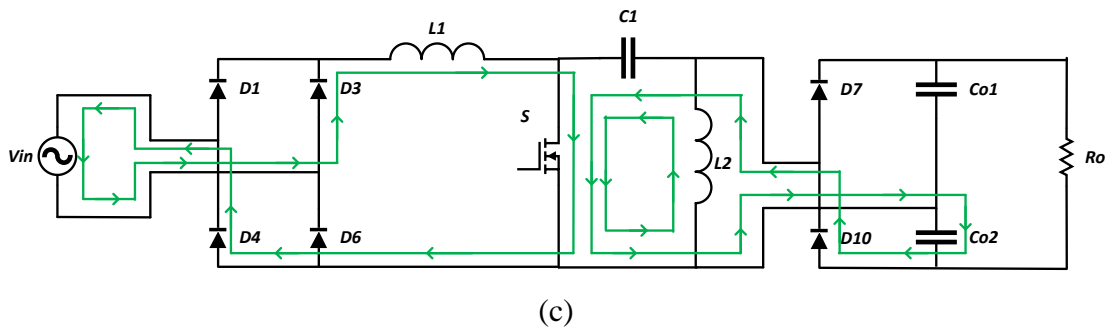
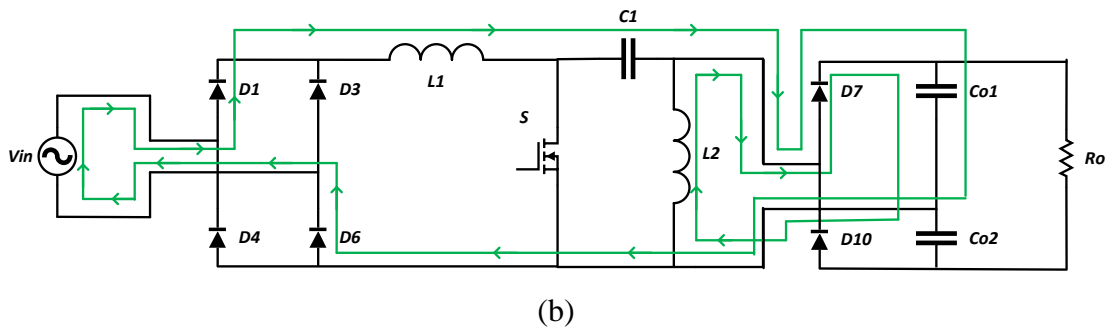


Figure 5.8 Four steps of operation of the converter in Figure 5.7,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.3.2 Open Loop Simulation

The simulation of the circuit of Figure 5.7 is carried out with the parameters of Table 5.7. The results of the simulation is given in Table 5.8.

Table 5.7 Parameters of the converter of Figure 5.7.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1$ $C_{o1}, C_{o2}$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.8 Simulation results of the converter of Figure 5.7.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	142.428	50.962	33.459	0.941
0.10	153.784	51.908	31.755	0.947
0.15	167.215	53.236	27.185	0.954
0.20	185.946	54.699	21.101	0.963
0.25	205.211	55.981	14.975	0.970
0.30	228.043	57.345	9.8763	0.976
0.35	252.061	58.612	5.386	0.980
0.40	278.916	60.000	2.877	0.983
0.45	306.261	61.361	1.935	0.985



### 5.3.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.7 with an applied input voltage of  $30V_P$  is given in Table 5.9. To derive the equation of the average output voltage of the converter the polarities of the voltages of the circuit during the positive half cycle is shown in Figure 5.9.

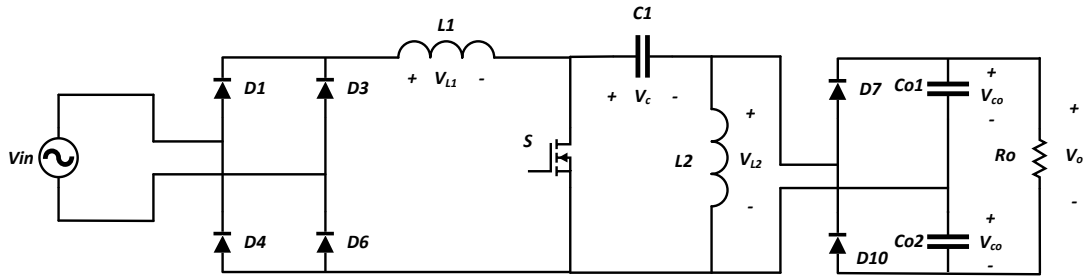


Figure 5.9 Output switched half-bridge AC to DC SEPIC Converter with voltage across the components.

#### At the input stage:

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - v_c - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{SW}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_{in} - v_c - v_{oc}) dt \quad (5.3)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.3),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_{in} - v_c - v_{oc}) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} \begin{bmatrix} V_{in\max} \sin(\omega t - \theta_{in}) \\ -V_{c\max} \sin(\omega t - \theta_c) \\ -V_{o\max} \sin(\omega t - \theta_o) \end{bmatrix} dt$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ & - \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] \\ \text{Or,} & - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] \end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
\text{Or, } & \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\
& + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]
\end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
\text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\
& + \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\
& + \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\
& + \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

Or,

$$V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

$$+ V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

Or,

$$\frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] =$$

$$V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)]$$

Or,

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] =$$

$$V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)]$$

Or,

$$V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] =$$

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] \quad (5.4)$$

**At the output stage:**

When switch is ON,

$$V_{L2} = -V_c$$

When switch is OFF,

$$V_{L2} = V_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt \quad (5.5)$$

Suppose,

$$v_c = V_{cmax} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{omax} \sin(\omega t - \theta_o)$$

From (5.5),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_c dt = \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{cmax} \sin(\omega t - \theta_c) dt = \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} V_{omax} \sin(\omega t - \theta_o) dt$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{cmax}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{sw}} = \sum_{n=1}^N \left[ -\frac{V_{omax}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\begin{aligned}
& \text{Or,} \\
& V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)] \\
& = V_{o\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] = \\
& \text{Or,} \\
& V_{o\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] = \\
& \text{Or,} \\
& V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\begin{aligned}
& \text{Or,} \\
& \frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] = \\
& \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]
\end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or,} \quad \frac{\frac{\omega DT_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or,} \quad \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] \quad (5.6)$$

Equating equation (5.4) and (5.6),

$$\text{Or, } \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \left( \frac{1-D-D}{D} \right) \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \frac{1}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

Thus the average output voltage of the converter can be derived as,

$$V_{OAV} = \frac{1}{\pi} \int_0^\pi V_{o\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^\pi \frac{D}{1-D} V_{in\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} \int_0^\pi \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} [-\cos \theta]_0^\pi$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)} \quad (5.7)$$

Table 5.9 Average output voltage vs duty cycle of the converter of Figure 5.7.

Duty Cycle	Vo (Simulation)
0.1	11.592
0.2	15.951
0.3	21.019
0.4	26.805
0.5	30.369

## 5.4 Capacitor Assisted Output Switched Half-Bridge AC to DC SEPIC Converter

The proposed converter is designed by splitting coupling capacitor into two equal capacitors. During  $T_{off}$ , both capacitor will be charged in series sharing equal voltage between them. During  $T_{on}$ , only capacitor will C1 will charge the inductor L2 with reduced voltage. The converter is show in Figure 5.10.

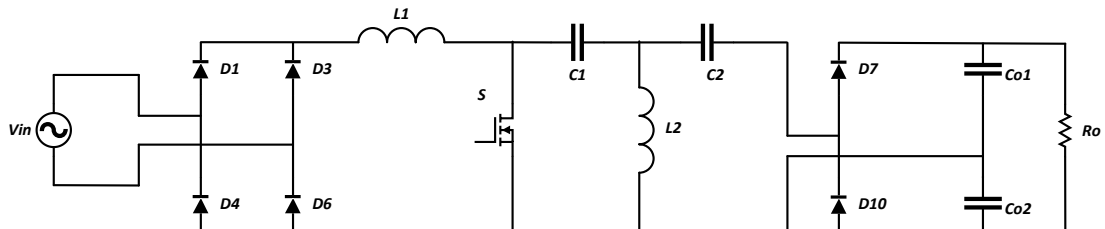
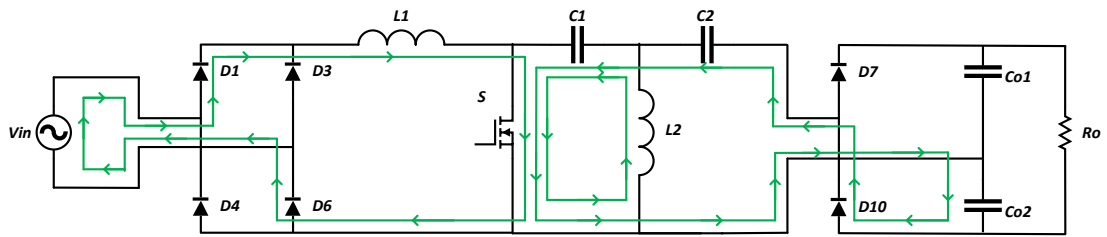


Figure 5.10 Proposed capacitor assisted output switched half-bridge AC to DC SEPIC converter.

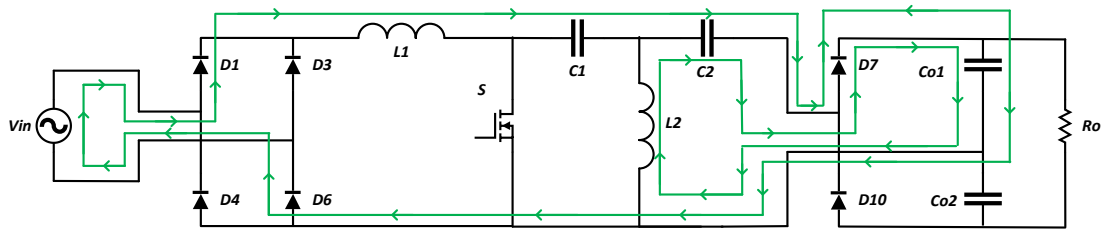
### 5.4.1 Principle of Operation

The four working stages of the converter is illustrated in Figure 5.11. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the SEPIC capacitor charges the output inductor and lower output capacitor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the SEPIC and upper output capacitor in series. Same operations happen when switch turns ON/OFF during negative supply cycle.

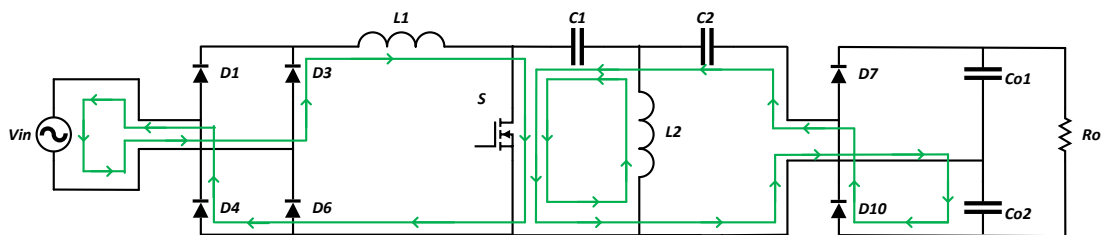




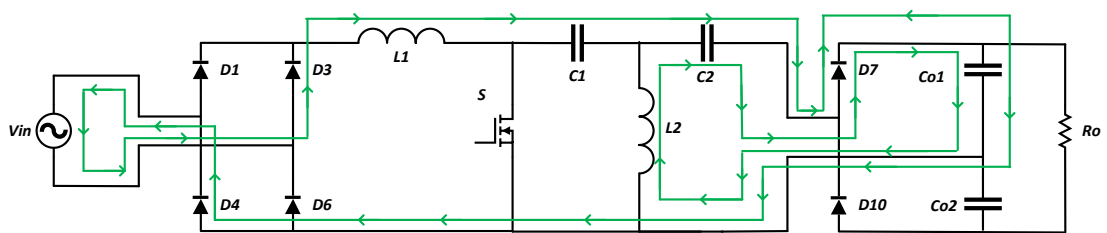
(a)



(b)



(c)



(d)

Figure 5.11 Four steps of operation of the converter in Figure 5.10,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.4.2 Open Loop Simulation

The simulation of the circuit of Figure 5.10 is carried out with the parameters of Table 5.10. The results of the simulation is given in Table 5.11.

Table 5.10 Parameters of the converter of Figure 5.10.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $Co_1, Co_2$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.11 Simulation results of the converter of Figure 5.10.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	85.108	62.688	36.523	0.927
0.10	103.297	76.244	33.612	0.935
0.15	127.165	89.407	30.996	0.935
0.20	149.203	95.171	33.135	0.936
0.25	168.643	98.700	36.444	0.939
0.30	187.358	99.962	34.151	0.941
0.35	203.796	99.451	31.895	0.946
0.40	1008.60	91.407	25.109	0.953
0.45	968.761	68.097	21.139	0.961

### 5.4.3 Ideal Voltage gain Expression

The voltage gain of the SEPIC converter in Figure 5.10 with an applied input voltage of  $30V_P$  is given in Table 5.12. Figure 5.12 shows the voltage across the components for positive half cycle of operation.

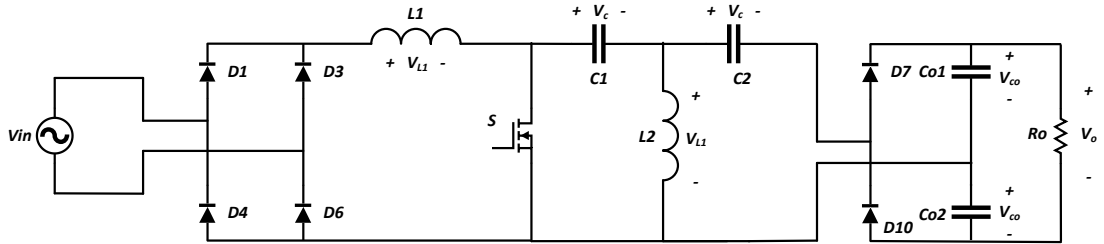


Figure 5.12 Proposed capacitor assisted output switched half-bridge AC to DC SEPIC converter with voltage across the components.

#### At the input stage:

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - 2v_c - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt$$

Where,  $v_{oc} = v_{cu} = v_{cd}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt \quad (5.8)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{co\max} \sin(\omega t - \theta_o)$$

From (5.8),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt$$

Or,

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{in\max} \sin(\omega t - \theta_{in}) dt - 2V_{c\max} \sin(\omega t - \theta_c) - V_{co\max} \sin(\omega t - \theta_o)] dt$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{sw}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ & - \sum_{n=1}^N \left[ -\frac{2V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} - \sum_{n=1}^N \left[ -\frac{V_{co\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] \\ & - \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_c) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_o) \right] \end{aligned}$$

Or,

$$\begin{aligned} & \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or, } & \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \frac{V_{co\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\ & + \sum_{n=1}^N \frac{V_{co\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N 2V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\ & + \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

Or,

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

$$+ \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

Or,

$$\frac{\frac{\omega T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] + \sum_{n=1}^N V_{co\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

Or,

$$\frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] + \sum_{n=1}^N V_{co\max} \left[ \sin(\omega t_i - \theta_o) \right] \quad (5.9)$$

**At the output stage:**

When switch is ON,

$$V_{L2} = -V_c$$

When switch is OFF,

$$V_{L2} = V_c + V_{co}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_c + v_{co}) dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_c + v_{co}) dt \quad (5.10)$$

Suppose,

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{co} = V_{co\max} \sin(\omega t - \theta_o)$$

From (5.10),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_c dt = \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_c + v_{co}) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{c\max} \sin(\omega t - \theta_c) dt = \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{c\max} \sin(\omega t - \theta_c) + V_{co\max} \sin(\omega t - \theta_o)] dt$$

After Integration,

$$\begin{aligned} \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{sw}} &= \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ + \sum_{n=1}^N \left[ -\frac{V_{co\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} & \end{aligned}$$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c) \right] \\
\text{Or,} \quad & = V_{c\max} \sum_{n=1}^N \left[ \cos(\omega t_i + \omega T_{SW} - \theta_c) - \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] \\
& + V_{co\max} \sum_{n=1}^N \left[ \cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] = \\
\text{Or,} \quad & V_{c\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_c + \omega t_i + \omega DT_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_c - \omega t_i - \omega T_{SW} + \theta_c}{2}} \right] \\
& + V_{co\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] = \\
\text{Or,} \quad & V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right] \\
& + V_{co\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\begin{aligned}
& \frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] = \\
\text{Or,} \quad & \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \\
& + \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]
\end{aligned}$$



Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

$$\text{Or, } \frac{\frac{\omega D T_{SW}}{2}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] + \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \left[ \frac{D}{(1-D)} - 1 \right] \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] \quad (5.11)$$

Equating equation (5.9) and (5.11),

$$\text{Or, } \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \frac{2(1-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] + V_{co\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \left( \frac{2-2D-D}{D} \right) \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \frac{(2-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)(2-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

Therefore the average output voltage can be derived as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{co\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{D}{(1-D)(2-D)} V_{in\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)(2-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)(2-D)} [-\cos \theta]_0^{\pi}$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)(2-D)} \quad (5.12)$$

Table 5.12 Average output voltage vs duty cycle of the converter of Figure 5.10.

Duty Cycle	Vo (Simulation)
0.1	11.891
0.2	16.788
0.3	22.035
0.4	27.161
0.5	31.109

## 5.5 Input Switched full-Bridge SEPIC AC to DC Converter

The conventional input switched full bridge converter is shown in Figure 5.13.

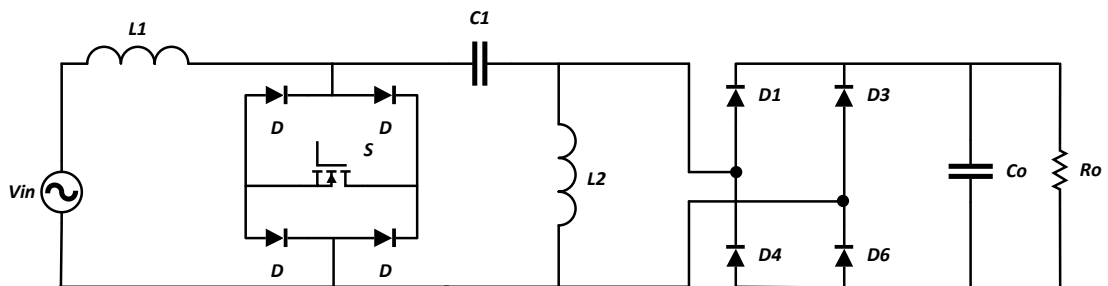
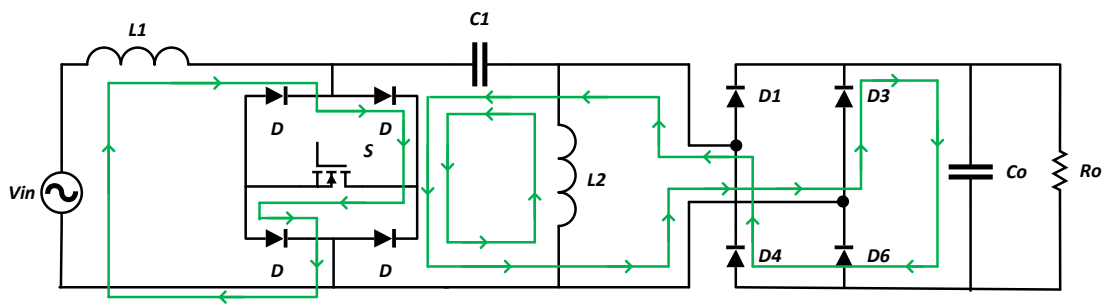


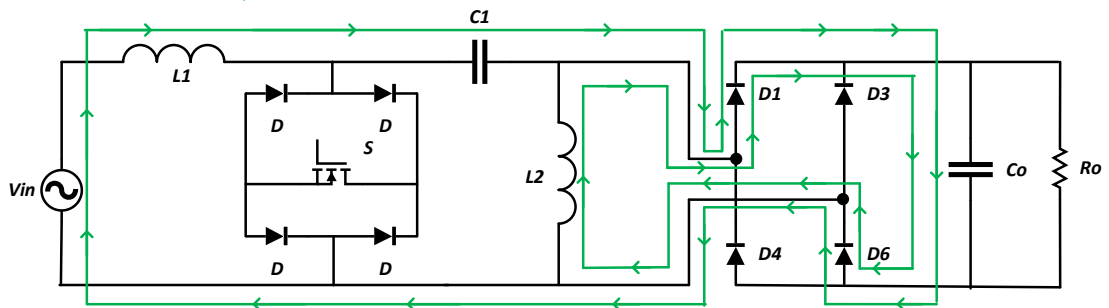
Figure 5.13 Conventional input switched full-bridge AC to DC SEPIC converter.

### 5.5.1 Principle of Operation

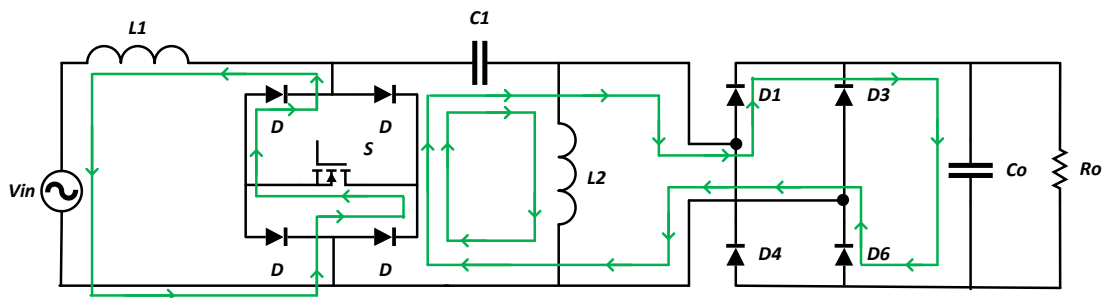
The four working stages of the converter is illustrated in Figure 5.14. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the SEPIC capacitor charges the output inductor and the output capacitor through the switch and the two forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the SEPIC and output capacitor in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



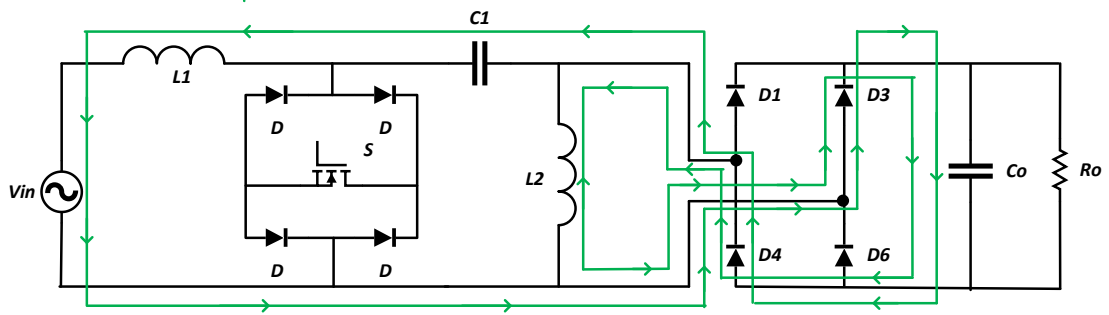
(a)



(b)



(c)



(d)

Figure 5.14 Four steps of operation of the converter in Figure 5.13,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.5.2 Open Loop Simulation

The simulation of the circuit of Figure 5.13 is carried out with the parameters of Table 5.13. The results of the simulation is given in Table 5.14.

Table 5.13 Parameters of the converter of Figure 5.13.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.14 Simulation results of the converter of Figure 5.13.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	153.183	54.704	32.124	0.944
0.10	165.908	61.285	30.50	0.949
0.15	178.321	67.124	27.096	0.956
0.20	205.684	78.542	21.383	0.963
0.25	221.571	80.171	14.668	0.969
0.30	254.055	85.019	8.4061	0.975
0.35	298.467	91.449	4.054	0.980
0.40	336.072	93.489	2.4002	0.983
0.45	386.487	97.077	3.3124	0.986

### 5.5.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.13 with an applied input voltage of  $30V_P$  is given in Table 5.15. The converter of the Figure 5.15 depicts the voltage across the components during positive half cycle of operation.

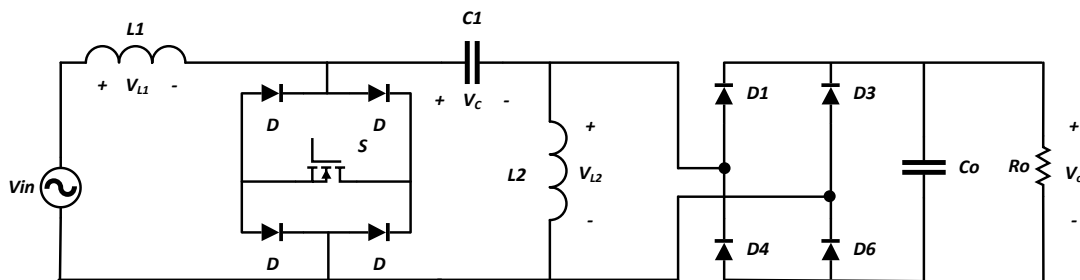


Figure 5.15 Conventional input switched full-bridge AC to DC SEPIC converter with voltage across the components.

**At the input stage:**

When switch is ON,

$$V_{L1} = V_{in}$$

When switch is OFF,

$$V_{L1} = V_{in} - V_c - V_o$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_o) dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_o) dt \quad (5.13)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_o = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.13),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_o) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} \begin{bmatrix} V_{in\max} \sin(\omega t - \theta_{in}) \\ -V_{c\max} \sin(\omega t - \theta_c) \\ -V_{o\max} \sin(\omega t - \theta_o) \end{bmatrix} dt$$

After Integration,

$$\begin{aligned} \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} &= + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ - \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} &- \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \end{aligned}$$

Or,

$$\begin{aligned} &- \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ &= \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] \\ &- \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] \\ &- \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] \end{aligned}$$

Or,

$$\begin{aligned} &\sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ &\sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ &+ \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

$$\begin{aligned} &\sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or, } &\sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ &+ \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\
& + \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\
& + \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\begin{aligned}
\text{Or, } & V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \\
& + V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]
\end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$T_{SW} \rightarrow 0$

$$\begin{aligned}
\text{Or, } & \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] = \\
& V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{o\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right]
\end{aligned}$$



$$\begin{aligned}
\text{Or, } & \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] \\
& + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] \\
\text{Or, } & V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] = \\
& \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] \tag{5.14}
\end{aligned}$$

**At the output stage:**

When switch is ON,

$$v_{L2} = -v_c$$

When switch is OFF,

$$v_{L2} = v_o$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_o dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_o dt \tag{5.15}$$

Suppose,

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_o = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.15),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_c dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} v_o dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{c\max} \sin(\omega t - \theta_c) dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} V_{o\max} \sin(\omega t - \theta_o) dt$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{SW}} = \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

Or,

$$V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)]$$

$$= V_{o\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)]$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] =$$

Or,

$$V_{o\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right]$$

Or,

$$V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] =$$

$$V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]$$

$$\text{Or, } \frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or, } \frac{\frac{\omega DT_{SW}}{2}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] \quad (5.16)$$

Equating equation (5.14) and (5.16),

$$\text{Or, } \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] =$$

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \left( \frac{1-D-D}{D} \right) \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \frac{1}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

Thus the average output voltage of the converter can be derived as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{o\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{D}{1-D} V_{in\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} [-\cos \theta]_0^{\pi}$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)} \tag{5.17}$$

Table 5.15 Average output voltage vs duty cycle of the converter of Figure 5.13.

Duty Cycle	Vo (Simulation)
0.1	11.960
0.2	18.289
0.3	26.160
0.4	32.801
0.5	39.318

## 5.6 Capacitor Assisted Input switched Full-Bridge AC to DC SEPIC Converter

The proposed converter is designed by splitting coupling capacitor into two equal capacitors. During Toff, both capacitor will be charged in series sharing equal voltage between them. During Ton, only capacitor will C1 will charge the inductor L2 with reduced voltage. The converter is show in Figure 5.16.

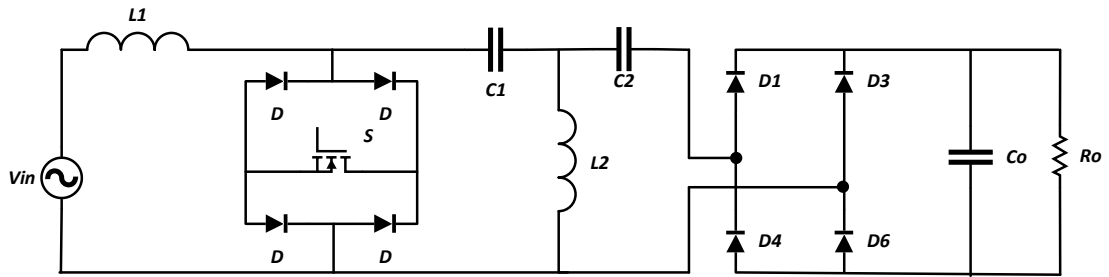
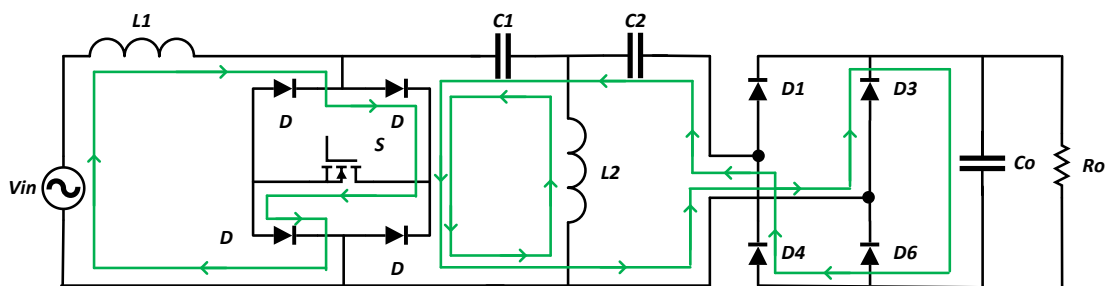


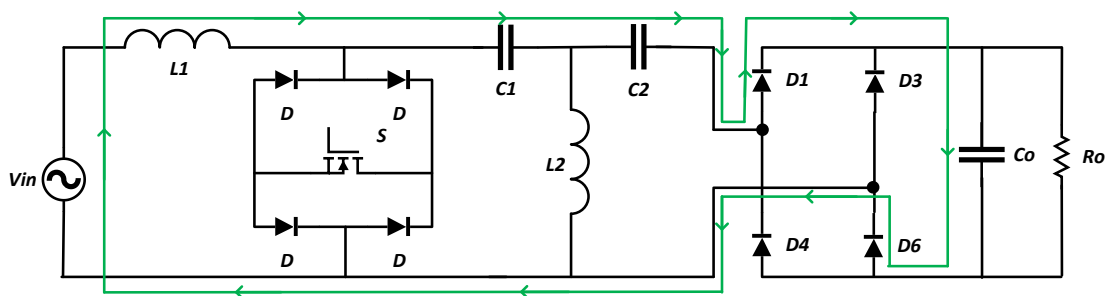
Figure 5.16 Proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter.

### 5.6.1 Principle of Operation

The four working stages of the converter is illustrated in Figure 5.17. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the first of the SEPIC capacitor charges the output inductor capacitor through the switch. When the switch is OFF, source and the inductor voltage charges the SEPIC capacitors and output capacitor in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)



(b)

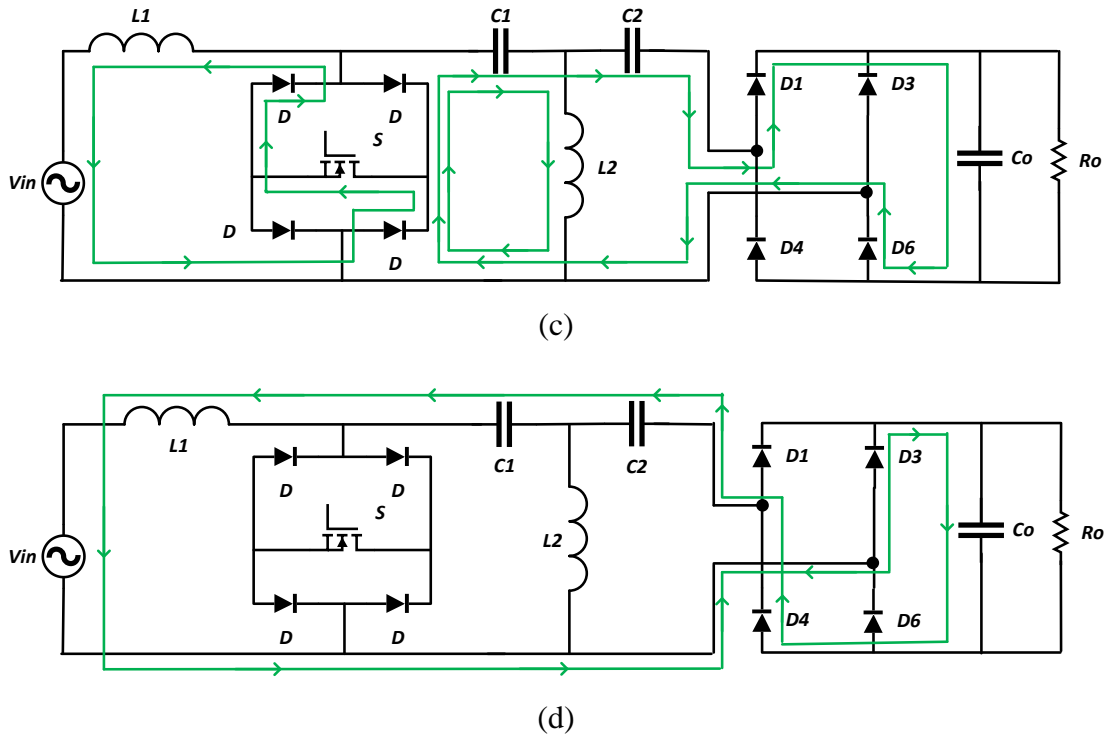


Figure 5.17 Four steps of operation of the converter in Figure 5.16,

- (a) circuit when the switch is ON during positive half cycle
- (b) circuit when the switch is OFF during positive half cycle
- (c) circuit when the switch is ON during negative half cycle
- (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.6.2 Open Loop Simulation

The simulation of the circuit of Figure 5.11 is carried out with the parameters of Table 5.16. The results of the simulation is given in Table 5.17.

Table 5.16 Parameters of the converter of Figure 5.16.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.17 Simulation results of the converter of Figure 5.16.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	87.099	54.619	24.708	0.922
0.10	107.662	62.461	17.734	0.948
0.15	139.064	75.773	11.887	0.962
0.20	176.370	86.027	7.784	0.971
0.25	210.328	89.558	4.9242	0.976
0.30	252.427	95.284	3.3499	0.980
0.35	289.320	97.219	2.7245	0.982
0.40	329.476	98.156	6.5542	0.983
0.45	378.747	97.732	10.444	0.982

### 5.6.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.16 with an applied input voltage of  $30V_P$  is given in Table 5.18. The converter of the Figure 5.18 shows the operation of the circuit for positive half cycle of operation.

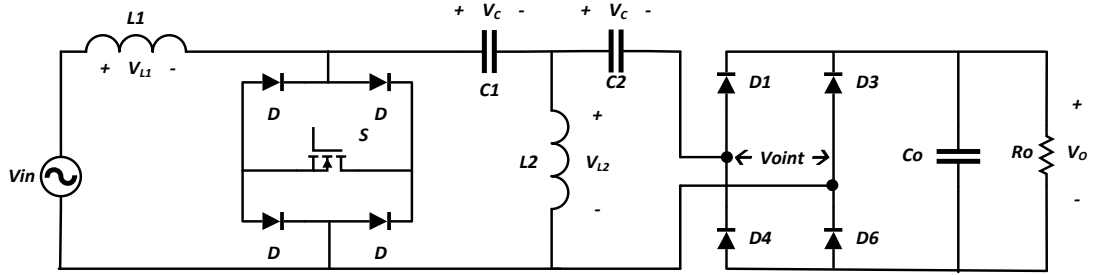


Figure 5.18 Proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter with voltage across the components.

#### At the input stage:

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - 2v_c - v_{oint}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oint}) dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oint}) dt \quad (5.18)$$



Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oint} = V_{oint\max} \sin(\omega t - \theta_o)$$

From (5.18),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_{in} - 2v_c - v_{oint}) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} \begin{bmatrix} V_{in\max} \sin(\omega t - \theta_{in}) \\ -2V_{c\max} \sin(\omega t - \theta_c) \\ -V_{oint\max} \sin(\omega t - \theta_o) \end{bmatrix} dt$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

$$- \sum_{n=1}^N \left[ -\frac{2V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{oint\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

$$- \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right]$$

$$= \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right]$$

Or,

$$- \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right]$$

$$- \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right]$$

$$\begin{aligned}
& \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
\text{Or, } & \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\
& + \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{oint\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]
\end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\
\text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\
& + \sum_{n=1}^N \frac{V_{oint\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\
& + \sum_{n=1}^N \frac{V_{oint\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\
\text{Or, } & \sum_{n=1}^N 2V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\
& + \sum_{n=1}^N V_{oint\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

Or,

$$2V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

$$+ V_{oint\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

Or,

$$\frac{\frac{\omega T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$2V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{oint\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right]$$

Or,

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$2V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{oint\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right]$$

Or,

$$2V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{oint\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right] =$$

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] \quad (5.19)$$

**At the output stage:**

When switch is ON,

$$V_{L2} = -V_c$$

When switch is OFF,

$$v_{L2} = v_{o\text{int}}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{o\text{int}} dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{o\text{int}} dt \quad (5.20)$$

Suppose,

$$v_c = V_{c\text{max}} \sin(\omega t - \theta_c)$$

$$v_{o\text{int}} = V_{o\text{intmax}} \sin(\omega t - \theta_o)$$

From (5.20),

$$\begin{aligned} \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_c dt &= \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{o\text{int}} dt \\ \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{c\text{max}} \sin(\omega t - \theta_c) dt &= \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} V_{o\text{intmax}} \sin(\omega t - \theta_o) dt \end{aligned}$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{c\text{max}}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{sw}} = \sum_{n=1}^N \left[ -\frac{V_{o\text{intmax}}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}}$$

$$\begin{aligned}
& \text{Or,} \\
& V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)] \\
& = V_{o\text{intmax}} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)]
\end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned}
& V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] = \\
& \text{Or,} \\
& V_{o\text{intmax}} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right]
\end{aligned}$$

$$\begin{aligned}
& \text{Or,} \\
& V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] = \\
& V_{o\text{intmax}} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]
\end{aligned}$$

$$\begin{aligned}
& \text{Or,} \\
& \frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] = \\
& \sum_{n=1}^N V_{o\text{intmax}} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]
\end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or,} \quad \frac{\frac{\omega DT_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{o\text{intmax}} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or,} \quad \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\text{intmax}} [\sin(\omega t_i - \theta_o)] \quad (5.21)$$

Equating equation (5.19) and (5.21),

$$\text{Or, } \frac{2(1-D)}{D} \times \sum_{n=1}^N V_{o\text{int max}} [\sin(\omega t_i - \theta_o)] + V_{o\text{int max}} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\text{ max}} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \left( \frac{2-2D-D}{D} \right) \times \sum_{n=1}^N V_{o\text{int max}} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\text{ max}} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \frac{(2-D)}{D} \times \sum_{n=1}^N V_{o\text{int max}} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\text{ max}} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{o\text{int max}} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)(2-D)} \times V_{in\text{ max}} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

Thus the average output voltage  $V_{OAV}$  can be calculated as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{o\text{int max}} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{D}{(1-D)(2-D)} V_{in\text{ max}} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\text{ max}}}{\pi(1-D)(2-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\text{ max}}}{\pi(1-D)(2-D)} [-\cos \theta]_0^{\pi}$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\text{ max}}}{\pi(1-D)(2-D)} \quad (5.22)$$

Table 5.18 Average output voltage vs duty cycle of the converter of Figure 5.16.

Duty Cycle	Vo (Simulation)
0.1	10.905
0.2	18.461
0.3	27.291
0.4	37.023
0.5	44.628

### 5.7 Input Switched Half-Bridge AC to DC SEPIC Converter

The converter is designed by modifying the input switched full-bridge by introducing split capacitors at the load side. The converter is shown in Figure 5.19.

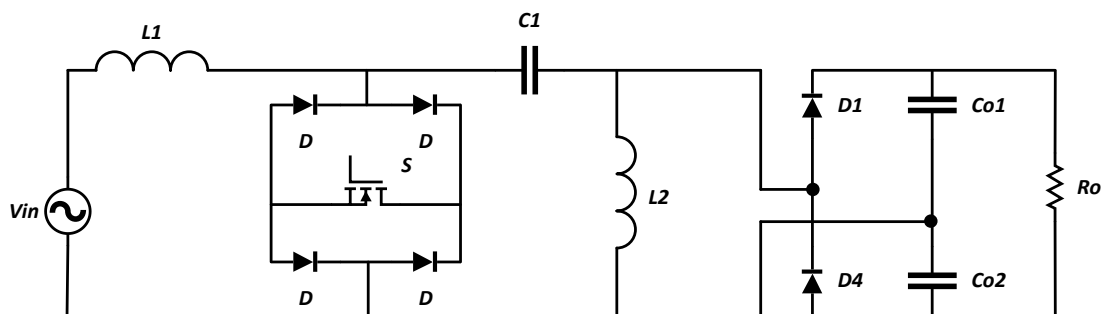
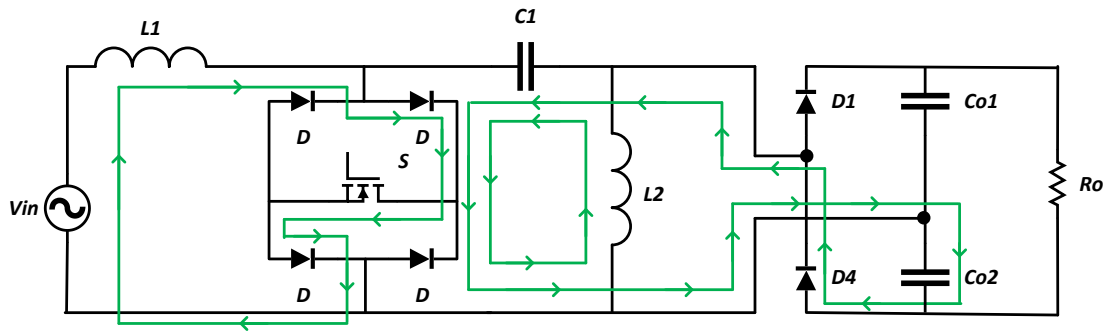


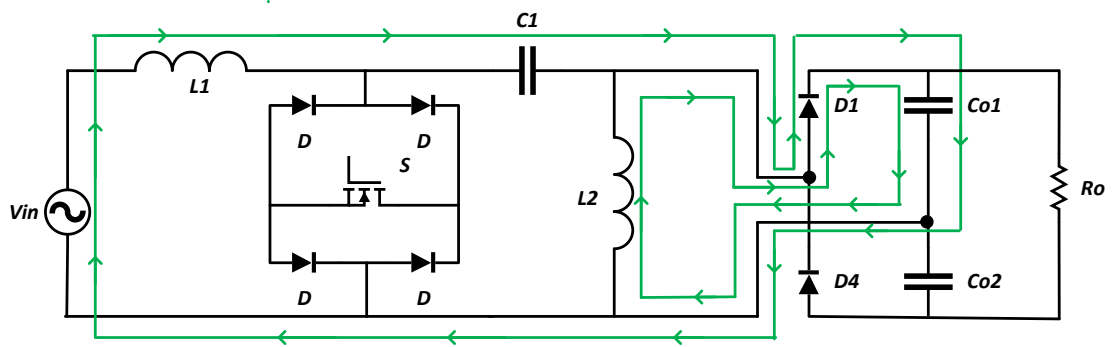
Figure 5.19 Input switched half-bridge AC to DC SEPIC converter.

#### 5.7.1 Principle of Operation

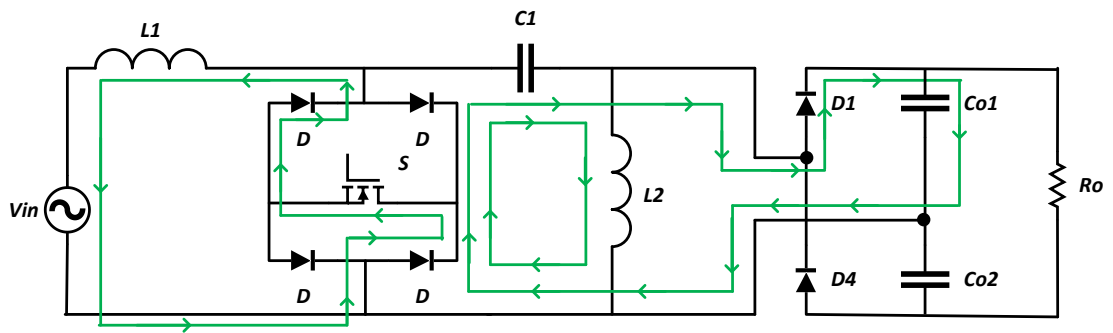
The four working stages of the converter is illustrated in Figure 5.20. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the SEPIC capacitor charges the output inductor and lower output capacitor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the SEPIC and upper output capacitor equally in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)



(b)



(c)



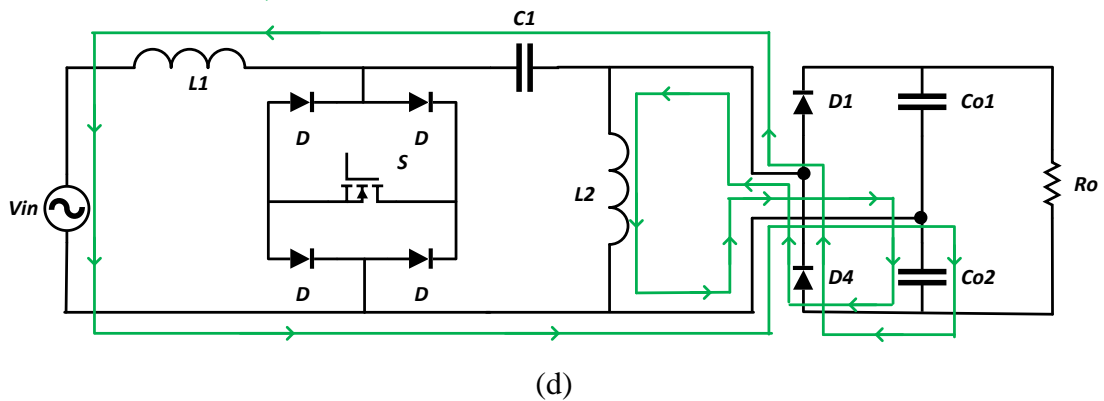


Figure 5.20 Four steps of operation of the converter in Figure 5.19,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.7.2 Open Loop Simulation

The simulation of the circuit of Figure 5.19 is carried out with the parameters of Table 5.19. The results of the simulation is given in Table 5.20.

Table 5.19 Parameters of the converter of Figure 5.19.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1$ $Co_1, Co_2$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.20 Simulation results of the converter of Figure 5.19.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	137.642	30.574	14.859	0.974
0.10	152.387	33.156	15.614	0.974
0.15	166.684	35.483	15.560	0.976
0.20	182.919	40.489	14.521	0.978
0.25	203.140	49.379	12.151	0.979
0.30	223.243	48.168	8.7298	0.980
0.35	246.853	53.004	4.9806	0.982
0.40	274.962	56.591	2.8507	0.984
0.45	305.946	60.838	1.7978	0.985

### 5.7.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.19 with an applied input voltage of  $30V_P$  is given in Table 5.21. The voltage across the component of the converter during positive half cycle of operation is shown in Figure 5.21.

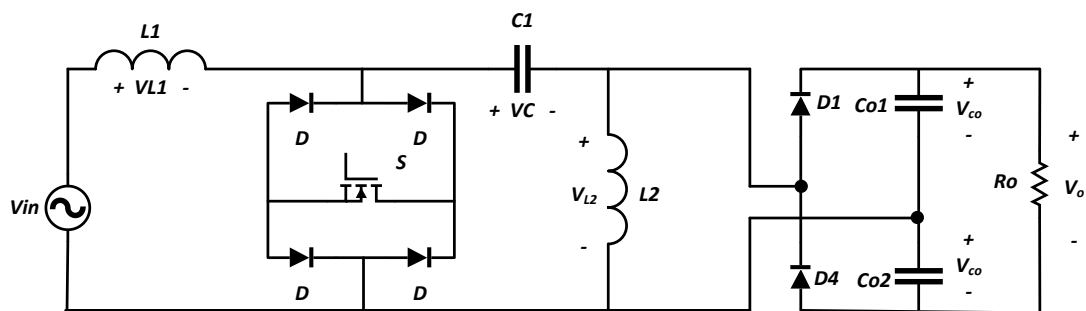


Figure 5.21 Input switched half-bridge AC to DC SEPIC converter with voltage across the components.

**At the input stage:**

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - v_c - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt \quad (5.23)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.23),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} \begin{bmatrix} V_{in\max} \sin(\omega t - \theta_{in}) \\ -V_{c\max} \sin(\omega t - \theta_c) \\ -V_{o\max} \sin(\omega t - \theta_o) \end{bmatrix} dt$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ & - \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \end{aligned}$$

Or,

$$\begin{aligned} & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] \end{aligned}$$

Or,

$$\begin{aligned} & \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ & \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

$$\sum_{n=1}^N \frac{V_{in\max}}{\omega} [\cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in})] =$$

$$\begin{aligned} \text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c)] \\ & + \sum_{n=1}^N \frac{V_{o\max}}{\omega} [\cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o)] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\ & + \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\ & + \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\begin{aligned} \text{Or, } & V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \\ & + V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$T_{SW} \rightarrow 0$

$$\begin{aligned} \text{Or, } & \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] = \\ & V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{o\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right] \end{aligned}$$

$$\begin{aligned}
\text{Or, } & \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \\
& V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] \\
\text{Or, } & V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] = \\
& \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] \tag{5.24}
\end{aligned}$$

**At the output stage:**

When switch is ON,

$$v_{L2} = -v_c$$

When switch is OFF,

$$v_{L2} = v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt \tag{5.25}$$

Suppose,

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.25),

$$\begin{aligned} \sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_c dt &= \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} v_{oc} dt \\ \sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{c\max} \sin(\omega t - \theta_c) dt &= \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} V_{o\max} \sin(\omega t - \theta_o) dt \end{aligned}$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{SW}} = \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

$$\begin{aligned} \text{Or,} \quad & V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)] \\ &= V_{o\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned} & V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] = \\ \text{Or,} \quad & V_{o\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right] \\ & \text{Or,} \quad V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] = \\ & \text{Or,} \quad V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\text{Or, } \frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$

$$\text{Or, } \frac{\frac{\omega DT_{SW}}{2}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)]$$

$$\text{Or, } \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] \quad (5.26)$$

Equating equation (5.24) and (5.26),

$$\text{Or, } \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] =$$

$$\frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \left( \frac{1-D-D}{D} \right) \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\text{Or, } \frac{1}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$



Therefore the average output voltage can be derived as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{o\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{D}{1-D} V_{in\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} [-\cos \theta]_0^{\pi}$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)} \quad (2.27)$$

Table 5.21 Average output voltage vs duty cycle of the converter of Figure 5.19.

Duty Cycle	Vo (Simulation)
0.1	11.516
0.2	15.364
0.3	18.388
0.4	20.975
0.5	24.835

## 5.8 Capacitor Assisted Input Switched Half-Bridge AC to DC SEPIC Converter

The proposed converter is designed by splitting coupling capacitor into two equal capacitors. During Toff, both capacitor will be charged in series sharing equal voltage between them. During Ton, only capacitor will C1 will charge the inductor L2 with reduced voltage. The converter is show in Figure 5.22.

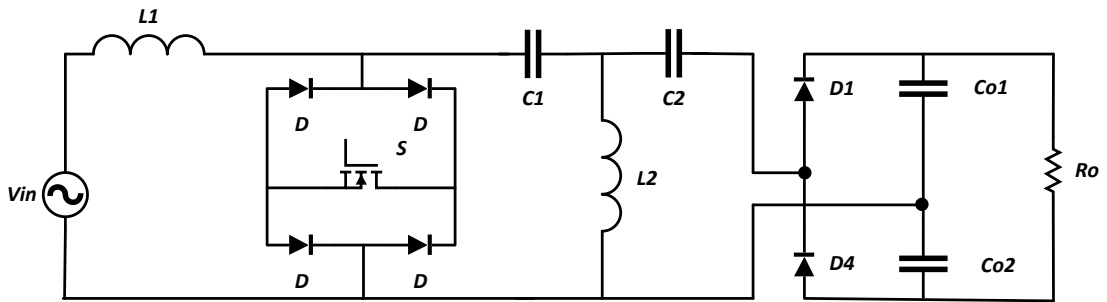
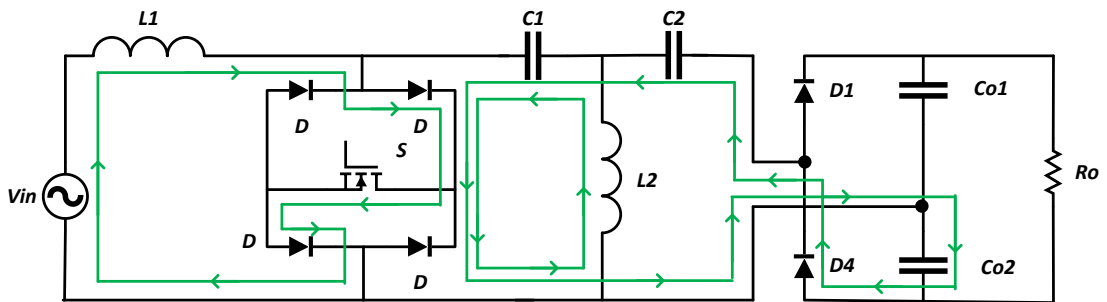


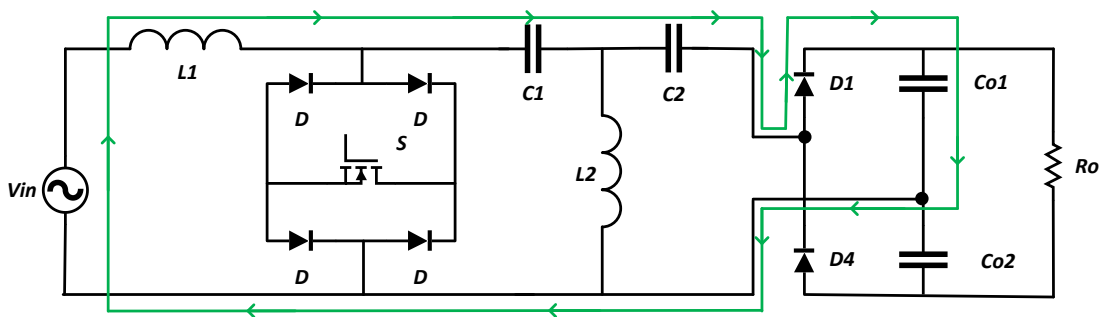
Figure 5.22 Capacitor assisted input switched half-bridge AC to DC SEPIC converter.

### 5.8.1 Principle of Operation

The four working stages of the converter is illustrated in Figure 5.23. When the switch is ON during positive supply cycle, the input inductor charges from the supply voltage and the first of the SEPIC capacitor charges the output inductor and lower output capacitor through the switch and the lower forward biased diode of the output stage. When the switch is OFF, source and the inductor voltage charges the SEPIC and upper output capacitor equally in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



(a)



(b)

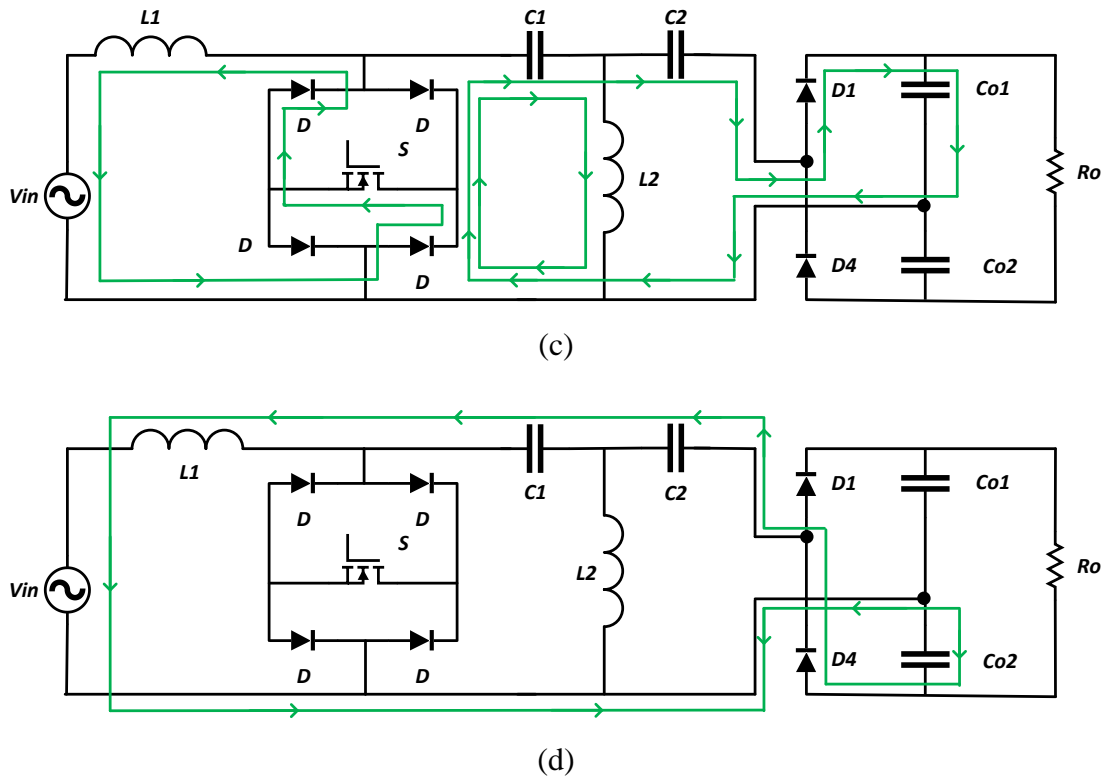


Figure 5.23 Four steps of operation of the converter in Figure 5.22,  
 (a) circuit when the switch is ON during positive half cycle  
 (b) circuit when the switch is OFF during positive half cycle  
 (c) circuit when the switch is ON during negative half cycle  
 (d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.8.2 Open Loop Simulation

The simulation of the circuit of Figure 5.22 is carried out with the parameters of Table 5.22. The results of the simulation is given in Table 2.23.

Table 5.22 Parameters of the converter of Figure 5.22.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $Co_1, Co_2$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_L$	100 $\Omega$

Table 5.23 Simulation results of the converter of Figure 5.22.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	82.997	57.202	33.618	0.932
0.10	98.191	66.594	30.762	0.943
0.15	119.425	78.705	29.722	0.942
0.20	149.251	86.898	31.311	0.941
0.25	173.906	90.984	28.474	0.943
0.30	194.895	93.351	28.792	0.945
0.35	209.783	93.130	30.997	0.947
0.40	222.587	91.108	27.470	0.953
0.45	240.027	87.554	23.353	0.960

### 5.8.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.22 with an applied input voltage of  $30V_P$  is given in Table 5.24. The voltage across the components during positive half cycle of operation is depicted in Figure 5.24.

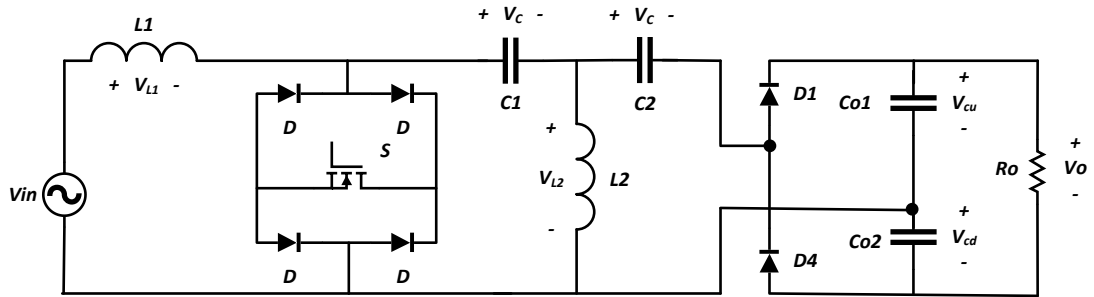


Figure 5.24 Capacitor assisted input switched half-bridge AC to DC SEPIC converter with voltage across the components.

**At the input stage:**

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - 2v_c - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt$$

$$\text{Where, } v_{oc} = v_{cu} = v_{cd}$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of  $N$  switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt \quad (5.28)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{co\max} \sin(\omega t - \theta_o)$$

From (5.28),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - 2v_c - v_{oc}) dt$$

Or,

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} [V_{in\max} \sin(\omega t - \theta_{in}) dt - 2V_{c\max} \sin(\omega t - \theta_c) - V_{co\max} \sin(\omega t - \theta_o)] dt$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{sw}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ & - \sum_{n=1}^N \left[ -\frac{2V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} - \sum_{n=1}^N \left[ -\frac{V_{co\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{sw}}^{t_i+T_{sw}} \\ & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_{in}) \right] \\ & - \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_c) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega T_{sw} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega DT_{sw} - \theta_o) \right] \end{aligned}$$

Or,

$$\begin{aligned} & \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or, } & \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{2V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{co\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ \cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \frac{V_{co\max}}{\omega} \left[ \cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{2V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\ & + \sum_{n=1}^N \frac{V_{co\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N 2V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\ & + \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

Or,

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

$$+ \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

Or,

$$\frac{\frac{\omega T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] + \sum_{n=1}^N V_{co\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

Or,

$$\frac{1}{(1-D)} \times \sum_{n=1}^N V_{in\max} \left[ \sin(\omega t_i - \theta_{in}) \right] =$$

$$\sum_{n=1}^N 2V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] + \sum_{n=1}^N V_{co\max} \left[ \sin(\omega t_i - \theta_o) \right] \quad (5.29)$$

**At the output stage:**

When switch is ON,

$$v_{L2} = -v_c$$

When switch is OFF,

$$v_{L2} = v_c + v_{co}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore



$$\int_{t_i}^{t_i+T_{SW}} v_{L2} dt = \int_{t_i}^{t_i+DT_{SW}} -v_c dt + \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_c + v_{co}) dt$$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{SW}} v_{L2} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_c + v_{co}) dt \quad (5.30)$$

Suppose,

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{co} = V_{co\max} \sin(\omega t - \theta_o)$$

From (5.30),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_c dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} (v_c + v_{co}) dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{c\max} \sin(\omega t - \theta_c) dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} [V_{c\max} \sin(\omega t - \theta_c) + V_{co\max} \sin(\omega t - \theta_o)] dt$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{SW}} = \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} + \sum_{n=1}^N \left[ -\frac{V_{co\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

$$\begin{aligned} & V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)] \\ \text{Or,} \quad & = V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_c) - \cos(\omega t_i + \omega DT_{SW} - \theta_c)] \\ & + V_{co\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] =$$

Or,

$$V_{c\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_c + \omega t_i + \omega DT_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_c - \omega t_i - \omega T_{SW} + \theta_c}{2}} \right]$$

$$+ V_{co\max} \sum_{n=1}^N \left[ \frac{2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2}} \right]$$

$$V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega DT_{SW}}{2} \right] =$$

Or,

$$V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]$$

$$+ V_{co\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right]$$

$$\frac{\sin \frac{\omega DT_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] =$$

Or,

$$\sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

$$+ \sum_{n=1}^N V_{co\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right]$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

$$\begin{aligned}
& \frac{\omega DT_{SW}}{(1-D)\omega T_{SW}} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \\
\text{Or, } & \frac{2}{2} \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] + \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] \\
& \left[ \frac{D}{(1-D)} - 1 \right] \times \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] \\
\text{Or, } & \sum_{n=1}^N V_{c\max} [\sin(\omega t_i - \theta_c)] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] \quad (5.31)
\end{aligned}$$

Equating equation (5.29) and (5.31),

$$\begin{aligned}
& \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \\
\text{Or, } & \frac{2(1-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] + V_{co\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] \\
\text{Or, } & \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \left( \frac{2-2D-D}{D} \right) \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] \\
\text{Or, } & \frac{(2-D)}{D} \times \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] \\
& \sum_{n=1}^N V_{co\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)(2-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]
\end{aligned}$$

Therefore the average output voltage can be derived as,

$$\begin{aligned}
V_{OAV} &= \frac{1}{\pi} \int_0^\pi V_{co\max} \sin \theta d\theta \\
\text{Or, } V_{OAV} &= \frac{1}{\pi} \int_0^\pi \frac{D}{(1-D)(2-D)} V_{in\max} \sin \theta d\theta
\end{aligned}$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)(2-D)} \int_0^\pi \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)(2-D)} [-\cos \theta]_0^\pi$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)(2-D)} \quad (5.32)$$

Table 5.24 Average output voltage vs duty cycle of the converter of Figure 5.22.

Duty Cycle	Vo (Simulation)
0.1	10.739
0.2	19.857
0.3	30.173
0.4	33.702
0.5	34.265

## 5.9 Modified Input Switched AC to DC SEPIC Converter

The proposed converter is designed by moving the switch in between the diode bridge.

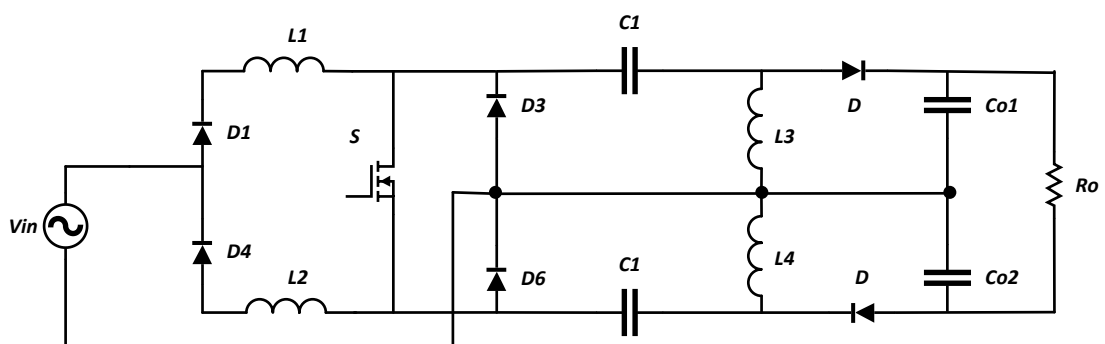
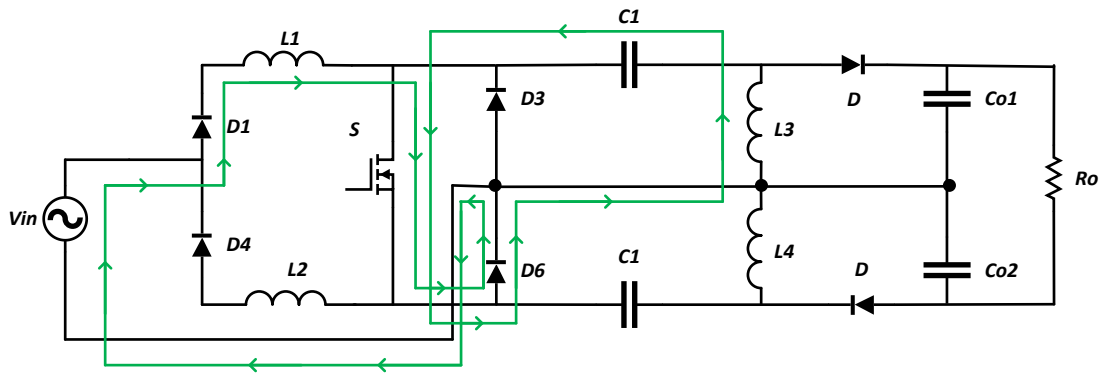


Figure 5.25 Modified input switched AC to DC SEPIC converter.

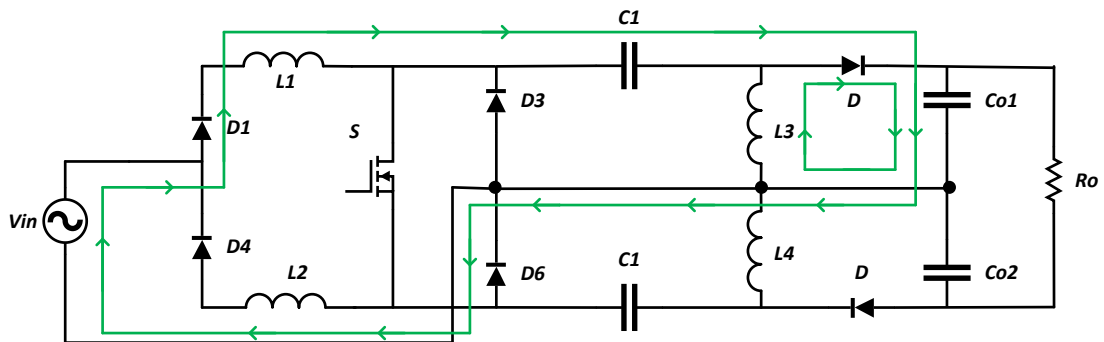
### 5.9.1 Principle of Operation

The four working stages of the converter is illustrated in Figure 5.26. When the switch is ON during positive supply cycle, the upper input inductor charges from the supply

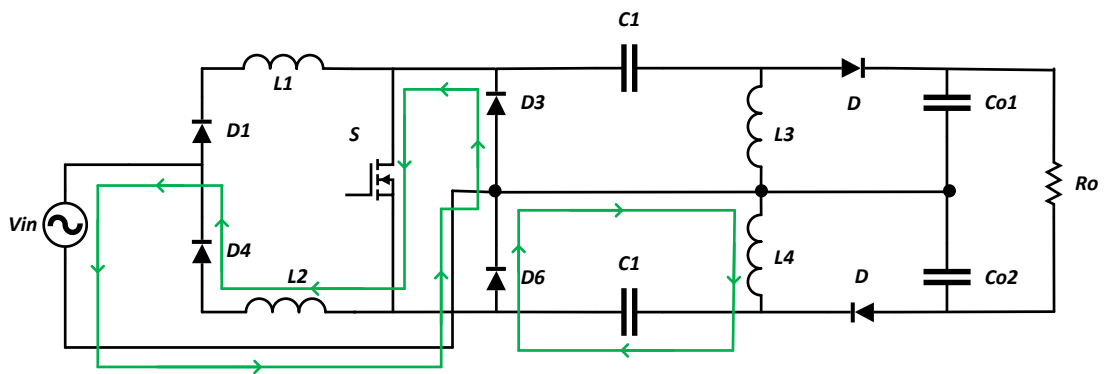
voltage and the upper SEPIC capacitor charges the upper output inductor through the switch and the forward biased diode. When the switch is OFF, source and the inductor voltage charges the upper SEPIC and upper output capacitor in series. Same operations happen when switch turns ON/OFF during negative supply cycle.



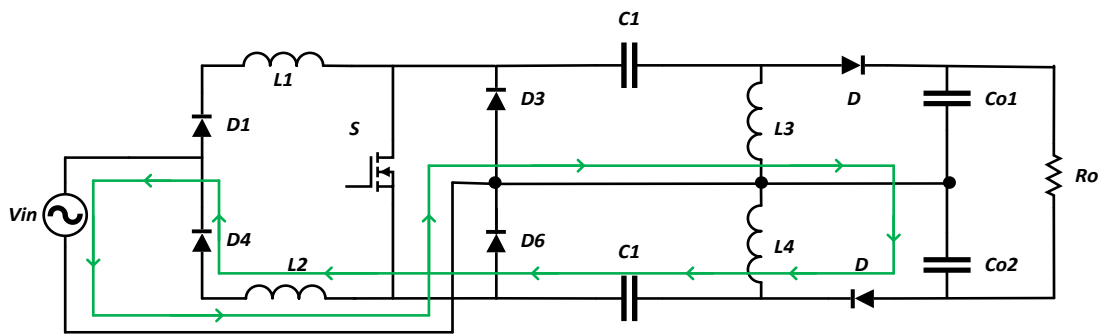
(a)



(b)



(c)



(d)

Figure 5.26 Four steps of operation of the converter in Figure 5.25,

(a) circuit when the switch is ON during positive half cycle

(b) circuit when the switch is OFF during positive half cycle

(c) circuit when the switch is ON during negative half cycle

(d) circuit when the switch is OFF during negative half cycle of line frequency.

### 5.9.2 Open Loop Simulation

The simulation of the circuit of Figure 5.25 is carried out with the parameters of Table 5.25. The results of the simulation is given in Table 5.26.

Table 5.25 Parameters of the converter of Figure 5.25.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 1 mH
Capacitors, $C_1, C_2$ $Co_1, Co_2$	2 $\mu$ F 220 $\mu$ F
Resistor, $RL$	100 $\Omega$

Table 5.26 Simulation results of the converter of Figure 5.25.

Voltage Gain	$V_o$	Efficiency	THD	PFi
0.05	48.128	71.321	172.05	0.627
0.10	77.117	87.449	182.92	0.731
0.15	109.605	91.482	103.79	0.837
0.20	147.466	92.431	46.595	0.895
0.25	189.721	92.320	40.431	0.918
0.30	238.622	91.464	40.319	0.926
0.35	292.523	90.152	37.858	0.934
0.40	352.273	88.943	28.172	0.958
0.45	407.861	87.558	20.133	0.976

### 5.9.3 Ideal Voltage Gain Expression

The voltage gain of the SEPIC converter in Figure 5.25 with an applied input voltage of  $30V_P$  is given in Table 5.27. Figure 5.27 shows the voltage across the components for positive half cycle of operation.

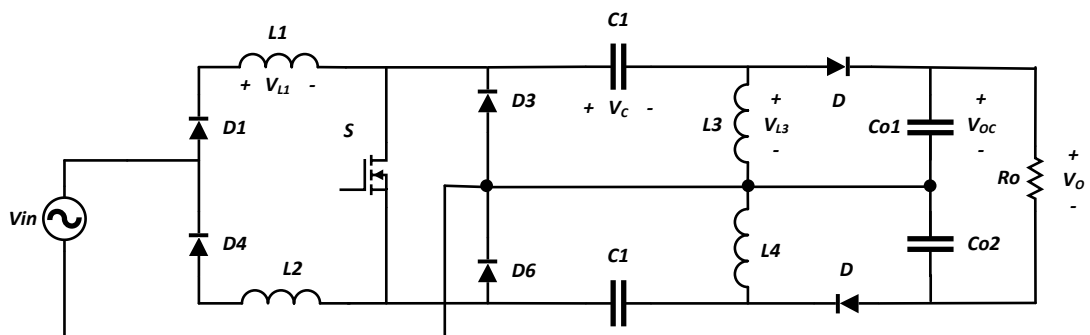


Figure 5.27 Modified input switched AC to DC SEPIC converter with voltage across the components.

**At the input stage:**

When switch is ON,

$$v_{L1} = v_{in}$$

When switch is OFF,

$$v_{L1} = v_{in} - v_c - v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L1} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt \quad (5.33)$$

Suppose,

$$v_{in} = V_{in\max} \sin(\omega t - \theta_{in})$$

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.33),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} v_{in} dt = - \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} (v_{in} - v_c - v_{oc}) dt$$



$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{in\max} \sin(\omega t - \theta_{in}) dt = - \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} \begin{bmatrix} V_{in\max} \sin(\omega t - \theta_{in}) \\ -V_{c\max} \sin(\omega t - \theta_c) \\ -V_{o\max} \sin(\omega t - \theta_o) \end{bmatrix} dt$$

After Integration,

$$\begin{aligned} & \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i}^{t_i+DT_{SW}} = + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t - \theta_{in}) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ & - \sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} - \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}} \\ & - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] + \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] \\ & = \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] - \sum_{n=1}^N \left[ -\frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_{in}) \right] \end{aligned}$$

Or,

$$\begin{aligned} & - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] + \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] \\ & - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i - \theta_{in}) \right] - \sum_{n=1}^N \left[ \frac{V_{in\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_{in}) \right] = \\ \text{Or,} & \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_c) \right] - \sum_{n=1}^N \left[ \frac{V_{c\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_c) \right] \\ & + \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega DT_{SW} - \theta_o) \right] - \sum_{n=1}^N \left[ \frac{V_{o\max}}{\omega} \cos(\omega t_i + \omega T_{SW} - \theta_o) \right] \end{aligned}$$

$$\sum_{n=1}^N \frac{V_{in\max}}{\omega} [\cos(\omega t_i - \theta_{in}) - \cos(\omega t_i + \omega T_{SW} - \theta_{in})] =$$

$$\begin{aligned} \text{Or,} & \sum_{n=1}^N \frac{V_{c\max}}{\omega} [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i + \omega T_{SW} - \theta_c)] \\ & + \sum_{n=1}^N \frac{V_{o\max}}{\omega} [\cos(\omega t_i + \omega DT_{SW} - \theta_o) - \cos(\omega t_i + \omega T_{SW} - \theta_o)] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$\begin{aligned} & \sum_{n=1}^N \frac{V_{in\max}}{\omega} \left[ 2 \sin \frac{\omega t_i - \theta_{in} + \omega t_i + \omega T_{SW} - \theta_{in}}{2} \sin \frac{\omega t_i + \omega T_{SW} - \theta_{in} - \omega t_i + \theta_{in}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N \frac{V_{c\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i + \omega T_{SW} - \theta_c}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2}} \right] \\ & + \sum_{n=1}^N \frac{V_{o\max}}{\omega} \left[ \frac{2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o + \omega t_i + \omega T_{SW} - \theta_o}{2}}{\sin \frac{\omega t_i + \omega T_{SW} - \theta_o - \omega t_i - \omega DT_{SW} + \theta_o}{2}} \right] \end{aligned}$$

$$\begin{aligned} & \sum_{n=1}^N V_{in\max} \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \sin \frac{\omega T_{SW}}{2} \right] = \\ \text{Or, } & \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \\ & + \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(1-D)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\frac{\sin \frac{\omega T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times V_{in\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_{in} + \frac{\omega T_{SW}}{2} \right) \right] =$$

$$\begin{aligned} \text{Or, } & V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \\ & + V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$T_{SW} \rightarrow 0$

$$\begin{aligned} \text{Or, } & \frac{\frac{\omega T_{SW}}{2}}{(1-D)\omega T_{SW}} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] = \\ & V_{c\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_c) \right] + V_{o\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right] \end{aligned}$$

$$\begin{aligned}
& \text{Or, } \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] = \\
& \quad V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] \\
& \text{Or, } V_{c\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_c)] + V_{o\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_o)] = \\
& \quad \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})] \tag{5.34}
\end{aligned}$$

**At the output stage:**

When switch is ON,

$$v_{L3} = -v_c$$

When switch is OFF,

$$v_{L3} = v_{oc}$$

Volt-sec balance over one switching cycle will not be equal to zero since the input is sinusoidal. Volt-Sec balance for one switching cycle is therefore

$$\int_{t_i}^{t_i+T_{sw}} v_{L3} dt = \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt$$

Where,  $v_{oc} = v_{o1} = v_{o2}$

The volt-sec balance over a line frequency period will be zero. For full supply cycle of N switching per period,

$$\sum_{n=1}^N \int_{t_i}^{t_i+T_{sw}} v_{L3} dt = \sum_{n=1}^N \int_{t_i}^{t_i+DT_{sw}} -v_c dt + \sum_{n=1}^N \int_{t_i+DT_{sw}}^{t_i+T_{sw}} v_{oc} dt \tag{5.35}$$

Suppose,

$$v_c = V_{c\max} \sin(\omega t - \theta_c)$$

$$v_{oc} = V_{o\max} \sin(\omega t - \theta_o)$$

From (5.35),

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} v_c dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} v_{oc} dt$$

$$\sum_{n=1}^N \int_{t_i}^{t_i+DT_{SW}} V_{c\max} \sin(\omega t - \theta_c) dt = \sum_{n=1}^N \int_{t_i+DT_{SW}}^{t_i+T_{SW}} V_{o\max} \sin(\omega t - \theta_o) dt$$

After Integration,

$$\sum_{n=1}^N \left[ -\frac{V_{c\max}}{\omega} \cos(\omega t - \theta_c) \right]_{t_i}^{t_i+DT_{SW}} = \sum_{n=1}^N \left[ -\frac{V_{o\max}}{\omega} \cos(\omega t - \theta_o) \right]_{t_i+DT_{SW}}^{t_i+T_{SW}}$$

$$\begin{aligned} \text{Or,} \quad & V_{c\max} \sum_{n=1}^N [\cos(\omega t_i + \omega DT_{SW} - \theta_c) - \cos(\omega t_i - \theta_c)] \\ & = V_{o\max} \sum_{n=1}^N [\cos(\omega t_i + \omega T_{SW} - \theta_o) - \cos(\omega t_i + \omega DT_{SW} - \theta_o)] \end{aligned}$$

Using identity,  $\cos A - \cos B = 2 \sin \frac{A+B}{2} \sin \frac{B-A}{2}$

$$V_{c\max} \sum_{n=1}^N \left[ 2 \sin \frac{\omega t_i + \omega DT_{SW} - \theta_c + \omega t_i - \theta_c}{2} \sin \frac{\omega t_i - \theta_c - \omega t_i - \omega DT_{SW} + \theta_c}{2} \right] =$$

$$\text{Or,} \quad V_{o\max} \sum_{n=1}^N \left[ \begin{array}{l} 2 \sin \frac{\omega t_i + \omega T_{SW} - \theta_o + \omega t_i + \omega DT_{SW} - \theta_o}{2} \\ \sin \frac{\omega t_i + \omega DT_{SW} - \theta_o - \omega t_i - \omega T_{SW} + \theta_o}{2} \end{array} \right]$$

$$\begin{aligned} & V_{c\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \sin \frac{-\omega D T_{SW}}{2} \right] = \\ \text{Or,} & V_{o\max} \sum_{n=1}^N \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \sin \frac{(D-1)\omega T_{SW}}{2} \right] \end{aligned}$$

$$\begin{aligned} & \frac{\sin \frac{\omega D T_{SW}}{2}}{\sin \frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin \left( \omega t_i - \theta_c + \frac{\omega T_{SW}}{2} \right) \right] = \\ \text{Or,} & \sum_{n=1}^N V_{o\max} \left[ \sin \left( \omega t_i - \theta_o + \frac{(1+D)\omega T_{SW}}{2} \right) \right] \end{aligned}$$

Using identities,  $\lim_{\theta \rightarrow 0} \frac{\sin \theta}{\theta} = 1$  and i.  $\frac{\omega T_{SW}}{2} \rightarrow 0$  as  $T_{SW} \rightarrow 0$  ii.  $\frac{(1+D)\omega T_{SW}}{2} \rightarrow 0$  as

$$T_{SW} \rightarrow 0$$

$$\text{Or,} \quad \frac{\frac{\omega D T_{SW}}{2}}{\frac{(1-D)\omega T_{SW}}{2}} \times \sum_{n=1}^N V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] = \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right]$$

$$\text{Or,} \quad \sum_{n=1}^N V_{c\max} \left[ \sin(\omega t_i - \theta_c) \right] = \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right] \quad (5.36)$$

Equating equation (5.34) and (5.36),

$$\begin{aligned} & \frac{(1-D)}{D} \times \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right] + V_{o\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_o) \right] = \\ \text{Or,} & \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right] \end{aligned}$$

$$\text{Or,} \quad \left( \frac{1-D-D}{D} \right) \times \sum_{n=1}^N V_{o\max} \left[ \sin(\omega t_i - \theta_o) \right] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N \left[ \sin(\omega t_i - \theta_{in}) \right]$$

$$\text{Or, } \frac{1}{D} \times \sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{1}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

$$\sum_{n=1}^N V_{o\max} [\sin(\omega t_i - \theta_o)] = \frac{D}{(1-D)} \times V_{in\max} \sum_{n=1}^N [\sin(\omega t_i - \theta_{in})]$$

So the average output voltage can be calculated as,

$$V_{OAV} = \frac{1}{\pi} \int_0^{\pi} V_{o\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{1}{\pi} \int_0^{\pi} \frac{D}{1-D} V_{in\max} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} \int_0^{\pi} \sin \theta d\theta$$

$$\text{Or, } V_{OAV} = \frac{DV_{in\max}}{\pi(1-D)} [-\cos \theta]_0^{\pi}$$

$$\text{Or, } V_{OAV} = \frac{2DV_{in\max}}{\pi(1-D)} \quad (5.37)$$

Table 5.27 Average output voltage vs duty cycle of the converter of Figure 5.25.

Duty Cycle	Vo (Simulation)
0.1	12.424
0.2	19.453
0.3	28.752
0.4	37.514
0.5	44.113

## 5.10 Comparison of Conversion Efficiency

The comparison among the conventional and the proposed converters in terms of conversion efficiency are shown in Table 5.28. The corresponding curves are shown in Figure 5.28.

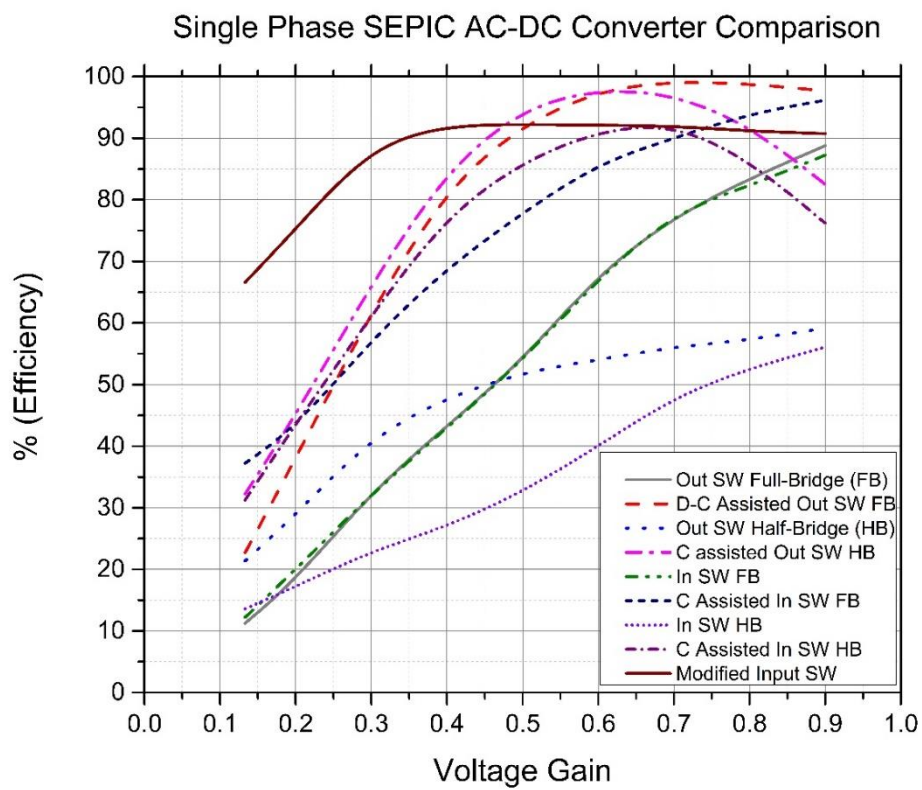


Figure 5.28 Comparison of AC to DC SEPIC converters in terms of conversion efficiency.

Table 5.28 Comparison of Single Phase AC-DC SEPIC Converters.

Voltage Gain	Output Switched Full-Bridge	Diode-Capacitor Assisted Output Switched Full-Bridge	Output Switched Half-Bridge	Capacitor Assisted Output Switched half-Bridge	Input Switched Full-Bridge	Capacitor assisted Input Switched Full-Bridge	Input Switched Half-Bridge	Capacitor assisted Input Switched Half-Bridge	Modified Input Switched
0.133	11.253	22.687	21.351	32.232	12.22	37.229	13.599	31.254	66.593
0.2	18.221	37.981	28.852	44.993	19.998	43.002	17.212	43.597	75.221
0.3	32.587	61.883	41.578	66.32	32.223	57.291	22.985	61.274	88.854
0.4	43.251	82.124	47.897	85.01	42.993	68.981	26.895	77.521	92.102
0.5	53.875	92.235	52.014	95.002	53.886	77.876	32.523	86.251	92.254
0.6	68.02	97.852	54.041	98.021	67.258	85.985	39.997	91.268	92.098
0.7	77.233	99.254	56.124	97.251	78.011	90.001	47.982	92.514	91.982
0.8	83.475	98.841	57.214	92.127	82.256	94.021	52.654	86.457	91.14
0.9	88.781	97.687	59.201	82.514	87.241	96.14	56.074	76.214	90.748



## **5.11 Discussions**

All three proposed converters show better conversion efficiency compared to corresponding conventional ones at extreme low voltage gain. Though the input power factor of the converters are reasonably good but the input current THD is high. For attaining low input current THD, the converters with conventional feedbacks are studied. To the feedback circuit studies, the output voltage regulations have also been included. Typical results of feedback controlled proposed circuits by simulation study are provided in chapter 6.

# Chapter 6

## Investigation of Step-Down Converters with Feedback

The proposed single phase AC to DC step-down converters intended for very low voltage gain are subjected to study with feedback control. Both voltage and current control are considered for the simulation. The objective of the investigation is to improve input power factor and reduce total harmonic distortion of the input current. Dynamic response of the converters in terms of sudden load change are also studied.

### 6.1 Modified input switched AC to DC SEPIC converter

#### 6.1.1 Feedback Analysis

The proposed modified input switched AC to DC converter with feedback control is shown in Figure 6.1. The parameters used for the simulation of the converter is given in Table 6.1. The results of the simulation with reference voltage variation is given in Table 6.2. Typical waveform of the circuit is shown in Figure 6.2. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

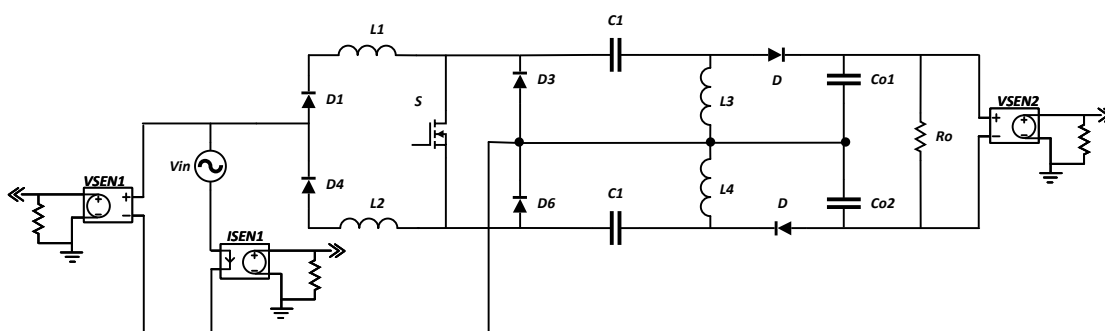


Figure 6.1 Modified input switched AC to DC SEPIC converter with feedback control.

Table 6.1 Parameters of the circuit of Figure 6.1.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_{o1}, C_{o2}$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	1.67

Table 6.2 Results of the feedback of the modified input switched AC to DC SEPIC converter.

Ref	$V_{in}$ (peak)	$I_{in}$ (RMS)	$V_o$ (Avg)	Input Current THD	Power Factor	Input Power
1.0	300	0.216	36.721	16.434	0.851	27.606
4.0	300	1.034	117.015	12.795	0.875	183.276
7.0	300	2.040	170.652	15.645	0.893	386.346
10.0	300	3.173	212.436	13.938	0.907	610.574

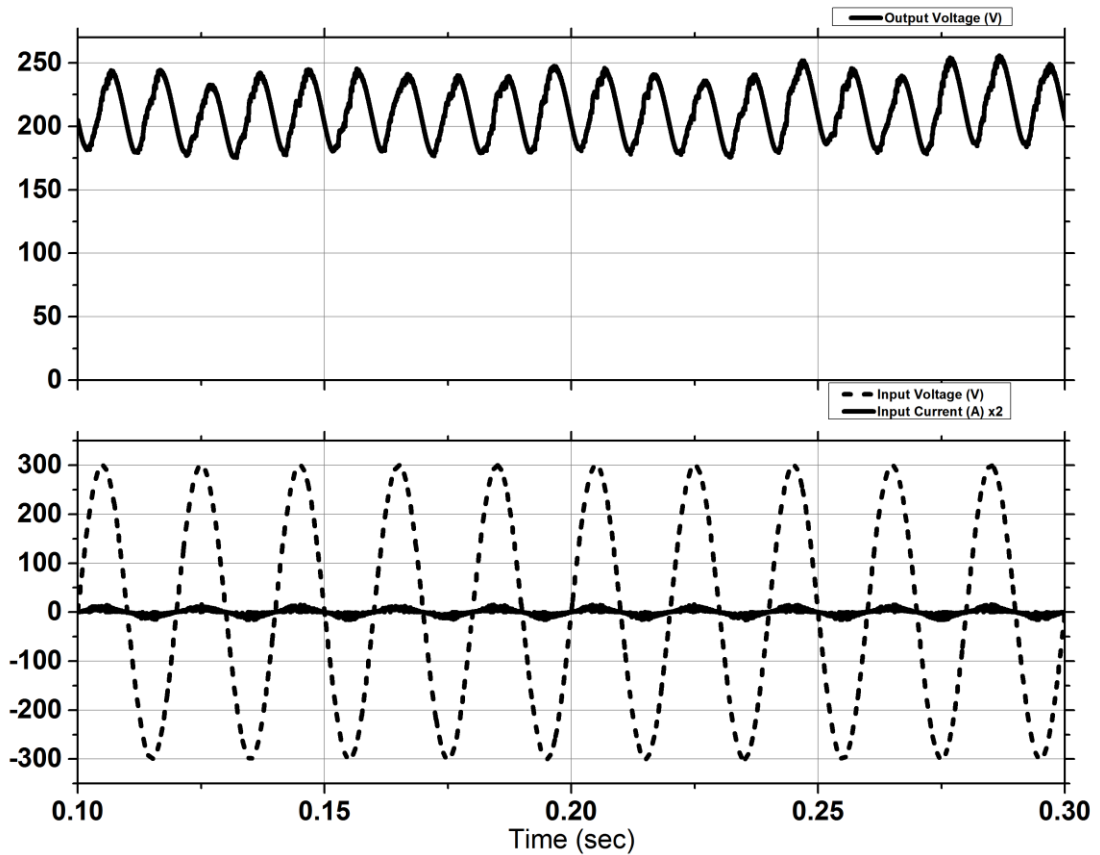


Figure 6.2 Typical input-output waveforms of the circuit of Figure 6.1.

### 6.1.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 177 Vdc output with a resistive load of 100  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 80  $\Omega$  at 250ms, 100  $\Omega$  at 450ms and 120  $\Omega$  at 650ms of the simulation time, which is given in Table 6.3. The circuit parameters are given in Table 6.4. The simulation result showing the variation of output voltage and input current for the circuit of Figure 6.3 is shown in Figure 6.4. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

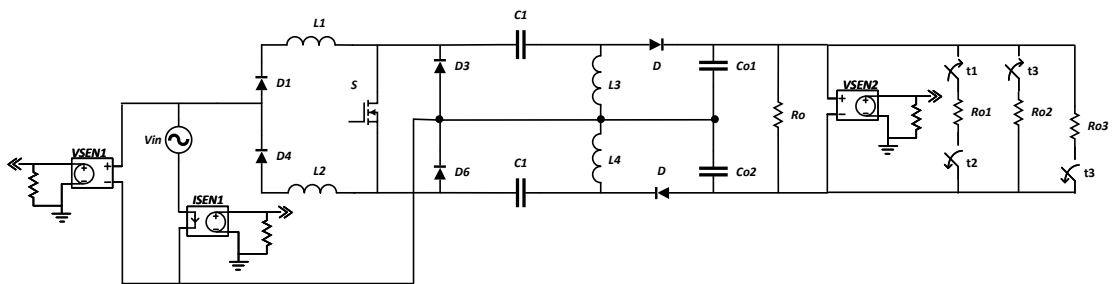


Figure 6.3 Modified input switched AC to DC SEPIC converter for dynamic analysis.

Table 6.3 Changes in load for Figure 6.3.

Time (ms)	Load ( $\Omega$ )
0-400	100
400-650	80
650-900	100
900-1200	120

Table 6.4 Parameters of the circuit of Figure 6.3.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$ $L_3, L_4$	5 mH 1 mH
Capacitors, $C_1, C_2$ $Co_1, Co_2$	2 $\mu$ F 680 $\mu$ F
Resistor, $R_o$ $Ro_1, Ro_2, Ro_3$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $VSEN1$ $VSEN2$	0.0033 0.00167
Gain of Current Sensor $ISEN1$	0.72
Time $t_1, t_2, t_3$	400 ms, 650 ms, 900 ms

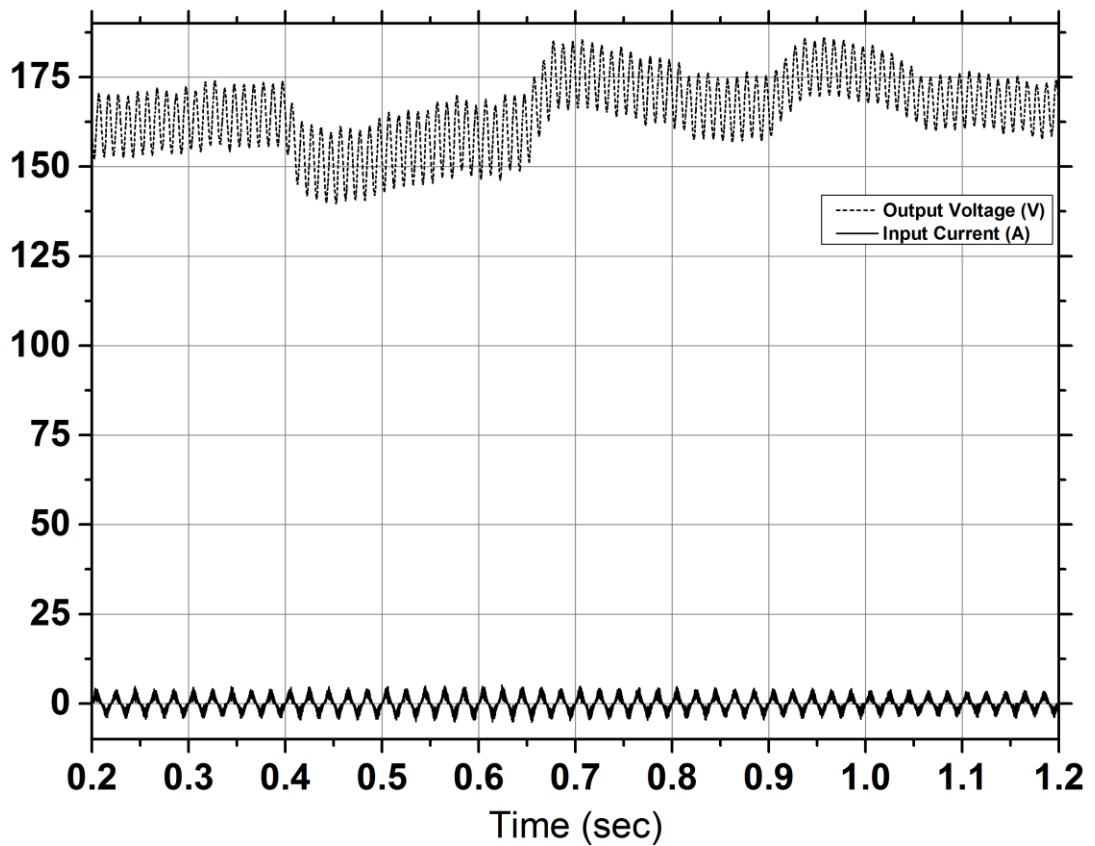


Figure 6.4 Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.3.

## 6.2 Capacitor Assisted Input switched Full-Bridge AC to DC SEPIC converter

### 6.2.1 Feedback Analysis

The proposed capacitor assisted input switched full-bridge AC to DC converter with feedback control is shown in Figure 6.5. The parameters used for the simulation of the converter is given in Table 6.5. The results of the simulation with reference voltage variation is given in Table 6.6. Typical waveform of the circuit is shown in Figure 6.6. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

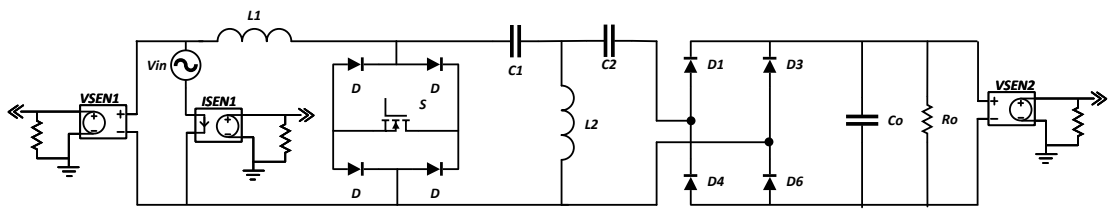


Figure 6.5 Capacitor assisted input switched full-bridge AC to DC SEPIC converter with feedback control.

Table 6.5 Parameters of the circuit of Figure 6.5.

Nominal input ac source voltage, $V_l$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors,	
$L_1$	5 mH
$L_2$	1 mH
Capacitors,	
$C_1, C_2$	2 $\mu$ F
$C_o$	220 $\mu$ F
Resistor,	
$R_o$	100 $\Omega$
Gain of Voltage Sensor	
$V_{SEN1}$	0.0033
$V_{SEN2}$	0.0033
Gain of Current Sensor	
$I_{SEN1}$	0.835



Table 6.6 Results of the feedback of the proposed capacitor assisted input switched full-bridge AC to DC SEPIC converter.

Ref	V <sub>in</sub> (peak)	I <sub>in</sub> (RMS)	V <sub>o</sub> (Avg)	Input Current THD	Power Factor	Input Power
0.5	300	1.2424	92.885	19.755	0.857	176.4
0.75	300	1.4687	124.27	12.946	0.912	286.26
1.0	300	1.6179	155.199	17.289	0.907	414.759
1.25	300	2.5424	181.126	18.122	0.918	495.402

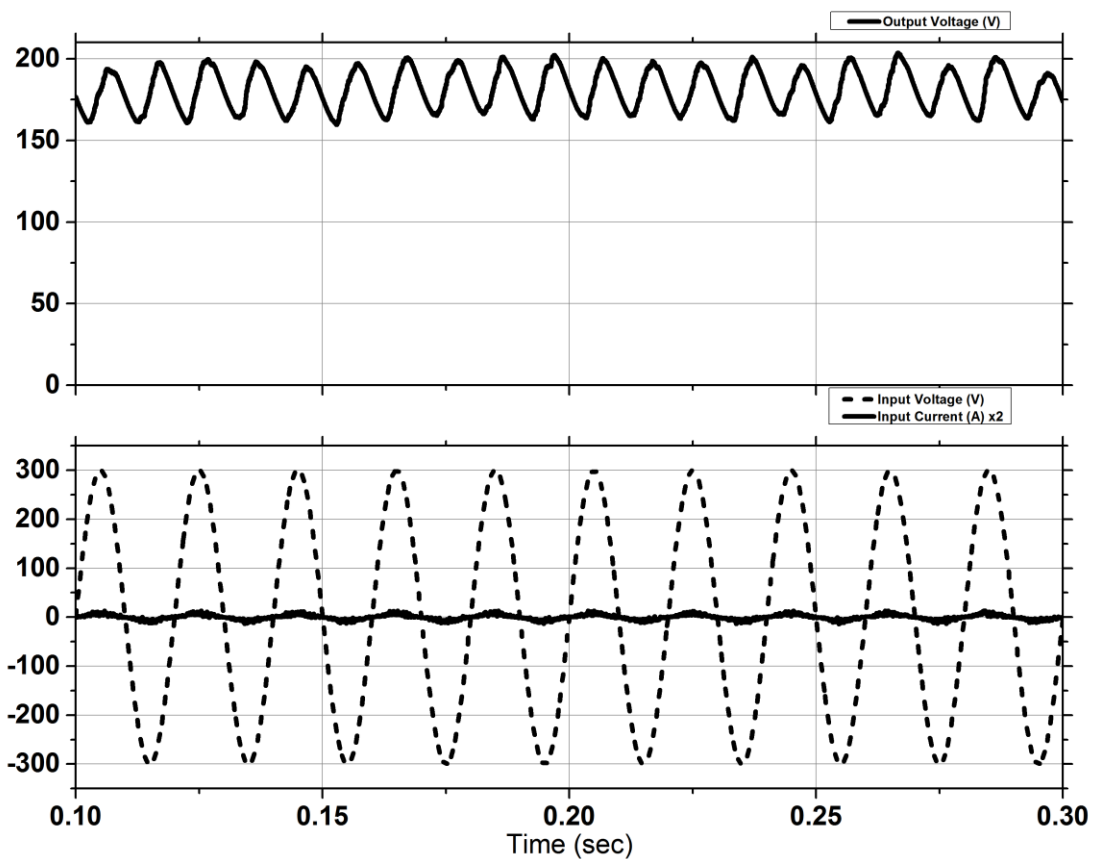


Figure 6.6 Typical input-output waveforms of the circuit of Figure 6.5.

### 6.2.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 152 Vdc output with a resistive load of 100  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 80  $\Omega$  at 250ms, 100  $\Omega$  at 450ms and 120  $\Omega$  at 650ms of the simulation time, which is given in Table 6.7. The circuit parameters are given in Table 6.8. The simulation result showing the variation of output voltage and input current for the circuit of Figure 6.7 is shown in Figure 6.8. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

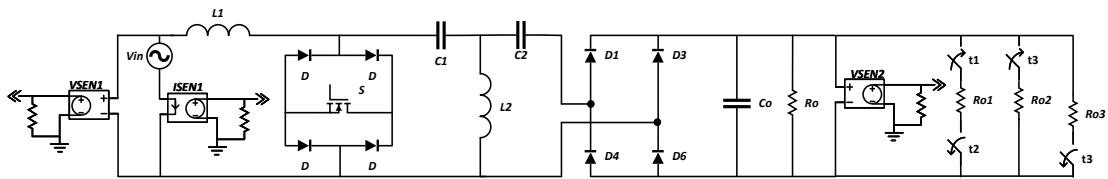


Figure 6.7 Capacitor assisted input switched full-bridge AC to DC SEPIC converter for dynamic analysis.

Table 6.7 Changes in load for Figure 6.7.

Time (ms)	Load ( $\Omega$ )
0-400	100
400-650	80
650-900	100
900-1200	120

Table 6.8 Parameters of the circuit of Figure 6.7.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_o$ $R_{o1}, R_{o2}, R_{o3}$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.67
Time $t_1, t_2, t_3$	400 ms, 650 ms, 900 ms

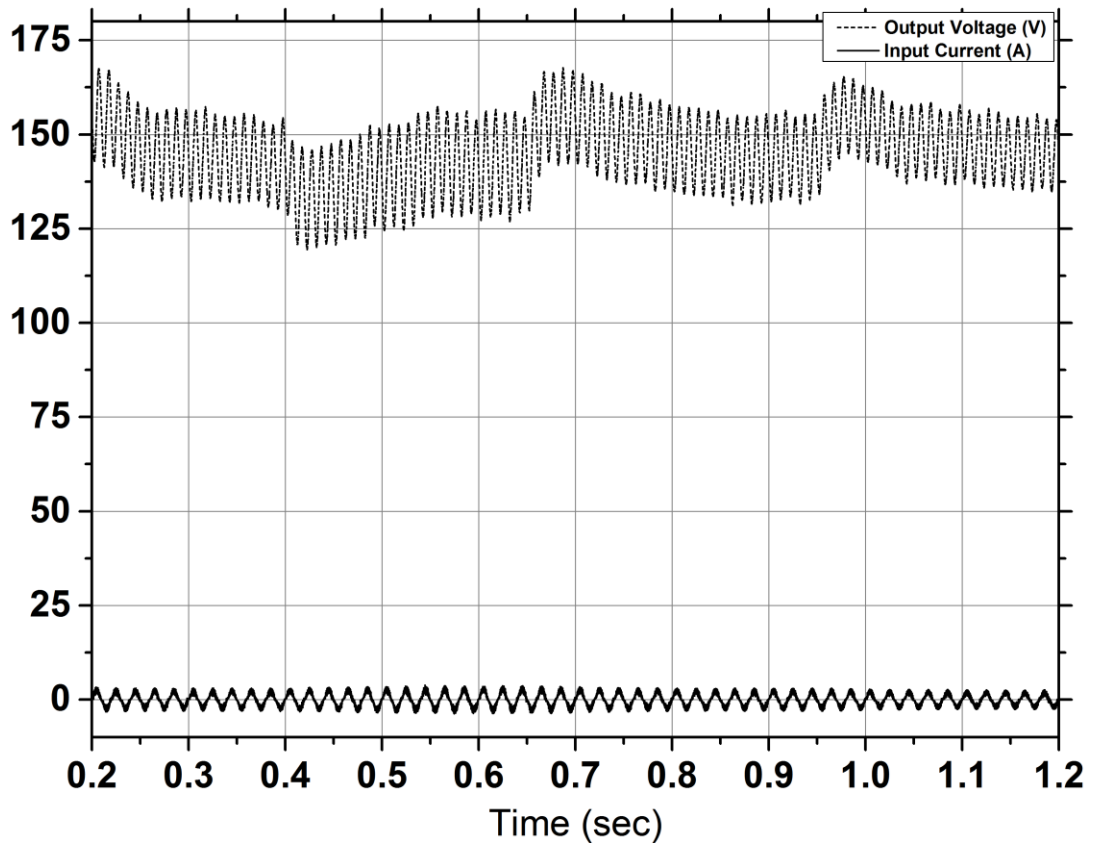


Figure 6.8 Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.7.

### 6.3 Capacitor Assisted Output Switched Half-Bridge AC to DC SEPIC converter

#### 6.3.1 Feedback Analysis

The proposed capacitor assisted output switched half-bridge AC to DC SEPIC converter with feedback control is shown in Figure 6.9. The parameters used for the simulation of the converter is given in Table 6.9. The results of the simulation with reference voltage variation is given in Table 6.10. Typical waveform of the circuit is shown in Figure 6.10. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

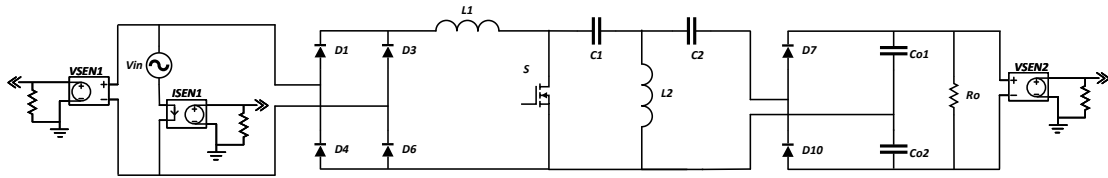


Figure 6.9 Capacitor assisted output switched half-bridge AC to DC SEPIC converter with feedback control.

Table 6.9 Parameters of the circuit of Figure 6.9.

Nominal input ac source voltage, $Vl$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $fs$	5 kHz
Inductors, $L1$ $L2$	5 mH 1 mH
Capacitors, $C1, C2$ $Co1, Co2$	2 $\mu$ F 220 $\mu$ F
Resistor, $Ro$	100 $\Omega$
Gain of Voltage Sensor $VSEN1$ $VSEN2$	0.0033 0.00167
Gain of Current Sensor $ISEN1$	1.67

Table 6.10 Results of the feedback of the capacitor assisted output switched half-bridge AC to DC SEPIC converter.

Ref	V <sub>in</sub> (peak)	I <sub>in</sub> (RMS)	V <sub>o</sub> (Avg)	Input Current THD	Power Factor	Input Power
0.25	300	1.2424	92.885	20.755	0.657	176.4
0.50	300	1.4687	124.27	17.946	0.912	286.26
0.75	300	1.6179	155.199	13.289	0.907	414.759
1.00	300	2.5424	181.126	15.122	0.918	495.402

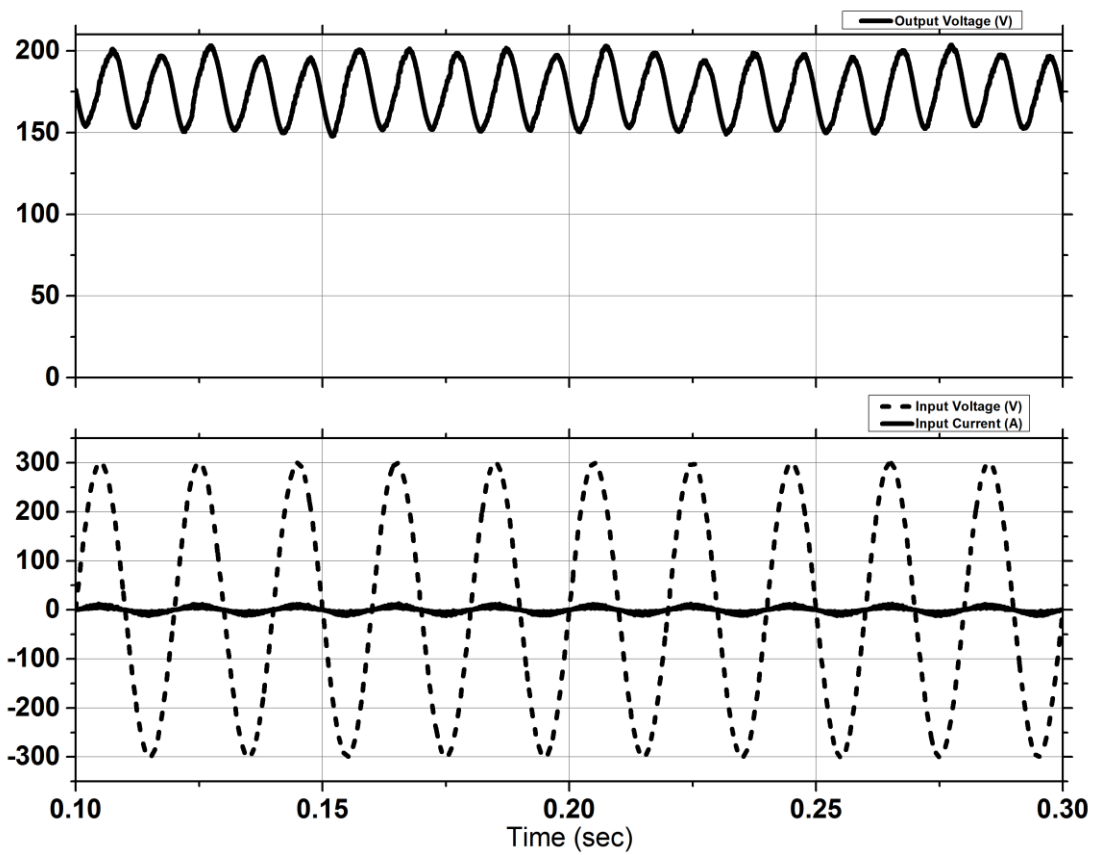


Figure 6.10 Typical input-output waveforms of the circuit of Figure 6.9.

### 6.3.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 295 Vdc output with a resistive load of 100  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 80  $\Omega$  at 250ms, 100  $\Omega$  at 450ms and 120  $\Omega$  at 650ms of the simulation time, which is given in Table 6.11. The circuit parameters are given in Table 6.12. The simulation result showing the variation of output voltage and input current for the circuit of Figure 6.11 is shown in Figure 6.12. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

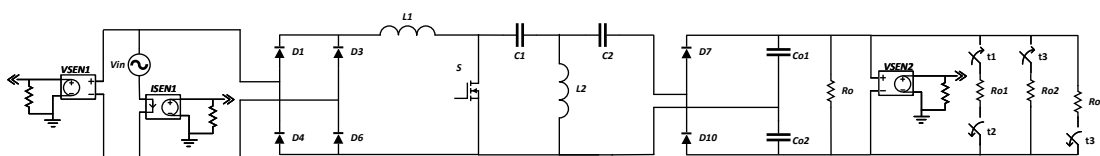


Figure 6.11 Capacitor assisted output switched half-bridge AC to DC SEPIC converter for dynamic analysis.

Table 6.11 Changes in load for Figure 6.11.

Time (ms)	Load ( $\Omega$ )
0-400	100
400-650	80
650-900	100
900-1200	120

Table 6.12 Parameters of the circuit of Figure 6.11.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_{o1}, C_{o2}$	2 $\mu$ F 680 $\mu$ F
Resistor, $R_L$ $R_{o1}, R_{o2}, R_{o3}$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	0.833
Time t1, t2, t3	400 ms, 650 ms, 900 ms



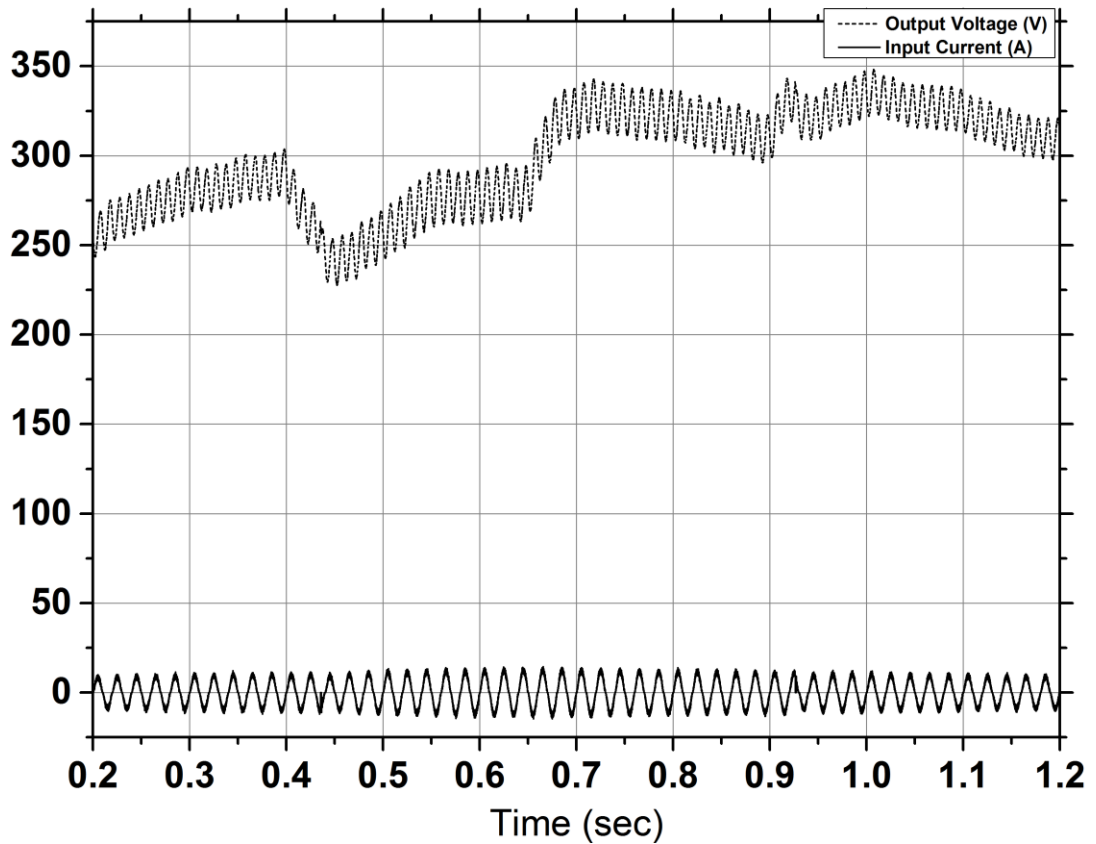


Figure 6.12 Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.11.

## 6.4 Capacitor Assisted Input switched Half-Bridge AC to DC SEPIC converter

### 6.4.1 Feedback Analysis

The proposed capacitor assisted input switched half-bridge AC to DC SEPIC converter with feedback control is shown in Figure 6.13. The parameters used for the simulation of the converter is given in Table 6.13. The results of the simulation with reference voltage variation is given in Table 6.14. Typical waveform of the circuit is shown in Figure 6.14. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

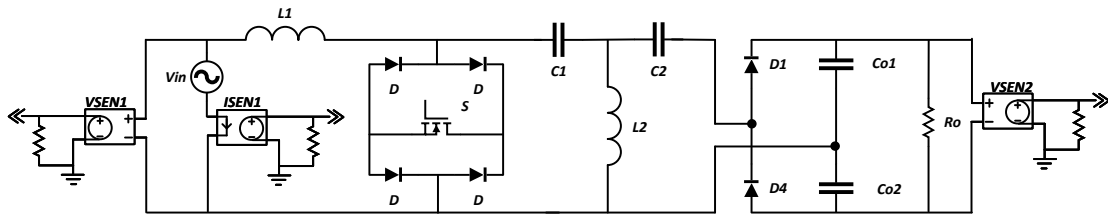


Figure 6.13 Capacitor assisted input switched half-bridge AC to DC SEPIC converter with feedback control.

Table 6.13 Parameters of the circuit of Figure 6.13.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_{o1}, C_{o2}$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.00167
Gain of Current Sensor $I_{SEN1}$	1.67

Table 6.14 Results of the feedback of the capacitor assisted input switched half-bridge AC to DC SEPIC converter.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
0.50	300	1.6749	78.383	20.86	0.866	166.955
0.75	300	1.7852	129.107	14.929	0.923	349.765
1.00	300	2.1931	151.078	17.453	0.938	436.372
1.25	300	2.6698	172.921	13.664	0.945	534.698

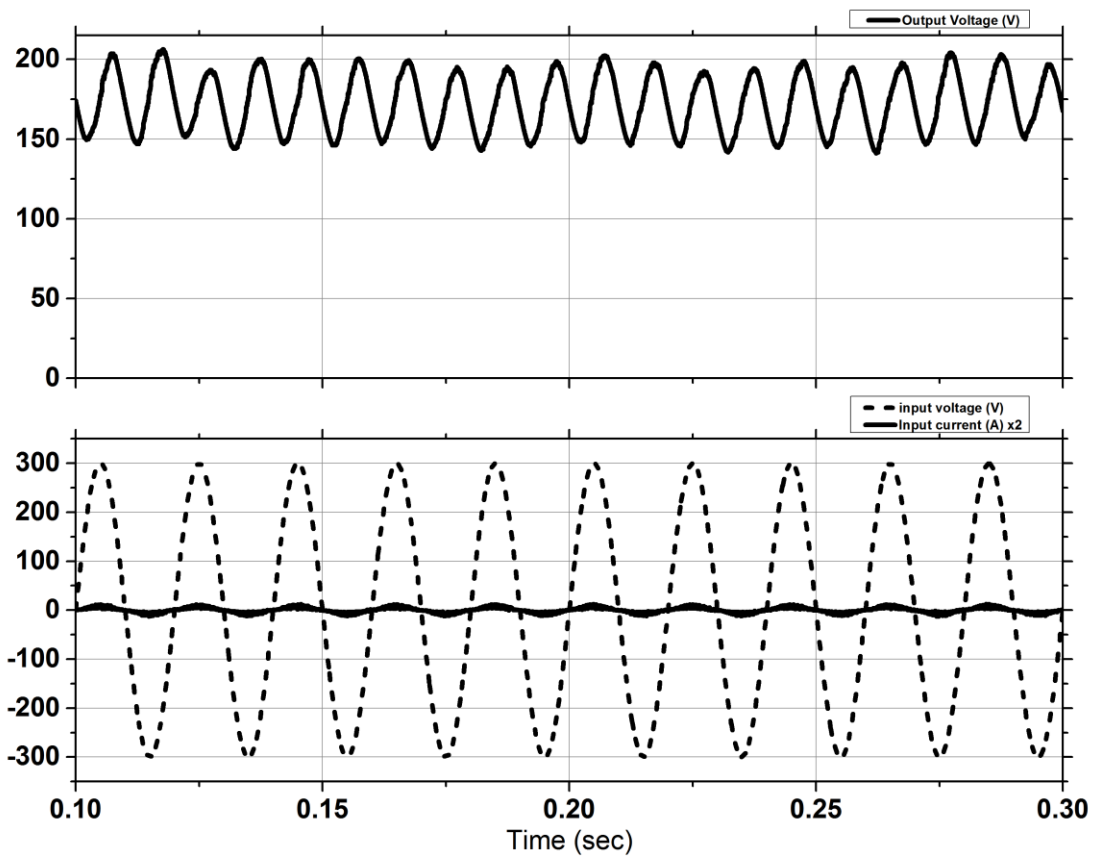


Figure 6.14 Typical input-output waveforms of the circuit of Figure 6.13.

### 6.4.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 120 Vdc output with a resistive load of 100  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 80  $\Omega$  at 250ms, 100  $\Omega$  at 450ms and 120  $\Omega$  at 650ms of the simulation time, which is given in Table 6.15. The circuit parameters are given in Table 6.16. The simulation result showing the variation of output voltage and input current for the circuit of Figure 6.15 is shown in Figure 6.16. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

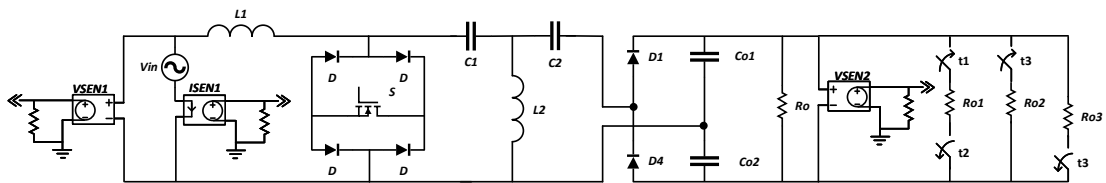


Figure 6.15 Capacitor assisted input switched half-bridge AC to DC SEPIC converter for dynamic analysis.

Table 6.15 Changes in load for Figure 6.15.

Time (ms)	Load ( $\Omega$ )
0-400	100
400-650	80
650-900	100
900-1200	120

Table 6.16 Parameters of the circuit of Figure 6.15.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $Co_1, Co_2$	2 $\mu$ F 680 $\mu$ F
Resistor, $R_L$ $Ro_1, Ro_2, Ro_3$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $VSEN1$ $VSEN2$	0.0033 0.00167
Gain of Current Sensor $ISEN1$	1.67
Time $t_1, t_2, t_3$	400 ms, 650 ms, 900 ms

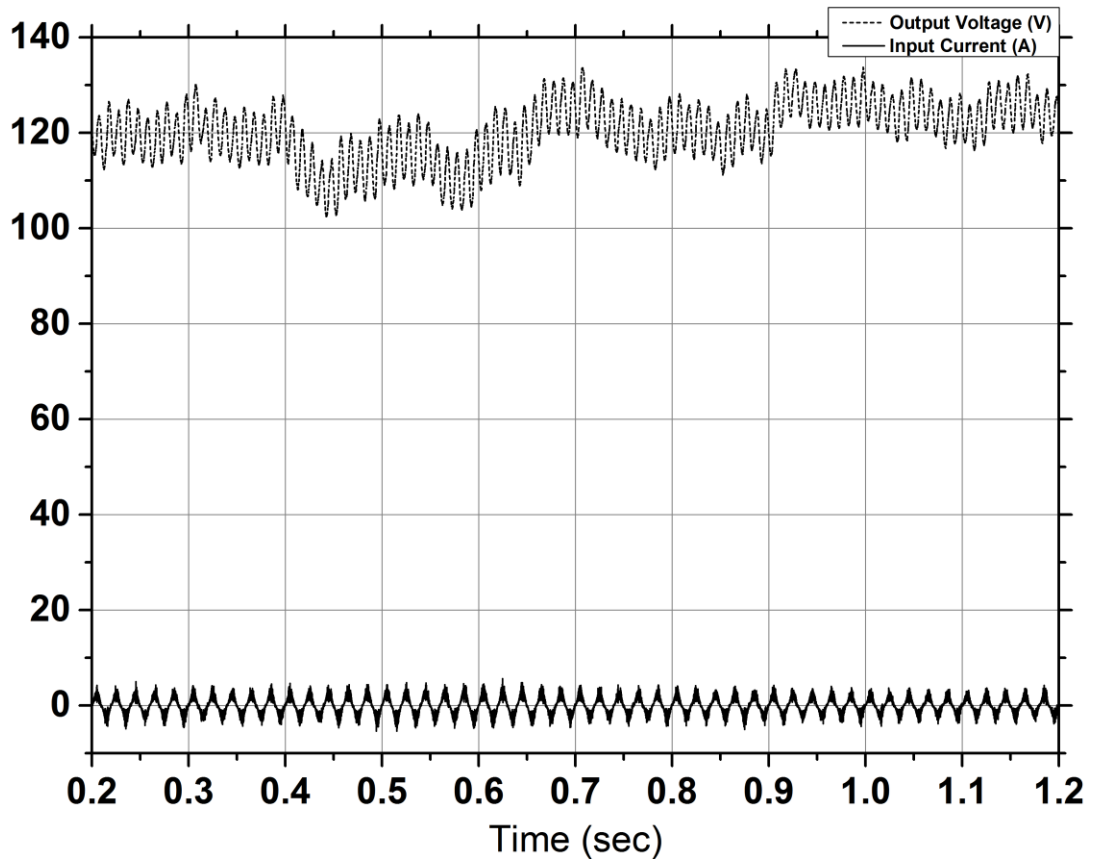


Figure 6.16 Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.15.

## 6.5 Diode-Capacitor Assisted Output Switched Full-bridge AC to DC SEPIC converter

### 6.5.1 Feedback Analysis

The proposed diode-capacitor assisted output switched AC to DC SEPIC converter with feedback control is shown in Figure 6.17. The parameters used for the simulation of the converter is given in Table 6.17. The results of the simulation with reference voltage variation is given in Table 6.18. Typical waveform of the circuit is shown in Figure 6.18. It is evident from the figures that the output voltage changes with the variation in reference voltage while keeping THD within tolerable limit and almost unity power factor.

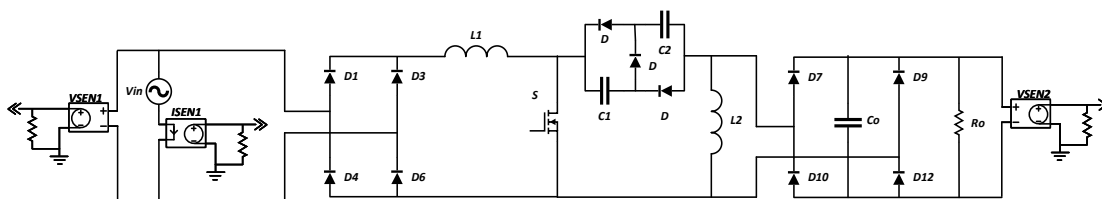


Figure 6.17 Diode-capacitor assisted output switched AC to DC converter with feedback control.

Table 6.17 Parameters of the circuit of Figure 6.17.

Nominal input ac source voltage, $V_l$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_o$	2 $\mu$ F 220 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.88

Table 6.18 Results of the feedback of the diode-capacitor assisted output switched AC to DC SEPIC converter.

Ref	Vin (peak)	Iin (RMS)	Vo (Avg)	Input Current THD	Power Factor	Input Power
0.50	300	0.579	58.739	19.651	0.815	88.303
0.75	300	1.0352	117.304	13.788	0.828	181.726
1.00	300	1.8014	174.304	10.484	0.857	326.941
1.25	300	2.9181	229.625	9.9306	0.915	566.833

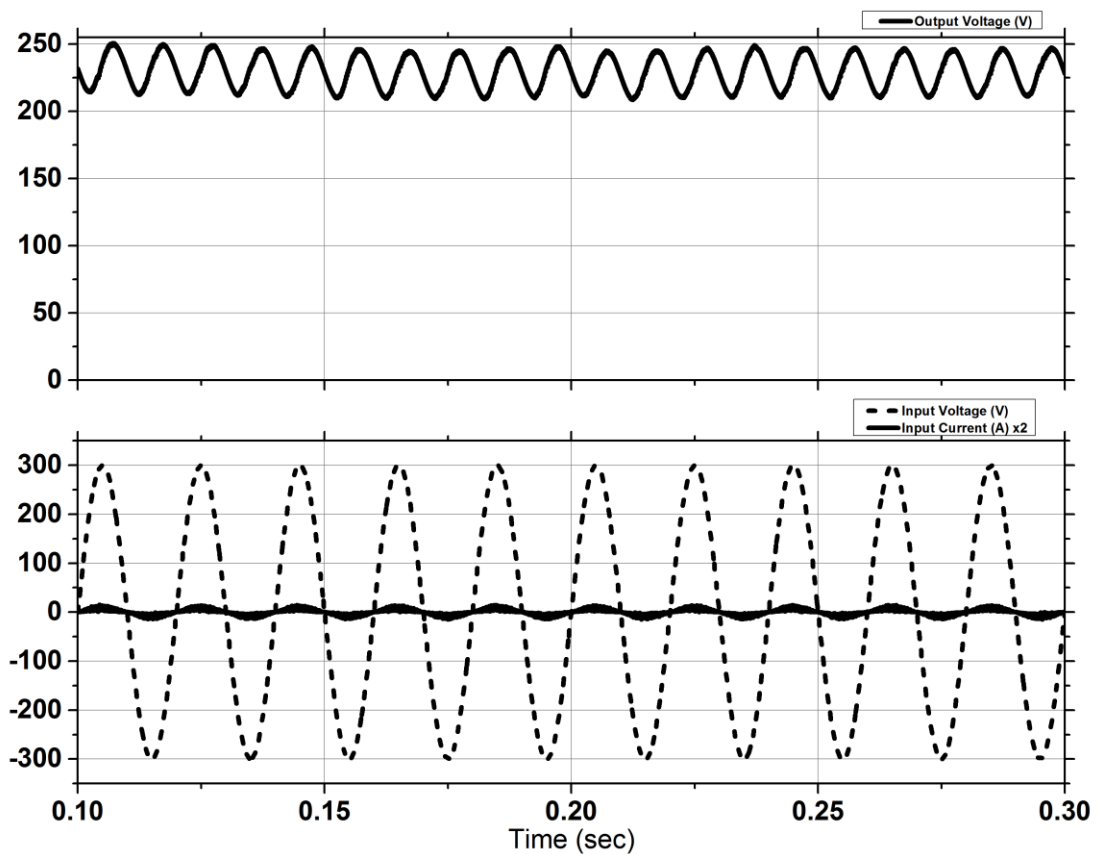


Figure 6.18 Typical input-output waveforms of the circuit of Figure 6.17.



### 6.5.2 Dynamic Response

To test the voltage regulation and the dynamic response of the proposed circuit with feedback control, the controller was set with the reference voltage to provide 155 Vdc output with a resistive load of 100  $\Omega$ . Simulation of the circuit is carried out with sudden load changes to 80  $\Omega$  at 250ms, 100  $\Omega$  at 450ms and 120  $\Omega$  at 650ms of the simulation time, which is given in Table 6.19. The circuit parameters are given in Table 6.20. The simulation result showing the variation of output voltage and input current for the circuit of Figure 6.19 is shown in Figure 6.20. It is evident from the waveforms that, due to feedback control the output voltage of the converter remains almost constant with the change of load while the input current changes to meet the load demand.

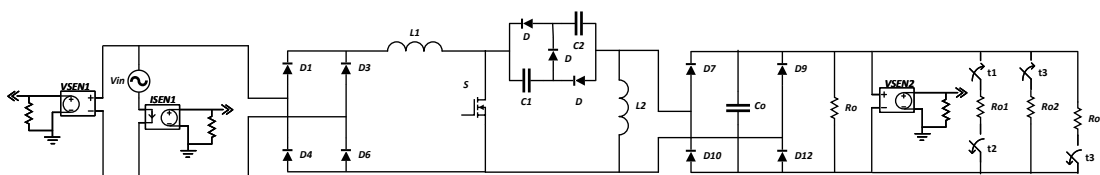


Figure 6.19 Diode-capacitor assisted output switched AC to DC converter for dynamic analysis.

Table 6.19 Changes in load for Figure 6.19.

Time (ms)	Load ( $\Omega$ )
0-300	100
300-550	80
550-800	100
800-1100	120

Table 6.20 Parameters of the circuit of Figure 6.19.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1$ $L_2$	5 mH 1 mH
Capacitors, $C_1, C_2$ $C_o$	2 $\mu$ F 470 $\mu$ F
Resistor, $R_L$ $R_{o1}, R_{o2}, R_{o3}$	200 $\Omega$ 400 $\Omega$ , 300 $\Omega$ , 200 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 0.0033
Gain of Current Sensor $I_{SEN1}$	0.67
Time $t_1, t_2, t_3$	300 ms, 550 ms, 800 ms

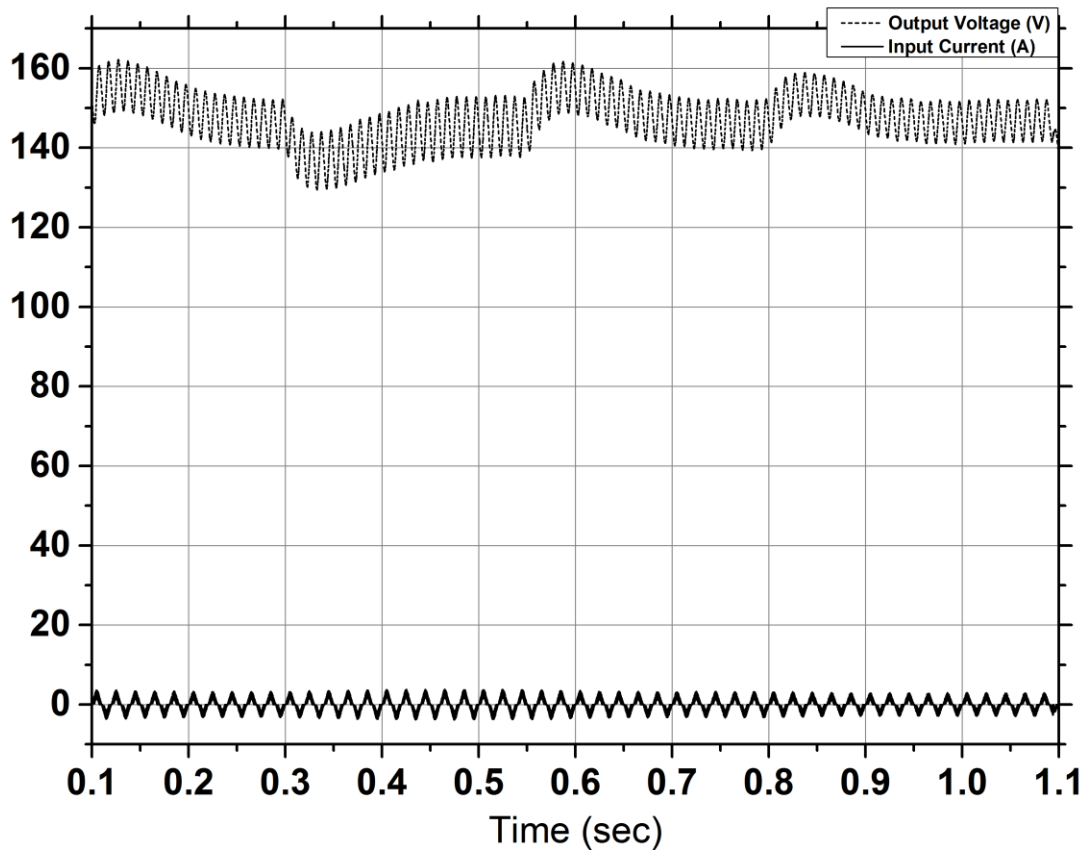


Figure 6.20 Typical waveforms of output voltage and input current for load change of the circuit of Figure 6.19.

## 6.6 Discussions

The input current THD of the proposed SEPIC converters are within prescribed limits with the feedback control. The input power factor is also reasonably high for low voltage gains. Most of the converters maintained constant output voltage under variable load condition.

## Chapter 7

### Design of Feedback Control

In general, the input power factor of AC to DC converters scheme are very low in open loop operation. Proper feedback control can improve the input power factor of the converters. The common PFC control consists of two loops. The inner current control loop and the outer voltage control loop. For simplicity average current mode control is applied to the inner current control loop. In this chapter, the feedback controller is designed in detail for the diode-capacitor assisted output switched AC to DC boost converter as shown in Figure 7.1. The same procedure can be applied to design feedback controller for any AC to DC converter.

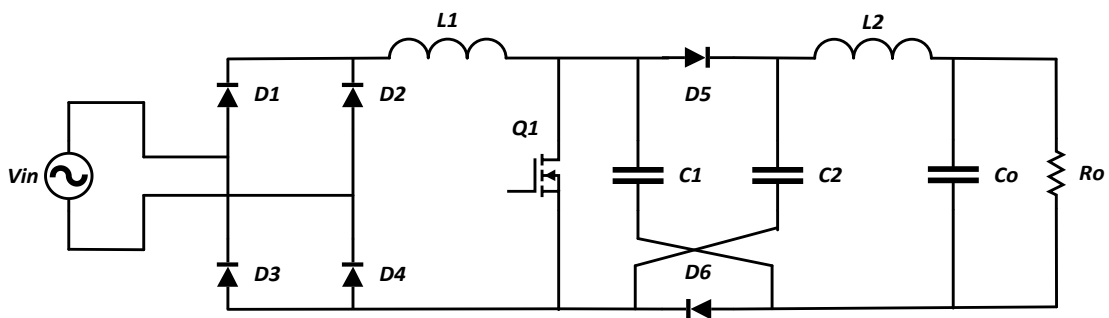


Figure 7.1 Diode-capacitor assisted output switched AC to DC Boost Converter.

#### 7.1 The Operating Principle of PFC

In proposed diode-capacitor assisted output switched AC to DC converter, the boost diode is replaced by hybrid diode-capacitor network. By pulse-width-modulating the MOSFET at constant switching frequency, the current  $i_L$  through the inductor L1 is shaped to have the full-wave-rectified waveform  $\bar{i}_L(t) = \hat{I}_L |\sin \omega t|$ , similar to  $|v_s(t)|$  as shown in Figure 7.2. The inductor current contains high switching frequency ripple, which is removed by a small filter.

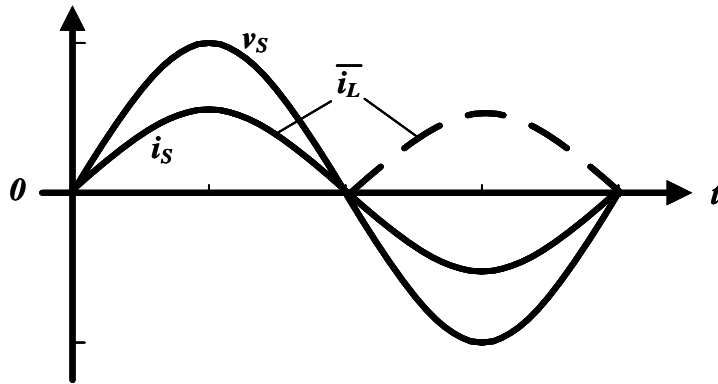


Figure 7.2 PFC waveforms.

The dc transformer model of the circuit of Figure 7.1 is shown in Figure 7.3, where  $|V_s|$  is the voltage after the rectifier (without any distortion due to load).

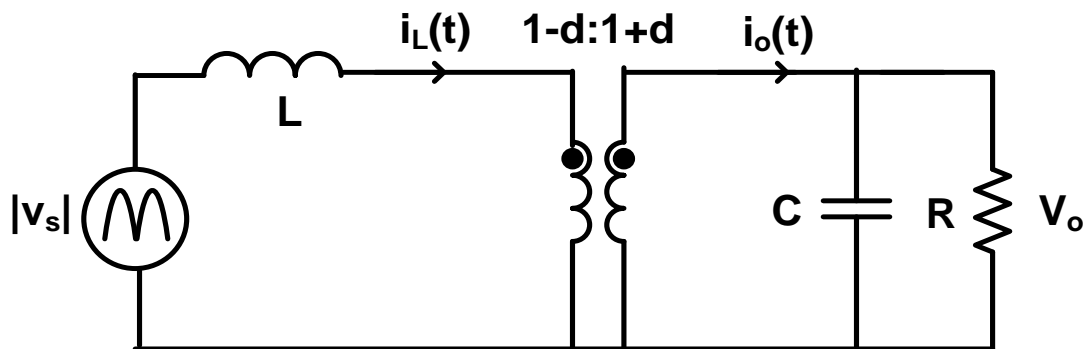


Figure 7.3 The DC transformer model of the diode-capacitor assisted output switched AC to DC Boost Converter.

The voltage gain of the converter is given below [44],

$$\frac{V_o}{|v_s|} = \frac{1+d(t)}{1-d(t)}$$

Where  $V_o$  and  $d(t)$  are the average output voltage and variable duty cycle.

$$\text{Or, } \frac{V_o - |v_s|}{V_o + |v_s|} = \frac{1+d(t) - 1+d(t)}{1+d(t) + 1-d(t)}$$

$$\text{Or, } d(t) = \frac{V_0 - |v_s|}{V_0 + |v_s|}$$

$$d(t) = \frac{V_0 - \hat{V}_s |\sin \omega t|}{V_0 + \hat{V}_s |\sin \omega t|} \quad (7.1)$$

Where,  $\hat{V}_s$  is the peak input voltage.

According to equation (7.1), a variable duty cycle is needed for keeping the input current in-phase with the supply voltage as shown in Figure 7.4. The MATLAB code for generating the signal as required in Figure 7.4 is presented in Figure 7.5.

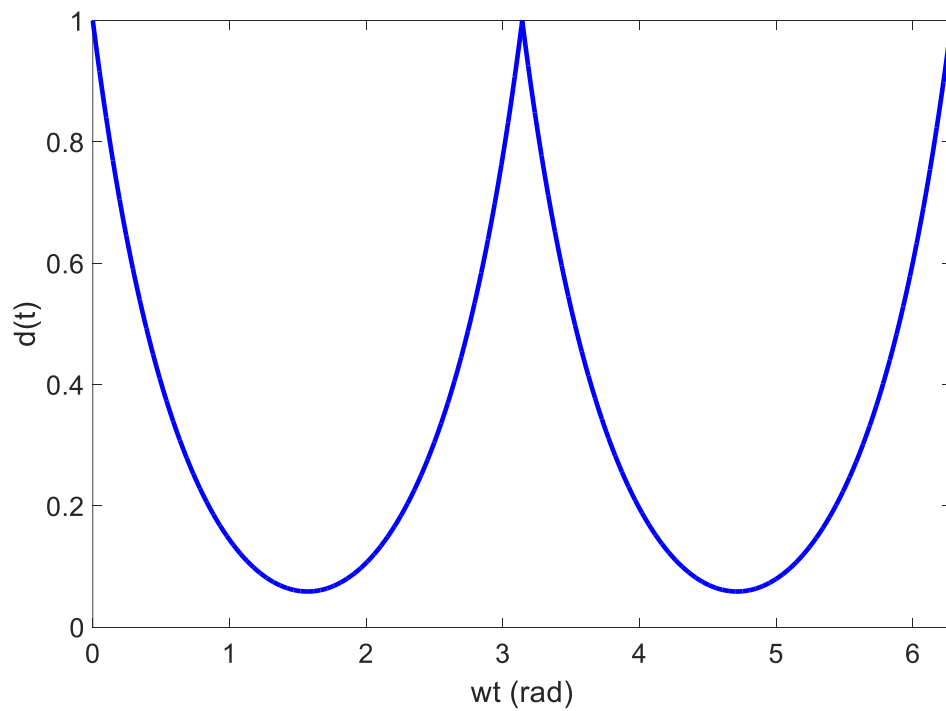


Figure 7.4 Required variable duty cycle for the PFC controller.

```

%MATLAB Code
Vo=350;
vrms=220;
vpk=sqrt(2)*vrms;
wt=0:0.001:2*pi;
d_t=(Vo-vpk*abs(sin(wt)))/(Vo+vpk*abs(sin(wt)));
plot(wt,d_t)

```

Figure 7.5 MATLAB code to generate the variable duty cycle of Figure 7.4.

The current ratio of the ideal transformer can be written as:

$$\frac{i_L(t)}{i_o(t)} = \frac{1+d(t)}{1-d(t)}$$

Where,  $i_L(t)$  and  $i_o(t)$  are instantaneous inductor and output current.

$$i_o(t) = \frac{1-d(t)}{1+d(t)} i_L(t)$$

$$i_o(t) = \frac{|v_s|}{V_o} i_L(t)$$

$$i_o(t) = \frac{\hat{V}_s |\sin \omega t|}{V_o} \times \hat{I}_L |\sin \omega t|$$

$$i_o(t) = \frac{\hat{V}_s \times \hat{I}_L}{V_o} \times \sin^2 \omega t$$

$$i_o(t) = \frac{\hat{V}_s \times \hat{I}_L}{V_o} \times \left( \frac{1}{2} - \frac{1}{2} \cos 2\omega t \right)$$

$$i_o(t) = \frac{1}{2} \frac{\hat{V}_s \times \hat{I}_L}{V_o} - \frac{1}{2} \frac{\hat{V}_s \times \hat{I}_L}{V_o} \cos 2\omega t$$

The output current contains both DC component and a second harmonic ripple. The second harmonic output current can be defined as:

$$i_{o2}(t) = \frac{1}{2} \frac{\hat{V}_s \times \hat{I}_L}{V_o} \cos 2\omega t$$

Where the peak value of the second harmonic is defined as:

$$\hat{I}_{o2} = \frac{1}{2} \frac{\hat{V}_s \times \hat{I}_L}{V_o}$$

The second harmonic current is assumed to flow through the output capacitor entirely. So the peak ripple voltage due to second harmonic current can be calculated as:

$$\hat{V}_{o2} \approx \hat{I}_{o2} \times X_c = \frac{1}{2} \frac{\hat{V}_s \times \hat{I}_L}{V_o} \times \frac{1}{2\omega C}$$

$$\hat{V}_{o2} = \frac{\hat{V}_s \times \hat{I}_L}{4\omega C V_o}$$

Where,  $\hat{V}_{o2}$ ,  $X_c$ ,  $2\omega$  and C are peak ripple voltage, reactance output capacitor, second harmonic frequency and output capacitor.

The equation has to be used to calculate the value of smoothing capacitor at the output.

$$C = \frac{\hat{V}_s \times \hat{I}_L}{4\omega \times \hat{V}_{o2} \times V_o} \quad (7.2)$$

## 7.2 Control of PFCs

Figure 7.6 shows the PFC power circuit along with its control circuit in block diagram form. In controlling a PFC, the main objective is to draw a sinusoidal current, in-phase



with the utility voltage. The reference inductor current  $i_L^*$  is of the full-wave rectified form, similar to that in Figure 7.2. The requirements on the form and the amplitude of the inductor current lead to two control loops, as shown in Figure 7.6, to pulse-width modulate the switch of the proposed boost converter:

- The average inner current control loop ensures the form of  $i_L^*$  based on the template  $\sin|\omega t|$  provided by measuring the rectifier output voltage  $|v_s(t)|$ .
- The outer voltage control loop determines the amplitude  $\hat{I}_L$  of  $i_L^*$  based on the output voltage feedback. If the inductor current is insufficient for a given load supplied by the PFC, the output voltage will drop below its preselected reference value  $V_o^*$ . By measuring the output voltage and using it as the feedback signal, the voltage control loop adjusts the inductor current amplitude to bring the output voltage to its reference value. In addition to determining the inductor current amplitude, this voltage feedback control acts to regulate the output voltage of the PFC to the pre-selected dc voltage.

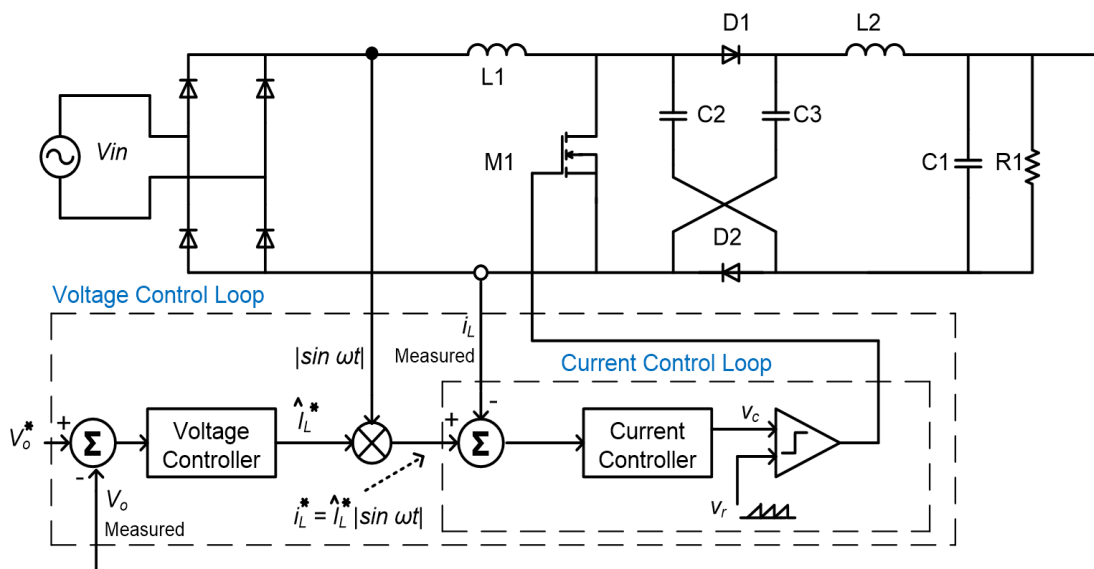


Figure 7.6 PFC control loops.

In Figure 7.6, the inner current-control loop is required to have a very high bandwidth compared to the outer voltage-control loop. Hence, each loop can be designed separately.

### 7.3 AC Equivalent Circuit Modelling of Proposed Boost Converter

The first step for designing the controller is to derive the small signal model of the converter topology. The next step is to find the power stage transfer function for both the inner current control loop and outer voltage control loop.

#### 7.3.1 Small-Signal Model of Proposed Boost Converter

To design feedback controller, the power stage of the converter must be linearized around the steady-state operating point, assuming a small-signal disturbance. Figure 7.7 shows the average model of the switching power-pole, where the subscript “vp” refers to the voltage-port and “cp” to the current-port. Each average quantity in Figure 7.5 can be expressed as the sum of its steady state dc value (represented by an uppercase letter) and a small-signal perturbation (represented by a “~” on top):

$$d(t) = D + \tilde{d}(t)$$

$$\bar{v}_{vp} = V_{vp} + \tilde{v}_{vp}$$

$$\bar{v}_{cp} = V_{cp} + \tilde{v}_{cp}$$

$$\bar{i}_{vp} = I_{vp} + \tilde{i}_{vp}$$

$$\bar{i}_{cp} = I_{cp} + \tilde{i}_{cp}$$

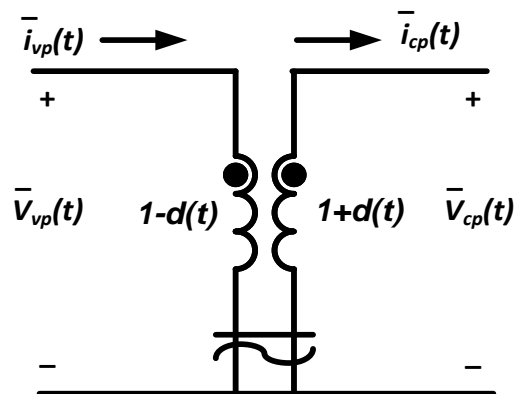


Figure 7.7 Linearizing the switching power-pole.

Utilizing the voltage and current relationships between the two ports in Figure 7.7:

$$V_{vp} + \tilde{v}_{vp} = \left( \frac{1-D-\tilde{d}}{1+D+\tilde{d}} \right) (V_{cp} + \tilde{v}_{cp})$$

$$(V_{vp} + \tilde{v}_{vp})(1+D+\tilde{d}) = (1-D-\tilde{d})(V_{cp} + \tilde{v}_{cp})$$

$$V_{vp}(1+D) + V_{vp}\tilde{d} + \tilde{v}_{vp}(1+D) + \tilde{v}_{vp}\tilde{d} = V_{cp}(1-D) - V_{cp}\tilde{d} + \tilde{v}_{cp}(1-D) - \tilde{v}_{cp}\tilde{d}$$

Ignoring the DC and the non-linear terms from the both side of the above equation:

$$V_{vp}\tilde{d} + \tilde{v}_{vp}(1+D) = -V_{cp}\tilde{d} + \tilde{v}_{cp}(1-D)$$

$$\tilde{v}_{vp}(1+D) + V_{vp}\tilde{d} = -V_{cp}\tilde{d} + \tilde{v}_{cp}(1-D)$$

$$\tilde{v}_{vp} + \frac{\tilde{d}V_{vp}}{(1+D)} = \frac{\tilde{v}_{cp}(1-D)}{(1+D)} - \frac{V_{cp}\tilde{d}}{(1+D)}$$

$$\tilde{v}_{vp} = \frac{(1-D)}{(1+D)} \tilde{v}_{cp} - \frac{\tilde{d}(V_{cp} + V_{vp})}{(1+D)}$$

The voltage port is the input side and the current port is the output side. So,

$$V_{vp} = \hat{V}_{in}$$

$$V_{cp} = V_o$$

$$\tilde{v}_{vp} = \tilde{v}_{in}$$

$$\tilde{v}_{cp} = \tilde{v}_o$$

Where,  $\hat{V}_{in}$ ,  $V_o$ ,  $\tilde{v}_{in}$  and  $\tilde{v}_o$  are peak input voltage, average output voltage, input voltage perturbation and output voltage perturbation. Therefore,

$$\tilde{v}_{in} = \frac{(1-D)}{(1+D)} \tilde{v}_o - \frac{\tilde{d}(V_o + \hat{V}_{in})}{(1+D)}$$

For the current port,

$$I_{cp} + \tilde{i}_{cp} = \left( \frac{1 - D - \tilde{d}}{1 + D + \tilde{d}} \right) (I_{vp} + \tilde{i}_{vp})$$

$$(I_{cp} + \tilde{i}_{cp})(1 + D + \tilde{d}) = (1 - D - \tilde{d})(I_{vp} + \tilde{i}_{vp})$$

$$I_{cp}(1 + D) + I_{cp}\tilde{d} + \tilde{i}_{cp}(1 + D) + \tilde{i}_{cp}\tilde{d} = I_{vp}(1 - D) - I_{vp}\tilde{d} + \tilde{i}_{vp}(1 - D) - \tilde{i}_{vp}\tilde{d}$$

Ignoring the DC and the non-linear terms from the both side of the above equation:

$$I_{cp}\tilde{d} + \tilde{i}_{cp}(1 + D) = -I_{vp}\tilde{d} + \tilde{i}_{vp}(1 - D)$$

$$\tilde{i}_{cp}(1 + D) + I_{cp}\tilde{d} = -I_{vp}\tilde{d} + \tilde{i}_{vp}(1 - D)$$

$$\tilde{i}_{cp} + \frac{\tilde{d}I_{cp}}{(1 + D)} = \frac{\tilde{i}_{vp}(1 - D)}{(1 + D)} - \frac{I_{vp}\tilde{d}}{(1 + D)}$$

$$\tilde{i}_{cp} = \frac{(1 - D)}{(1 + D)}\tilde{i}_{vp} - \frac{\tilde{d}(I_{vp} + I_{cp})}{(1 + D)}$$

The voltage port is the input side and the current port is the output side. So,

$$I_{vp} = \hat{I}_{in} = \hat{I}_L$$

$$I_{cp} = I_o$$

$$\tilde{i}_{vp} = \tilde{i}_{in} = \tilde{i}_L$$

$$\tilde{i}_{cp} = \tilde{i}_o$$

$$\tilde{i}_o = \frac{(1 - D)}{(1 + D)}\tilde{i}_L - \frac{\tilde{d}(I_o + \hat{I}_L)}{(1 + D)}$$

Thus the derived small signal AC model of hybrid boost converter is shown in Figure 7.8.

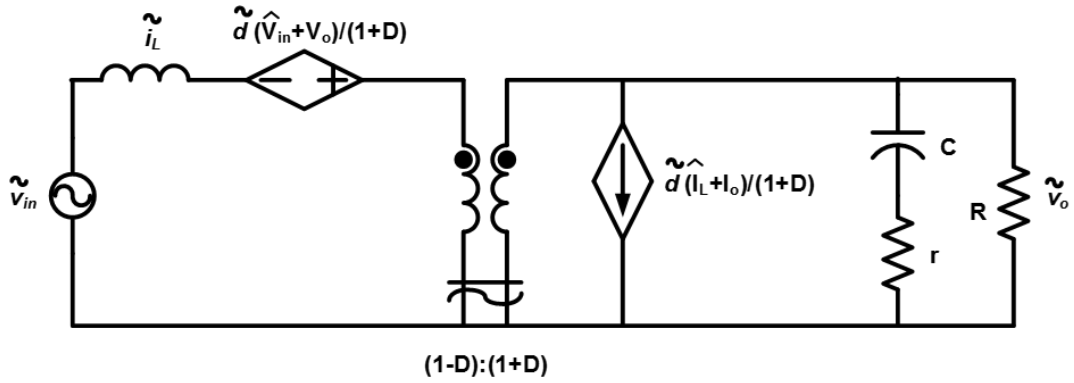


Figure 7.8 Derived small signal model of the diode-capacitor assisted output switched AC to DC Boost Converter.

The equivalent circuit contains three independent inputs: control input variation  $\tilde{d}$ , the power input variation  $\tilde{v}_{in}$  and the load current variation. The output voltage variation/perturbation (ignoring load variation) can be expressed as a linear combination of the two independent inputs, as follows,

$$\tilde{v}_o = G_{vg}(s)\tilde{v}_{in} + G_{vd}(s)\tilde{d}$$

Where,  $G_{vg}(s) = \frac{\tilde{v}_o}{\tilde{v}_{in}}$  = Converter line to output transfer function,

$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}}$  = Converter control to output transfer function.

### 7.3.2 The Control-to-Output Transfer Function

For voltage mode control the transfer function of the power stage has to be,  $\tilde{v}_o/\tilde{d}$ . So the input voltage perturbation has to be zero,  $\tilde{v}_{in} = 0$ . Thus control-to-output transfer function be,

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)}$$

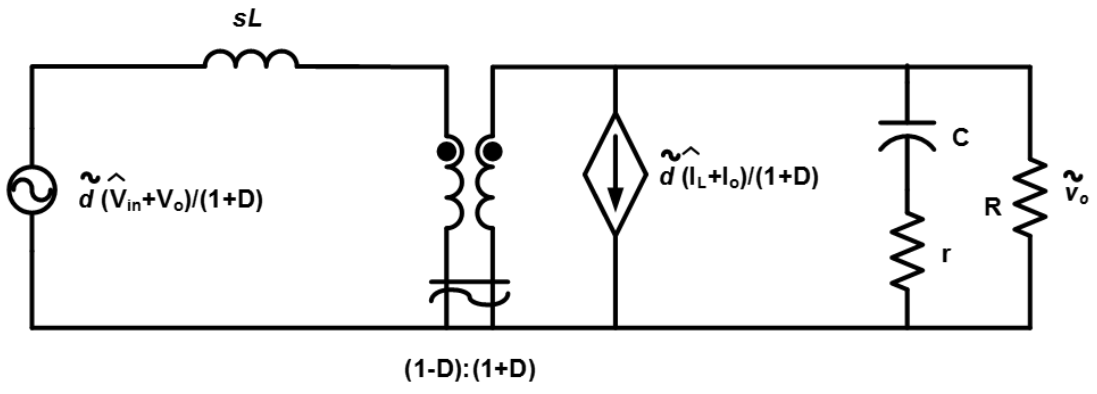


Figure 7.9 Reduced small signal model for deriving control to output transfer function.

Converting the voltage source in the primary side of the ideal transformer (capable of transforming both AC and DC) into a current source:

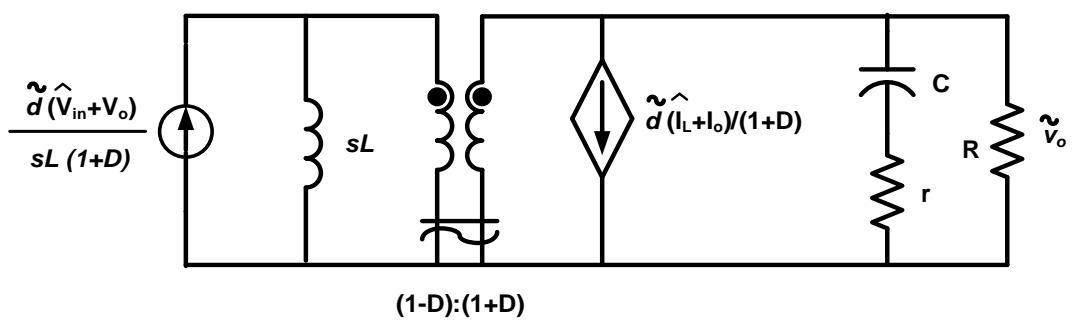


Figure 7.10 Circuit after source transformation.

Transferring primary current source and the impedance to the secondary side current multiplied by turns-ratio, impedance divided by square of turns-ratio:

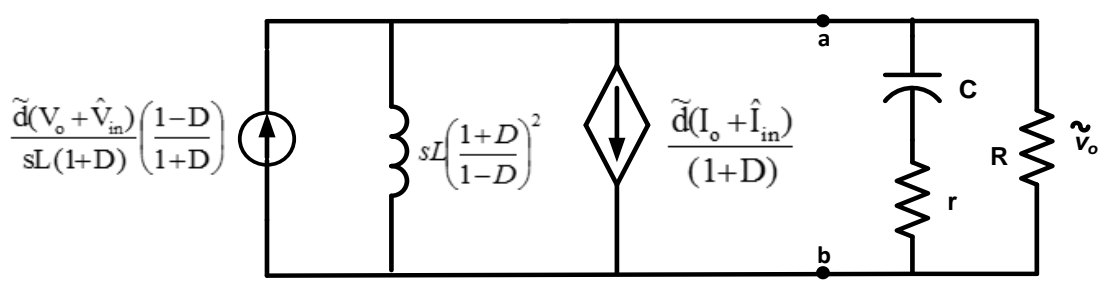


Figure 7.11 Circuit after impedance transformation.

Finding the equivalent circuit at terminal (a-b) looking towards the source side:

Thevenin's equivalent impedance,

$$Z_{ab} = sL \left( \frac{1+D}{1-D} \right)^2$$

$$Z_{ab} = sL_e$$

Where,  $L_e = L \left( \frac{1+D}{1-D} \right)^2$

Thevenin's equivalent voltage,

$$v_{ab} = v_1 - v_2$$

For the first current source,

$$v_1 = \frac{\tilde{d}(V_0 + \hat{V}_{in})}{sL(1+D)} \left( \frac{1-D}{1+D} \right) \times sL \left( \frac{1+D}{1-D} \right)^2$$

For the second current source,

$$v_2 = \frac{\tilde{d}(I_o + \hat{I}_L)}{(1+D)} \times sL \left( \frac{1+D}{1-D} \right)^2$$

$$v_{ab} = \left[ \frac{\tilde{d}(V_0 + \hat{V}_{in})}{sL(1+D)} \left( \frac{1-D}{1+D} \right) \times sL \left( \frac{1+D}{1-D} \right)^2 \right] - \left[ \frac{\tilde{d}(I_o + \hat{I}_L)}{(1+D)} \times sL \left( \frac{1+D}{1-D} \right)^2 \right]$$

$$v_{ab} = \left[ \frac{\tilde{d}(V_0 + \hat{V}_{in})}{(1-D)} \right] - \left[ \tilde{d}(I_o + \hat{I}_L) \times sL \left( \frac{1+D}{1-D} \right)^2 \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1+D)}{(1-D)^2} \left[ \left( \frac{1-D}{1+D} \right) - sL \left( \frac{I_o + \hat{I}_L}{V_0 + \hat{V}_{in}} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1+D)}{(1-D)^2} \left[ \frac{\hat{V}_{in}}{V_0} - sL \left( \frac{I_o + \hat{I}_L}{V_0 + \hat{V}_{in}} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1+D)}{(1-D)^2} \left[ \frac{\hat{V}_{in}}{V_0} - sL \left( \frac{\frac{V_o}{R} + \frac{V_o^2}{R\hat{V}_{in}}}{V_0 + \hat{V}_{in}} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \left[ \frac{\hat{V}_{in}}{V_0} - sL \left( \frac{V_0 \hat{V}_{in} + V_0^2}{R \hat{V}_{in}} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \left[ \frac{\hat{V}_{in}}{V_0} - sL \left( \frac{V_0(\hat{V}_{in} + V_0)}{R \hat{V}_{in}} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \left[ \frac{V_{in}}{V_0} - sL \left( \frac{V_0(\hat{V}_{in} + V_0)}{R \hat{V}_{in}} \times \frac{1}{(\hat{V}_{in} + V_0)} \right) \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \left[ \frac{\hat{V}_{in}}{V_0} - sL \frac{V_0}{R \hat{V}_{in}} \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \times \frac{\hat{V}_{in}}{V_0} \left[ 1 - \frac{sL}{R} \left( \frac{V_0}{\hat{V}_{in}} \right)^2 \right]$$

$$v_{ab} = \frac{\tilde{d}(V_0 + \hat{V}_{in})(1 + D)}{(1 - D)^2} \times \frac{\hat{V}_{in}}{V_0} \left[ 1 - \frac{sL}{R} \left( \frac{1 + D}{1 - D} \right)^2 \right]$$

$$v_{ab} = \frac{\tilde{d}(1 + D)}{(1 - D)^2} [(V_0 + \hat{V}_{in})] \times \frac{\hat{V}_{in}}{V_0} \left[ 1 - \frac{sL_e}{R} \right]$$

$$v_{ab} = \frac{\tilde{d}(1 + D)}{(1 - D)^2} \left[ V_0 + \left( \frac{1 - D}{1 + D} \right) V_0 \right] \times \frac{\hat{V}_{in}}{V_0} \left[ 1 - \frac{sL_e}{R} \right]$$

$$v_{ab} = \frac{\tilde{d}(1 + D)}{(1 - D)^2} \left[ 1 + \left( \frac{1 - D}{1 + D} \right) \right] \times \hat{V}_{in} \left[ 1 - \frac{sL_e}{R} \right]$$

$$v_{ab} = \frac{\tilde{d}(1 + D)}{(1 - D)^2} \left( \frac{1 + D + 1 - D}{1 + D} \right) \times \hat{V}_{in} \left[ 1 - \frac{sL_e}{R} \right]$$

$$v_{ab} = \frac{\tilde{d}(1 + D)}{(1 - D)^2} \times \left( \frac{2}{1 + D} \right) \times \hat{V}_{in} \left[ 1 - \frac{sL_e}{R} \right]$$

$$v_{ab} = \frac{2\tilde{d}\hat{V}_{in}}{(1 - D)^2} \times \left[ 1 - \frac{sL_e}{R} \right]$$



So the equivalent circuit becomes:

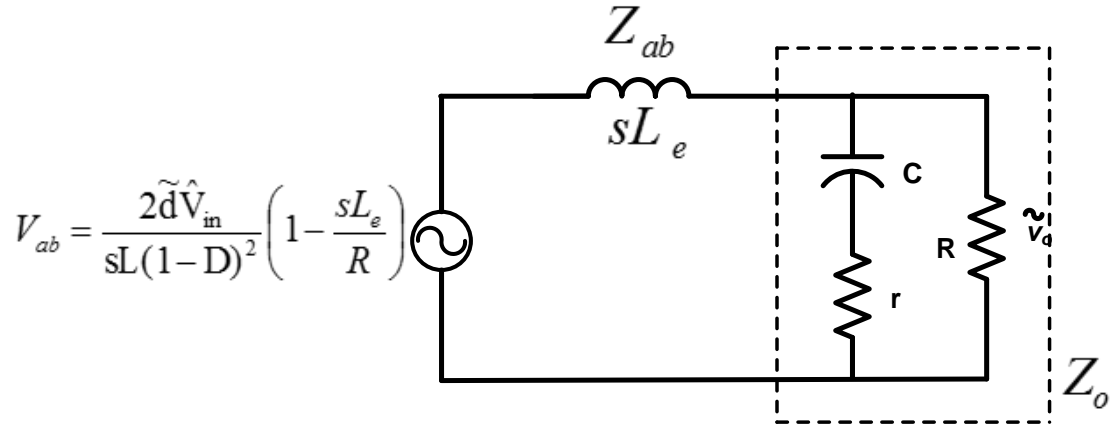


Figure 7.12 The equivalent Thevenin's model of the circuit.

$$\tilde{v}_o = v_{ab} \times \frac{Z_o}{Z_{ab} + Z_o}$$

$$\tilde{v}_o = \frac{2\tilde{d}\hat{V}_{in}}{(1-D)^2} \times \left[1 - \frac{sL_e}{R}\right] \times \left[\frac{R \parallel (1/sC)}{sL_e + (R \parallel (1/sC))}\right]$$

Assuming  $r_c \neq 0$

$$\tilde{v}_o = \frac{2\tilde{d}\hat{V}_{in}}{(1-D)^2} \times \left[1 - \frac{sL_e}{R}\right] \times \left[\frac{1 + sr_c C}{s^2 L_e C + s\left(\frac{L_e}{R} + r_c C\right) + 1}\right]$$

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{2\hat{V}_{in}}{(1-D)^2} \times \left[1 - \frac{sL_e}{R}\right] \times \left[\frac{1 + sr_c C}{s^2 L_e C + s\left(\frac{L_e}{R} + r_c C\right) + 1}\right]$$

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}} = \frac{2\hat{V}_{in}}{(1-D)^2} \times \left[1 - \frac{sL_e}{R}\right] \times \left[\frac{1 + sr_c C}{s^2 L_e C + s\left(\frac{L_e}{R} + r_c C\right) + 1}\right]$$

If  $r_c = 0$  then

$$G_{vd}(s) = \frac{\tilde{v}_o}{\tilde{d}} = \frac{2\hat{V}_{in}}{(1-D)^2} \times \left[1 - \frac{sL_e}{R}\right] \times \left[\frac{1}{s^2 L_e C + s\frac{L_e}{R} + 1}\right]$$

### 7.3.3 Line-to-Output Transfer Function (Power Stage Transfer Function for Voltage Control Loop)

For deriving the line-to-voltage transfer function of the power stage the duty cycle perturbation has to be zero,  $\tilde{d} = 0$ . Thus the transfer function will be  $\tilde{v}_o/\tilde{v}_{in}$ . Since for the voltage control loop of the hybrid boost converter, the transfer function has to be output voltage perturbation with respect to the input/inductor current perturbation instead of input voltage perturbation, more appropriate transfer function will be,  $\tilde{v}_o/\tilde{i}_L$ . For  $\tilde{d} = 0$  the small signal model reduces to the following diagram (assume  $r_C = 0$ ):

$$G_{vl}(s) = \frac{\tilde{v}_o}{\tilde{v}_{in}}$$

Modified as required for voltage control loop:

$$G_{vl}(s) = \frac{\tilde{v}_o}{\tilde{i}_L}$$

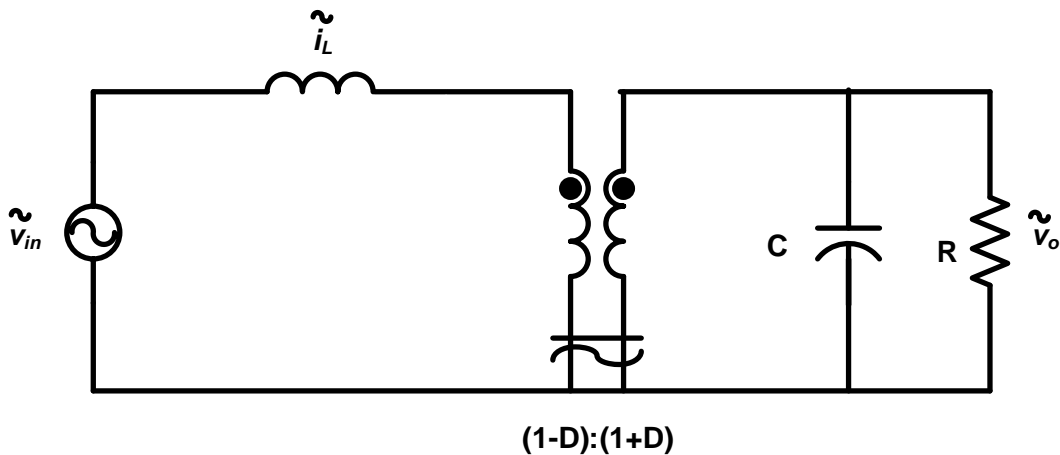


Figure 7.13 The reduced model to derive line to output transfer function.

Referring to the primary side of the ideal transformer (Its preferable to refer to the secondary side for finding,  $\tilde{v}_o/\tilde{v}_{in}$ ):

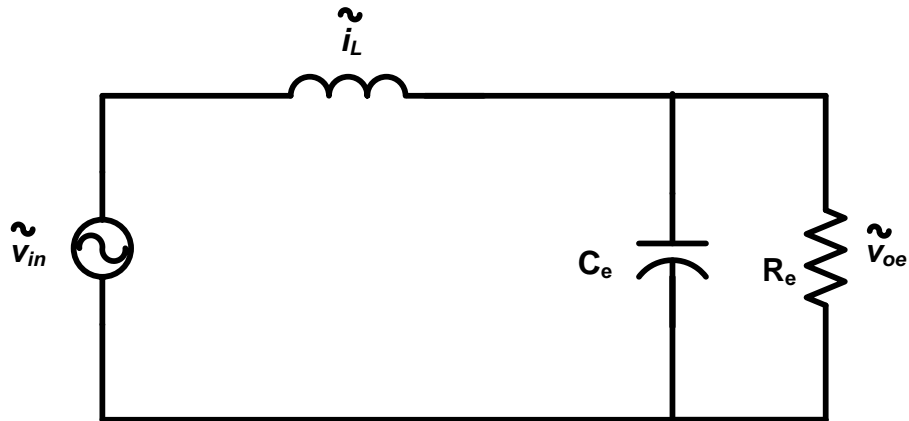


Figure 7.14 The impedance transformed model.

Where,

$$R_e = R \left( \frac{1-D}{1+D} \right)^2$$

$$C_e = C \left( \frac{1-D}{1+D} \right)^2$$

$$\tilde{v}_{oe} = \tilde{v}_o \frac{1-D}{1+D}$$

The input/inductor current,

$$\tilde{i}_L = \frac{\tilde{v}_{in}}{sL + (R_e || (1/sC_e))}$$

$$\tilde{i}_L = \frac{\tilde{v}_{in}}{sL + \left( \frac{R_e/sC_e}{R_e + 1/sC_e} \right)}$$

$$\tilde{i}_L = \frac{\tilde{v}_{in}}{\left( \frac{sL(R_e + 1/sC_e) + R_e/sC_e}{R_e + 1/sC_e} \right)}$$

$$\tilde{i}_L = \tilde{v}_{in} \frac{R_e + 1/sC_e}{sL(R_e + 1/sC_e) + R_e/sC_e}$$

$$\tilde{i}_L = \tilde{v}_{in} \frac{\frac{sR_e C_e + 1}{sC_e}}{\frac{s^2 LR_e C_e + sL + R_e}{sC_e}}$$

$$\tilde{i}_L = \tilde{v}_{in} \left[ \frac{sR_e C_e + 1}{s^2 LR_e C_e + sL + R_e} \right]$$

The equivalent output voltage,

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{(R_e || (1/sC_e))}{sL + (R_e || (1/sC_e))}$$

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{\frac{R_e/sC_e}{R_e + 1/sC_e}}{sL + \left( \frac{R_e/sC_e}{R_e + 1/sC_e} \right)}$$

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{\frac{R_e/sC_e}{R_e + 1/sC_e}}{\left( \frac{sL(R_e + 1/sC_e) + R_e/sC_e}{R_e + 1/sC_e} \right)}$$

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{R_e/sC_e}{sL(R_e + 1/sC_e) + R_e/sC_e}$$

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{R_e/sC_e}{\frac{s^2 LR_e C_e + sL + R_e}{sC_e}}$$

$$\tilde{v}_{oe} = \tilde{v}_{in} \times \frac{R_e}{s^2 LR_e C_e + sL + R_e}$$

$$\tilde{v}_{in} = \tilde{v}_{oe} \times \frac{s^2 LR_e C_e + sL + R_e}{R_e}$$

Putting the value of  $\tilde{v}_{in}$  into the equation of  $\tilde{i}_L$ :

$$\tilde{i}_L = \left[ \tilde{v}_{oe} \times \frac{s^2 LR_e C_e + sL + R_e}{R_e} \right] \times \left[ \frac{sR_e C_e + 1}{s^2 LR_e C_e + sL + R_e} \right]$$

$$\tilde{i}_L = \tilde{v}_{oe} \left[ \frac{sR_e C_e + 1}{R_e} \right]$$

$$\begin{aligned}\tilde{v}_{oe} &= \tilde{i}_L \left[ \frac{R_e}{sR_e C_e + 1} \right] \\ \tilde{v}_o \left( \frac{1-D}{1+D} \right) &= \tilde{i}_L \left[ \frac{R_e}{sR_e C_e + 1} \right] \\ \frac{\tilde{v}_o}{\tilde{i}_L} &= \left( \frac{1+D}{1-D} \right) \left[ \frac{R_e}{sR_e C_e + 1} \right]\end{aligned}\quad (7.3)$$

### 7.3.4 Power Stage Transfer Function for Current Control loop

For the high frequency current control loop, the secondary side of the ideal transformer in the small signal equivalent circuit gets short-circuited. Because at high frequency the capacitor acts as short-circuit (Assume  $r_c = 0$ ). So the equivalent circuit reduces to:

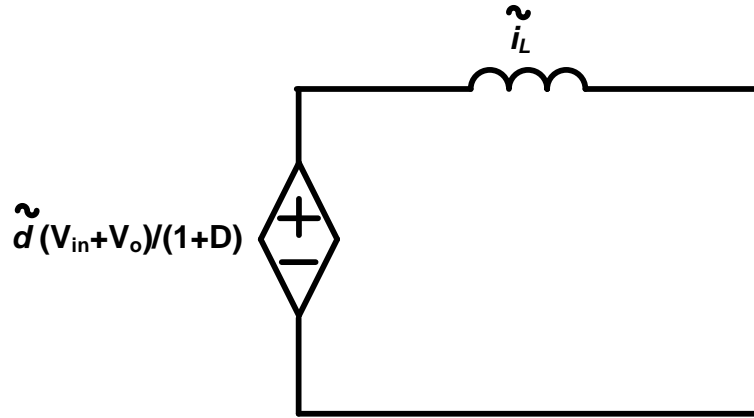


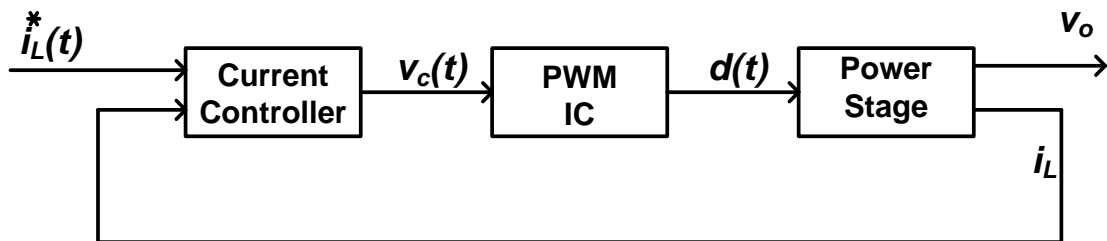
Figure 7.15 The reduced small signal model for current control loop.

The input perturbation  $\tilde{v}_{in} = 0$  since we are deriving control to output transfer function (for current control loop output is  $\tilde{i}_L$ ).

$$\begin{aligned}\tilde{i}_L &= \frac{\tilde{d}(V_o + \hat{V}_{in})}{sL(1+D)} \\ \frac{\tilde{i}_L}{\tilde{d}} &= \frac{(V_o + \hat{V}_{in})}{sL(1+D)}\end{aligned}\quad (7.4)$$

## 7.4 Design of Inner Average Current Control Loop

The inner current control loop is shown within the inner dotted box in Figure 7.6. In order to follow the reference with as little THD as possible, an average-current-mode control is used with a high bandwidth, where the error between the reference  $i_L^*(t)$  and the measured inductor current  $i_L(t)$  is amplified by a current controller to produce the control voltage  $v_c(t)$ . This control voltage is compared with a ramp signal  $v_r(t)$ , with a peak of  $\hat{V}_r$  at the switching frequency  $f_s$  in the PWM controller to produce the switching signal. Just the inner current control loop of Figure 7.6 can be simplified, as shown in Figure 7.15 (a). The reference input  $i_L^*(t)$  varies with time as shown in Figure 7.2. However, the variation is much slower compared to the current control-loop bandwidth, approximately 10 kHz in the numerical example considered later on. Therefore, at each instant of time, the circuit of Figure 7.2 can be considered in a “dc” steady state with the associated variables having values of  $i_L(t)$ ,  $|v_s(t)|$  and  $|d(t)|$ . This equilibrium condition varies slowly with time, compared to the current-control-loop bandwidth, which is designed to be much larger. In Laplace domain, this current loop is shown in Figure 7.15 (b), as discussed below, where “~” on top represents small signal perturbations at very high frequencies in the range of the current-control-loop bandwidth, for example 10 kHz.



(a)

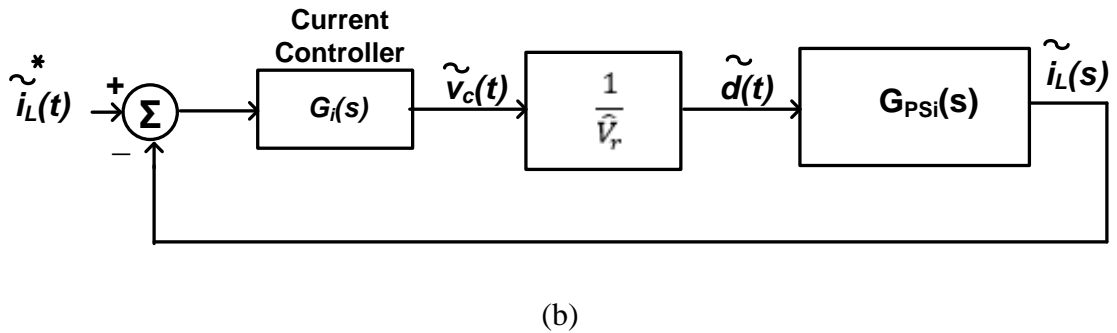


Figure 7.16 Simplified current control loop for PFC

#### 7.4.1 PWM Controller Transfer Function

In the feedback control, a high-speed PWM integrated circuit such as the UC3824 from Unitrode/Texas Instruments may be used. Functionally, within this PWM-IC shown in Figure 7.17 (a), the control voltage  $v_c(t)$  generated by the error amplifier is compared with a ramp signal  $v_r(t)$  with a constant amplitude  $\hat{V}_r$  at a constant switching frequency  $f_s$ , as shown in Figure 7.17 (b). The output switching signal is represented by the switching function  $q(t)$ , which equals 1 if  $v_c(t) \geq v_r$ ; otherwise 0. The switch duty-ratio in Figure 7.17 (b) is given as,

$$d(t) = \frac{v_c(t)}{\hat{V}_r} \quad (7.5)$$

In terms of a disturbance around the dc steady state operating point, the control voltage can be expressed as,

$$v_c(t) = V_c + \tilde{v}_c \quad (7.6)$$

Substituting equation 7.6 into equation 7.5,

$$d(t) = \frac{V_c}{\hat{V}_r} + \frac{\tilde{v}_c}{\hat{V}_r} \quad (7.7)$$

In equation 7.7, the second term on the right side equals  $\tilde{d}(t)$ , from which the transfer function of the PWM-IC is,

$$G_{PWM}(s) = \frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{\hat{V}_r} \quad (7.8)$$

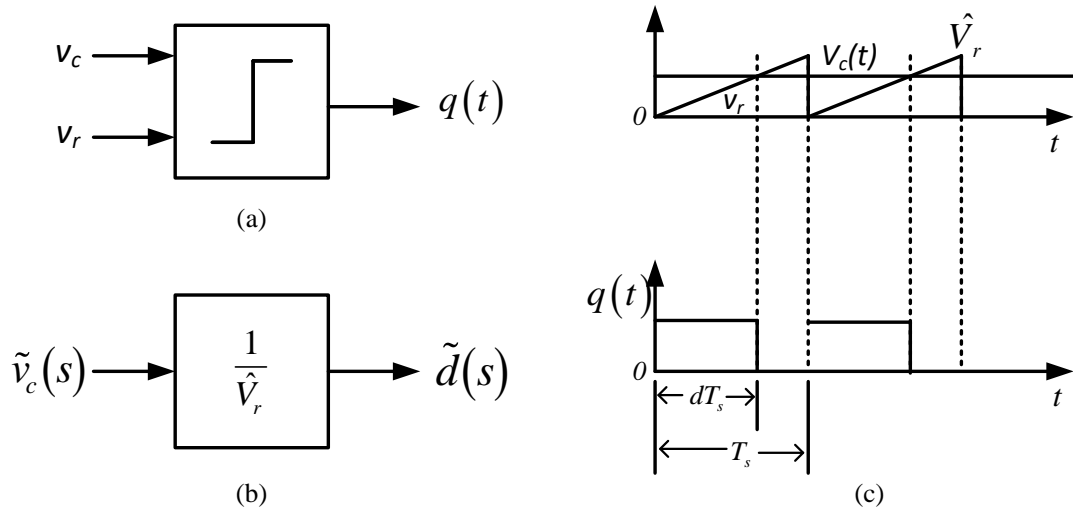


Figure 7.17 PWM waveforms

#### 7.4.2 Transfer Function of the Converter for Current Control Loop

The power stage transfer function for the current control loop is derived in section 7.3.4. Therefore the transfer function is,

$$\frac{\tilde{i}_L}{\tilde{d}} = \frac{(V_o + \hat{V}_{in})}{sL(1+D)} \quad (7.4)$$

#### 7.4.3 Designing the Current Controller

The transfer function in equation 7.4 is not a pure integrator. Therefore, to have a high loop dc gain and a zero dc steady state error in Figure 7.17 (b), the current controller transfer function  $G_i(s)$  must have a pole at the origin. In the loop in Figure 7.17 (b), the phase due to the pole at origin in  $G_i(s)$  and that of the power-stage transfer function (equation 7.4) add up to  $180^\circ$ . Hence,  $G_i(s)$  includes a pole-zero pair that provides a phase boost, and hence the specified phase margin, for example  $60^\circ$  at the loop crossover frequency:



$$G_i(s) = \frac{k_c}{s} \frac{1+s/\omega_z}{1+s/\omega_p} \quad (7.9)$$

where,  $k_c$  is the controller gain. Knowing the phase boost,  $\phi_{boost}$ , we can calculate the pole-zero locations to provide the necessary phase boost:

$$K_{boost} = \tan\left(45^\circ + \frac{\phi_{boost}}{2}\right)$$

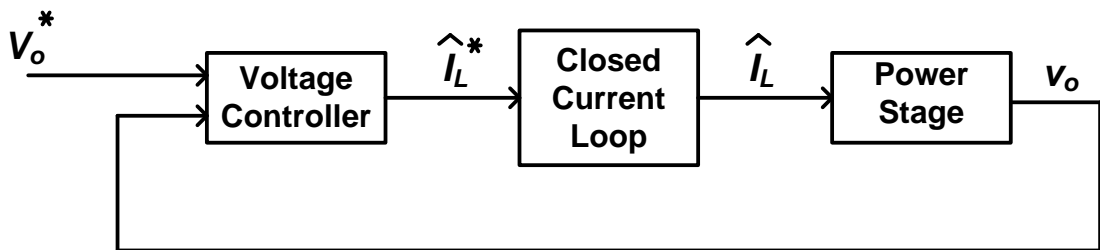
$$f_z = \frac{f_{ci}}{K_{boost}}$$

$$f_p = K_{boost} f_{ci}$$

where  $f_{ci}$  is the crossover frequency of the current loop transfer function.

## 7.5 Design of Outer Voltage Control Loop

The outer voltage-control loop is needed to determine the peak,  $\hat{I}_L$ , of the inductor current. In the voltage loop, the bandwidth is limited to approximately 15 Hz. The reason has to do with the fact that the output voltage across the capacitor contains a component  $v_{o2}$  at twice the line-frequency (at 100 Hz in 50-Hz line-frequency systems). This output voltage ripple must not be corrected by the voltage loop; otherwise it will lead to a third-harmonic distortion in the input current.



(a)

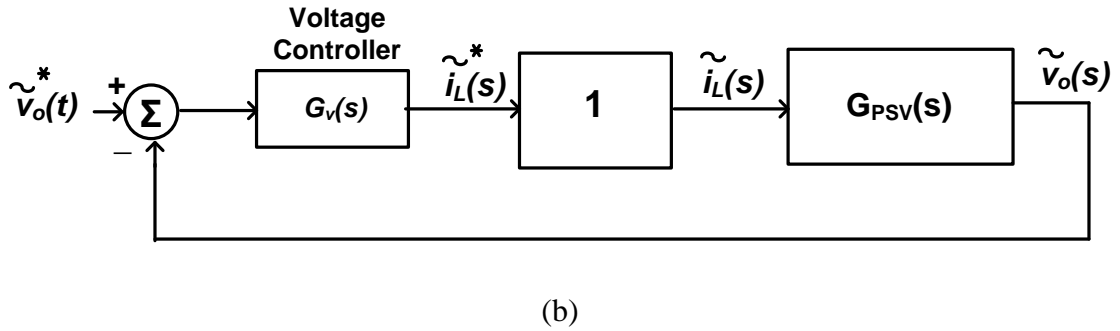


Figure 7.18 Voltage control loop for PFC.

For such a low bandwidth of the voltage-control loop (approximately three orders of magnitude below the current-loop bandwidth of  $\sim 10$  kHz), it is perfectly reasonable to assume the current loop to be ideal at low frequencies around 15 Hz. Therefore, in the voltage-control block diagram shown in Figure 7.18 (a), the current closed loop produces  $\hat{I}_L$  equal to its reference value  $\hat{I}_L^*$ . In addition to a large dc component,  $\hat{I}_L^*$  contains an unwanted second-harmonic frequency component  $\hat{I}_{L2}$  due to  $v_{o2}$  in the input to the voltage controller.  $\hat{I}_{L2}$  at the second-harmonic frequency results in a third-harmonic frequency distortion in the current drawn from the utility. Therefore, in the output of the voltage controller block in Figure 7.18 (a),  $\hat{I}_{L2}$  is limited to approximately 1.5% of the dc component in  $\hat{I}_L^*$ . The voltage control loop for low-frequency perturbations, in the range of the voltage-loop bandwidth of approximately 15 Hz, is shown in Figure 7.18 (b). As derived in section 7.3.3, the transfer function of the power stage in Figure 7.18 (b) at these low perturbation frequencies (ignoring the capacitor ESR) is:

$$\frac{\tilde{v}_o}{\tilde{i}_L} = \left( \frac{1+D}{1-D} \right) \left[ \frac{R_e}{sR_e C_e + 1} \right] \quad (7.3)$$

To achieve a zero steady state error, the voltage-controller transfer function should have a pole at the origin. However, since the PFC circuit is often a pre-regulator (not a strict regulator), this requirement is waived, which otherwise would make the voltage controller design much more complicated. The following simple transfer function is

often used for the voltage controller in Figure 7.18 (b), where a pole is placed at the voltage-loop crossover frequency  $\omega_{cv}$  below 15 Hz,

$$G_v(s) = \frac{k_v}{1 + s/\omega_{cv}} \quad (7.10)$$

At full-load, the power stage transfer function given by equation 7.3 has a pole at a very low frequency, for example of the order of one or two Hz, which introduces a phase lag approaching  $90^\circ$  much beyond the frequency at which this pole occurs. The transfer function of the controller given by equation 7.10 introduces a lag of  $45^\circ$  at the loop crossover frequency. Therefore, these two phase lags of  $\sim 135^\circ$  at the crossover frequency result in a satisfactory phase margin of  $45^\circ$ . Using equations 7.3 and 7.10, by definition, at the crossover frequency  $f_{cv}$ , the loop transfer function in Figure 7.18 (b) has a magnitude equal to unity,

$$\left| \frac{k_v}{1 + s/\omega_{cv}} \times \left( \frac{1+D}{1-D} \right) \frac{R_e}{1 + sR_eC_e} \right|_{s=j2\pi f_{cv}} = 1 \quad (7.11)$$

In the voltage controller of Figure 7.18 (b) and equation 7.10, the input  $\hat{V}_{o2}$  results in an output  $\hat{I}_{L2}$ . Therefore, at the second-harmonic frequency in the voltage controller of equation 7.10,

$$\left| \frac{k_v}{1 + s/\omega_{cv}} \right|_{s=j(2\pi \times 100)} = \frac{\hat{I}_{L2}}{\hat{V}_{o2}} \quad (7.12)$$

From equations 7.11 and 7.12, the two unknowns  $k_v$  and  $\omega_{cv}$  in the voltage controller transfer function of equation 7.10 can be calculated.

## 7.6 Controller Design

A suitable feedback control has to be designed to improve the input power factor. The input voltage applied is 220V (rms). The boost regulator has to regulate the output voltage around 350V (DC) with an allowable ripple of 1%. The converter is designed for a load of  $350\Omega$  and to deliver output power of 350W.

The output capacitor has to be selected with the requirement of 1% ripple of the second harmonic component of the ripple voltage. Percentage ripple is defined as:

$$\% \text{ Ripple} = \frac{V_{\text{Ripple}} (RMS)}{V_o (DC)} \times 100$$

$$\% \text{ Ripple} = \frac{\hat{V}_{\text{Ripple}} / \sqrt{2}}{V_o (DC)} \times 100$$

To have an output voltage ripple of 1% of the second harmonic component of the load voltage should have following value:

$$1\% = \frac{\hat{V}_{02} / \sqrt{2}}{V_o}$$

$$1\% = \frac{\hat{V}_{02}}{\sqrt{2} \times V_o}$$

$$0.01 = \frac{\hat{V}_{02}}{\sqrt{2} \times 350}$$

$$\hat{V}_{02} = 4.949747V$$

Using the value of this ripple the value of the smoothing capacitor has to be calculated from the formula:

$$C = \frac{\hat{V}_s \times \hat{I}_L}{4\omega \times \hat{V}_{o2} \times V_o}$$

To find out the value of  $\hat{I}_L$  the PFC is assumed to be lossless, so the input power is equal to the output power.

$$\therefore P_o = V_s (RMS) \times I_s (RMS)$$

$$P_o = V_s (RMS) \times \hat{I}_s / \sqrt{2}$$

$$\hat{I}_s = \frac{\sqrt{2} \times P_o}{V_s(RMS)}$$

And from the diagram it is evident that the  $\hat{I}_L = \hat{I}_s$  so,

$$\hat{I}_L = \frac{\sqrt{2} \times P_o}{V_s(RMS)}$$

$$\hat{I}_L = \frac{\sqrt{2} \times 350}{220} = 2.249885A$$

Therefore the value of the output capacitor has to be:

$$C = \frac{(220 \times \sqrt{2}) \times 2.249885}{4 \times (2 \times \pi \times f) \times 4.949747 \times 350}$$

$$C = \frac{(220 \times \sqrt{2}) \times 2.249885}{4 \times (2 \times \pi \times 50) \times 4.949747 \times 350} = 321.5415 \mu F$$

The formula for choosing a suitable inductor to keep the current in continuous conduction mode is:

$$L = \frac{\hat{V}_m \times DT_s}{\hat{i}_{L2}} = \frac{\hat{V}_m \times D}{\hat{i}_{L2} \times f_s}$$

The peak value of the second harmonic inductor current is generally 1.5% of the peak inductor current, thus

$$\hat{i}_{L2} = \frac{1.5}{100} \times 2.249885 = 0.03374828A$$

And the switching frequency is assumed to be  $f_s = 100kHz$ . The duty cycle at desired operating condition is:

$$D = \frac{V_o - \hat{V}_{in}}{V_o + \hat{V}_{in}} = \frac{350 - (220 \times \sqrt{2})}{350 + (220 \times \sqrt{2})} = 0.058798$$

So the required inductor is calculated to be:

$$L = \frac{(220 \times \sqrt{2}) \times 0.058798}{0.03374828 \times 100 \times 10^3} = 5.420625 \text{mH}$$

**Designing current control loop:**

In equation 7.8, assume that  $\hat{V}_r = 1$ . For the loop crossover frequency of 10 kHz ( $\omega_{ci} = 2\pi \times 10^4$  rad/s) and the phase margin of  $60^\circ$ , the parameters in the current controller of equation 7.9 are as follows:

$$k_c = 2295.8$$

$$\omega_z = 8.4179 \times 10^3 \text{ rad/s}$$

$$\omega_p = 1.1725 \times 10^5 \text{ rad/s}$$

Calculation for the components of analogue current controller:

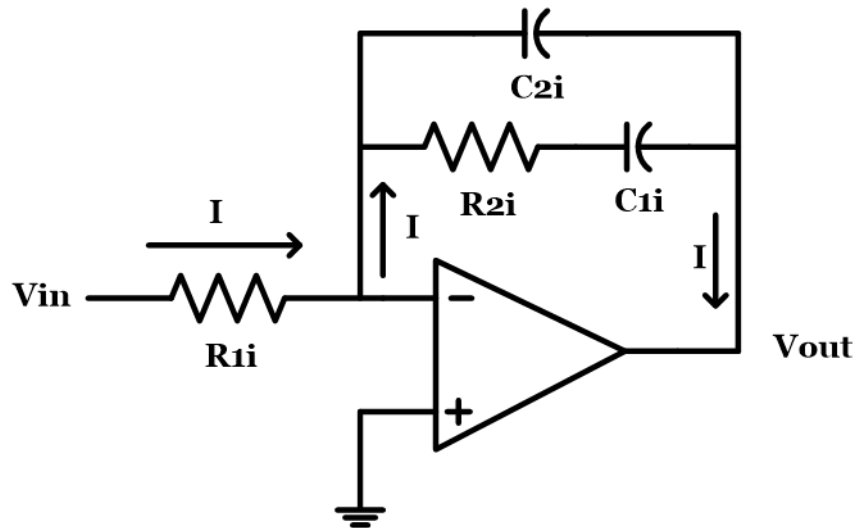


Figure 7.19 Op-amp circuit to implement current control loop.

$$\frac{V_{in}}{R_{1i}} = \frac{V_{out}}{\left( \frac{1}{sC_{2i}} \parallel \left( R_{2i} + \frac{1}{sC_{1i}} \right) \right)}$$

$$\frac{V_{out}}{V_{in}} = \frac{\left( \frac{1}{sC_{2i}} \parallel \left( R_{2i} + \frac{1}{sC_{1i}} \right) \right)}{R_{1i}}$$

The numerator of the transfer function can be calculated as,

$$\begin{aligned} & \left( \frac{1}{sC_{2i}} \parallel \left( R_{2i} + \frac{1}{sC_{1i}} \right) \right) \\ &= \left( \frac{1}{sC_{2i}} \parallel \left( \frac{1 + sC_{1i}R_{2i}}{sC_{1i}} \right) \right) \\ &= \frac{\frac{1}{sC_{2i}} \times \frac{1 + sC_{1i}R_{2i}}{sC_{1i}}}{\frac{1}{sC_{2i}} + \frac{1 + sC_{1i}R_{2i}}{sC_{1i}}} \\ &= \frac{\frac{1 + sC_{1i}R_{2i}}{s^2C_{1i}C_{2i}}}{\frac{sC_{1i} + sC_{2i} + s^2C_{1i}C_{2i}R_{2i}}{s^2C_{1i}C_{2i}}} \\ &= \frac{1 + sC_{1i}R_{2i}}{sC_{1i} + sC_{2i} + s^2C_{1i}C_{2i}R_{2i}} \\ &= \frac{1 + sC_{1i}R_{2i}}{s[C_{1i} + C_{2i} + sC_{1i}C_{2i}R_{2i}]} \\ &= \frac{1}{s} \frac{1 + sC_{1i}R_{2i}}{(C_{1i} + C_{2i}) \left[ 1 + \frac{sC_{1i}C_{2i}R_{2i}}{(C_{1i} + C_{2i})} \right]} \end{aligned}$$

$$= \frac{1}{s} \frac{1/(C_{1i} + C_{2i}) \times \left(1 + s/(1/C_{2i}R_{2i})\right)}{\left[1 + s/((C_{1i} + C_{2i})/C_{1i}C_{2i}R_{2i})\right]}$$

Thus,

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{s} \frac{1/(C_{1i} + C_{2i}) \times \left(1 + s/(1/C_{2i}R_{2i})\right)}{\left[1 + s/((C_{1i} + C_{2i})/C_{1i}C_{2i}R_{2i})\right]}}{R_{1i}}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{s} \frac{1/(R_{1i} \times (C_{1i} + C_{2i})) \times \left(1 + s/(1/C_{2i}R_{2i})\right)}{\left[1 + s/((C_{1i} + C_{2i})/C_{1i}C_{2i}R_{2i})\right]}$$

So the formulas can found as,

$$k_c = 1/R_{1i} (C_{1i} + C_{2i})$$

$$\omega_z = 1/C_{2i}R_{2i}$$

$$\omega_p = (C_{1i} + C_{2i})/C_{1i}C_{2i}R_{2i}$$

From the value of  $k_c$  we can find,

$$C_{1i} + C_{2i} = 1/k_c R_{1i}$$

Putting the value into the equation of  $\omega_p$ ,

$$\omega_p = \frac{1}{k_c R_{1i} C_{2i} R_{2i} C_{1i}}$$

Realizing  $R_{2i}C_{1i} = 1/\omega_z$ ,



$$\omega_p = \frac{1}{k_c R_{1i} C_{2i} \omega_z}$$

$$C_{2i} = \frac{1}{k_c R_{1i} \omega_z \omega_p}$$

Dividing  $\omega_p$  by  $\omega_z$ ,

$$\frac{\omega_p}{\omega_z} = \left( \frac{C_{1i} + C_{2i}}{R_{2i} C_{1i} C_{2i}} \right) \div \left( \frac{1}{R_{2i} C_{1i}} \right)$$

$$\frac{\omega_p}{\omega_z} = \left( \frac{C_{1i} + C_{2i}}{C_{2i}} \right)$$

$$\frac{\omega_p}{\omega_z} = \left( \frac{C_{1i}}{C_{2i}} + 1 \right)$$

$$\frac{C_{1i}}{C_{2i}} = \frac{\omega_p}{\omega_z} - 1$$

$$C_{1i} = C_{2i} \left( \frac{\omega_p}{\omega_z} - 1 \right)$$

Finally the value of  $R_{2i}$  can be calculated using,

$$R_{2i} = \frac{1}{\omega_z C_{2i}}$$

Therefore,

$$R_{2i} = 29.382k\Omega$$

$$C_{1i} = 4.0431nF$$

$$C_{2i} = 0.31273nF$$

### Calculations of Voltage Control Loop:

The magnitude of the loop transfer function at the crossover frequency should be unity.

$$\left| \frac{k_v}{1+s/\omega_{cv}} \times \left( \frac{1+D}{1-D} \right) \frac{R_e}{1+sR_eC_e} \right|_{s=j2\pi f_{cv}} = 1$$

$$\left| \frac{k_v}{1+j(\omega_{cv}/\omega_{cv})} \times \left( \frac{1+D}{1-D} \right) \frac{R_e}{1+j\omega_{cv}R_eC_e} \right| = 1$$

$$\left| \frac{R_e k_v (1+D)}{(1-D)} \times \frac{1}{(1+j)(1+j\omega_{cv}R_eC_e)} \right| = 1$$

$$\frac{R_e k_v (1+D)}{(1-D)} \times \left| \frac{1}{(1+j)(1+j\omega_{cv}R_eC_e)} \right| = 1$$

The magnitude of the complex portion of the equation in the denominator can be evaluated separately as (Assuming,  $m = R_e C_e$ ),

$$\begin{aligned} & |(1+j)(1+j\omega_{cv}R_eC_e)| \\ &= |(1+j)(1+j\omega_{cv}m)| \\ &= |1+jm\omega_{cv} + j + j^2m\omega_{cv}| \\ &= |1+jm\omega_{cv} + j - m\omega_{cv}| \\ &= |(1-m\omega_{cv}) + j(1+m\omega_{cv})| \\ &= \sqrt{(1-m\omega_{cv})^2 + (1+m\omega_{cv})^2} \\ &= \sqrt{1-2m\omega_{cv} + (m\omega_{cv})^2 + 1+2m\omega_{cv} + (m\omega_{cv})^2} \\ &= \sqrt{2+2(m\omega_{cv})^2} \end{aligned}$$

Thus the equation becomes

$$\frac{R_e k_v (1+D)}{(1-D)} \times \frac{1}{\sqrt{2+2(m\omega_{cv})^2}} = 1 \quad (7.13)$$

At the second harmonic frequency the magnitude of the voltage controller becomes:

$$\left| \frac{k_v}{1+s/\omega_{cv}} \right|_{s=j2\pi \times 100} = \frac{\hat{I}_{L2}}{\hat{V}_{o2}} = \frac{0.03374828}{4.94974} = 6.81819 \times 10^{-3}$$

$$\left| \frac{k_v}{1+j\omega_2/\omega_{cv}} \right| = 6.81819 \times 10^{-3}$$

$$\frac{k_v}{\sqrt{1+(\omega_2/\omega_{cv})^2}} = 6.81819 \times 10^{-3}$$

$$k_v = \sqrt{1+(\omega_2/\omega_{cv})^2} \times 6.81819 \times 10^{-3}$$

Putting the value of  $k_v$  into equation 7.13 to evaluate  $\omega_{cv}$  we have,

$$\frac{R_e k_v (1+D)}{(1-D)} \times \frac{1}{\sqrt{2+2(m\omega_{cv})^2}} = 1$$

$$\frac{R_e (1+D)}{(1-D)} \times \frac{k_v}{\sqrt{2+2(m\omega_{cv})^2}} = 1$$

$$\frac{R_e (1+D)}{(1-D)} \times \frac{\sqrt{1+(\omega_2/\omega_{cv})^2} \times 6.81819 \times 10^{-3}}{\sqrt{2+2(m\omega_{cv})^2}} = 1$$

$$\frac{\sqrt{1+(\omega_2/\omega_{cv})^2} \times 6.81819 \times 10^{-3}}{\sqrt{2} \times \sqrt{1+(m\omega_{cv})^2}} = \frac{(1-D)}{R_e (1+D)}$$

$$\frac{\sqrt{1+(\omega_2/\omega_{cv})^2}}{\sqrt{1+(m\omega_{cv})^2}} = \frac{\sqrt{2} \times (1-D)}{R_e (1+D) \times 6.81819 \times 10^{-3}}$$

Where,

$$R_e = R \left( \frac{1-D}{1+D} \right)^2 = 350 \times \left( \frac{1-0.058798}{1+0.058798} \right)^2 = 276.571549 \Omega$$

$$C_e = C \left( \frac{1-D}{1+D} \right)^2 = 321.5415 \mu \times \left( \frac{1-0.058798}{1+0.058798} \right)^2 = 254.0835 \mu F$$

Thus the value of  $\omega_{cv}$  can be calculated,

$$\frac{\sqrt{1+(\omega_2/\omega_{cv})^2}}{\sqrt{1+(m\omega_{cv})^2}} = \frac{\sqrt{2} \times (1-0.058798)}{276.571549 \times (1+0.058798) \times 6.81819 \times 10^{-3}}$$

$$\frac{\sqrt{1+(\omega_2/\omega_{cv})^2}}{\sqrt{1+(m\omega_{cv})^2}} = 0.6666657$$

$$\frac{1+(\omega_2/\omega_{cv})^2}{1+(m\omega_{cv})^2} = (0.6666657)^2 = .444443$$

$$1 + \omega_2^2 / \omega_{cv}^2 = 0.444443 \times (1 + m^2 \omega_{cv}^2)$$

$$1 + (2 \times \pi \times 100)^2 / \omega_{cv}^2 = 0.444443 + 0.444443 \times (276.571549 \times 254.0835 \mu)^2 \omega_{cv}^2$$

$$2.194745 \times 10^{-3} \omega_{cv}^4 - 0.555557 \omega_{cv}^2 - 394784.176 = 0$$

Solutions of the equation are

$$\omega_{cv1} = -116.3570963572339512112235625054$$

$$\omega_{cv2} = 116.3570963572339512112235625054$$

$$\omega_{cv3} = 115.26423740836603407242305130443i$$

$$\omega_{cv3} = -115.26423740836603407242305130443i$$

The value of  $\omega_{cv}$  has to be a positive real number thus,

$$\omega_{cv} = 116.357096$$

So  $k_v$  can be calculated as,

$$k_v = \sqrt{1 + (\omega_2/\omega_{cv})^2} \times 6.81819 \times 10^{-3}$$

$$k_v = \sqrt{1 + ((2 \times \pi \times 100)/116.357096)^2} \times 6.81819 \times 10^{-3}$$

$$k_v = 37.44365 \times 10^{-3}$$

Calculation for the components of analogue voltage controller:

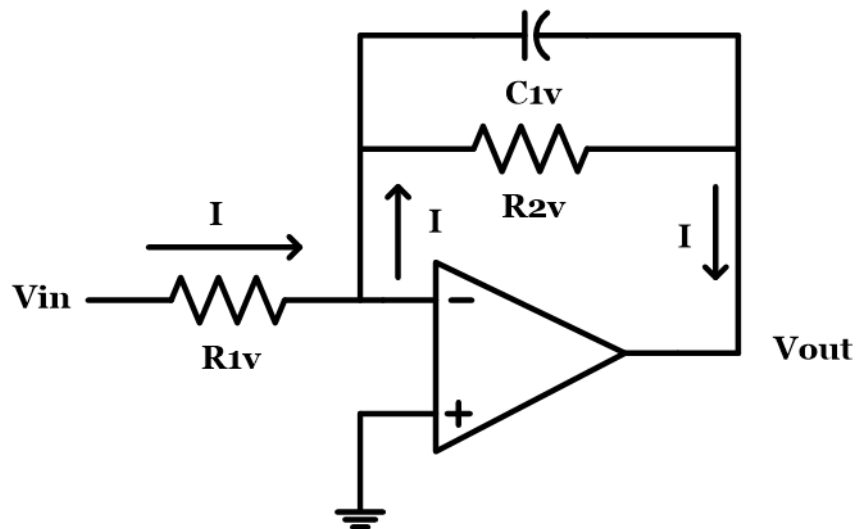


Figure 7.20 Op-amp circuit to implement voltage control loop.

$$V_{in} = I \times R_{1v}$$

$$V_{out} = I \times \left( \frac{1}{sC_{1v}} \parallel R_{2v} \right)$$

Equating current from both equations, we have

$$\frac{V_{in}}{R_{1v}} = \frac{V_{out}}{\left( \frac{1}{sC_{1v}} \parallel R_{2v} \right)}$$

$$\frac{V_{out}}{V_{in}} = \frac{\left( \frac{1}{sC_{1v}} \parallel R_{2v} \right)}{R_{1v}}$$

$$\frac{V_{out}}{V_{in}} = \frac{\left( \frac{1}{sC_{1v}} \times R_{2v} \right)}{\left( \frac{1}{sC_{1v}} + R_{2v} \right)} \frac{1}{R_{1v}}$$

$$\frac{V_{out}}{V_{in}} = \frac{\left( \frac{R_{2v}}{sC_{1v}} \right)}{\left( \frac{1 + sC_{1v}R_{2v}}{sC_{1v}} \right)} \frac{1}{R_{1v}}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_{2v}}{R_{1v}(1 + sC_{1v}R_{2v})}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_{2v}/R_{1v}}{\left( 1 + \frac{s}{1/C_{1v}R_{2v}} \right)}$$

$$k_v = R_{2v}/R_{1v}$$

$$\omega_{cv} = 1/C_{1v}R_{2v}$$

Assuming  $R_{1v} = 100k\Omega$ ,

$$R_{2v} = k_v R_{1v} = 37.44365 \times 10^{-3} \times 100k = 3.744365k\Omega$$

$$C_{1v} = 1/\omega_{cv}R_{2v} = 1/(116.357096 \times 3.744365k) = 2.29524\mu F$$

## 7.7 Simulation with Designed Controller

Figure 7.21 shows the proposed converter with the feedback control. The parameters of circuit is given in Table 7.1. The PFC controller is designed to obtain an average output voltage of 350 Vdc. The simulation of the designed controller is given in Table 7.2. Typical input-output waveforms of the proposed controller is shown in Figure 7.22.

Table 7.1 Parameters of the converter of Figure 7.21.

Nominal input ac source voltage, $V_I$	300V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	100 kHz
Inductors, $L_1, L_2$	2.5 mH
Capacitors, $C_1, C_2$ $C_o$	1 $\mu$ F 321 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Gain of Voltage Sensor $V_{SEN1}$ $V_{SEN2}$	0.0033 1
Gain of Current Sensor $I_{SEN1}$	1

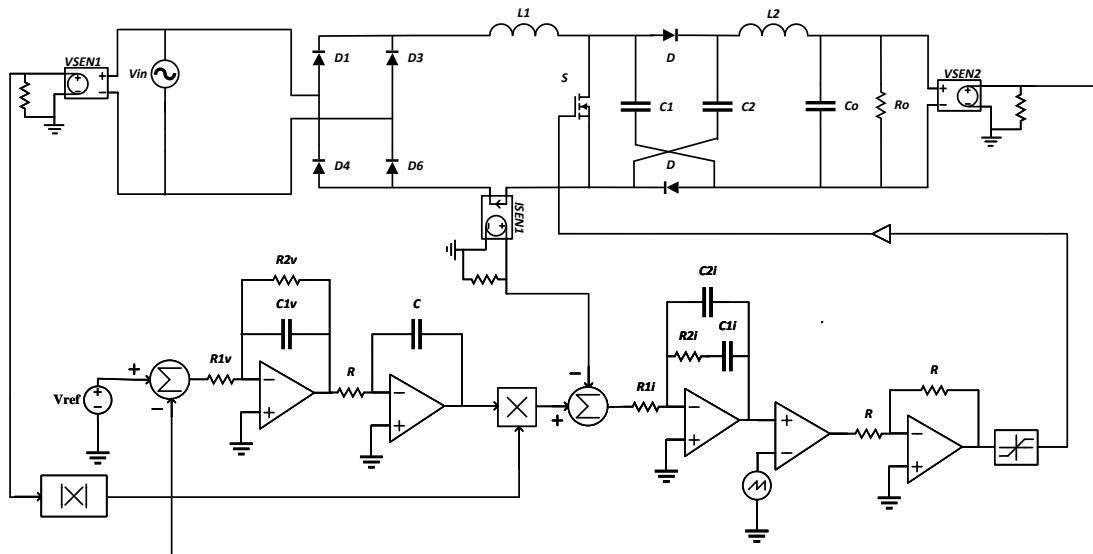


Figure 7.21 Diode capacitor assisted output switched AC to DC boost converter with PFC control.

Table 7.2 Results of the simulation of the converter with feedback control.

Performance Parameters	Conventional Boost	Proposed Boost Without Feedback	Proposed Boost With Feedback
Conversion Efficiency	90.132%	99.873%	99.502%
Input Current THD	92.589%	97.761%	3.857%
Input Power Factor	0.727	0.694	0.998



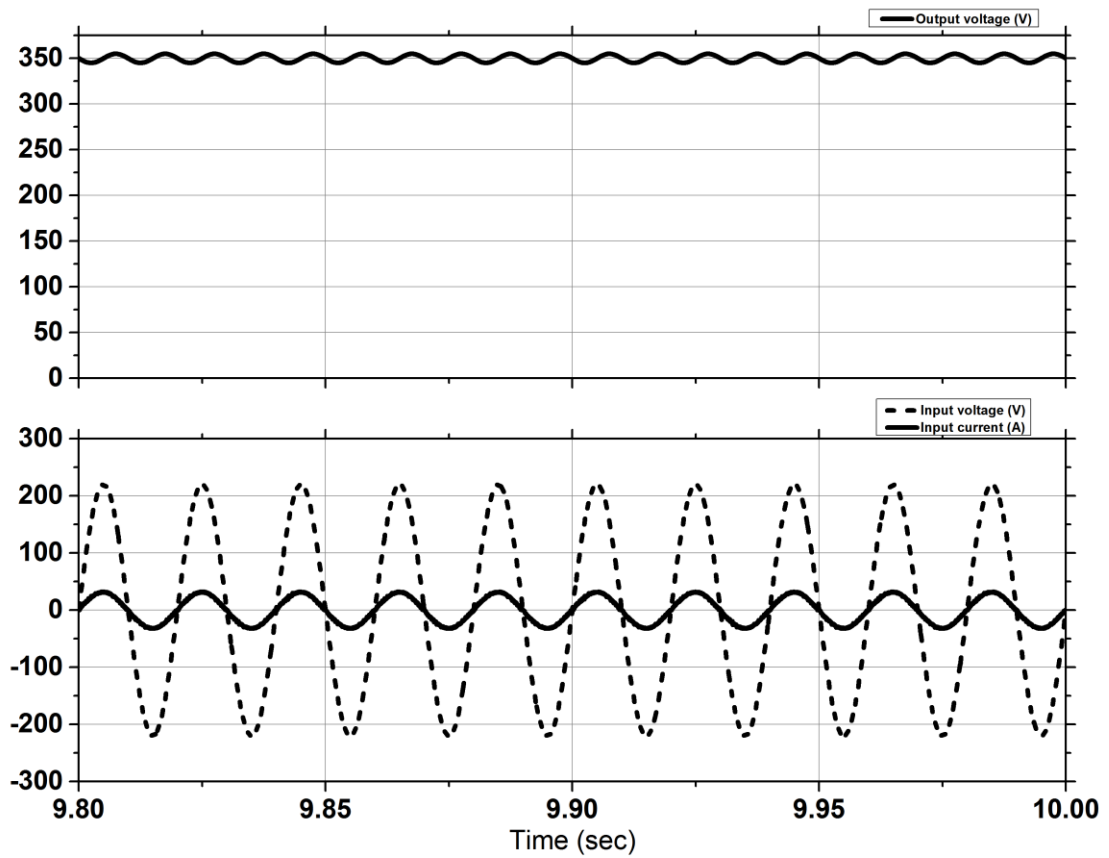


Figure 7.22 Typical input –output waveforms of the PFC controlled converter of Figure 7.21.

## 7.8 Discussions

The controller is designed to achieve best possible outcome under ideal condition. The input current THD is below 5%. The input power factor is almost unity (0.998). The proposed converter with feedback offered higher conversion efficiency compared to the conventional AC to DC boost converter. There is a slight decrease in conversion efficiency due to feedback, which can be neglected since other performance parameters improved significantly. The proposed converter with feedback offered 99.5% of conversion efficiency.

# Chapter 8

## Experimental Results

### 8.1 Experimental Results for Modified Input Switched AC to DC Boost Converter.

The circuit diagram of the implemented converter is shown in following Figure 8.1. Parameters used in the circuit are provided in Table 8.1. A photo of the laboratory set up is given in Figure 8.2. Typical gate pulse generated to turn the switch ON/OFF is shown in Figure 8.3 (a), whereas the output voltage and input voltage-input current are shown in Figure 8.3 (b) and (c) respectively for the circuit without feedback control for 25 percent duty cycle. Similar waveforms are shown in Figures 8.4 (a)-(c) and 8.5 (a)-(c) for 50 percent and 75 percent duty cycles respectively. The average output voltage and the performance parameters obtained from the experimentation are compared with the simulated results in Table 8.2 and Table 8.3 respectively.

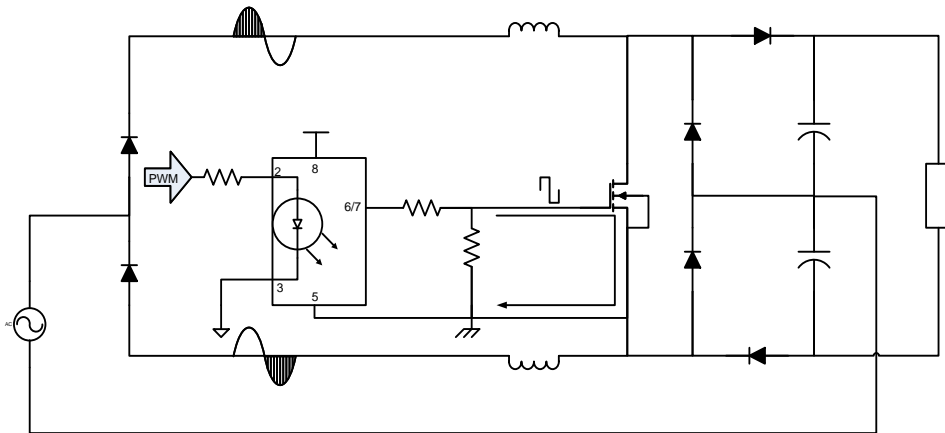


Figure 8.1 The equivalent circuit of experimental set up done in Laboratory on single phase modified input switched AC to DC boost converter.

Table 8.1 Parameters of circuit of Figure 8.1 for experimental set up.

Nominal input ac source voltage, $V_I$	15V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	15.54 mH
Capacitors, $C_1, C_2$	305 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Diode	MUR3060PT
MOSFET	IRFP460

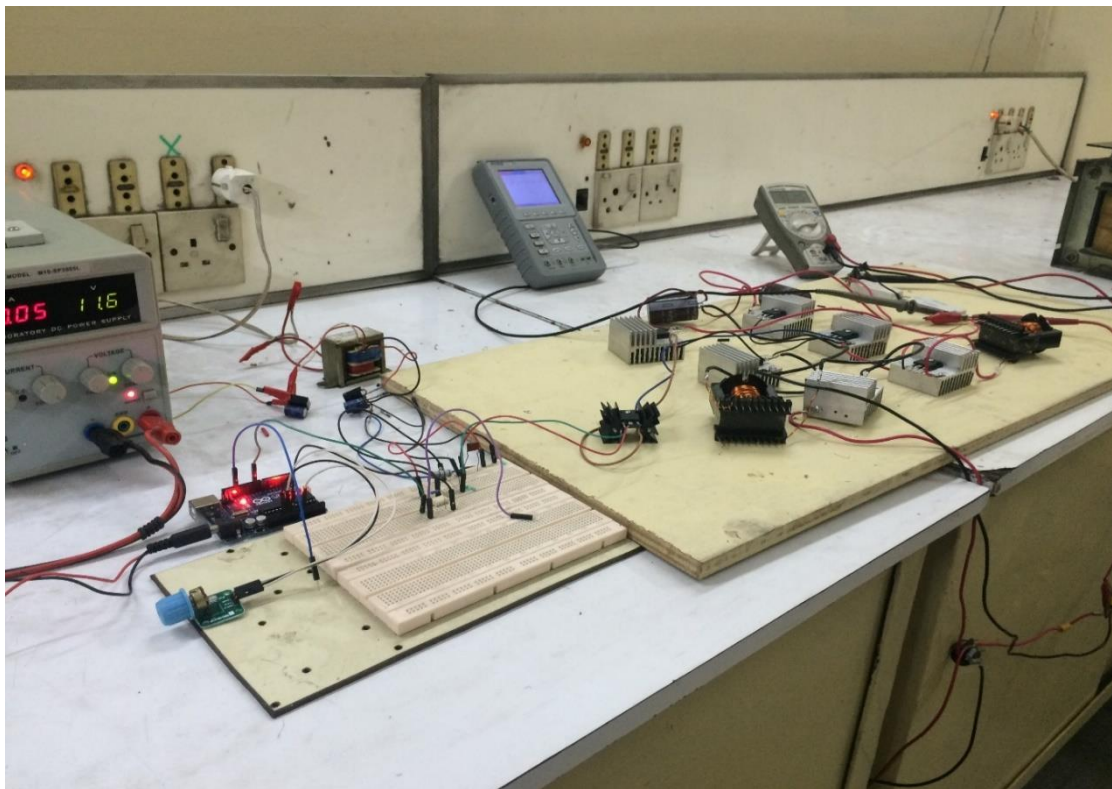
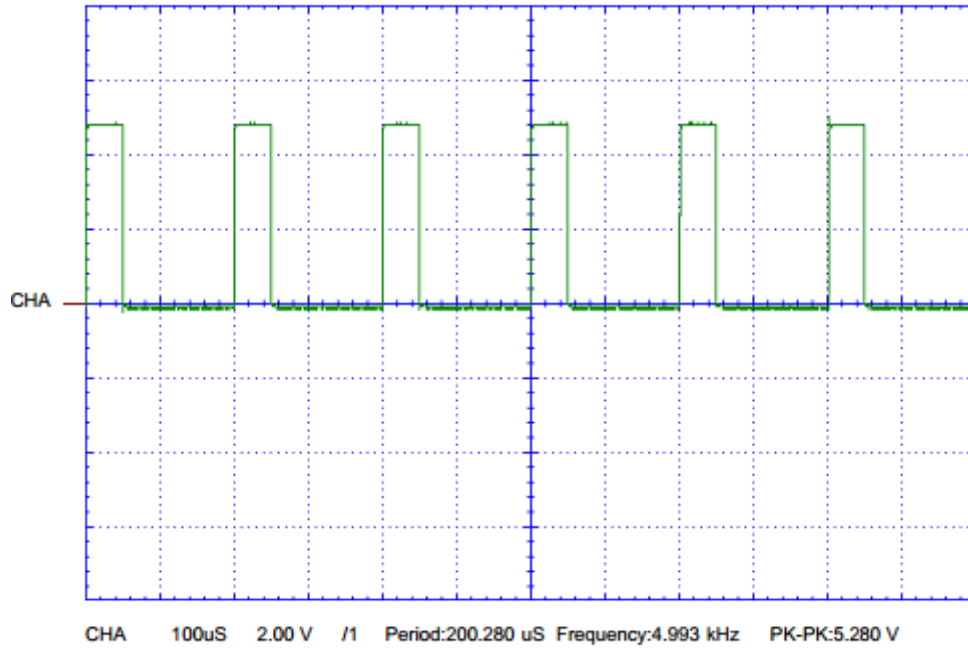
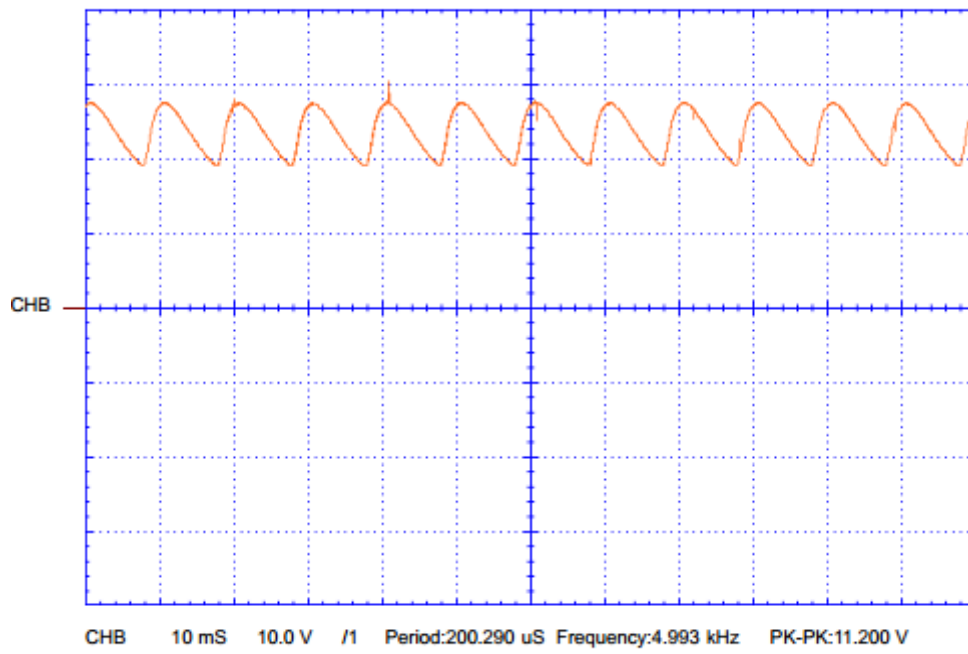


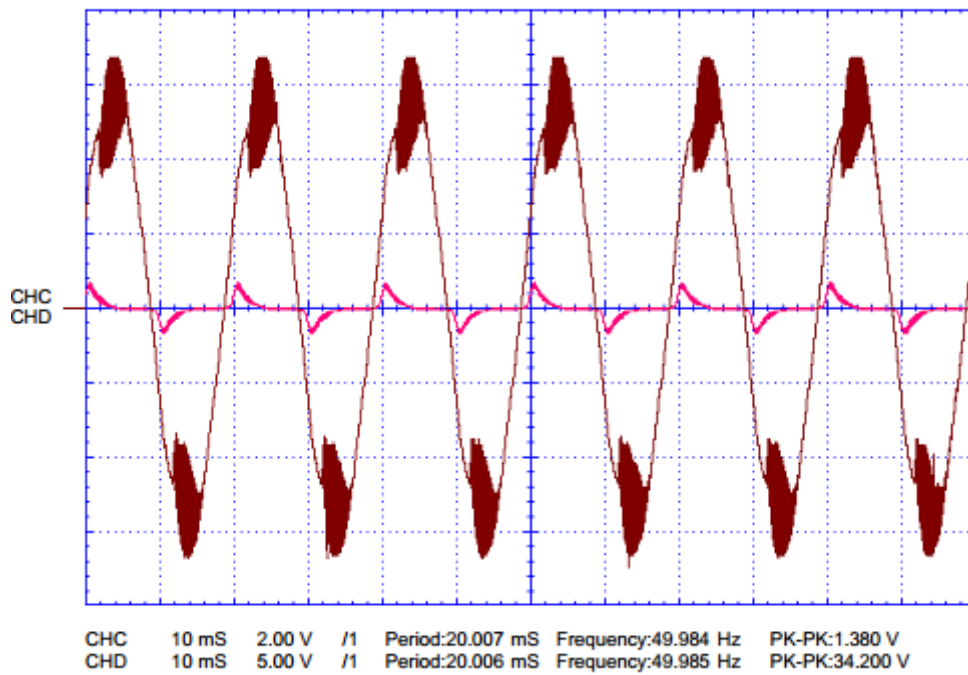
Figure 8.2 The experimental set up done in laboratory for proposed boost converter.



(a)

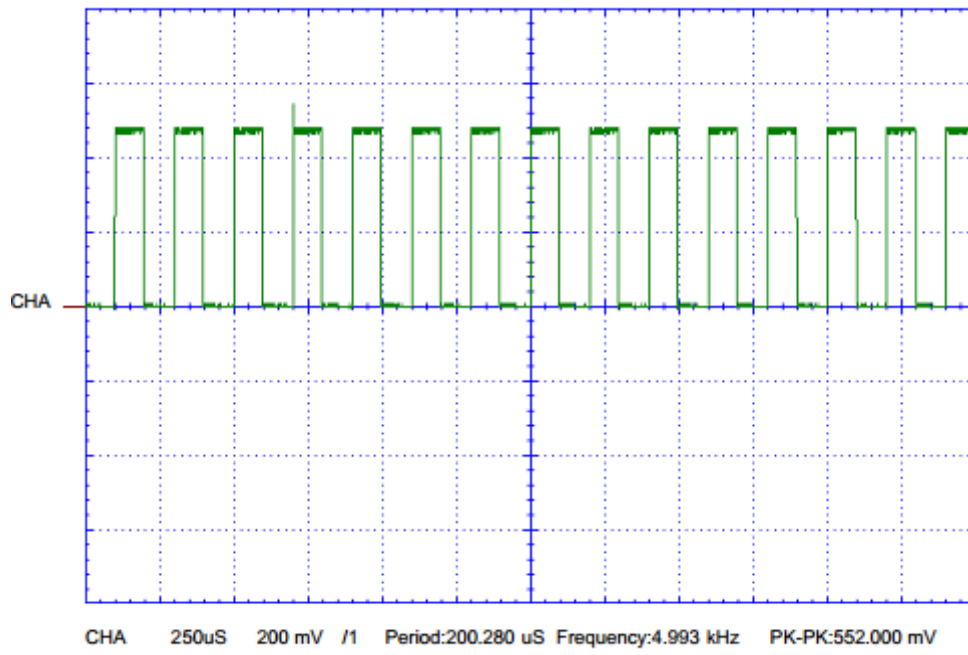


(b)

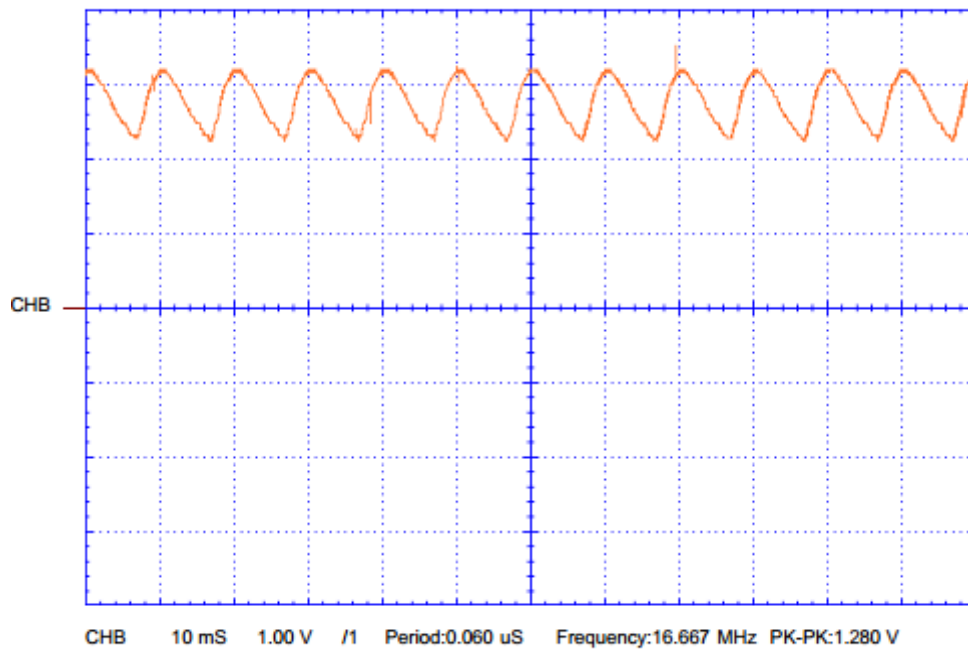


(c)

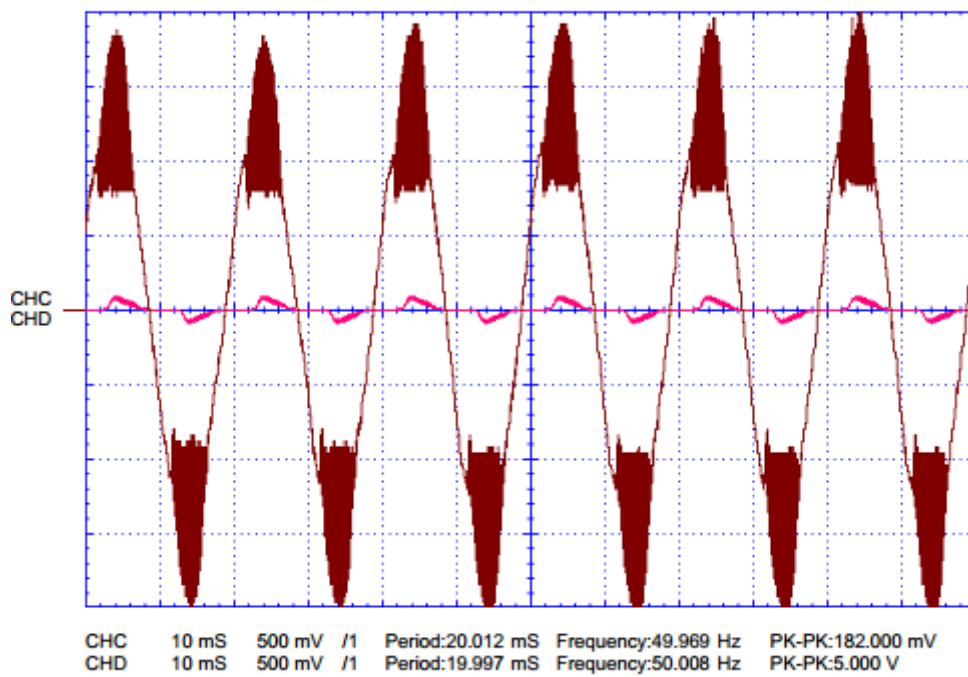
Figure 8.3 Waveforms of Oscilloscope for modified input switched AC to DC converter for 25% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.



(a)

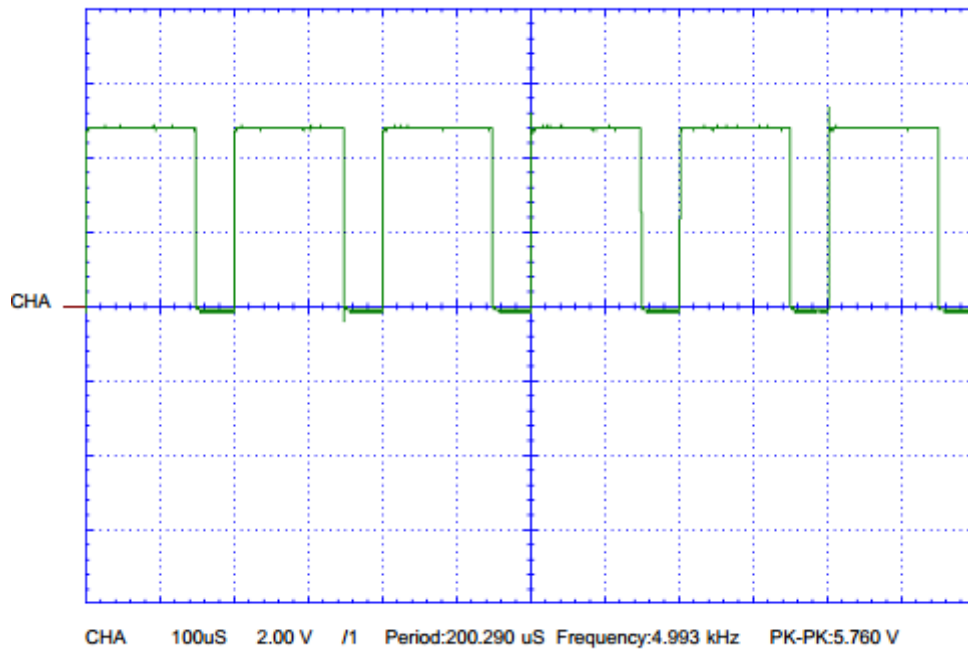


(b)

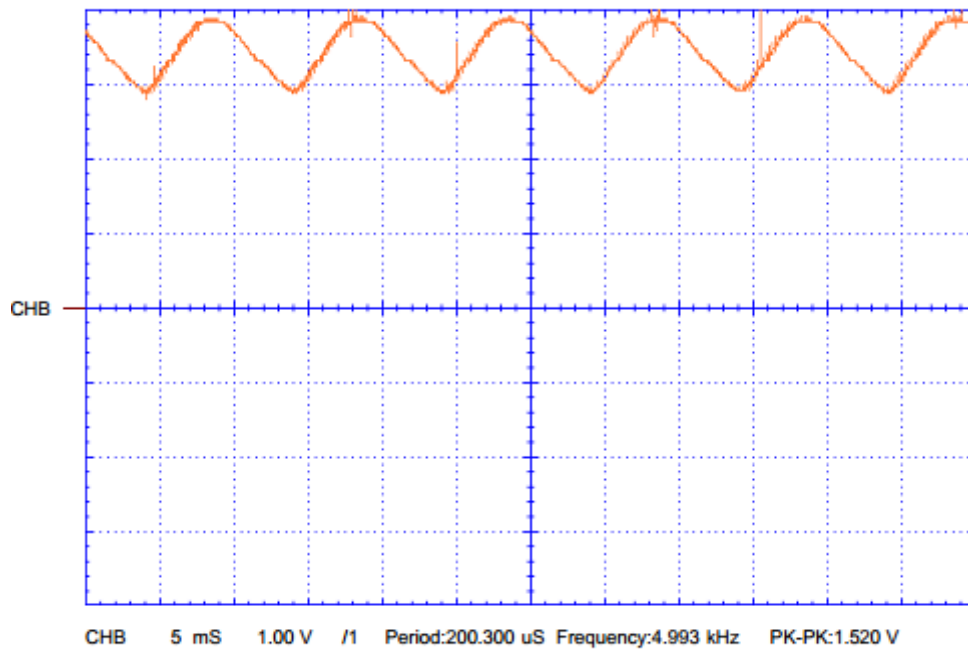


(c)

Figure 8.4 Waveforms of Oscilloscope for modified input switched AC to DC converter for 50% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.

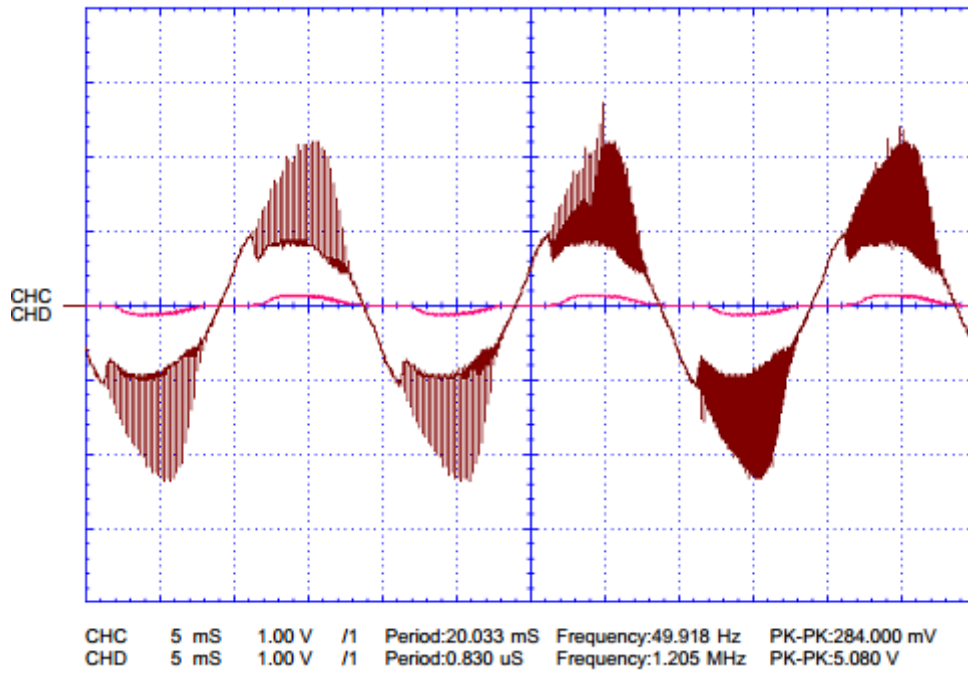


(a)



(b)





(c)

Figure 8.5 Waveforms of Oscilloscope for modified input switched AC to DC converter for 75% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.

Table 8.2 Results of the experimentation of the modified input switched AC to DC boost converter.

DC	$V_{in}$ (RMS)	$V_{OAV}$ (Simulation)	$V_{OAV}$ (Practical)
0.25	10.78	25.123	23.78
0.50	10.78	27.563	28.62
0.75	10.78	26.763	35.49

Table 8.3 Comparison of performance parameters of the modified input switched AC to DC boost converter for  $D = 0.75$ .

Parameters	Simulation	Experimentation
$V_{rms}$	10.607	10.67
$I_{rms}$	2.2465	3.35
$V_{oav}$	26.763	35.44
$PF_i$	0.564	0.707
$P_{in}$	13.435	25.3
$\% \eta$	53.310	49.644

## 8.2 Experimental Results for Modified Input Switched AC to DC SEPIC Converter.

The circuit diagram of the implemented converter is shown in following Figure 8.6. Parameters used in the circuit are provided in Table 8.4. A photo of the laboratory set up is given in Figure 8.7. Typical gate pulse generated to turn the switch ON/OFF is shown in Figure 8.8 (a), whereas the output voltage and input voltage-input current are shown in Figure 8.8 (b) and (c) respectively for the circuit without feedback control for 25 percent duty cycle. Similar waveforms are shown in Figures 8.9 (a)-(c) and 8.10 (a)-(c) for 50 percent and 75 percent duty cycles respectively. The average output voltage and the performance parameters obtained from the experimentation are compared with the simulated results in Table 8.5 and Table 8.6 respectively.

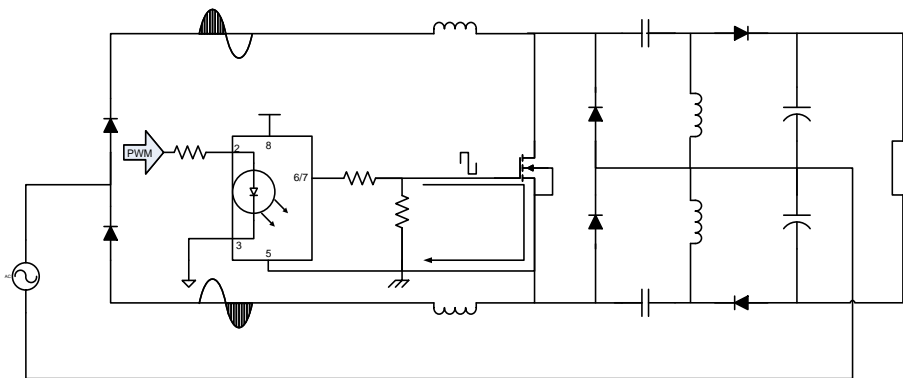


Figure 8.6 The equivalent circuit of experimental set up done in Laboratory on single phase modified input switched AC to DC SEPIC converter.

Table 8.4 Parameters of circuit of Figure 8.6 for experimental set up.

Nominal input ac source voltage, $V_I$	15V Peak
Line frequency, $f$	50 Hz
Switching Frequency, $f_s$	5 kHz
Inductors, $L_1, L_2$	4.45 mH
Capacitors, $C_1, C_2$	305 $\mu$ F
Resistor, $R_o$	100 $\Omega$
Diode	MUR3060PT
MOSFET	IRFP460

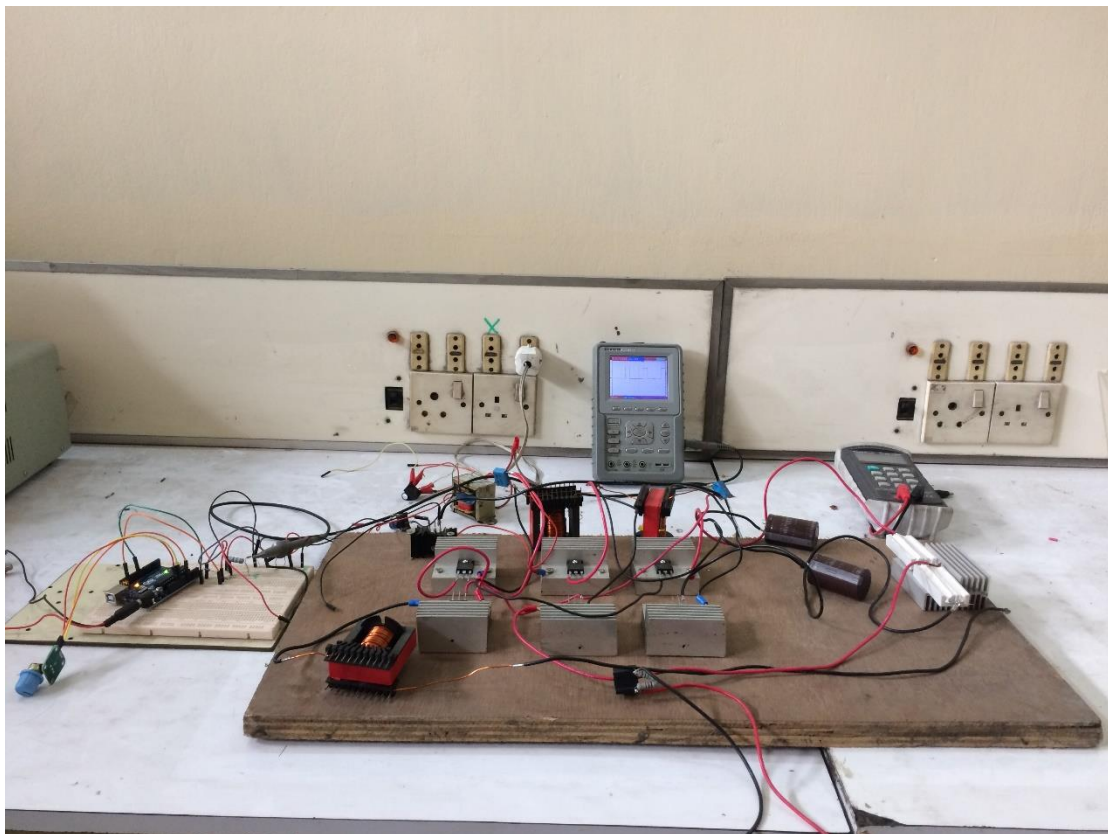
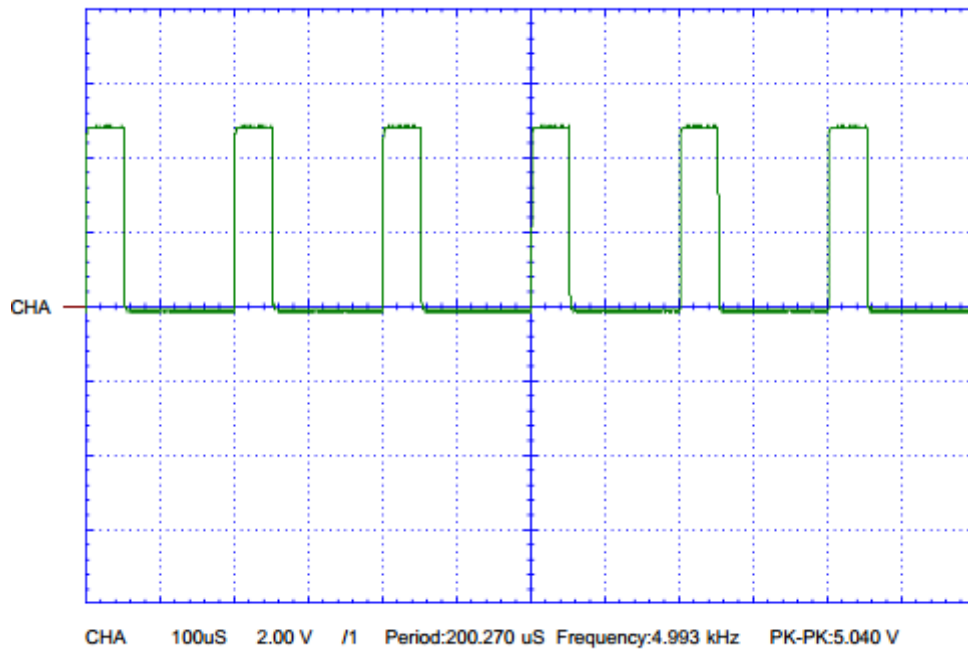
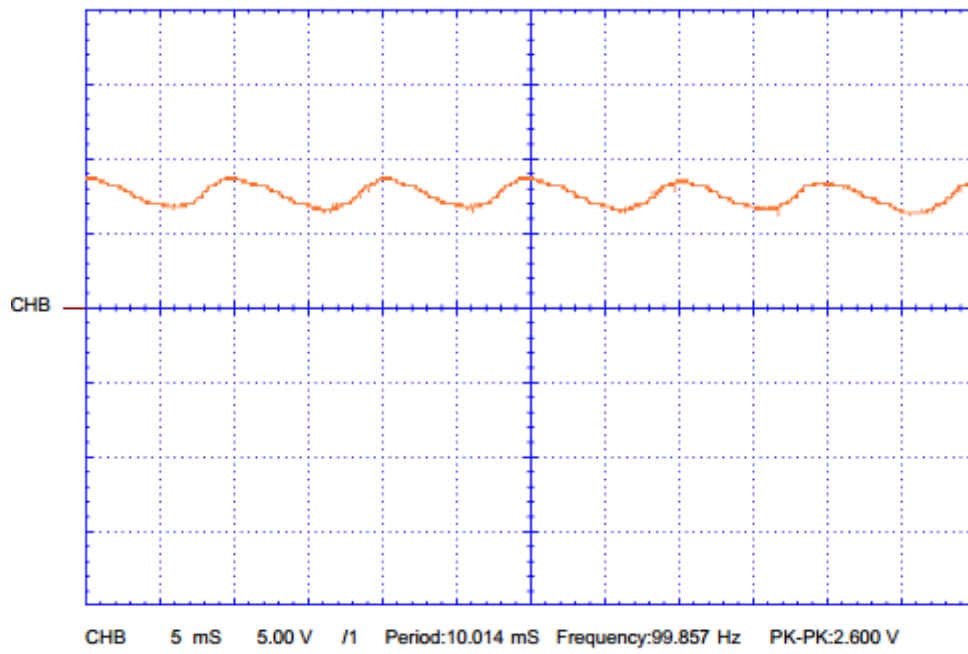


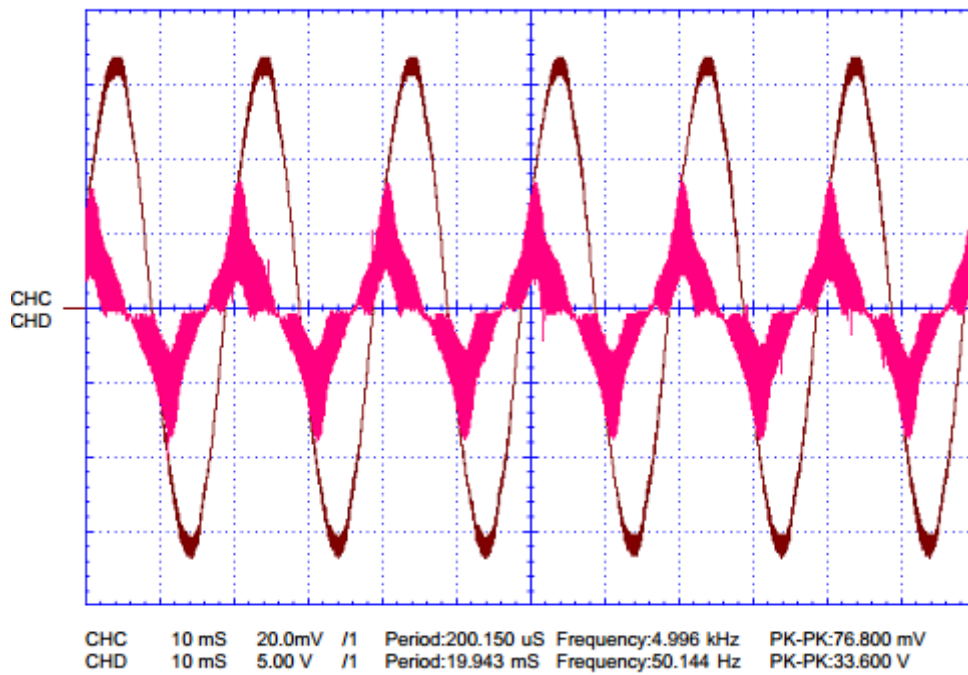
Figure 8.7 The experimental set up done in laboratory for SEPIC converter.



(a)

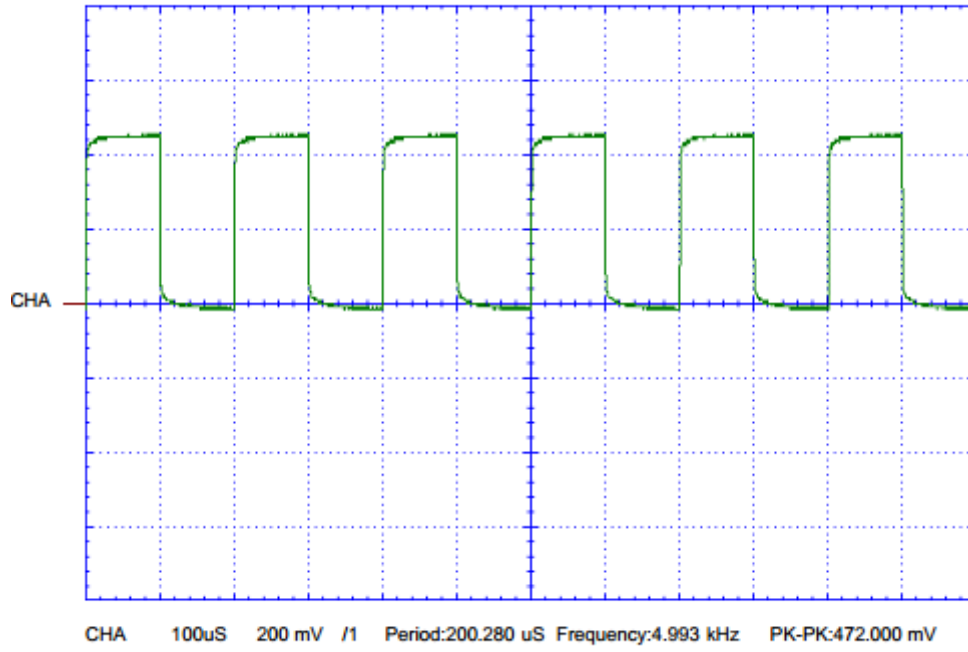


(b)

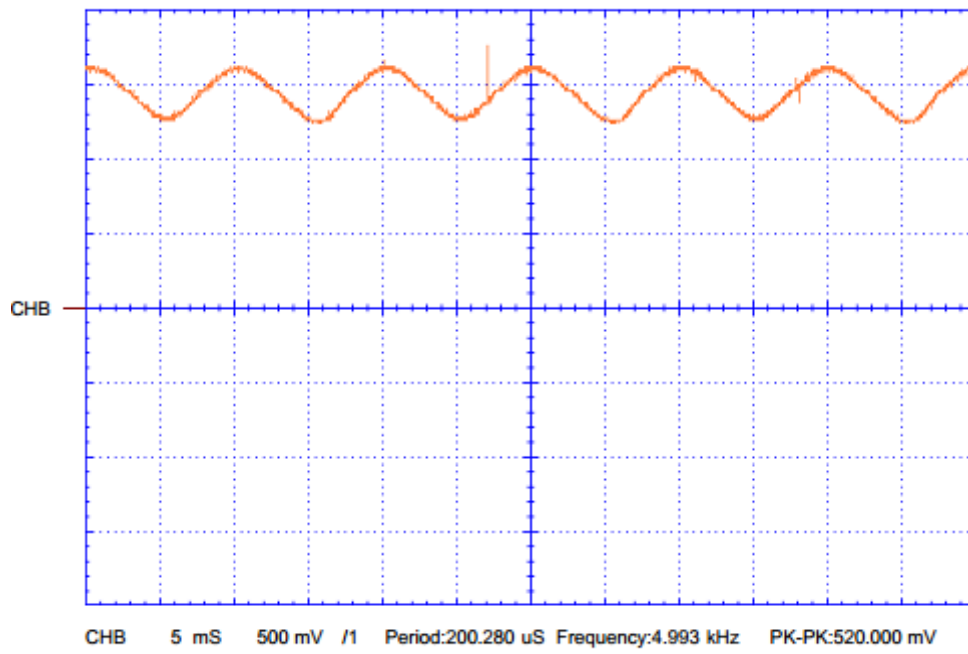


(c)

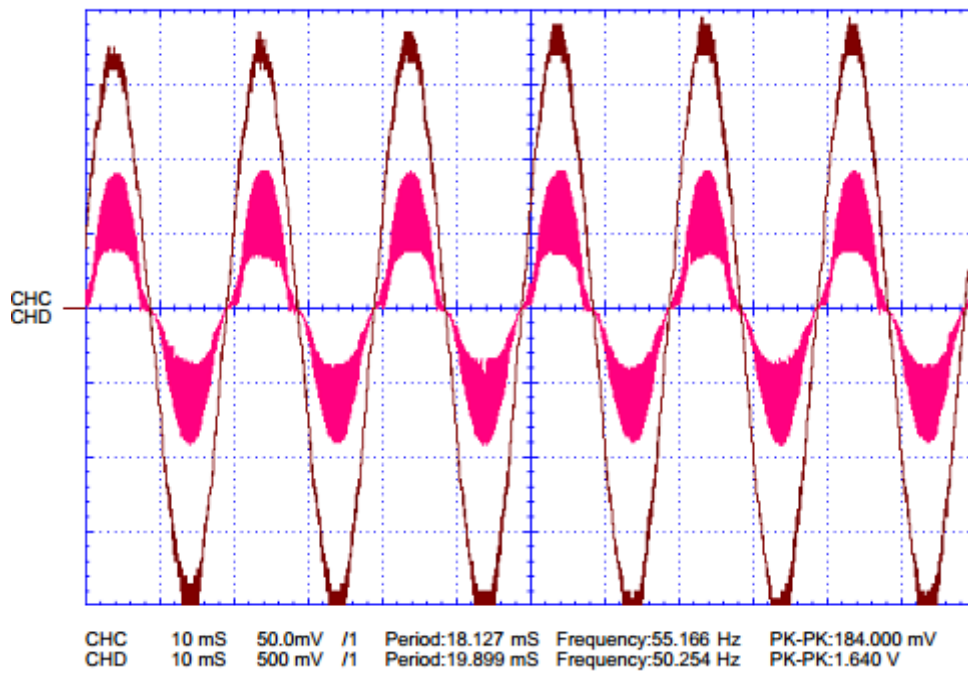
Figure 8.8 Waveforms of Oscilloscope for modified input switched AC to DC converter for 25% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.



(a)

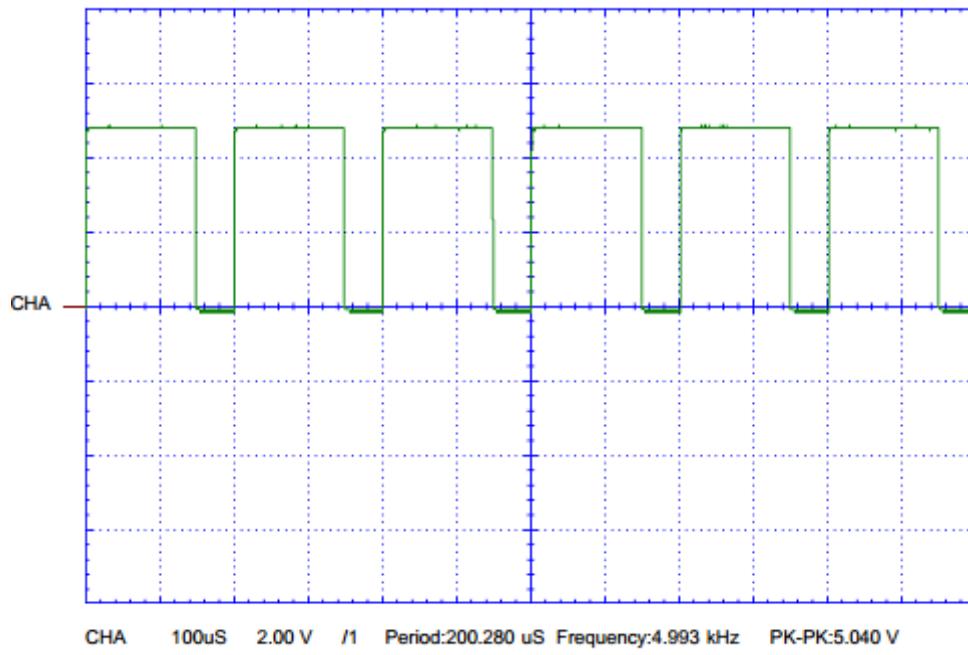


(b)

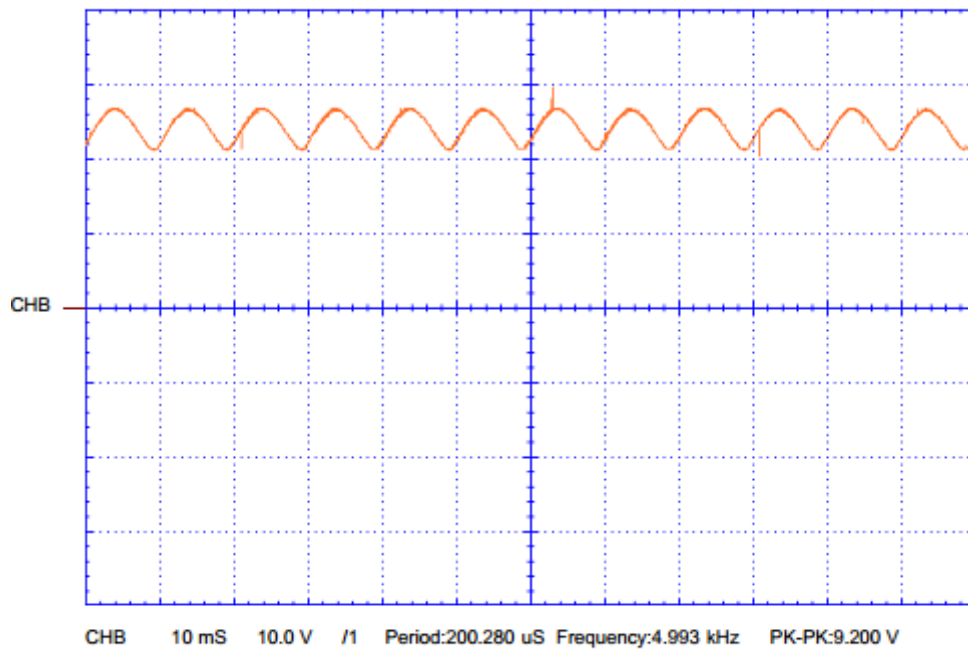


(c)

Figure 8.9 Waveforms of Oscilloscope for modified input switched AC to DC converter for 50% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.

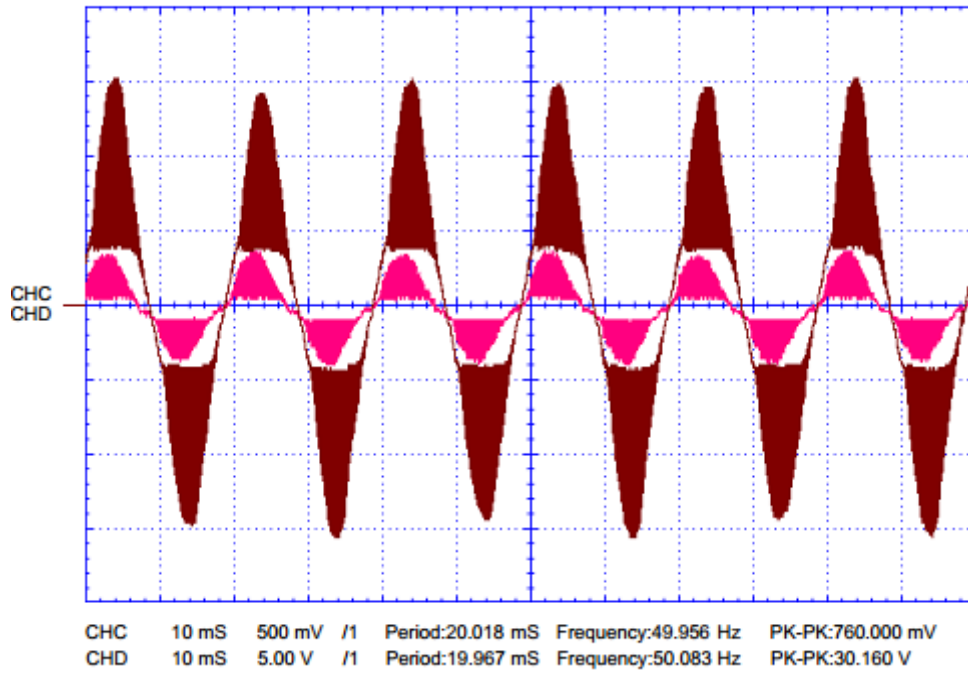


(a)



(b)





(c)

Figure 8.10 Waveforms of Oscilloscope for modified input switched AC to DC converter for 75% duty cycle: (a) Switching pulses (b) Output Voltage (c) Input voltage-current.

Table 8.5 Results of the experimentation of the modified input switched AC to DC SEPIC converter

DC	$V_{in}$ (RMS)	$V_{OAV}$ (Simulation)	$V_{OAV}$ (Practical)
0.25	10.78	6.95	7.59
0.50	10.78	15.07	15.02
0.75	10.78	29.31	24.41

Table 8.6 Comparison of performance parameters of the modified input switched AC to DC boost converter for  $D = 0.50$ .

Parameters	Simulation	Experimentation
$V_{rms}$	10.607	10.770
$I_{rms}$	0.324	0.326
$V_{oav}$	15.446	15.240
$PF_i$	0.953	0.968
$P_{in}$	3.276	3.40
$\% \eta$	72.837	68.311

### 8.3 Discussions

One of the problem in experimentation is the availability of the resources in Bangladesh. The experimental set up is established with available components and with a reduced input voltage environment. Therefore to compare the results with the simulated values, the simulation is repeated creating similar environment. In both experimental setup, the obtained average output voltage was very close to the simulated values. The value differed at high duty cycle (above 75%) due to non-ideal behaviour of the circuit components. One of the major problem was to find appropriate inductor for the modified input switched boost circuit. The conversion efficiency for the boost configuration from the experimental set-up (49.644%) is comparable with simulated value (53.310%). Low efficiency is due to open loop operation in practice and its counterpart in theoretical study.

The modified input switched SEPIC converter shown non-ideal behaviour due to the variation of the coupling capacitor. The input current and the voltage is almost in phase. The power factor calculated at 50% duty cycle is almost unity (0.968). The SEPIC converters result needed to be evaluated for low duty cycle, since the power consumption was so small it was not possible to show that result. Instead the result was compared for 50% duty cycle. The conversion efficiency from the experimental set-up (68.311%) is comparable with simulated value (72.837%). Further improvement in power conversion will result if feedback controller is used.

## Chapter 9

### Summary and Conclusion

High conversion efficiency, low input current THD and high input power factor are the criteria necessary in design and implementation of single phase AC to DC converter. Review of literature enables us to conclude that, new generation input switched AC to DC converters (for both step-up and step-down application) has the potential to fulfil the required criteria of high conversion efficiency at extreme high and low duty cycle of operation.

Conventional single phase AC to DC converters using switch mode topologies (e.g boost, Buck-Boost, Ćuk, SEPIC) have been proposed that suffers due to low conversion efficiency at extremely high and low duty cycle. This is because of the fact that, the gain and the attenuation property of the converter differs from ideal behaviour due to the internal resistance of the inductor and non-linear behaviour of the switch in achieving extreme high gain or extreme attenuation. The deviations from ideal behaviour is tackled by fly-back and feed-forward converters using transformers for step-up or step-down prior to DC to DC or AC to DC conversion.

The use of transformer for gain and attenuation can be replaced by hybrid diode-capacitor or diode-inductor circuits. Investigation is carried on hybrid DC to DC converter to have better efficiency at extreme duty cycles. Hybrid DC to DC converter has shown improved efficiency compared to the conventional DC to DC converter specifically at extremely high and extremely low duty cycle of operation. In addition, it is a prerequisite for AC to DC conversion to maintain high power factor and low input current THD. In single phase AC to DC conversion to adopt power factor correction and to keep the input current THD low, input side of the converter should have boost topology. So in single phase AC to DC converter for step-up or step-down conversion, converters like Boost, SEPIC or Ćuk has to be used. Again the direct input current switching also makes it easy to maintain high input power factor and low input current THD. Therefore new input switched hybrid topologies are designed by modifying boost and SEPIC topology for improved power quality. The Ćuk topology is avoided since it

has negative output voltage. The encouraging performance of hybrid DC to DC converter provided the motivation to design single phase input switched hybrid AC to DC converter for extreme duty cycle of operation.

In chapter 1, an extensive literature survey on single phase AC to DC converter is carried out. A critical review of different types of converters with various control structures provide a clear picture associated with AC to Dc converters. The problem in AC to DC conversion is identified and solution using different passive networks has been suggested.

In chapter 2, the background of the identified problem is described and the performance parameters are discussed. Investigation on hybrid DC to DC converters are carried out. The converters offered higher conversion efficiency at extreme duty cycle of operation. The study provided the motivation to carry out the investigation with single phase AC to DC converters using hybrid networks.

In chapter 3, the working principle of the conventional and proposed single phase AC to DC boost converters are discussed with necessary voltage gain relations. Open loop investigation is carried out. The proposed converters offered higher conversion efficiency at high voltage gains.

In chapter 4, the feedback analysis of the proposed single phase AC to DC boost converters are carried out. The simulation results ensured high input power factor and low input current THD. The feedback controller is also tested with a sudden load change to maintain constant output voltage.

In chapter 5, single phase step-down AC to DC SEPIC converters are proposed. The working principle of the conventional and the proposed converters are explained in detail. The necessary voltage gain relations are also derived. The open loop simulation results showed that, the proposed converters offered higher conversion efficiency at extremely low voltage gain.

In chapter 6, The feedback analysis of the proposed SEPIC converters are carried out with an objective to maintain high input power factor and low input current THD.

Dynamic analyses are also carried out to maintain constant output voltage with sudden load change.

Chapter 7 mainly concentrates on the derivation and design of the two loop feedback control system for the proposed output switched AC to DC converter. The small-signal of the converter is derived. The two loop feedback control is designed with example. Simulation results of the proposed converter with feedback validated the precision of the design.

Chapter 8 describes the experimental implementation of the proposed modified input-switched Boost and SEPIC converter. The experimental results have been presented which verify the simulated performances of the corresponding converter with similar operation condition.

## **9.1 Major Contributions of the Thesis**

The major contributions of the thesis are:

- Input switched boost converters are designed to achieve high conversion efficiency for extreme high voltage gain using passive networks to provide additional voltage gain at relatively low duty cycle.
- Input switched SEPIC converters are designed using passive voltage divider networks to achieve low voltage gain at relatively high duty cycle. Thus conversion efficiency is achieved at extremely low voltage gain.
- Mathematical formulation of the average output voltage of the proposed converters are developed to compare with the simulated results.
- The proposed converters are investigated under feedback control to achieve near unity input power factor and to maintain the sinusoidal shape of the input current.
- The proposed converters are forced to maintain constant output voltage under variable load condition with suitable feedback control.
- A detailed design of the feedback control for a proposed converter is formulated and verified by simulation.

- Experimental implementation of the proposed converters validated the simulation results.

## 9.2 Conclusion

Some of the major conclusions of the study are

- The proposed boost converters are designed for high voltage gain at better conversion efficiency than conventional AC to DC converters. The converter can be used for high voltage DC systems or in renewable energy application where the generated voltage is very low and needs a high voltage gain.
- The proposed SEPIC converters are designed for low voltage gain at better conversion efficiency than conventional AC to DC converters. The step-down converter is used vast applications like low voltage LED lighting and power supplies for modern day equipment.
- The proposed boost converters offer better performance compared to the conventional counterpart for large voltage gain. The best of them is the modified input switched AC to DC boost converter. The converter shows 95.984% of converter efficiency in order to achieve a high voltage of 1000V, which is higher than the other converters under study (conventional and proposed). Higher voltage gain were achieved at better input current THD and input power factor by feedback control of the proposed converters. This is additional design criterion for AC to DC converters over DC to DC converters counterpart.
- Experimentation is done with this topology to validate the simulation result. Then the proposed boost converters are investigated under feedback condition to improve the input power factor and to keep the input current THD within the prescribed limits. Feedback analysis is also carried out to check whether the converters can track reference output voltage for variation in load. Acceptable results are achieved.
- The proposed SEPIC converters offer better conversion efficiency at very low voltage gain compared to the conventional ones. Modified input switched AC to DC SEPIC converter offered highest efficiency of 66.593% in order to achieve a voltage gain of 0.133.

- Experimentation is done to validate the outcome. Acceptable performance (high input power factor and low input current THD) are also achieved by investigating the proposed converters under feedback condition. The converters also can maintain almost constant voltage for load variation.
- Investigation of the input switched hybrid AC to DC converter topologies give simple, cost effective, high performance solution suitable for AC to DC application. The proposed converters will be efficient, reliable, compact, robust and easy to control converters.

### **9.3 Future Work**

Proposed single phase AC to DC converters with high conversion efficiency at extreme conditions have been simulated and practically implemented for low voltage low power prototype setup. As a future work converter design, operation and simulation at working voltage, current and power are recommended. The voltage gain of the proposed boost and SEPIC converters are derived. The voltage gain of SEPIC converters differ from derived expressions due to non-linear effect of the coupling capacitor. Therefore circuit and device analysis may be carried out in detail to obtain ideal and practical voltage/current gain expression of the proposed circuits. Appropriate expressions need to be derived for counting switching and conduction losses of the semiconductor devices and stray losses of the energy storage components of the circuit. Available literature does not involve the losses in circuit and feedback development phases. So desired result may not be achieved. Three phase version of the proposed converters are also recommended to implement in future.

## References

- [1] R. W. Erickson, D. Maksimovic, and ebrary Inc. (2001). *Fundamentals of power electronics* (2nd ed.). <http://site.ebrary.com/lib/georgemason/Doc?id=10067440>
- [2] B. K. Bose, *Modern power electronics and AC drives*. Upper Saddle River, NJ: Prentice Hall PTR, 2002.
- [3] S. Buso and P. Mattavelli, *Digital control in power electronics*, 1st ed. San Rafael, Calif.: Morgan & Claypool Publishers, 2006.
- [4] D. W. Hart, *Power electronics*. New York: McGraw-Hill, 2011.
- [5] B. W. Kennedy. (2000). *Power quality primer*. Available: <http://www.loc.gov/catdir/toc/mh021/00033257.html>
- [6] N. Mohan, *Power electronics : a first course*. Hoboken, N.J.: Wiley, 2012.
- [7] N. Mohan, T. M. Undeland, and W. P. Robbins. (2003). *Power electronics : converters, applications, and design* (3rd ed.).
- [8] D. O. Neacsu. (2006). *Power-switching converters medium and high power*.
- [9] M. H. Rashid, *Power electronics : circuits, devices, and applications*, 3rd ed. Upper Saddle River, N.J.: Pearson/Prentice Hall, 2004.
- [10] T. L. Skvarenina, *The power electronics handbook*. Boca Raton, Fla.: CRC Press, 2002.
- [11] K. Sozański. *Digital Signal Processing in Power Electronics Control Circuits*. Available: <http://proxy.lib.uiowa.edu/login?url=http://dx.doi.org/10.1007/978-1-4471-5267-5>
- [12] K. C. Wu, *Switch-mode power converters : design and analysis*. Amsterdam ; Boston: Elsevier Academic Press, 2006.
- [13] M. Alam, W. Eberle, and N. Dohmeier, "An inrush limited, surge tolerant hybrid resonant bridgeless PWM AC-DC PFC converter," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 5647-5651.
- [14] X. Li, S. Dusmez, B. Akin, and K. Rajashekara, "Capacitor voltage balancing control of a fully integrated three-level isolated AC-DC PFC converter for reliable operations," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 534-539.
- [15] D. D. C. Lu, D. K. W. Cheng, and Y. S. Lee, "Storage capacitor voltage control of single-stage AC-DC PFC converter," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 3794-3797 Vol.5.
- [16] Y. Lung-Sheng and C. En-Chih, "Analysis of Modified Single-Phase PFC AC-DC Buck-Boost Converter," in *Robot, Vision and Signal Processing (RVSP), 2011 First International Conference on*, 2011, pp. 272-275.
- [17] Y. Lung-Sheng and L. Tsorng-Juu, "Analysis and design of a novel single-phase PFC AC-DC step-up/down converter," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, 2011, pp. 1470-1474.



- [18] M. Mahesh and A. K. Panda, "A high performance single-phase AC-DC PFC boost converter with passive snubber circuit," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 2888-2894.
- [19] M. Mahesh, A. K. Panda, and B. K. Keshavan, "Analysis of a single-phase AC-DC PFC boost converter with fast dynamic response," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*, 2012, pp. 1-5.
- [20] F. Musavi, W. Eberle, and W. G. Dunford, "Efficiency evaluation of single-phase solutions for AC-DC PFC boost converters for plug-in-hybrid electric vehicle battery chargers," in *Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE*, 2010, pp. 1-6.
- [21] M. Narimani and G. Moschopoulos, "Analysis and design of a single-stage three-level PFC AC-DC-converter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 1134-1141.
- [22] M. Narimani and G. Moschopoulos, "Analysis and design of a new three-level PFC AC-DC converter," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 4808-4813.
- [23] M. Narimani and G. Moschopoulos, "A new interleaved three-phase single-stage PFC AC-DC converter with flying capacitor," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 894-899.
- [24] Y. Ohnuma and J. Itoh, "A novel single-phase buck PFC AC-DC converter using an active buffer," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 4223-4229.
- [25] C. S. Postiglione, A. L. Fuerback, D. C. Martins, A. J. Perin, and C. B. Nascimento, "Single-stage PFC AC-DC converter based on serial-interleaved boost," in *Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference on*, 2012, pp. 1-8.
- [26] K. Rezaei, N. Golbon, and G. Moschopoulos, "A new control scheme for an AC-DC single-stage buck-boost PFC converter with improved output ripple reduction and transient response," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 1866-1873.
- [27] P. Das, M. Pahlevaninezhad, J. Drobniak, G. Moschopoulos, and P. K. Jain, "A Nonlinear Controller Based on a Discrete Energy Function for an AC/DC Boost PFC Converter," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 5458-5476, 2013.
- [28] Y. Kai, R. Xinbo, M. Xiaojing, and Y. Zhihong, "Reducing Storage Capacitor of a DCM Boost PFC Converter," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 151-160, 2012.
- [29] O. Chang-Yeol, K. Dong-Hee, W. Dong-Gyun, S. Won-Yong, K. Yun-Sung, and L. Byoung-Kuk, "A High-Efficient Nonisolated Single-Stage On-Board Battery Charger for Electric Vehicles," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 5746-5757, 2013.
- [30] M. SangCheol, K. Gwan-Bon, and M. Gun-Woo, "A New Control Method of Interleaved Single-Stage Flyback AC-DC Converter for Outdoor LED

- Lighting Systems," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4051-4062, 2013.
- [31] T. Fengfeng and F. C. Lee, "A critical-conduction-mode single-stage power-factor-correction electronic ballast," in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, 2000, pp. 603-609 vol.1.
- [32] B. Jongbok, S. Jongwon, P. Jang, and C. Bohyung, "A critical conduction mode bridgeless flyback converter," in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 487-492.
- [33] A. H. Abedin, M. H. Rahaman, M. M. S. Khan, M. A. Choudhury, M. Rubaiyat, T. Hossain, *et al.*, "Input switched single phase high performance bridgeless C&#x00FB;K AC-DC converter," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*, 2012, pp. 1-5.
- [34] M. M. U. Alam, W. Eberle, D. Gautom, and F. Musavi, "A soft-switching bridgeless AC-DC power factor correction converter for off-road and neighborhood electric vehicle battery charging," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 103-108.
- [35] H.-S. Cho, J.-S. Yoo, J.-Y. Choi, M.-K. Yang, and W.-Y. Choi, "Bridgeless half-bridge AC-DC converter with series-connected two transformers," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 3241-3245.
- [36] A. A. Fardoun, E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali, "New &#x201C;real&#x201D; bridgeless high efficiency AC-DC converter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 317-323.
- [37] M. R. T. Hossain, M. H. Rahaman, M. S. Arifin, M. A. Choudhury, A. H. Abedin, and M. N. Uddin, "Input switched single phase high performance bridgeless AC-DC Zeta converter," in *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*, 2012, pp. 1-5.
- [38] M. Mahmood, C. Huang-Jen, L. Yu-Kang, N. Quang Trong, P. Phu Hieu, and I. Purnama, "Isolated dual boost bridgeless power factor correction AC-DC converter," in *Future Energy Electronics Conference (IFEEC), 2013 1st International*, 2013, pp. 465-470.
- [39] M. Muntasir UI Alam, W. Eberle, and F. Musavi, "A hybrid resonant bridgeless AC-DC power factor correction converter for off-road and neighborhood electric vehicle battery charging," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 1641-1647.
- [40] M. R. Sahid and A. H. M. Yatim, "An isolated bridgeless AC-DC converter with high power factor," in *Power and Energy (PECon), 2010 IEEE International Conference on*, 2010, pp. 791-796.
- [41] M. R. Sahid, A. H. M. Yatim, and T. Taufik, "A new AC-DC converter using bridgeless SEPIC," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 286-290.
- [42] C. Woo-Young, C. Jae-Yeon, and Y. Ju-Seung, "Single-stage bridgeless three-level AC/DC converter with current doubler rectifier," in *Power Electronics and*

- ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 2704-2708.
- [43] T. Yichao and A. Khaligh, "A novel bridgeless high-frequency resonant AC-DC converter," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 125-130.
- [44] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC&#x2013;DC PWM Converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 55, pp. 687-696, 2008.
- [45] M. Arias, Ferna, x, M. ndez Diaz, D. G. Lamar, D. Balocco, *et al.*, "High-Efficiency Asymmetrical Half-Bridge Converter Without Electrolytic Capacitor for Low-Output-Voltage AC&#x2013;DC LED Drivers," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 2539-2550, 2013.
- [46] M. Arias, M. Fernandez, J. E. Rodriguez, D. G. Lamar, and J. Sebastian, "Digital implementation of the feedforward loop of the asymmetrical half-bridge converter for LED lighting applications," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 3465-3472.
- [47] R. Baca Arroyo, G. R. Paredes, and R. Pena Sierra, "AC-DC Power-Factor-Corrected Switching Converter Based on Air-Gap Transformer and Pulse Position Modulator for Lighting Applications," in *Electronics, Robotics and Automotive Mechanics Conference (CERMA), 2011 IEEE*, 2011, pp. 296-300.
- [48] S. Chenh, M. Sautreuil, D. Riu, Retie, x, and N. re, "Quasi-static decoupled load flow modelling of a power supply network with AC-DC converters applied to light rail system," in *Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1-10.
- [49] C. Chun-An, C. Hung-Liang, and C. Tsung-Yuan, "A novel single-stage high-power-factor LED street-lighting driver with coupled inductors," in *Industry Applications Society Annual Meeting, 2013 IEEE*, 2013, pp. 1-7.
- [50] C. Chun-An, C. Hung-Liang, and C. Tsung-Yuan, "A Novel Single-Stage High-Power-Factor LED Street-Lighting Driver With Coupled Inductors," *Industry Applications, IEEE Transactions on*, vol. 50, pp. 3037-3045, 2014.
- [51] K. Jun-Ho, D.-Y. Cho, J.-P. Hong, and M. Gun-Woo, "Boost integrated flyback AC-DC converter with valley fill circuit for LED light bulb," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, 2012, pp. 457-462.
- [52] D. G. Lamar, M. Arias, M. M. Hernando, and J. Sebastian, "Using the loss-free resistor concept to design a simple ac-dc HB-LED driver for retrofit lamp applications," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 117-124.
- [53] C. Park, K. Jang, S. Woo, H. Yu, J. Lee, and J. Choi, "AC-DC converter using  $V_{GS}$ -multiplier circuit for LED lighting applications," *Electronics Letters*, vol. 49, pp. 984-985, 2013.
- [54] W. Shu, R. Xinbo, Y. Kai, and Y. Zhihong, "A flicker-free electrolytic capacitor-less ac-dc LED driver," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2318-2325.

- [55] B. Singh and A. Shrivastava, "Buck converter-based power supply design for low power light emitting diode lamp lighting," *Power Electronics, IET*, vol. 7, pp. 946-956, 2014.
- [56] F. Weifeng, H. Yongzhi, and F. G. Shi, "Packaging and AC powering of LED array," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 512-514.
- [57] M. Arias, M. Fernandez, D. G. Lamar, D. Balocco, A. Diallo, and J. Sebastian, "Self-driven synchronous-rectification technique for the Asymmetrical Half-Bridge converter in led lighting applications," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 862-869.
- [58] E. Hyunchul, L. Chun-Ching, Y. Ta-Yung, and Y. Seunguk, "Design optimization of TRIAC-dimmable AC-DC converter in LED lighting," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 831-835.
- [59] E. Paul, "A single stage high power factor supply for HB-LEDs," in *Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), 2011 International Conference on*, 2011, pp. 727-732.
- [60] M. SangCheol, K. Gwan-Bon, and M. Gun-Woo, "An interleaved single-stage flyback AC-DC converter with wide output power range for outdoor LED lighting system," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 823-830.
- [61] A. Idris, R. Baharom, N. R. Hamzah, and M. K. Hamzah, "Controlled AC-DC converter fed permanent magnet DC motor using single-phase matrix converter," in *Business, Engineering and Industrial Applications (ISBEIA), 2012 IEEE Symposium on*, 2012, pp. 7-12.
- [62] A. Idris, R. Baharom, N. R. Hamzah, and M. K. Hamzah, "Controlled AC-DC converter fed permanent magnet DC motor using single-phase matrix converter," in *Power Engineering and Optimization Conference (PEOCO), 2013 IEEE 7th International*, 2013, pp. 764-769.
- [63] B. H. Khan, S. R. Droadla, and G. K. Dubey, "A three-phase AC-DC GTO thyristor converter employing equal pulse width modulation (EPWM) (for DC motor control)," in *Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE*, 1989, pp. 891-900 vol.1.
- [64] S. Nakhaee and A. Jalilian, "Application of pulse multiplication in autotransformer based AC-DC converters for direct torque control induction motor drives," in *Harmonics and Quality of Power (ICHQP), 2010 14th International Conference on*, 2010, pp. 1-6.
- [65] S. Samanta, T. Tanesha, and D. Vijayakumar, "Design and simulation of speed controller using ac-dc buck boost converter for dc motor drive with soft starter," in *Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on*, 2013, pp. 1230-1237.
- [66] B. Singh, G. Bhuvaneswari, and V. Garg, "Scott-Connected Autotransformer Based Multipulse AC-DC Converters for Power Quality Improvement In Vector Controlled Induction Motor Drives," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 1491-1496.

- [67] B. Singh, G. Bhuvaneswari, and V. Garg, "Eighteen-Pulse AC-DC Converter for Harmonic Mitigation in Vector Controlled Induction Motor Drives," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 1514-1519.
- [68] B. Singh, G. Bhuvaneswari, and V. Garg, "Nine-Phase AC-DC Converter for Vector Controlled Induction Motor Drives," in *INDICON, 2005 Annual IEEE*, 2005, pp. 137-142.
- [69] B. Singh, G. Bhuvaneswari, and V. Garg, "Passive Waveshaping Techniques in AC-DC Converters Feeding Vector Controlled Induction Motor Drives," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, 2005, pp. 966-971.
- [70] B. Singh, G. Bhuvaneswari, and V. Garg, "A Twelve-Phase AC-DC Converter for Power Quality Improvement in Direct Torque Controlled Induction Motor Drives," in *Industrial Electronics and Applications, 2006 1ST IEEE Conference on*, 2006, pp. 1-7.
- [71] B. Singh, G. Bhuvaneswari, and V. Garg, "An 18-Pulse AC-DC Converter for Power Quality Improvement in Vector Controlled Induction Motor Drives," in *Industrial Electronics and Applications, 2006 1ST IEEE Conference on*, 2006, pp. 1-6.
- [72] B. Singh, G. Bhuvaneswari, and V. Garg, "Harmonic mitigation using 12-pulse AC-DC converter in vector-controlled induction motor drives," *Power Delivery, IEEE Transactions on*, vol. 21, pp. 1483-1492, 2006.
- [73] B. Singh, G. Bhuvaneswari, V. Garg, A. Chandra, and K. Al-Haddad, "A Tapped Delta Autotransformer Based 24-Pulse AC-DC Converter for Variable Frequency Induction Motor Drives," in *Industrial Electronics, 2006 IEEE International Symposium on*, 2006, pp. 2046-2051.
- [74] B. Singh and S. Gairola, "Design and Development of a 36-Pulse AC-DC Converter for Vector Controlled Induction Motor Drive," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, 2007, pp. 694-701.
- [75] B. Singh, V. Garg, and G. Bhuvaneswari, "Design and Development of Autotransformer Based 24-Pulse AC-DC Converter fed Induction Motor Drive," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, 2007, pp. 73-80.
- [76] M. R. Subbamma, M. L. Dwarakanath, P. B. Chakravarthy, and V. Madhusudhan, "Implementation of performance analysis of 18-pulse AC-DC converter fed switched reluctance motor drives to robotics," in *Emerging Trends in Robotics and Communication Technologies (INTERACT), 2010 International Conference on*, 2010, pp. 154-157.
- [77] B. Singh, G. Bhuvaneswari, and V. Garg, "Power-quality improvements in vector-controlled induction motor drive employing pulse multiplication in AC-DC converters," *Power Delivery, IEEE Transactions on*, vol. 21, pp. 1578-1586, 2006.
- [78] B. Singh, G. Bhuvaneswari, and V. Garg, "T-connected autotransformer-based 24-pulse AC-DC converter for variable frequency induction motor drives," *Energy Conversion, IEEE Transactions on*, vol. 21, pp. 663-672, 2006.

- [79] B. Singh, G. Bhuvaneswari, and V. Garg, "Autotransformer Based Nine-Phase AC-DC Converter for Harmonic Mitigation in Induction Motor drives," in *Industrial Electronics, 2006 IEEE International Symposium on*, 2006, pp. 2439-2444.
- [80] B. Singh, G. Bhuvaneswari, V. Garg, and A. Chandra, "Star connected autotransformer based 30-pulse AC-DC converter for power quality improvement in vector controlled induction motor drives," in *Power India Conference, 2006 IEEE*, 2006, p. 6 pp.
- [81] B. Singh, G. Bhuvaneswari, V. Garg, and S. Gairola, "Pulse multiplication in AC-DC converters for harmonic mitigation in vector-controlled induction motor drives," *Energy Conversion, IEEE Transactions on*, vol. 21, pp. 342-352, 2006.
- [82] B. Singh and S. Gairola, "A 40-Pulse AC--DC Converter Fed Vector-Controlled Induction Motor Drive," *Energy Conversion, IEEE Transactions on*, vol. 23, pp. 403-411, 2008.
- [83] B. Singh, B. P. Singh, and S. Dwivedi, "Improved power quality AC-DC flyback converter for variable speed permanent magnet synchronous motor drive," in *Power India Conference, 2006 IEEE*, 2006, p. 8 pp.
- [84] C. Haixian, Y. Ito, K. Nakano, N. Yokoyama, and B. Hong, "100kVA electric vehicle charger using resonant buck-type AC-DC converter," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, 2012, pp. 416-421.
- [85] F. Jauch and J. Biela, "Single-phase single-stage bidirectional isolated ZVS AC-DC converter with PFC," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. LS5d.1-1-LS5d.1-8.
- [86] S. Lisheng, A. Meintz, and M. Ferdowsi, "Single-phase bidirectional AC-DC converters for plug-in hybrid electric vehicle applications," in *Vehicle Power and Propulsion Conference, 2008. VPPC '08. IEEE*, 2008, pp. 1-5.
- [87] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase AC-DC power factor corrected boost converter for plug in hybrid electric vehicle battery chargers," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 3588-3595.
- [88] D. O'Sullivan, M. Willers, M. G. Egan, J. G. Hayes, P. T. Nguyen, and C. P. Henze, "Power-factor-corrected single-stage inductive charger for electric-vehicle batteries," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 509-516 vol.1.
- [89] A. K. Verma, B. Singh, and D. T. Shahani, "Grid to vehicle and vehicle to grid energy transfer using single-phase bidirectional AC-DC converter and bidirectional DC-DC converter," in *Energy, Automation, and Signal (ICEAS), 2011 International Conference on*, 2011, pp. 1-5.
- [90] G. Gong, M. L. Heldwein, U. Drofenik, K. Mino, and J. W. Kolar, "Comparative evaluation of three-phase high power factor AC-DC converter concepts for application in future more electric aircrafts," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, pp. 1152-1159 vol.2.
- [91] G. Guanghai, M. L. Heldwein, U. Drofenik, J. Minibock, K. Mino, and J. W. Kolar, "Comparative evaluation of three-phase high-power-factor AC-DC

- converter concepts for application in future More Electric Aircraft," *Industrial Electronics, IEEE Transactions on*, vol. 52, pp. 727-737, 2005.
- [92] B. M. H. Jassim, "SEPIC AC-DC converter for aircraft application," in *Mediterranean Electrotechnical Conference (MELECON), 2014 17th IEEE*, 2014, pp. 12-16.
- [93] Y. Keping, X. Dan, M. F. Rahman, and M. N. Uddin, "Applying Reduced General Direct Space Vector Modulation Approach of AC-AC Matrix Converter Theory to Achieve Direct Power Factor Controlled Three-Phase AC-DC Matrix Rectifier," *Industry Applications, IEEE Transactions on*, vol. 50, pp. 2243-2257, 2014.
- [94] J. C. P. Liu, C. K. Tse, N. K. Poon, Y. M. Lai, and M. H. Pong, "A PFC topology with low input current distortion suitable for aircraft power supplies," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, pp. 166-169 Vol.1.
- [95] S. A. N. Niaki, R. Iravani, and H. Kojori, "A robust commutation circuit for reliable single-step commutation of the matrix converter," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 3349-3355.
- [96] A. N. Arvindan, "Transformer Less Power Transfer at Unity Power Factor via HVDC Link Using Improved Power Quality HCC PWM AC-DC Converter," in *India Conference (INDICON), 2009 Annual IEEE*, 2009, pp. 1-4.
- [97] C. Jaipradidtham and V. Kinnares, "Harmonic Flow Analysis of HVDC Systems for Discrete Wavelet Transform with Advanced of the Harmonic Impedances and Voltage Source Transients Model of AC-DC Converters," in *TENCON 2006. 2006 IEEE Region 10 Conference*, 2006, pp. 1-4.
- [98] Y.-H. Song and A. Johns, *Flexible ac transmission systems (FACTS)*.
- [99] A. Hadri-Hamida, A. Allag, S. M. Mimoune, M. Y. Ayad, M. Becherif, E. Miliani, *et al.*, "Application of an Adaptive Nonlinear Control Strategy to AC-DC-PWM Converter Feeding Induction Heating," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, 2006, pp. 1598-1602.
- [100] J. Mucko, "Parallel resonant inverter with auxiliary AC/DC converter used for induction heating," in *Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop*, 2011, pp. 415-419.
- [101] B. Singh and S. Gairola, "Pulse Doubling in 18-Pulse AC-DC Converters," in *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, 2007, pp. 533-539.
- [102] B. Singh and S. Gairola, "A 28-pulse AC-DC converter for line current harmonic reduction," *Power Electronics, IET*, vol. 1, pp. 287-295, 2008.
- [103] C. Daolian, "Research on single stage combined uninterruptible AC-DC converters with high power factor," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3354-3359.
- [104] K. S. Muhammad, R. Baharom, and M. K. Hamzah, "Advance battery charger topology using SPMC incorporating active power filter," in *Science and Social Research (CSSR), 2010 International Conference on*, 2010, pp. 548-553.
- [105] M. Pahlevaninezhad, P. Das, P. Jain, A. Bakhshai, and G. Moschopoulos, "A self sustained oscillation controlled three level AC-DC single stage converter,"

- in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 1172-1178.
- [106] R. Oruganti and M. Palaniapan, "Inductor voltage controlled variable power factor buck-type AC-DC converter," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 230-237 vol.1.
- [107] R. Srinivasan, M. Palaniapan, and R. Oruganti, "A single phase two-switch buck type AC-DC converter topology with inductor voltage control," in *Power Electronics Specialists Conference, 1997. PESC '97 Record., 28th Annual IEEE*, 1997, pp. 556-563 vol.1.
- [108] M. Chen, A. Mathew, and S. Jian, "Nonlinear Current Control of Single-Phase PFC Suitable for Mixed-Signal IC Implementation," in *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*, 2006, pp. 1-7.
- [109] M. Chen, A. Mathew, and S. Jian, "Nonlinear Current Control of Single-Phase PFC Converters," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 2187-2194, 2007.
- [110] C. Min, A. Mathew, and S. Jian, "Mixed-Signal Control of Single-Phase PFC Based on a Nonlinear Current Control Method," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-7.
- [111] M. Dongsheng, K. Wing-Hung, and T. Chi-ying, "An integrated one-cycle control buck converter with adaptive output and dual loops for output error correction," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 140-149, 2004.
- [112] A. A. Ghodke and K. Chatterjee, "One-cycle-controlled bidirectional three-phase unity power factor ac-dc converter without having voltage sensors," *Power Electronics, IET*, vol. 5, pp. 1944-1955, 2012.
- [113] A. A. Ghodke and K. Chatterjee, "Three-phase three-level one-cycle controlled bidirectional AC-to-DC NPC converter," in *Control and Modeling for Power Electronics (COMPEL), 2012 IEEE 13th Workshop on*, 2012, pp. 1-7.
- [114] M. Orabi, R. Haron, and M. Z. Youssef, "Stability analysis of PFC converters with one-cycle control," in *Telecommunications Energy Conference, 2009. INTELEC 2009. 31st International*, 2009, pp. 1-6.
- [115] F. Alonge, F. Librizzi, F. M. Raimondi, P. Scalia, and A. Urso, "Improved peak-current-mode control for unity power factor AC/DC converters in discontinuous conduction mode," in *Power Electronics and Drive Systems, 1999. PEDS '99. Proceedings of the IEEE 1999 International Conference on*, 1999, pp. 927-932 vol.2.
- [116] J. P. Gegner and C. Q. Lee, "Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 196-202 vol.1.
- [117] D. G. Lamar, J. Sebastian, M. Arias, and M. M. Hernando, "A low-cost AC-DC High-Brightness LED driver with Power Factor Correction based on standard Peak-Current Mode Integrated Controllers," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 463-470.
- [118] D. G. Lamar, J. Sebastian, M. Arias, A. Rodriguez, and M. M. Hernando, "A low-cost battery charger with high power factor correction based on standard



- peak-current mode integrated controllers," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.
- [119] M. Subbarao, C. Sai Babu, S. Satyanarayana, and S. L. V. S. Kumar, "Analysis and design of Peak Current controlled IBFC for high power factor and tight voltage regulation," in *Advances in Electrical Engineering (ICAEE), 2014 International Conference on*, 2014, pp. 1-4.
- [120] W. Chien-Ming, "A Novel Soft-Switching Single-Phase AC-DC-AC Converter Using New ZVS-PWM Strategy," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 1941-1948, 2007.
- [121] P. N. Ekemezie, "Design of a power factor correction ac-dc converter," in *AFRICON 2007*, 2007, pp. 1-8.
- [122] S. M. Hoseini, Y. A. Beromi, and S. M. Sadeghzadeh, "Implementation and comparison of two common power factor correction techniques in AC/DC switching converters," in *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2014 5th*, 2014, pp. 285-290.
- [123] K. P. Louganski and L. Jih-Sheng, "A 20-kW, 10-kHz, Single-Phase Multilevel Active-Front-End Converter with Reactive Power Control," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, 2006, pp. 576-582.
- [124] J. C. Wang and C. Hon-Ji, "Design and analysis of AC/DC converters with interleaved Power Factor Correction," in *Intelligent Control and Automation, 2008. WCICA 2008. 7th World Congress on*, 2008, pp. 9385-9387.
- [125] A. N. Arvindan and V. K. Sharma, "Hysteresis-Band Current Control of a Four Quadrant AC-DC Converter giving IEEE 519 compliant performance at any Power Factor," in *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, 2006, pp. 1-6.
- [126] A. N. Arvindan and V. K. Sharma, "Current Control of a High Power Factor Improved Power Quality Four Quadrant AC-DC Converter," in *Industrial Technology, 2006. ICIT 2006. IEEE International Conference on*, 2006, pp. 1397-1402.
- [127] R. K. Behera and S. P. Das, "Analysis and experimental investigation for switching frequency characterisation of a three-level ac-dc converter using frequency domain approach," *Power Electronics, IET*, vol. 4, pp. 936-942, 2011.
- [128] R. C. Fernandes and F. J. M. de Seixas, "AC-DC three-phase multipulse converter with boost DC-DC stage and constant hysteresis control," in *Power Electronics Conference (COBEP), 2011 Brazilian*, 2011, pp. 403-408.
- [129] L. Jae Sik and L. Young Il, "Model predictive control of current and voltage for Li-Ion battery charger using 3-phase AC/DC converter," in *SICE Annual Conference 2010, Proceedings of*, 2010, pp. 215-218.
- [130] M. Parvez, S. Mekhilef, N. M. L. Tan, and H. Akagi, "Model predictive control of a bidirectional AC-DC converter for V2G and G2V applications in electric vehicle battery charger," in *Transportation Electrification Conference and Expo (ITEC), 2014 IEEE*, 2014, pp. 1-6.
- [131] A. Roman-Loera, L. A. Flores, F. de J. Rizo-Diaz, and L. E. Arambula-Miranda, "Current sensorless predictive algorithm control for three-phase power factor

- correction," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, 2008, pp. 653-658.
- [132] W. Wei-Hsiang and T. Ying-Yu, "Current control techniques for utility interface converters with low THD," in *Sustainable Energy Technologies (ICSET), 2012 IEEE Third International Conference on*, 2012, pp. 91-96.
- [133] D. Zhang, H. Lin, Z. Lu, and S. Wang, "Predictive current control based multi-pulse flexible-topology thyristor AC/DC converter and its application in wind energy conversion system," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, 2013, pp. 1202-1207.
- [134] N. Weise, "DQ current control of a bidirectional, isolated, single-stage AC-DC converter for vehicle-to-grid applications," in *Power and Energy Society General Meeting (PES), 2013 IEEE*, 2013, pp. 1-5.
- [135] F. Kurokawa and K. Ueno, "Performance characteristics digital boundary current control AC-DC converter," in *Renewable Energy Research and Applications (ICRERA), 2012 International Conference on*, 2012, pp. 1-5.
- [136] F. Kurokawa and K. Ueno, "A novel digital boundary current control AC-DC converter," in *Control and Modeling for Power Electronics (COMPEL), 2012 IEEE 13th Workshop on*, 2012, pp. 1-5.
- [137] M. Pahlevaninezhad, P. Das, S. Eren, A. Bakhshai, and P. Jain, "An optimal control strategy for digitally controlled single-phase power factor correction AC-DC boost converter," in *Telecommunications Energy Conference (INTELEC), 2011 IEEE 33rd International*, 2011, pp. 1-5.
- [138] V. F. Pires and J. F. Silva, "Half-bridge single-phase buck-boost type AC-DC converter with sliding-mode control of the input source current," *Electric Power Applications, IEE Proceedings -*, vol. 147, pp. 61-67, 2000.
- [139] P. Huong, J. Hoeguk, and H. Tingshu, "Ripple reduction in AC-DC power converters via a Lyapunov approach," in *American Control Conference (ACC), 2012*, 2012, pp. 2141-2146.
- [140] M. Pahlevaninezhad, P. Das, A. Safaee, P. Jain, A. Bakshai, and G. Moschopoulos, "An optimal Lyapunov-based control strategy for digitally controlled single-phase power factor correction AC/DC converters," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2873-2878.
- [141] L. Chih-Wei and T. Ying-Yu, "Digital voltage control of boost CRM PFC AC/DC converters with TRIAC Phase Control dimmer," in *Power System Technology (POWERCON), 2012 IEEE International Conference on*, 2012, pp. 1-6.
- [142] L. Ko-Yen, H. Hsiang-Yu, and L. Yen-Shin, "Simple Digital-Controlled AC/DC Converter with Power Factor Correction for Universal Input Applications," in *Industrial Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE*, 2007, pp. 1472-1477.
- [143] H. Matsuo, M. Suetomi, S. Fujino, K. Harada, L. Wengzong, and S. Yue, "A bidirectional AC-DC converter with high power efficiency and high power factor using fast FPGA digital control," in *Telecommunications Energy Conference (INTELEC), 2012 IEEE 34th International*, 2012, pp. 1-7.
- [144] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *IEEE Std 519-1992*, pp. 1-112, 1993.

## **Published Works**

1. Golam Sarowar, Md. Ashraful Hoque, Mohammad Ali Choudhury, “Simulation of High Efficiency Switched Capacitor AC to DC SEPIC Converter for Improved Power Quality”. International Journal of Computer Science and Network Security. Vol. 16 No. 10 pp. 9-15, 2016, ISSN 1738-7906.
2. Golam Sarowar, Md. Ashraful Hoque, “High Efficiency Single Phase Switched Capacitor AC to DC Step Down Converter”. Volume 195, pp. 2527-2536, Procedia - Social and Behavioral Sciences, 3 July 2015, [www.sciencedirect.com/science/article/pii/S1877042815039166](http://www.sciencedirect.com/science/article/pii/S1877042815039166)
3. Golam Sarowar, Md. Ashraful Hoque, Mohammad Ali Choudhury, “Hybrid Single Phase Buck AC-DC Converter with Improved Power Quality”. IUT Journal of Engineering and Technology (JET), Vol. 12, No. 1, JUNE 2015