Declaration of Authorship

We, Ahmed Shariful Alam (092408), Abu Hena Md. Mustafa Kamal (092411) and Md. Abdur Rahman (092427), declare that this thesis titled,'Structure and Operation of Single Electron Transistor (SET) and Its Circuit Implementation 'and the works presented in it are our own. We confirm that:

- This work has been done for the partial fulfillment of the Bachelor of Science in Electrical and Electronic Engineering degree at this university.
- Any part of this thesis has not been submitted anywhere else for obtaining any degree.
- Where we have consulted the published work of others, we have always clearly attributed the sources.

Submitted By:

Ahmed Shariful Alam (092408)

Abu Hena Md. Mustafa Kamal (092411)

Md. Abdur Rahman (092427)

Structure and Operation of Single Electron Transistor and Its Circuit Implementation

Approved By:

Syed Iftekhar Ali
Thesis Supervisor,
Assistant Professor,
Department of Electrical and Electronic Engineering,
Islamic University of Technology.

Prof. Dr. Md. Shahid Ullah
Head of the Department,
Department of Electrical and Electronic Engineering,
Islamic University of Technology.

Structure and Operation of Single Electron Transistor and Its Circuit Implementation

A Thesis Presented to

The Academic Faculty

by

Ahmed Shariful Alam (092408)
Abu Hena Md. Mustafa Kamal (092411)
Md. Abdur Rahman (092427)

In Partial Fulfillment
of the Requirements for the Degree B.Sc in
Electrical and Electronic Engineering

Academic Year: 2012-2013

Islamic University Of Technology
A Subsidiary Organ of the Organisation of Islamic Cooperation (OIC)
Dhaka, Bangladesh.

October 2013

Contents

List of Figures

List of Tables

Abstract

CMOS Technology has advanced for decades under the rule of Moores law. But all good things must come to an end. Researchers estimate that CMOS will reach a lower limit on feature size within the next 7 to 10 years. In order to assure further progress in the field, new computing architectures must be investigated. These nanoscale architectures are many and varied. It remains to be seen if any will become a legitimate successor to CMOS.

Single electron tunneling is a process by which electrons can be transported (tunnel) across a thin insulating surface. SETs exhibit higher functionality than traditional MOSFETs, and function best at very small feature sizes, in the neighborhood of 1nm.

SETs have several advantages over MOSFETs. One of the most important of these advantages is low power consumption. Power consumption level of SET is ultra-low. As for example, in this thesis work all the simulation have been done with 35mV supply voltage, whereas the supply voltage of MOSFET based digital circuits is in 3.5V - 12V range. This advantage gives SETs a new ground to develop its field in VLSI circuits. Many circuits must be developed before SETs can be considered a viable contender to CMOS technology. In this thesis work several digital circuits such as Inverter, 2-input NAND Gate, 2-input NOR Gate, Half Adder and Full Adder have been discussed. All the circuits have been built using complementary logic. For this Complementary Single Electron Transistors (CSET) were used.

We propose four possible SET Inverters designs and characterize them with a PSPICE SET simulation model developed by Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley. Among them we chose the best one. Then that bias was used in the next digital circuits.

Acknowledgements

All praise and thanks to Almighty Allah who has showered us with His invaluable blessings throughout our lives, giving us strength and spirit to complete this thesis.

We would like to express our deepest gratitude to our thesis supervisor **Mr. Syed Iftekhar Ali**, Assistant Professor, Electrical and Electronic Engineering, IUT, whose personal supervision, advice and valuable guidance helped us to go through all the stages and complete appreciably our final year project. Without his stimulus for work and knowledge of the thesis idea, the completion of the thesis would have been impossible.

We would like to thank our department for supporting us. We convey our respect to all the teachers, friends and family members who gave us their support.

Chapter 1

Introduction To SET

1.1 Introduction

With increasing demand of higher processor speed and power efficient integrated circuit components scientist are in pursuit of newer devices. Although few works had been done in the similar field earlier, for the last few years tremendous advancement has been made on nano-electronics circuits and devices. Single Electron Transistor (SET) is one of those unique devices which hold promise to dominate the future world of minuscule circuitry. This chapter focuses on the history of this quantum device, discusses the basic physics of the transistor and finally explains the motivation of this thesis work.

1.2 History Of Single Electron Transistor

The effects of charge quantization were first observed in tunnel junctions containing metal particles as early as 1968. Later, the idea that the Coulomb blockade can be overcome with a gate electrode was proposed by a number of authors, and Kulik and Shekhter developed the theory of Coulomb-blockade oscillations, the periodic variation of conductance as a function of gate voltage. Their theory was classical, including charge quantization but not energy quantization. However, it was not until 1987 that Fulton and Dolan made the first SET, entirely out of metal and observed predicted oscillation. They made a metal particle connected to two metal leads with tunnel junctions, all on top of an insulator with a gate electrode underneath. Since then, the capacitances of such metal SETs have been reduced to produce very precise charge quantization.

The first semiconductor SET was fabricated accidentally in 1989 by Scott-Thomas et al. in narrow Si field effect transistors. In this case the tunnel barriers were produced by interface charges. Shortly thereafter Meirav et al. made controlled devices, albeit with an unusual heterostructure with AlGaAs on the bottom instead of the top. In these and similar devices the effects of energy quantization were easily observed. Only in the past few years have metal SETs been made small enough to observe energy quantization. Foxman et al. also measured the level width and showed how the energy and charge quantization are lost as the resistance decreases toward h/e^2. In most cases the potential confining the electrons in a SET is of sufficiently low symmetry that one is in the regime of quantum chaos: the only quantity that is quantized is the energy.In this case there is a very sophisticated approach, based in part on random matrix theory, for predicting the distributions of peak spacing and peak heights. There are challenging problems in this area that are still unsolved. In particular, there is great interest in how the interplay of exchange and level spacing determines the spin of a small metal SET. In a SET of sufficiently high symmetry, angular momentum in the plane of the 2DEG is conserved, so shell structure is apparent. Another way to eliminate the scattering that destroys angular momentum conservation is to apply a magnetic field perpendicular to the 2DEG. At sufficiently high fields elegant patterns are seen in the single-electron-peak positions as a function of field.

The evolution of Coulomb charging peaks with magnetic field has been interpreted with various degrees of sophistication, imitating the development of the theory of atoms. First one tries the constant interaction model in which electrons are treated as independent except for a constant Coulomb charging energy. This gives only a qualitative picture of the physics. In order to be quantitative, one needs to at least treat the electron-electron interactions self-consistently (analogous to the Thomas Fermi model), and for some cases one needs to include exchange and correlations. In particular, it is found that electrons in an SET undergo a series of phase transitions at high magnetic field. One of these is well described by Hartree-Fock theory, but others appear to require additional correlations.

The future of research on SETs looks very bright. There are strong efforts around the world to make the artificial atoms in SETs smaller, in order to raise the temperature at which charge quantization can be observed. These involve self-assembly techniques and novel lithographic and oxidation methods whereby artificial atoms can be made nearly as small as natural ones. This is, of course, driven by an interest in using SETs for practical applications. However, as SETs get smaller, all of their energy scales can be larger, so it is very likely that new phenomena will emerge.

1.3 Basic Physics of Single Electron Transistor

A conventional field-effect transistor, the kind that makes all modern electronics work, is a switch that turns on when electrons are added to a semiconductor and turns off when they are removed. These on and off states give the ones and zeros that digital computers use for calculation. Interestingly, these transistors are almost completely classical in their physics. Their behaviors are rarely affected by quantum mechanics. However, if one makes a new kind of transistor, in which the electrons are confined within a small volume and communicate with the electrical leads by tunneling, all this changes. One then has a transistor that turns on and off again every time one electron is added to it; we call it a single electron transistor (SET). Furthermore, the behavior of the device is entirely quantum mechanical.
The manipulation of single electrons was demonstrated in the seminal experiments by Millikan at the very beginning of the century, but in solid state circuits it was not implemented until the late 1980s, despite some important earlier background work. The main reason for this delay is that the manipulation requires the reproducible fabrication of very small conducting particles, and their accurate positioning against external electrodes. The necessary nanofabrication techniques have become available during the past two decades, and have made possible a new field of solid state physics.
The basic concept of single-electronics is illustrated in Fig. 1.1. Let a small conductor (traditionally called an island) be initially electro-neutral, i.e. have exactly as many (m) electrons as it has protons in its crystal lattice. In this state the island does not generate any appreciable electric field beyond its borders, and a weak external force F may bring in an additional electron from outside. (In most single-electron devices, this injection is carried out by tunneling through an energy barrier created by a thin insulating layer).Now the net charge Q of the island is (-e), and the resulting electric field E repulses the following electrons which might be added. Though the fundamental charge e 1.6x10-19 Coulomb is very small on the human scale of things, the field E is inversely proportional to the square of the island size, and may become rather strong for nanoscale structures.
For example, the field is as large as 140 kV/cm on the surface of a 10-nm sphere in vacuum. The theory of single-electron phenomena shows that a more adequate measure of the strength of these effects is not the electric field, but the *charging energy*

$$E_C = \frac{e^2}{C} \tag{1.1}$$

where C is the capacitance of the island (For a two-electrode capacitor, the

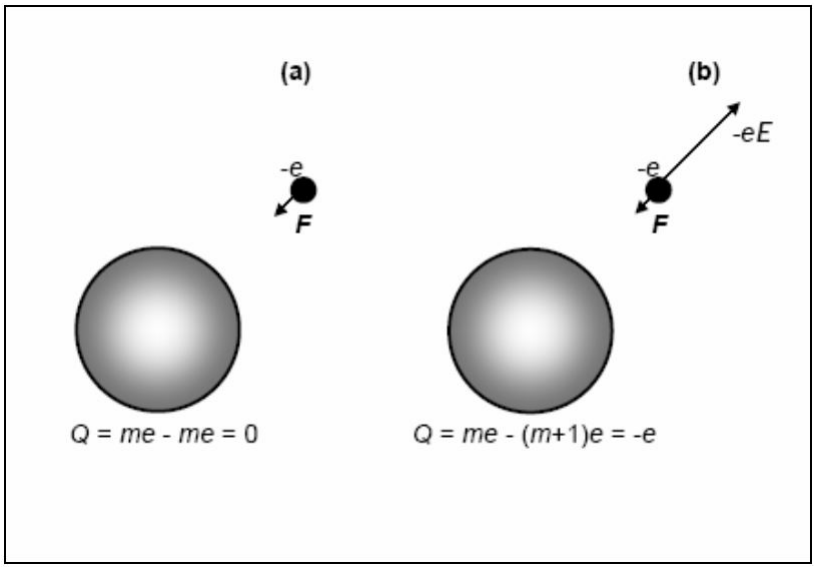

Figure 1.1: The basic concept of single-electron control: a conducting island (a) before and (b) after the addition of a single electron. The addition of a single uncompensated electron charge creates an electric field E which may prevent the addition of the following electrons.

elementary charging energy is of course $\frac{e^2}{2C} = \frac{E_C}{2}$, rather than E_C. However, if a single small conductor is charged with electrons from a source kept at a fixed electrochemical potential μ, this is E_C which gives the electrostatic contribution to the energy necessary for the transfer of one additional electron to the conductor:

$$e\Delta\mu = E_a \approx E_C + kineticenergy \tag{1.2}$$

in Eqn. (1.2) this relationship is established. When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial. In this case the energy scale of the charging effects is given by a more general notion, the electron addition energy E_a. In most cases of interest, E_a may be well approximated by the following simple formula:

$$E_a = E_c + E_k \tag{1.3}$$

Here E_k is the quantum kinetic energy of the added electron; for a degenerate electron gas, $E_k = \frac{1}{g(\varepsilon_F)V}$,where V is the island volume and $g(\varepsilon_F)V$ is the density of states on the Fermi surface.

Fig. 1.2 shows the total electron addition energy as a function of the island diameter, as calculated using Eqn. (1.3) for a simple but representative model. For 100-nm-scale devices which were typical for the initial stages of experimental single-electronics, E_a is dominated by the charging energy E_c and is of the order of 1 meV, i.e. 10 K in temperature units. Since thermal fluctuations suppress most single-electron effects unless E_a 10 kT these experiments have to be carried out in the sub-1-K range (typically, using helium dilution refrigerators). On the other hand, if the island size is reduced below 10 nm, Ea approaches 100 meV, and some single-electron effects become visible at room temperature. However, most suggested digital single-electron devices require even higher values of E_a (100 kT) in order to avoid thermally-induced random tunneling events, so that for room temperature operation the electron addition energy E_a has to be as large as a few electron-volts, and the minimum feature size of single-electron devices has to be smaller than 1 nm (Fig. 1.2). In this size range the electron quantization energy Ek becomes comparable with or larger than the charging energy E_c for most materials; this is why islands this small are frequently called quantum dots. Their use involves not only extremely difficult nanofabrication technology (especially challenging for large scale integration), but also some major physics problems including the high sensitivity of transport properties to small variations of the quantum dot size and shape. This is why it is very important to develop single-electron devices capable of operating with the lowest possible ratio $\frac{E_a}{kT}$. As we will see below, some devices may work in the size range where $E_c > E_k$ even at room temperature, thus avoiding complications stemming from the energy quantization effects.

1.4 Motivation

Single Electron Transistor (SET) is continually being tested by researchers and engineering scientist in various applications. Being a nano-electronic device, SET is a potential candidate for components of molecular computing, quantum computing and nano-electro-mechanical devices (NEMS). SET island is also explained to behave like artificial atom because electrons are confined in the quantum dot island.

This work has shown the application of SETs in digital circuits. All the circuitries are shown here using complementary digital logic. Ultra low power consumption and ultra small size of device makes SET based logic circuits more prominent than the MOSFET based logic circuits.

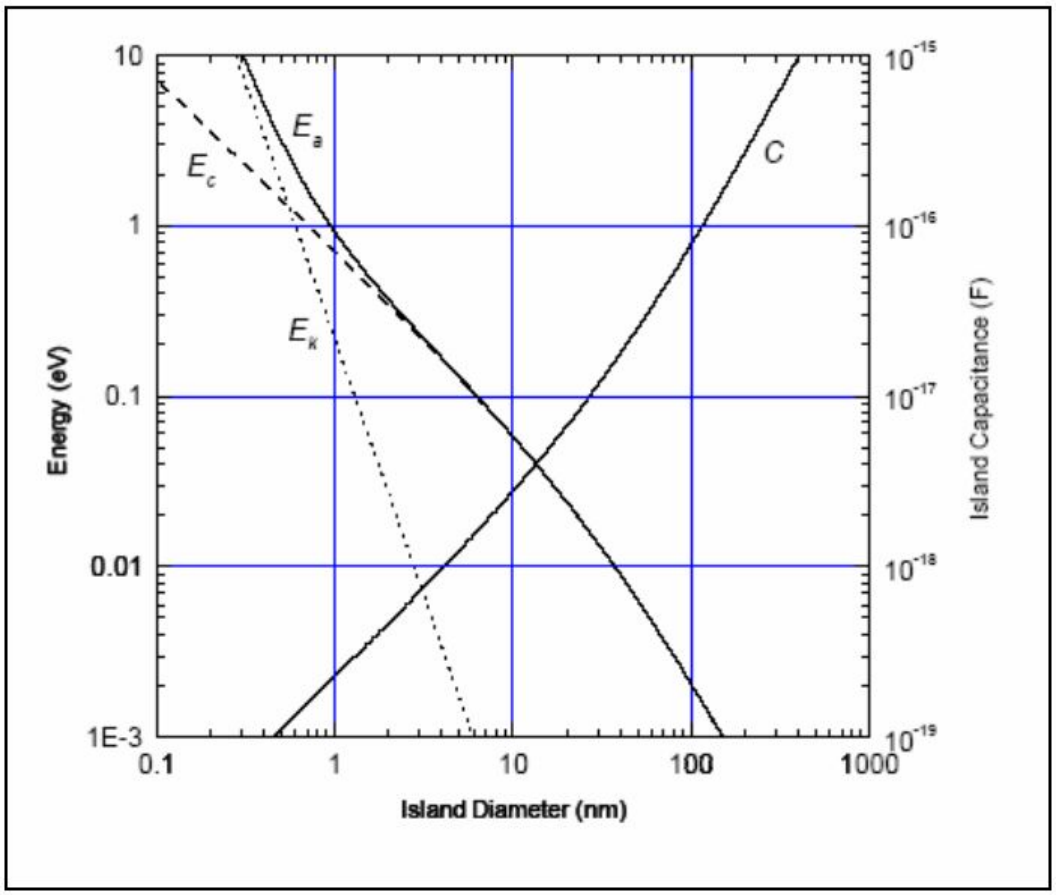

Figure 1.2: Single-electron addition energy E_a (solid line), and its components: charging energy E_c (dashed line) and electron kinetic energy E_k (dotted line), as calculated using Eqs. (1.1) and (1.3) for a simple model of a conducting island. In this model the island is a round 3D ball with a free, degenerate electron gas (electron density n = 1022 cm^3, electron effective mass $m = m_0$), embedded into a dielectric matrix (dielectric constant, ε_r= 4), with 10 of its surface area occupied by tunnel junctions with a barrier thickness d = 2 nm.

Chapter 2

SET Structure And Operation

2.1 Introduction

Single electron transistor is unique in its structure, operation and characteristics. This chapter describes the physical structure of SET. The equivalent circuit is also discussed with simplified transistor view. The theory of Coulomb blockade which is the heart of the transistor operation is discussed which is followed by the operating principle of the transistor itself.

2.2 Physical Structure of Single Electron Transistor

The SET transistor can be viewed as an electron box that has two separate junctions for the entrance and exit of single electrons (Fig. 2.1).It can also be viewed as a field-effect transistor in which the channel is replaced by two tunnel junctions forming a metallic island. The voltage applied to the gate electrode affects the amount of energy needed to change the number of electrons on the island.

The SET transistor comes in two versions that have been nicknamed "metallic" and "semiconducting". These names are slightly misleading, however, since the principle of both devices is based on the use of insulating tunnel barriers to separate conducting electrodes.

In this semiconducting version of the SET, the island is often referred to as a quantum dot, since the electrons in the dot are confined in all three directions.In the last few years researchers at the Delft University of Technology in the Netherlands

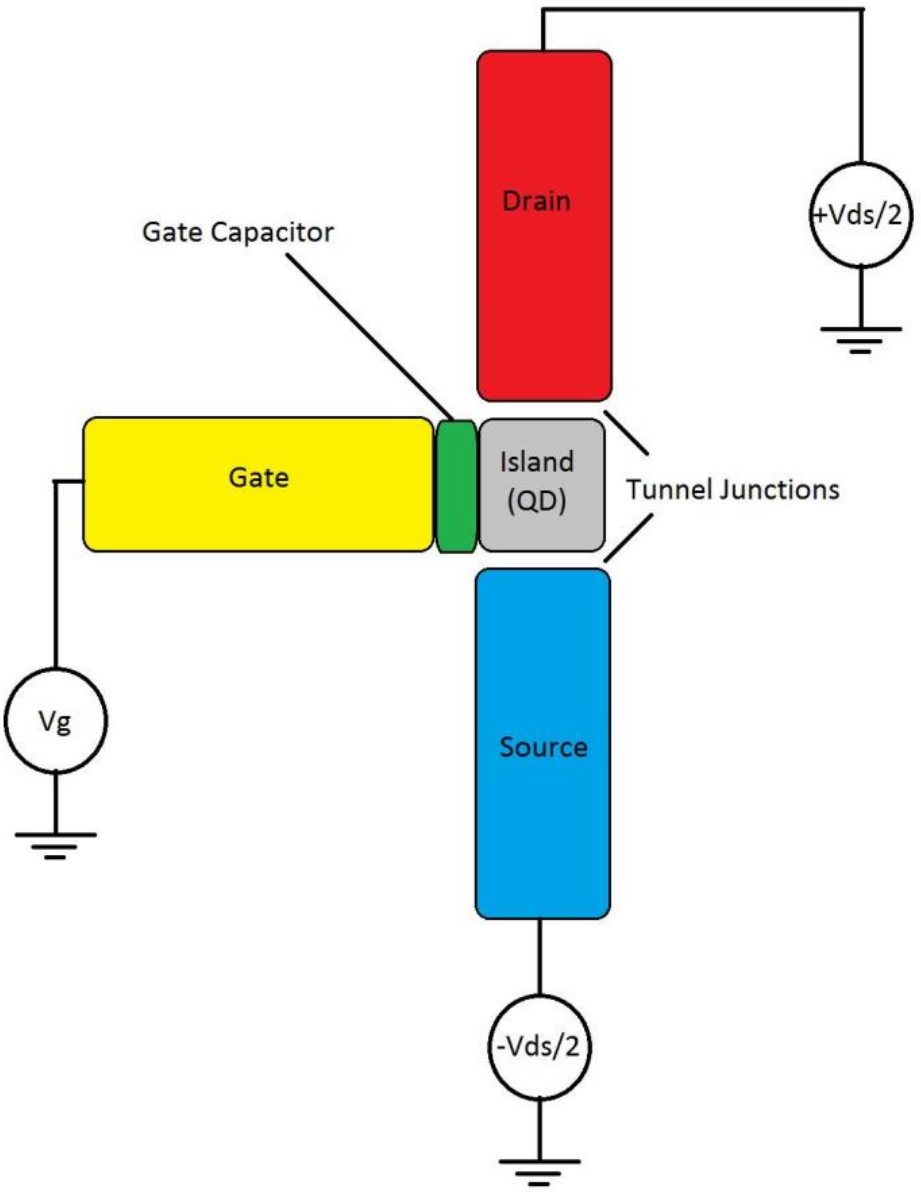

Figure 2.1: Structural view of SET

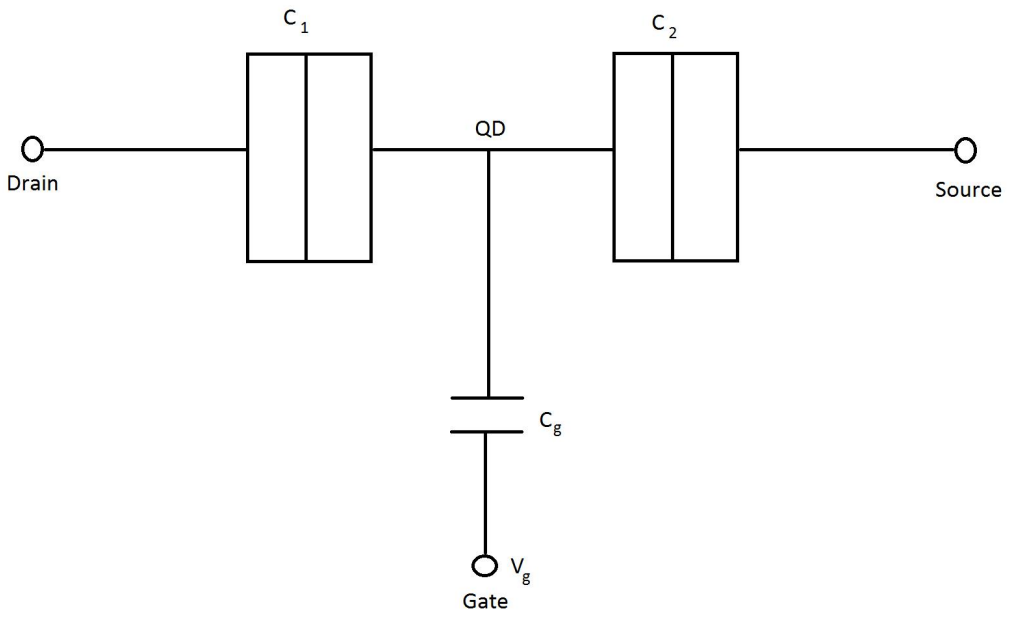

Figure 2.2: Schematic representation of SET

and at NTT in Japan have shown that quantum dots can behave like artificial atoms.Indeed, it has been possible to construct a new periodic table that describes dots containing different numbers of electrons.

A simplified schematic representation of SET may look like as shown in Fig. 2.2,where drain, source and the gate electrodes are shown capacitively coupled to the quantum dot island.In this model all isolation barriers are replaced by capacitor including the gate dielectric.

Fig. 2.3 shows a possible 3-D view of a SET where quantum dot island is exaggerated for illustration purposes.In reality, the island is usually 35 50nm in length/width. An atomic force microscopy image of fabricated SET is shown in Fig. 2.4.This fabricated SET is demonstrated to operate at room temperature. In this figure the gate electrode is not shown.But two TiOx barriers indicate that two gate electrode can be placed on the other sides of the barriers. Discussion on SET with two gates or Dual Gate SET (DGSET) is given on chapter 3.

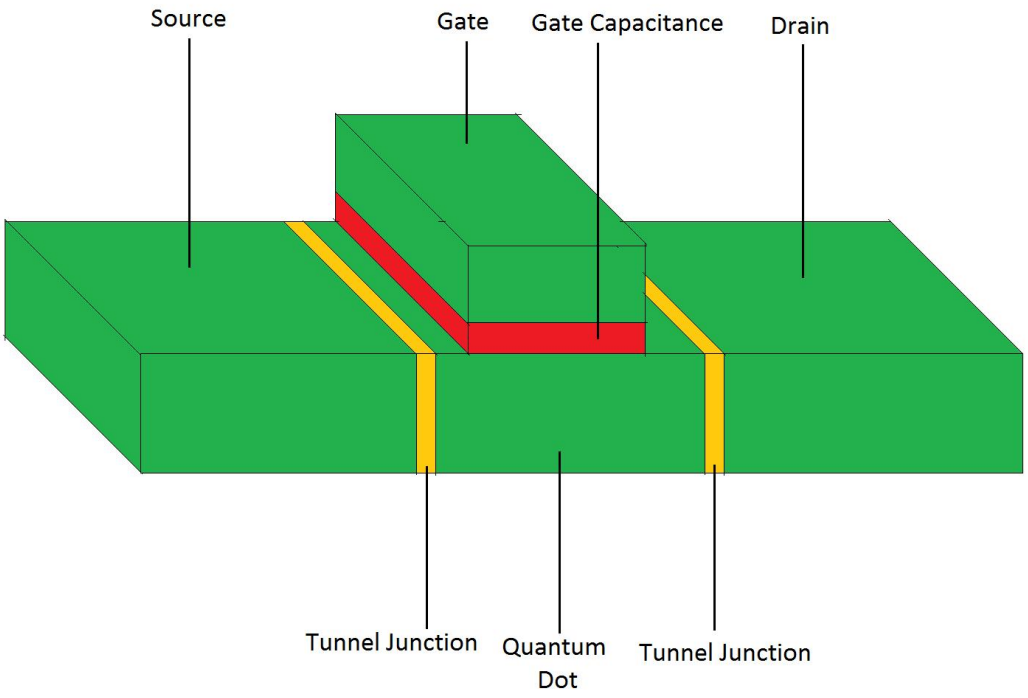

Figure 2.3: A 3-D representation of SET

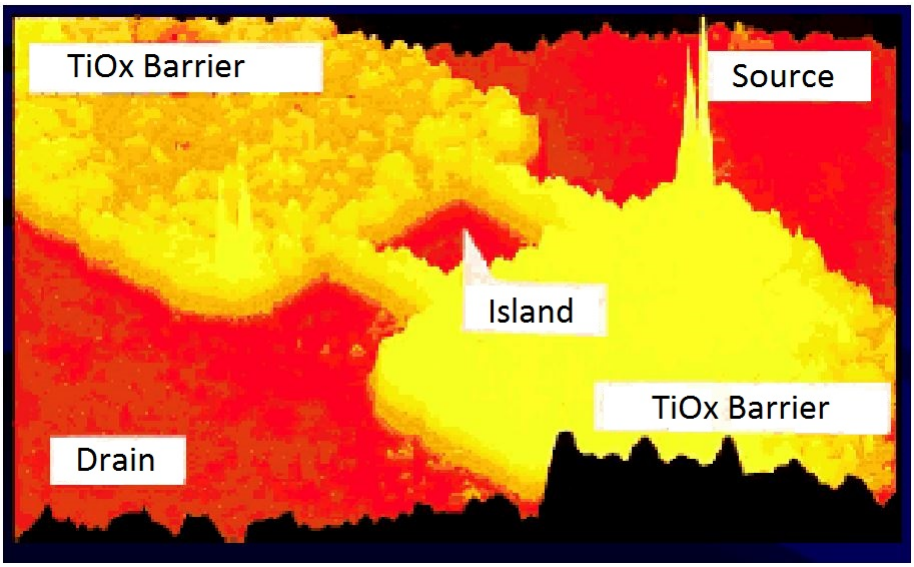

Figure 2.4: An AFM (atomic force microscopy) image of a SET built by the STM (scanning tunneling microscope) nano-oxidation process. The TiOx tunneling barrier shown here surrounds the quantum dot island which is 35nm X 35nm in area, the width of the TiOx dielectric is 20nm with a relative permittivity of r=24 and barrier height of 285meV. With the 3-nm thick Ti blanket layer this structure ensures small tunneling junction area and corresponding tunnel capacitance becomes as small as 10-19 F, which allows the set to be operated at room temperature.

2.3 Coulomb Blockade

In physics, a Coulomb blockade, named after Charles-Augustin de Coulomb, is the increased resistance at small bias voltages of an electronic device comprising of at least one low-capacitance tunnel junction.

A tunnel junction is, in its simplest form, a thin insulating barrier between two conducting electrodes. If the electrodes are superconducting, Cooper pairs with a charge of two elementary charges carrythe current. In the case that the electrodes are normal conducting, i.e. neither superconducting nor semiconducting, electrons with a charge of one elementary charge carry the current. The following reasoning is for the case of tunnel junctions with an insulating barrier between two normal-conducting electrodes (NIN junctions).

According to the laws of classical electrodynamics, no current can flow through an insulating barrier. According to the laws of quantum mechanics, however, there is a nonvanishing (larger than zero) probability for an electron on one side of the barrier to reach the other side which is generally known as quantum tunneling.When a bias voltage is applied, this means that there will be a current flow. In first-order approximation,that is, neglecting additional effects, the tunneling current will be proportional to the bias voltage. In electrical terms, the tunnel junction behaves as a resistor with a constant resistance, also known as an ohmic resistor.The resistance depends exponentially on the barrier thickness.Typical barrier thicknesses are on the order of one to several nanometers.

An arrangement of two conductors with an insulating layer in between not only has a resistance, but also a finite capacitance. The insulator is called dielectric in this context, as the tunnel junction behaves as a capacitor.

Due to the discreteness of electrical charge,current flow through a tunnel junction is a series of events in which exactly one electron passes (tunnels) through the tunnel barrier (We neglect events in which two electrons tunnel simultaneously).The tunnel junction capacitor is charged with one tunneling electron (elementary charge unit),causing a voltage buildup $U = \frac{e}{C}$, where e is the elementary charge of 1.6×10^{-19} Coulomb and C the capacitance of the junction.

If the capacitance is very small, the voltage buildup can be large enough to prevent another electron from tunneling. The electrical current is then suppressed at low bias voltages; the resistance of the device is no longer constant. The increase of the differential resistance around zero bias is called the Coulomb blockade. In order for the Coulomb blockade to be observable, the temperature has to be low

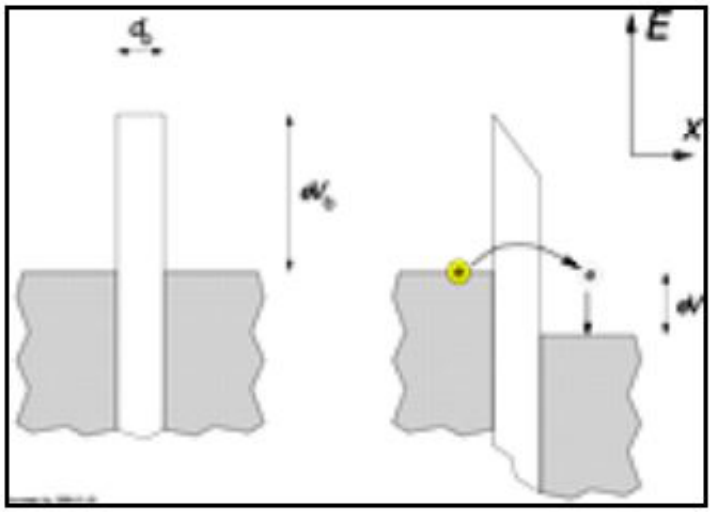

Figure 2.5: Schematic representation of an electron tunneling through a barrier

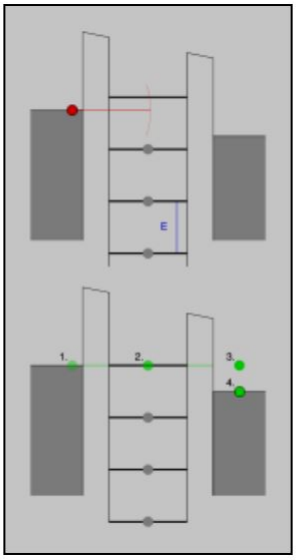

Figure 2.6: Energy level of source, island and drain of a SET (left to right). (Top) blocking stage and (Bottom) transmitting stage

enough so that the characteristic charging energy (the energy that is required to charge the junction with one elementary charge) is larger than the thermal energy of the charge carriers. For capacitances below 1 femto-farad (10^{-15} farad), this implies that the temperature has to be below about 1 Kelvin. This temperature range is routinely reached for example by dilution refrigerators.

To make a tunnel junction in plate condenser geometry with a capacitance 1 femto-farad, using an oxide layer of electric permeability 10 and thickness one nanometer, one has to create electrodes with dimensions of approximately 100 by 100 nanometers. This range of dimensions is routinely reached for example by electron beam lithography and appropriate pattern transfer technologies, like the Niemeyer-Dolan technique, also known as shadow evaporation technique.

Another problem with the observation of the Coulomb blockade is the relatively large capacitance of the leads that connect the tunnel junction to the measurement electronics.

The simplest device in which the effect of Coulomb blockade can be observed is the so-called single electron transistor. It consists of two tunnel junctions sharing one common electrode with a low self-capacitance, known as the island. The electrical potential of the island can be tuned by a third electrode (the gate), capacitively coupled to the island.

In the blocking state, as shown in the Fig. 2.6 (top portion), no accessible energy levels are within tunneling range of the electron on the source contact. All energy levels on the island electrode with lower energies are occupied.

In Fig. 2.6 (bottom portion),when a positive voltage is applied to the gate electrode the energy levels of the island electrode are lowered.The electron (marked 1) can tunnel onto the island (marked 2),occupying a previously vacant energy level.From there it can tunnel onto the drain electrode (marked 3) where it inelastically scatters and reaches the drain electrode Fermi level (marked 4).

The energy levels of the island electrode are evenly spaced with a separation of ΔE. ΔE is the energy needed to each subsequent electron to the island, which acts as a self capacitance C.The lower the C, the bigger ΔE gets.It is crucial for ΔE to be larger than the energy of thermal fluctuations kT,otherwise an electron from the source electrode can always be thermally excited onto an unoccupied level of the island electrode,and no blocking can be observed.

2.4 Theory of Operation

Fig. 2.7 shows a device schematic of a single electron transistor, where a dot is surrounded by three electrodes. All three electrodes are coupled to the dot capacitively;a Potential change in any of them can cause an electrostatic energy change in the dot.

Only two electrodes (source and drain) are tunnel coupled to the dot and electron transport is allowed only between the dot and these two electrodes. Since the dot is connected to the source and drain electrodes by a tunnel barrier (meaning an electron is either on the dot or one of the electrodes), the number of electrons on the dot, N is well defined. We assume that all interactions between an electron on the dot and all other electrons on the dot or on the electrodes can be parameterized by the total capacitance C. We also assume that C does not depend on different charge states of the dot. Then the total electrostatic energy for a dot with N electrons will become $\frac{Q^2}{2C} = \frac{(Ne)^2}{2C}$. When N electrons reside on the dot, the total energy is

$$U(N) = \sum_{i=1}^{N} E_i + \frac{(Ne)^2}{2C} \tag{2.1}$$

After an additional electron is added to the dot, the total energy increases to

$$U(N+1) = \sum_{i=1}^{N+1} E_i + \frac{[(N+1)e]^2}{2C} \tag{2.2}$$

Here E_i is the chemical potential of the dot with i electrons. This is the energy of the orbital of the dot that the i^{th} electron would occupy if there were no electron-electron interactions. The electrochemical potential is then,

$$\mu_N = E_N + (N + \frac{1}{2}).\frac{e^2}{C} \tag{2.3}$$

By definition, the electrochemical potential μ_N the minimum energy required for adding N-th electron. As long as μ_N is below both μ_S and μ_D, the N-th electron will be added to the dot.Likewise, to add one more electron to a dot with N electrons,

$$\mu(N+1) = \mu_N + \frac{e^2}{C} + \Delta E \tag{2.4}$$

needs to be lower than both μ_S and μ_D, where $\Delta E = E_{N+1} - E_N$. For simplicity, we will assume that ΔE does not change for different charge states of the dot.

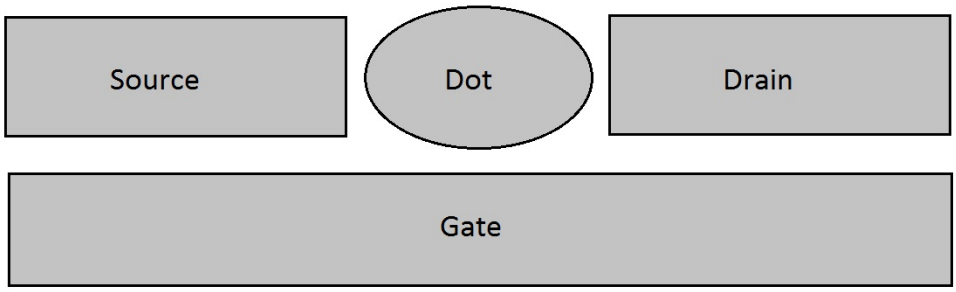

Figure 2.7: The single electron transistor. A small dot is separated from the source and drain electrodes by tunnel barriers. It is also coupled to the gate electrode capacitively.

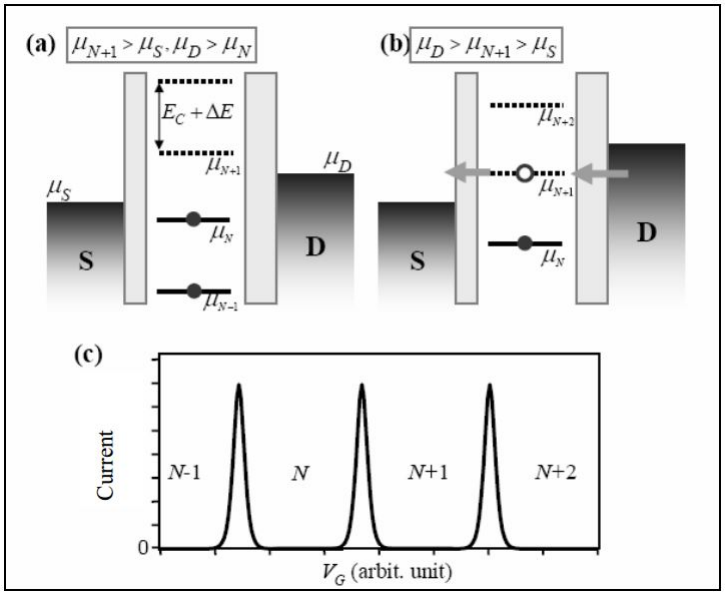

Figure 2.8: Electron transport in a single electron transistor and $I - V$ characteristics of SET

This allows us to drop the subscript N for ΔE.Therefore,the $N+1$-th electron needs to have energy larger than the one for the N-th electron by $\frac{e^2}{C}+\Delta E$. This is the charge addition energy. The first term $\frac{e^2}{C} \equiv E_C$,which is called the charging energy, is the energy that is required to overcome the Coulomb repulsion among different electrons.

The second term ΔE is the result of quantized excitation spectrum of the dot. Fig. 2.8(a) illustrates the energy diagram of a single electron transistor with $\mu_{N+1} > \mu_S$ and $\mu_D > \mu_N$. The dot will have N electrons and the solid lines below μ_N represent all the filled electrochemical levels. The lowest dotted line represents $\mu_N + 1$ and it cannot be occupied since it is above the electrode Fermi levels. Therefore, the dot is stable with N electrons and hence the current cannot flow through the dot. In other words, the current is blocked due to the charge addition energy. Fig. 2.8(b) illustrates another case where $\mu_D > \mu_{N+1} > \mu_S$. In this case, the $N+1$-th electron can be added from the drain and then it can leave the source electrode. This process allows electric current to flow, constantly switching the charge state of the dot between N and $N+1$.

When we sweep the gate voltage V_G, the electrochemical potential of the dot changes linearly with V_G and this allows one to change the number of electrons on the dot. The drain source current as a function of V_G at a low bias is illustrated in Fig. 2.8(c). The current characteristic shows a series of peaks as well as valleys. In the valleys, the number of electrons on the dot is fixed and the current is blocked by the charge addition energy $\frac{e^2}{C}+\Delta E$. This corresponds to the case depicted in Fig. 2.8(a). The dot has a well defined electron number in each valley; N, $N+1$,$N+2$ and so on. The conductance peak in this plot corresponds to the case depicted in Fig. 2.8(b), where the dot can oscillate between two adjacent charge states. For example, the conductance peak located between the N-electron valley and the $(N+1)$-electron valley represents the dot carrying current by oscillating between N and $N+1$ electron states. These conductance peaks are called Coulomb oscillations. To be able to observe Coulomb oscillations, the charge addition energy should be much larger than the thermal energy kT. Otherwise, thermal fluctuation effect will be dominant and the Coulomb oscillation will disappear. Also the electron number on the quantum dot should be a well-defined observable, which requires the contact between the dot and the leads to be resistive. Quantitatively, the contact resistance needs to be larger than the resistance of a single conductance channel (e.g. a point contact), $\frac{h}{e^2} \sim 25.81k\Omega$. These conditions are summarized below.

$$\frac{e^2}{C}+\Delta E \gg kT \tag{2.5}$$

$$R_{contact} \gg he^2 \tag{2.6}$$

To date, single electron transport behavior has been observed from many different nanostructures. They include metallic nanoparticles, semiconductor heterostructures, carbon nanotubes and semiconducting nanocrystals. More recently, similar behaviors were observed from devices made from single molecules.

2.5 Stability Plot

Proper operation of the SET requires proper biasing of gate and drains electrodes with respect to the gate electrode. Depending on the biasing, the SET can exhibit continuous oscillation characteristics in the drain current or a static ON state operation or a static OFF condition. Different regions of operation based on different level of biasing are best studied via stability plots. Depending on the biasing level, stability plot identifies the operating point of the SET describing whether the transistor will remain ON or OFF. Fig. 2.9 shows a typical stability plot with Coulomb diamonds. The diamond shaped shaded regions shown in the middle of the figure is called Coulomb diamond. These shaded regions correspond to particular value of gate and drain biasing (V_G and V_D respectively). These shaded diamonds are also known as stable regions for SET operation. While inside the region, there is always an excess amount of electron in the quantum dot island and so electron transport is effectively suppressed by the Coulomb blockade. Outside the stable region, there are numerous operating points where SET can be operated in a mode when it allows tunneling. In this mode of operation, the tunneling is not suppressed by the Coulomb blockade energy. The operating point, hence the mode of operation is defined both by the gate voltage (V_G) and the drain-source voltage difference (V_D).

2.6 Regions of Operation and I-V characteristics

Two separate conditions are described below to clarify the operating regions.

Case 1: Gate voltage fixed, Drain bias swept:

Fig. 2.10 shows a typical circuit setup for stability plot. As shown in Fig. 2.11, the gate voltage is fixed at some level and the drain-source voltage is swept from one direction to the other. One can observe three distinct regions of operation. Internal shaded region, where the electron tunneling is suppressed by the

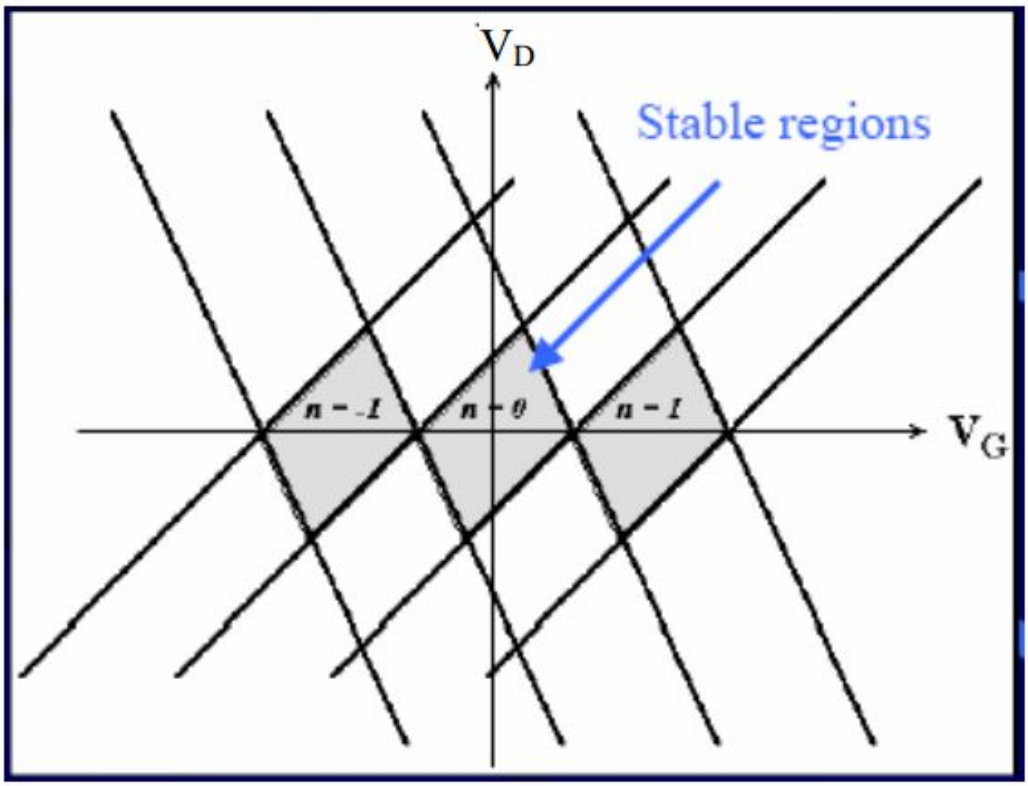

Figure 2.9: Stability plot. Shaded diamonds corresponds to stable region where electron transportation is effectively suppressed by Coulomb blockade.

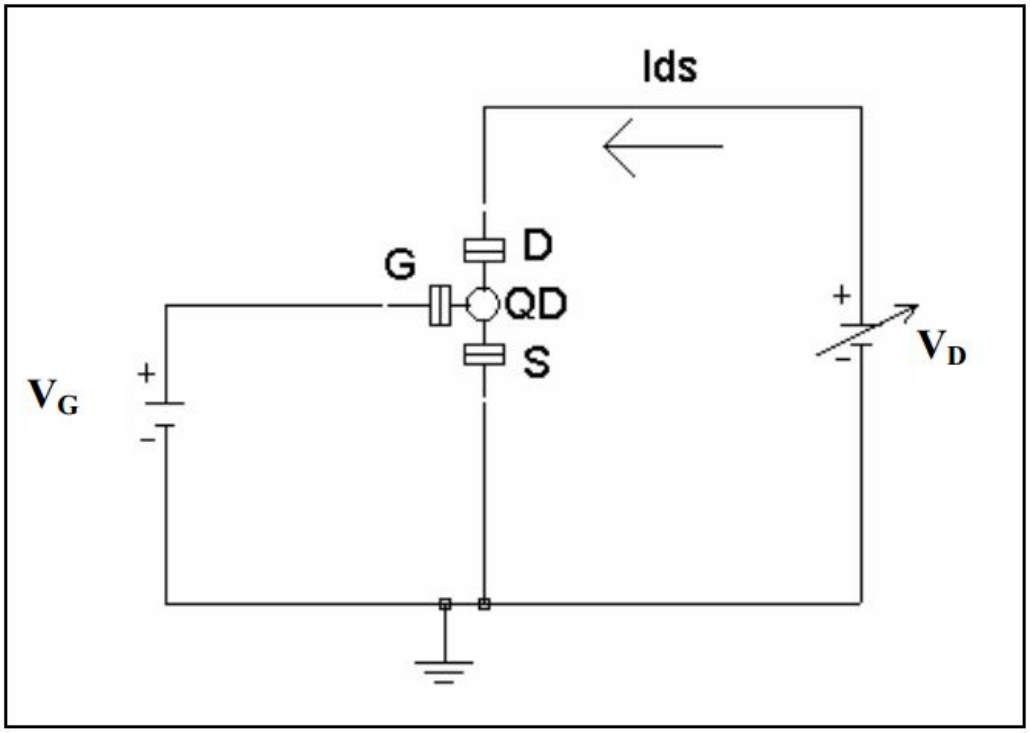

Figure 2.10: A circuit setup for stability plot

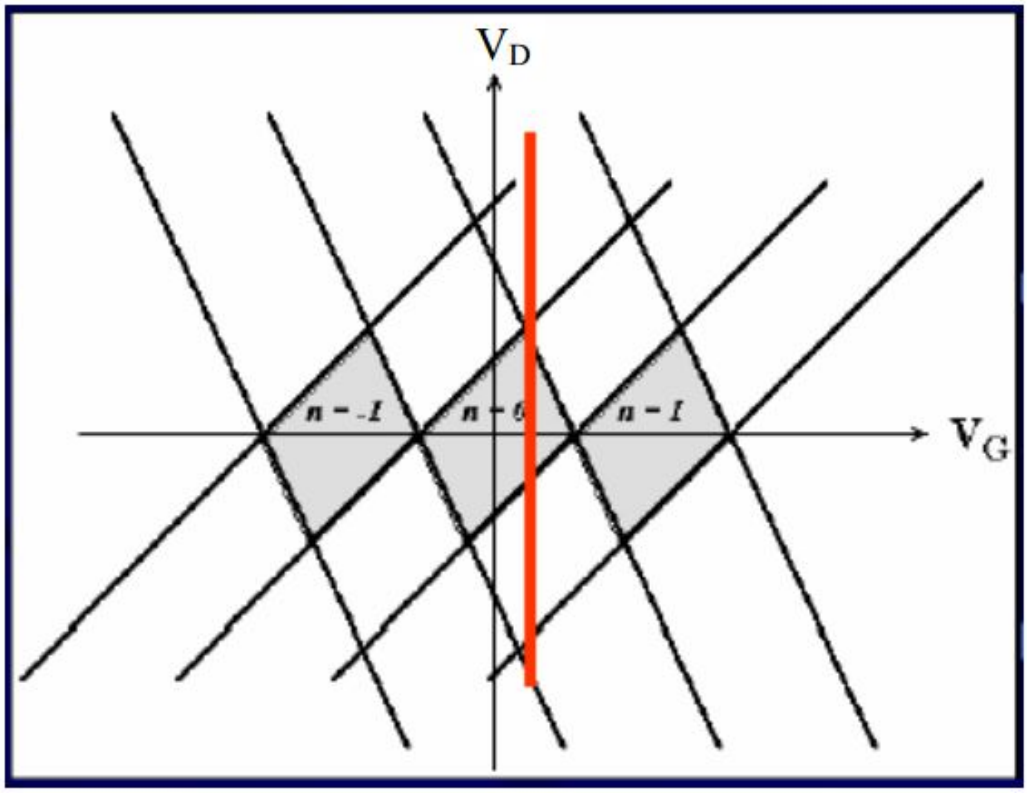

Figure 2.11: Stability plot. V_D(connected to drain electrode) is being swept while gate bias is kept constant

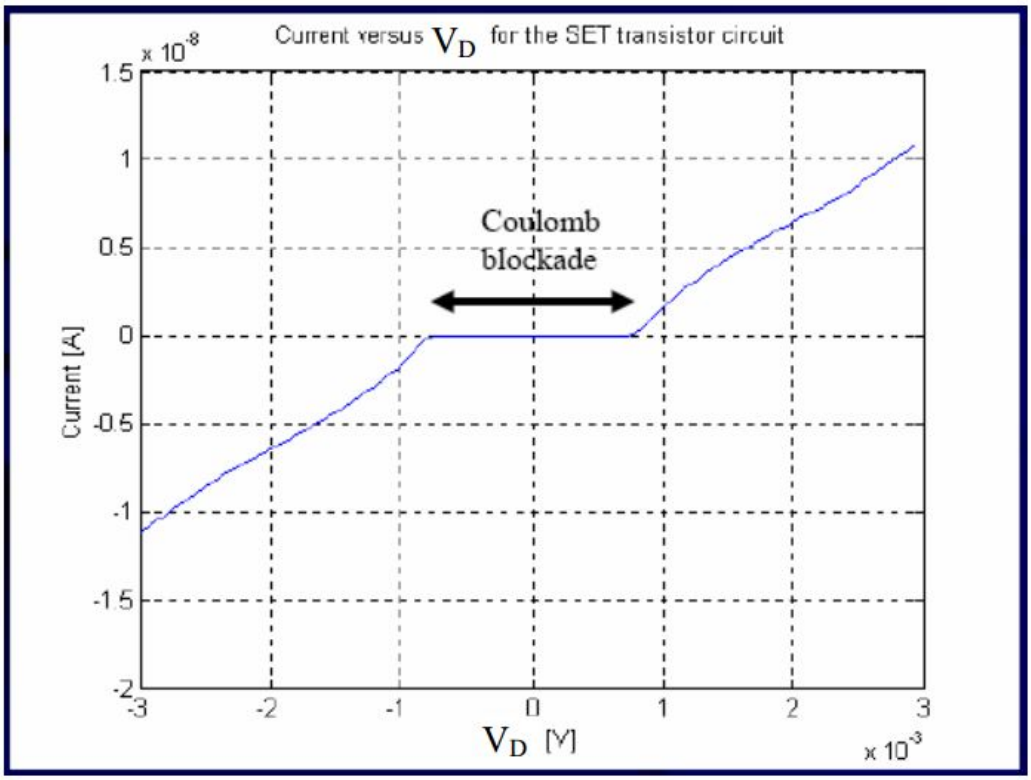

Figure 2.12: I_D vs V_D characteristics for a fixed gate bias. Two unstable (tunneling allowed) and stable (tunneling blocked) region are obvious.

Coulomb blockade is surrounded by the regions where tunneling is allowed. This region pattern doesnt repeat. Once the transistor is out of the stable region in either side, if the bias voltage continues to move in the same direction, it will never get another stable region. Thus at this condition the transistor has only one stable region (OFF state) which is bounded by two unstable regions (ON state). The resulting current voltage characteristic is shown in Fig. 2.12.

Case 2: Drain bias fixed, Gate voltage swept:

Similarly, if we can now setup the circuit as shown in Fig. 2.13, where the drain bias is fixed and the gate bias is being swept. This condition is much more interesting than the earlier condition. It is clearly seen from Fig. 2.14 that sweeping the gate potential from left to right while keeping the V_D fixed, traverses the transistor into alternating stable(OFF state) and unstable regions (ON state) of

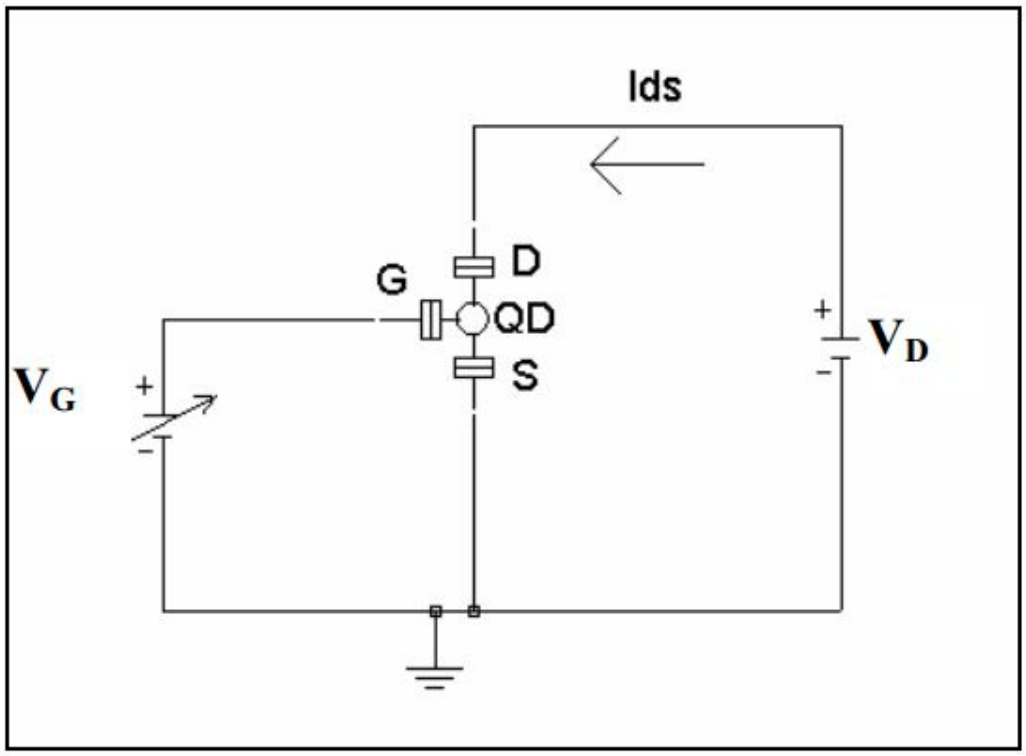

Figure 2.13: Modified circuit setup for stability plot

operation repeatedly. This condition gives a clear idea, how the changing potential at gate electrode creates OFF and ON states alternatively. Also it shows that, the V_D potential must be leveled to a certain value so as to ensure the successive ON-OFF regions of operations. If V_D is kept at zero level, the transistor will always remain in stable (OFF) condition. This happens as it enters a diamond immediately after coming out of another diamond-ensuring guaranteed OFF state. On the other hand if V_D is leveled too high so as not to intersect any shaded diamond, it keeps the transistor in permanent ON state. By carefully choosing V_D one can get alternative ON and OFF state by sweeping VG. Such a level of VD is illustrated in the Fig. 2.14.

As the gate voltage moves, the transistor experiences successive stable and unstable regions. These results, oscillating drain to source current. The result is shown in Fig. 2.15 depicting successive current peaks and valleys.

Stability plot (also called stability diagram) gives a clear insight of the region of operation as well as better understanding of the $I - V$ characteristics of the

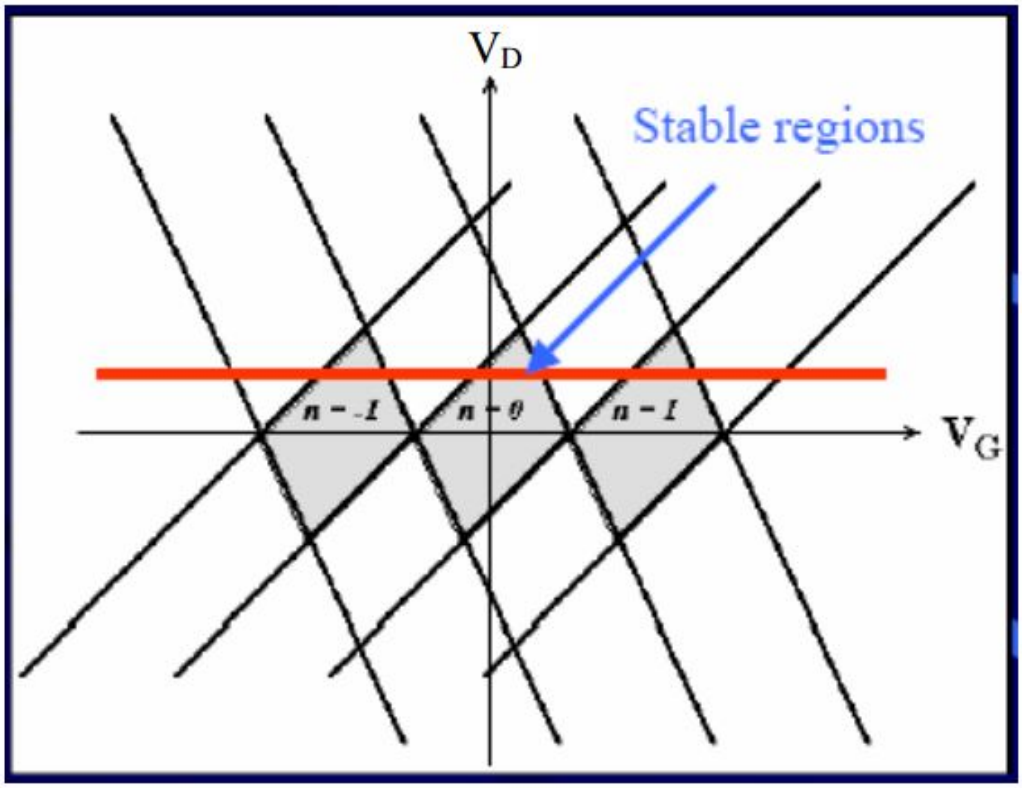

Figure 2.14: Sweeping V_G while V_D is kept constant. The transistor undergoes repetitive stable and unstable regions resulting oscillation drain current.

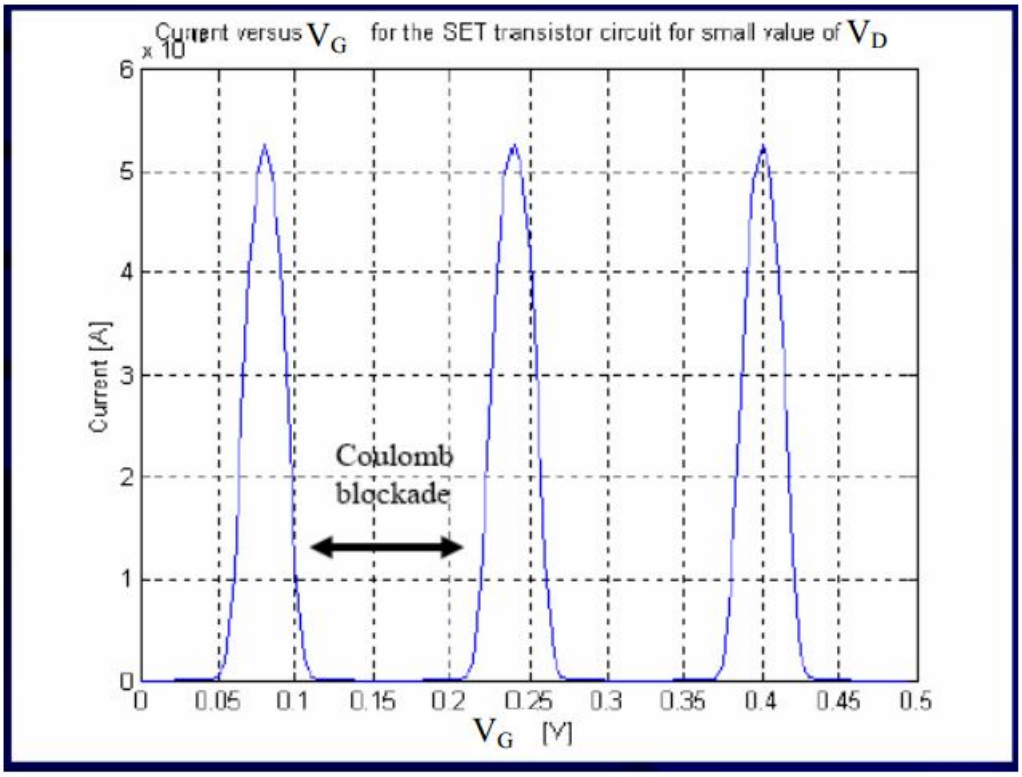

Figure 2.15: $I-V$ characteristics of SET. Coulomb oscillation with successive peaks and valleys resulting from the repetitive traversing of the transistor through unstable and stable regions

SET. By selecting biasing voltages the desired region of operation of the SET can be chosen which will deliver predicted current voltage characteristics.

Chapter 3

Dual Gate Single Electron Transistor

3.1 Introduction

A typical single electron transistor has one gate. Introduction of another gate (control gate and side gate) is needed for proper biasing and improved switching of a single electron transistor. This newly built device is called Dual Gate Single Electron Transistor. In this chapter the structure and operation of DGSET is discussed. Using different voltage in the gates the P-type and N-type DGSET can be created. Their operation is also discussed in this chapter.

3.2 Structure of Dual Gate SET (DGSET)

A dual gate single electron transistor has two gates. One gate is called the control gate. Another one is called the side gate or back gate. Control gate is used to take input for a digital circuit. Bias gate voltage makes the DGSET either P-type or N-type depending on the voltage applied on it.

In Fig. 3.1 the structure of a fabricated dual gate single electron transistor (DGSET) and the top view of it are given.

3.3 DGSET operation

Single Electron Transistor is based on the Coulomb Blockade phenomenon. As shown in Fig. 3.2, the structure of SET consists of two tunnel junctions separated

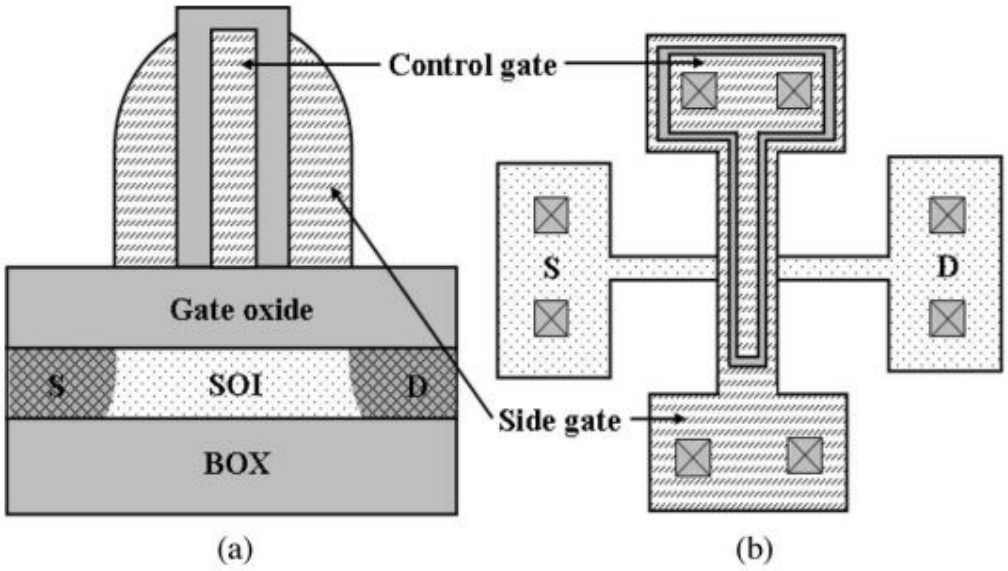

Figure 3.1: (a) Structure and (b) top view of the fabricated device

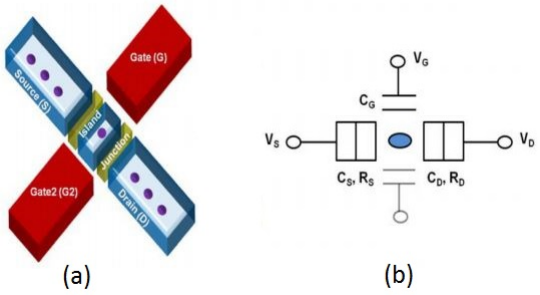

Figure 3.2: (a) 3D structure and (b) circuit representation of DGSET

from source and drain electrodes by a conductive island. In addition, two gates are coupled to the island enabling the ON/OFF state switch of the device. Each tunnel junction is depicted by junction capacitances (C_B, C_D) and tunneling resistances (R_S, R_D) as illustrated in Fig. 3.2.

The drain-source threshold voltage reduces or rises by changing the potential on the gate electrode (C_G). The threshold voltage dependence on gate voltage is a periodic function with period $\frac{e}{C_G}$. In fact the Coulomb Blockade is maximized when $V_{GS} = \frac{ne}{C_G}$ and vanishes when $V_{GS} = \frac{ne}{2C_G}$, where n is the number of electrons in the SET. In order to observe the Coulomb Blockade effect the tunnel junction resistances must be higher than the quantum resistances ($RT > 26k$), and the electrostatic charging energy must be greater than the thermal energy, $\frac{E_C}{2C} \gg kT$, where C the sum of the gate and junction capacitances, $k$is Boltzmanns constant and T the temperature.

3.4 Double Gate Single Electron Transistor Biasing

The bias conditions for turning SETs ON/OFF are introduced for two control gates. By exploiting the unique behavior of SETs i.e. periodicity of the Coulomb oscillations and the second gate capacitance we are able to have both pull-up and pull-down switching devices. In fact, the second gate enables to shift Coulomb Blockade region and thus we obtain P-type and N-type behavior by the same SETs transistors (Fig. 3.3). By applying an appropriate gate voltage, we can control charge transfer through the SET and then switch it from OFF state (Coulomb Blockade) to ON state (current conduction). Therefore, it is possible to build Boolean logic gates similar to existing in CMOS technology. The main advantage to use SETs that way is to reuse existing knowledge and design tools at very little cost and effort while overcoming fundamental physical restriction of CMOS technology.

For easier understanding the term background polarization charge or simply background charge or offset charge should be known. Apart from the charge effects of the voltages of gate, drain and source an additional background polarization charge Q_0 has been included on the center electrode, representing effects due to impurity charges located within the oxide barriers and any work function differences between the electrodes.

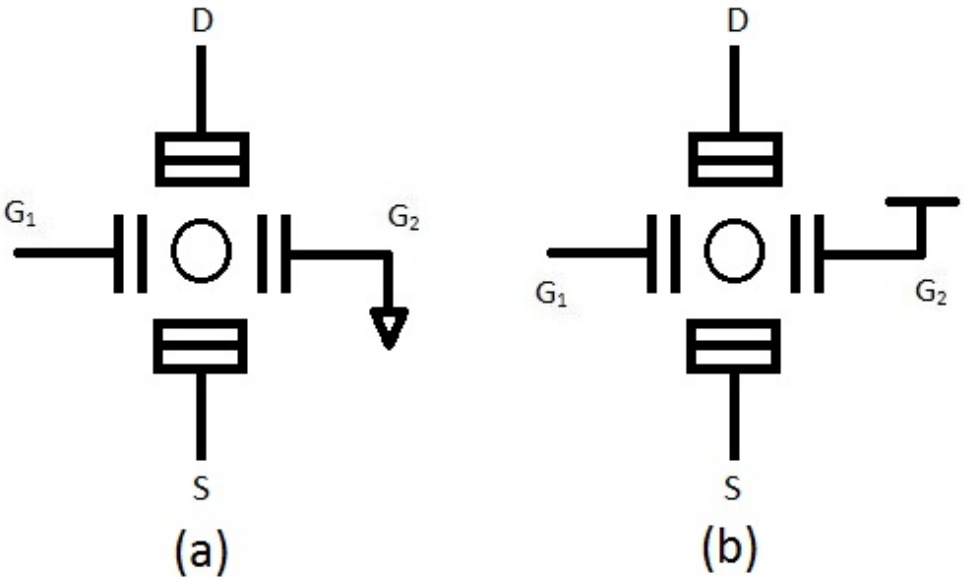

Figure 3.3: (a) P-Type, (b) N-type SET configuration

3.4.1 N-type DGSET

The device utilizes two separate capacitors coupled to the center electrode, labeled here as the bias capacitor C_G2, and the gate capacitor C_G1. Because this switch is intended for digital logic applications, only two voltage levels are to be present in stead state. These logic levels are indicated as ground (0) and supply voltage (V_DD). Junction 2 is connected to ground, and during a switching cycle voltages lying anywhere within the range $0 < V < V_{DD}$ may be present across the array at junction 1. The voltage applied across the switch will represent charges located on subsequent logic gates and interconnects, schematically represented in Fig. 3.4 by a load capacitor C_L. A high gate voltage $V_{G1} = V_{DD}$, should turn the double-junction switch on, draining the load capacitor and causing the output voltage across the device to fall all the way to $V = 0$. A low gate voltage $V_{G1} = 0$, on the other hand, should turn the double junction off, so that no current can flow even when the maximum voltage $V = V_{DD}$, is applied across the switch. Symmetry arguments show that a separate bias capacitor connected to the supply voltage V_{DD} is required in order to realize a double-junction on/off switch using only two voltage levels.

This threshold for junction 2 is plotted in Fig. 10 for a particular choice of example parameters which will be utilized throughout the following discussions,

$$C_1 = 2C_2, C_{G2} = 7C_2, C_{G1} = 8C_2, C_\Sigma = 18C_2, V_{DD} = \frac{1.5e}{2C_\Sigma} \tag{3.1}$$

The threshold voltage across junction 1 and 2 are given below respectively,

$$V_1(N) = \frac{1}{C_\Sigma}[(C_\Sigma - C_1)V - C_{G1}V_{G1} - C_{G2}V_{DD} - Ne] \tag{3.2}$$

$$V_2(N) = \frac{1}{C_\Sigma}[C_1V + C_{G1}V_{G1} + C_{G2}V_{DD} + Ne] \tag{3.3}$$

The total capacitance of the DGSET is,

$$C_\Sigma = C_1 + C_2 + C_{G1} + C_{G2} \tag{3.4}$$

3.4.2 P-type DGSET

Fig. 3.6 illustrates the complementary form of this device, the double-junction p switch. The p switch is to be connected between the positive supply and the output, with its bias capacitor grounded. Just as in standard CMOS, the n switch

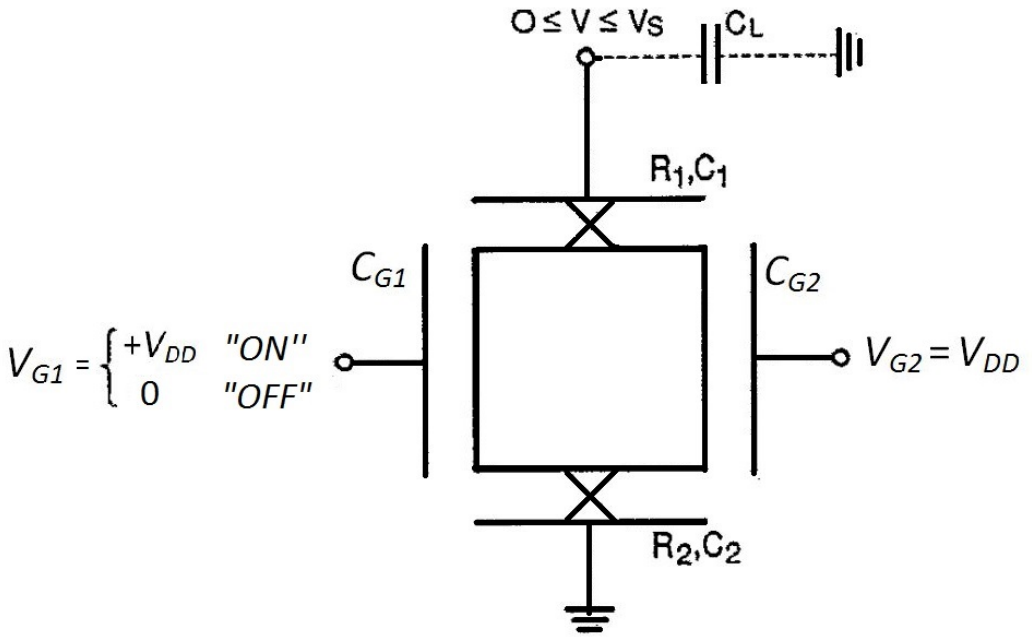

Figure 3.4: Capacitively biased double-junction n switch for digital logic applications. The switch is an open circuit for low gate voltage $V_{G1} = 0$, and drains charge off the output load capacitor C_L when high gate voltage $V_{G1} = V_{DD}$ is applied.

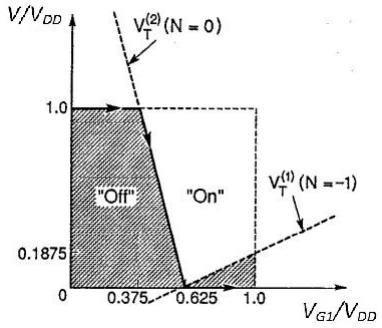

Figure 3.5: Output voltage appearing on the load capacitor C_L of the n switch in Fig. 3.4 as the gate voltage is swept quasistatically from off to on, $V_{G1} = [V_{DD}, 0]$

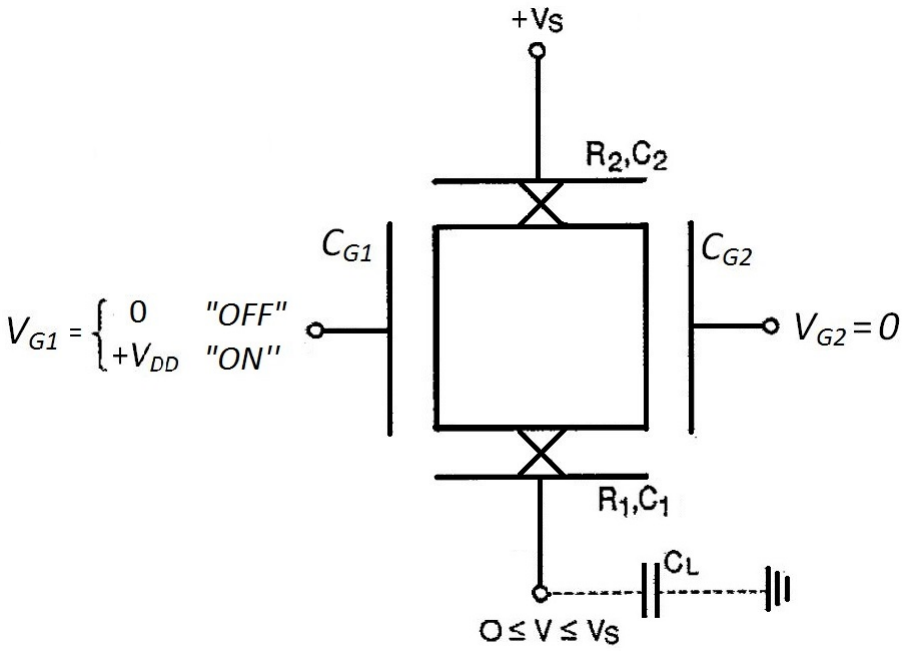

Figure 3.6: Capacitively biased double-junction p switch for digital logic applications. The switch is an open circuit for high gate voltage $V_{G1} = V_{DD}$, and drains charge off the output load capacitor C_L when low gate voltage $V_{G1} = 0$ is applied

will be on and the p switch off when the gate voltage is high, and conversely. Unlike CMOS, the n switch and p switch are physically identical devices, with asymmetry provided only by the biasing arrangements. The properties of the p switch may be obtained directly from those of the n switch via the following transformations,

$$V \to (V_{DD} - V), V_{G1} \to (V_{DD} - V_{G1}), N \to -N \tag{3.5}$$

As indicated in Fig. 3.6, the voltage appearing on the output terminal of the p switch lies within the range $0 < V < V_{DD}$ and the p switch will be nominally off for gate voltage $V_{G1} = V_{DD}$and on for $V_{G1} = 0$. Fig. 3.7 plots the quasistatic output voltage appearing across the p switch as it is turned from off to on for gate voltages $V_{G1} = [V_{DD}, 0]$ assuming the load capacitor C_L to be initially uncharged and using the example parameters given in Eq. (3.1). The p switch will be nonconducting in the shaded regions marked off in Fig. 3.7 with both junction voltages lying within the Coulomb gap. The p switch will be conducting in the unshaded the regions.

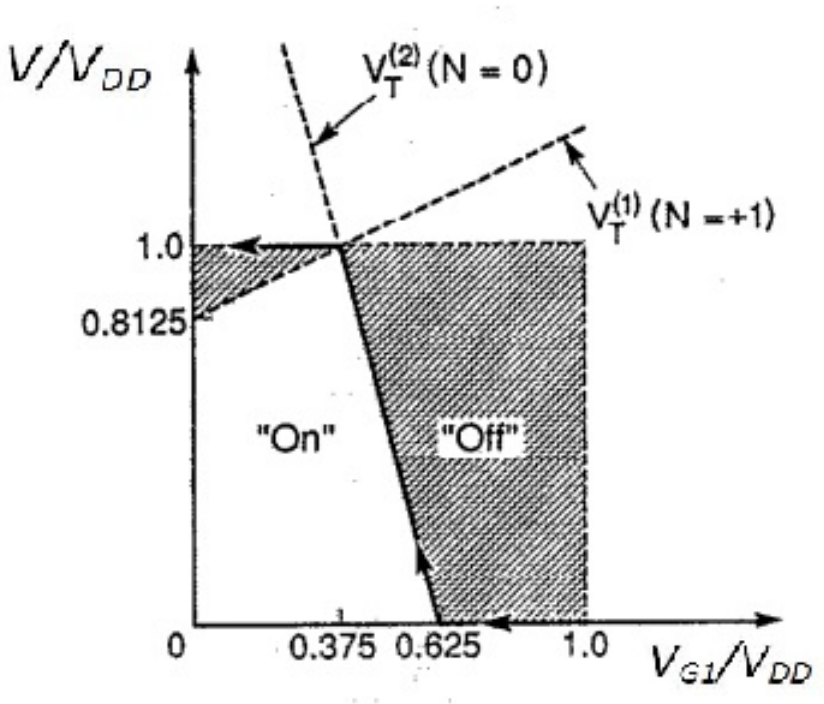

Figure 3.7: Output voltage appearing on the load capacitor C_L of the n switch in Fig. 3.6 as the gate voltage is swept quasistatically from off to on, $V_{G1} = [V_{DD}, 0]$

Chapter 4

Fabrication Techniques

4.1 Introduction

Charge quantization effects - single-electron tunneling - were first observed in thin granular metal films. Since the size and position of individual grains could not be controlled the effects were observed in an averaged way, which denied a more thorough and detailed study. However, I. Kulik and R. Shekhter devised a comprehensive theory for these systems. It took several years until single ultra small tunnel junctions could be manufactured reproducibly. The first process for metal tunnel junctions was developed by T. Fulton and G. Dolan and is referred to as 'shadow mask evaporation'. Today with this technique researchers routinely produce Al-Al_2O_3-Al tunnel junctions with $30nm \times 30nm$. In semiconductor structures a laterally patterned two-dimensional electron gas was used to form quantum dots. The size of the dots and tunnel junctions were still too big to observe single-electron phenomena at room temperature. The junctions had to be studied at cryogenic temperatures. Consequently a search for production techniques for even smaller tunnel junctions started, which brought about various techniques with Scanning-Tunneling-Microscopes and Atomic-Force-Microscopes. These experiments showed that single-electron effects are present at room temperature if the structure is sufficiently small. However, these laboratory procedures are not suitable for industrial mass production. Today the trend goes back to granular films, because their nano-meter size grains with self-assembling properties provide the small feature sizes required for room temperature operation without the need for atomic precision lithography for the definition of individual grains. Granular films have been produced and used for SET devices in metals and semiconductors. Another promising approach is to fabricate polymer coated metal clusters which are assembled to planar grain films. Electron-beam lithography, ion-beam lithog-

raphy and dry etching are preferred patterning techniques for the larger device structures.

4.2 SET Fabrication Techniques

From a physical point of few single-electron devices work fine and are understood well. Their characteristics are promising and their production would mean a huge step in the miniaturization of electronic devices. However, whether they will have an economical impact depends on the successful industrial mass production. In the following sections some of the many proposed and used production techniques are described.

4.2.1 Shadow Mask Evaporation

The shadow mask evaporation or 'hanging resist system' which is shown in Fig. 4.1 was developed by T. Fulton and G. Dolan. The junctions are fabricated by use of a lift-off stencil formed through electron-beam lithography. The suspended mask is a germanium layer deposited on top of a polymeric resist. Some of the underlying polymer is removed with the germanium resist coating, forming the overhang. After the first angled evaporation an oxidation step follows. Then the second evaporation with a different angle is done. Typical recorded junctions have an area of $30nm \times 30nm$. The technique is well proven, and has been successfully used to fabricate a number of devices. The disadvantage is that it is an elaborate procedure with many steps and the position of unused stripes has to be well thought of to prevent their interference with existing tunnel junctions.

4.2.2 Step Edge Cut Off

A simpler method for metal tunnel junctions is the step edge cut-off process shown in Fig. 4.2. The particular process shown was proposed by W. Langheinrich and H. Ahmed. A similar technique is from S. Altmeyer. A step or groove is formed, over which a metal line is deposited. The capacitance of this tunnel junctions are small compared to the junctions produced by the shadow mask technique, since there is no overlap of the electrodes at all. This process is especially suitable for material systems with lower barrier heights than Al_2O_3 (about 2 eV), such as Pb/Cr_2O_3 (0.02 eV) and Cr/Cr_2O_3 (0.06 eV). The lower barrier height allows a

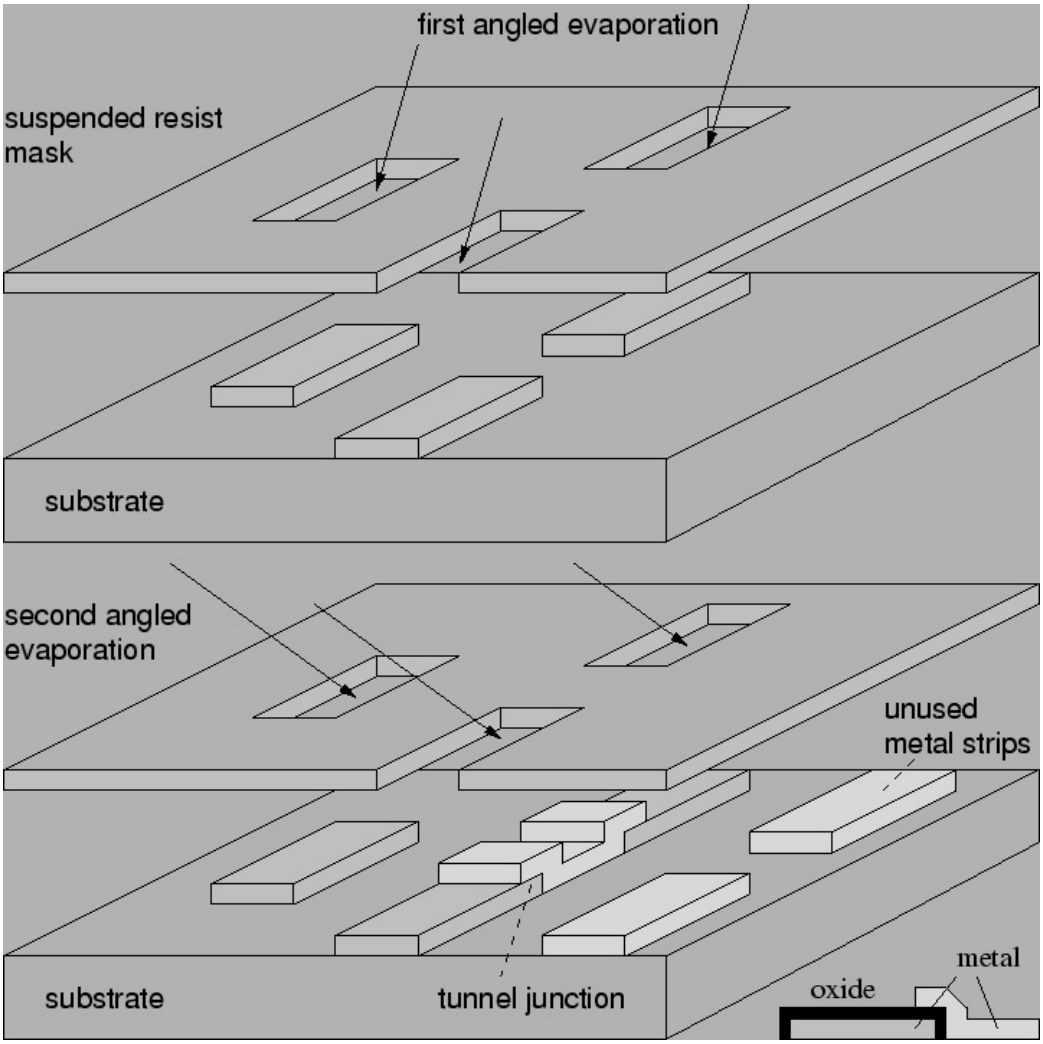

Figure 4.1: Shadow mask evaporation. Two metal depositions followed by an oxidation and a further metal deposition from a different angle form an overlap of two stripes; a tunnel junction.

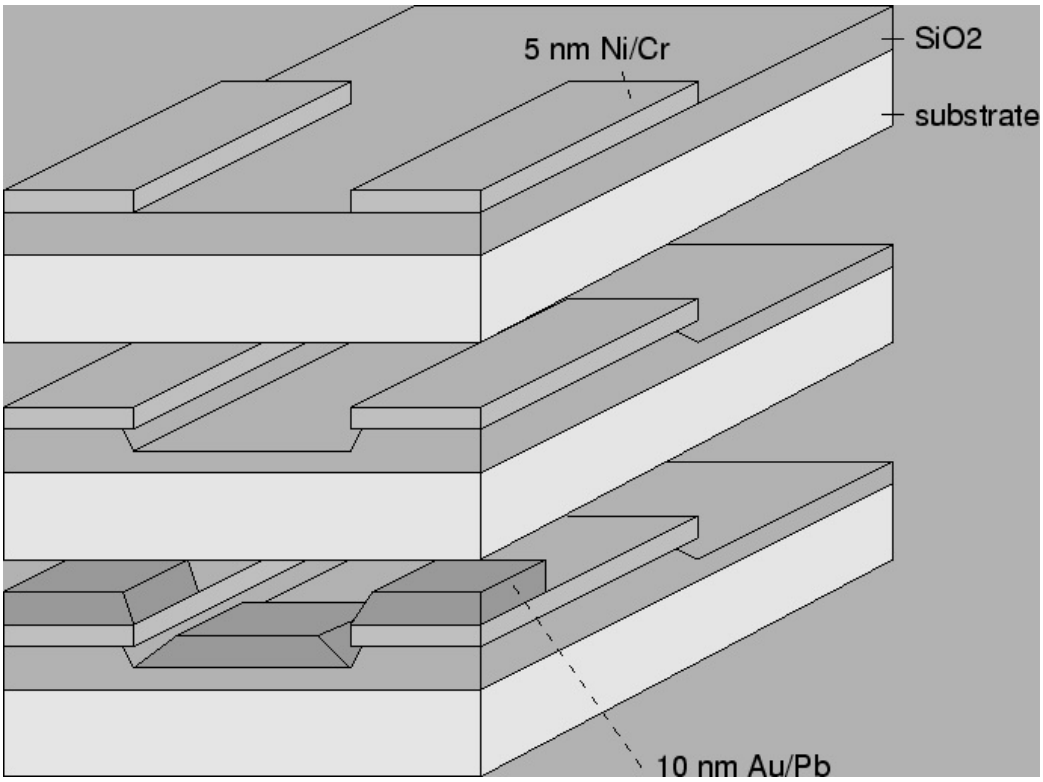

Figure 4.2: Step edge cut-off method. A metal line is evaporated over a step edge

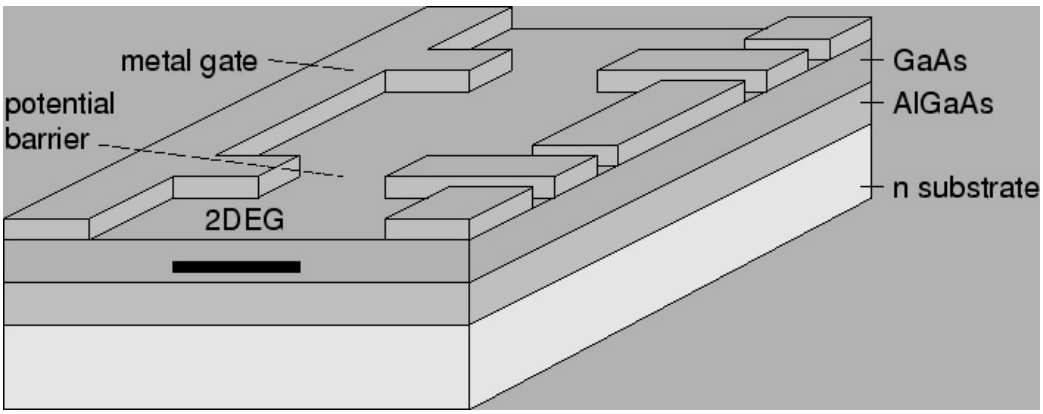

Figure 4.3: Laterally patterned two-dimensional electron gas in a semiconductor heterostructure. The fingers can be biased individually, which allows an independent change of barrier heights.

larger distance, about 10 nm compared to 1 nm, between the electrodes by equal barrier strength. This results in a further reduced tunnel junction capacitance and larger process tolerances.

4.2.3 Planar Quantum Dots

A commonly studied structure is a planar quantum dot, which is created by lateral patterning of several metal electrodes, or gates, on the surface of a two-dimensional electron gas. Often the heterostructure is formed by GaAs/AlGaAs layers, as shown in Fig. 4.3. Semiconductor quantum dots show richer characteristics, due to their larger energy level spacing. Interesting is, that the individual barrier heights are tunable by changing the finger electrode potentials. This is used to operate an oscillating-barrier turnstile, where the first barrier is lowered to let one electron pass into the quantum dot. Then this barrier is raised and the second barrier is lowered to let the electron exit the quantum dot. Electrons are passed turnstile like through the device. A different approach to realizing single-electron tunneling in semiconductors is to have current flow vertically with respect to heterostructure layers. The heterostructure layers provide vertical confinement and lithography defines in-plane confinement.

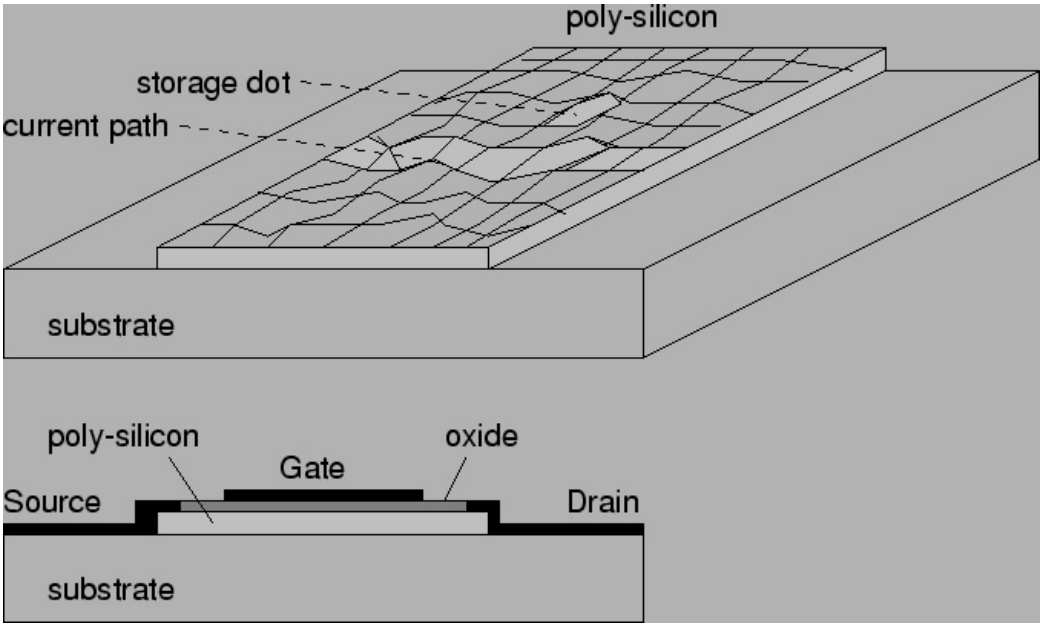

Figure 4.4: Poly-silicon batch contacted with a source, drain, and gate electrode. In the upper part the electrodes and oxide are left out. This structure behaves like a flash memory, where one electron is stored/trapped on a grain that lies close enough.

4.2.4 Poly Silicon Structures

A very promising technique is the patterning of a poly-silicon layer which is contacted with source, drain, and gate electrode. Fig. 4.4 shows the structure produced by K. Yano. They successfully built with it a 64-bit memory cell. Grain boundaries and varying grain size produce a 'Grand Canyon' like potential landscape. If a high enough bias voltage is applied to source and drain a narrow current path will form. An adjacent grain may act like a floating gate and modulate the current. By applying a high gate voltage, one electron is trapped in or ejected from this storage dot. It is a device which works close at the point, where one electron stores one bit of information. The advantage of semiconductor structures is that many production processes are well understood, controllable and for many years in permanent use. Additionally, semiconductor quantum dots show a discrete energy spectrum which enhances the Coulomb blockade, and which is favorable to reach a room temperature operation. However, this same advantage can turn into a disadvantage, whenever the absolute size of the Coulomb blockade is important. Small changes in grain size change unpredictably the Coulomb blockade in semi-

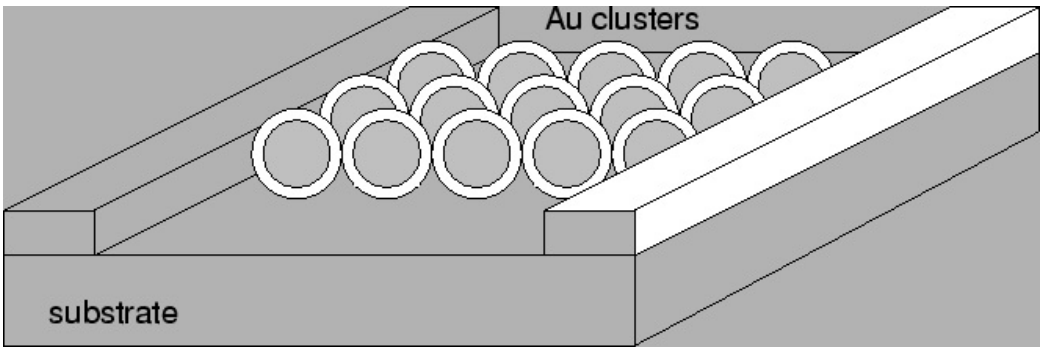

Figure 4.5: Array of linked gold clusters. The gold clusters are grown as aerosol particles, annealed, spread on a surface and linked with molecular wires.

conductor structures. Metallic structures are much more uniform in this respect.

4.2.5 Gold Clusters

Finally we want to mention linked gold clusters. Here a totally different approach of fabrication is followed. Instead of patterning or depositing material on a substrate, gold clusters, with a diameter in range from 1-20 nm with a narrow size distribution, covered with an organic layer are manufactured first. These clusters are then spread on a surface, as shown in Fig. 4.5, and linked with molecular wires, consisting of conductive organic molecules. The metal clusters are grown as aerosol particles in a gas aggregation reactor and are annealed in flight to yield perfect single crystal particles. An appealing feature is that this technique is close to an impurity and defect free production, which is, due to the extreme charge sensitivity of single-electron devices, a big advantage

4.3 DGSET Fabrication Techniques

A dual gate single electron transistor has an additional gate which is called side gate or bias gate. This difference in structure has made the fabrication technique different. Some DGSET fabrication techniques are discussed in this section.

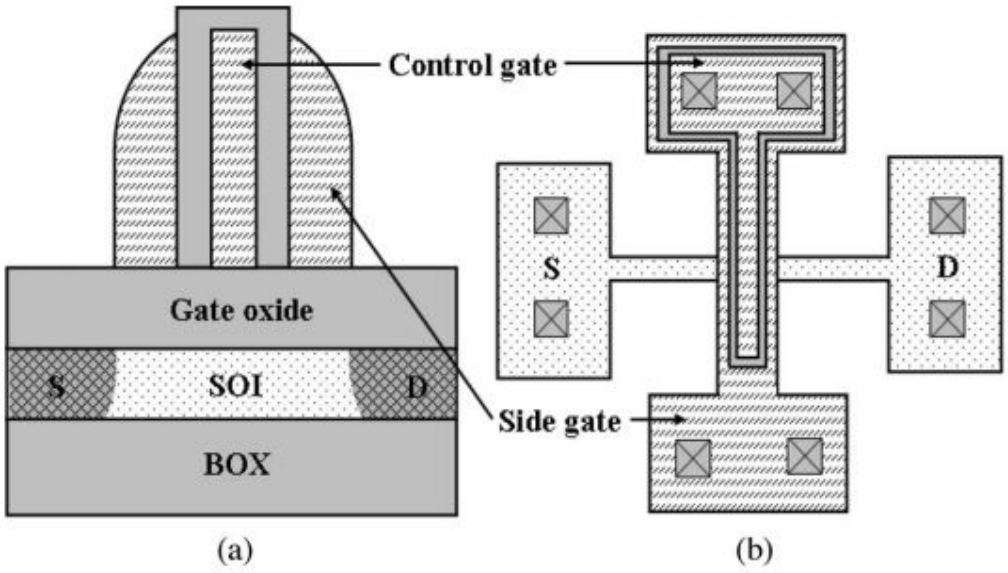

Figure 4.6: (a) Structure and (b) top view of the fabricated device

Self-Aligned DGSET

The basic device structure and main fabrication process flow are similar to the device presented in by our group, but the process parameters are modified to decrease the size of the quantum dot and improve its functionality, as shown in Fig. 4.6. The devices are fabricated on a p-type, separation-by-implantation of-oxygen (SIMOX) (1 0 0) wafer. The thickness of the buried oxide and initial top silicon layer is 360 and 200 nm, respectively. The top silicon layer that has a boron concentration of $1 \times 1015cm^{-3}$ is thinned down to 20 nm through repeated thermal oxidation and removal of the grown oxide. To prevent dopants acting as random barriers or quantum dots, no additional channel doping is conducted. The active region of which minimum width is 17 nm is defined through e-beam/photo mix- and match lithography and subsequent plasma silicon etches, as shown in Fig. 4.7. Next, 2.5 nm thermal oxide is grown at 850Cforfurther narrowing the active width and curing plasma etch damage. Afterwards, 22 nm control gate oxide and 105-nm amorphous silicon are deposited by plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD), respectively. To form the control gate, e-beam/photo mix-and-match process is carried out, and 20 nm minimum gate lengths are obtained. To isolate the control gate from the side gates, 10 nm inter gate oxide is formed through thermal oxidation of the

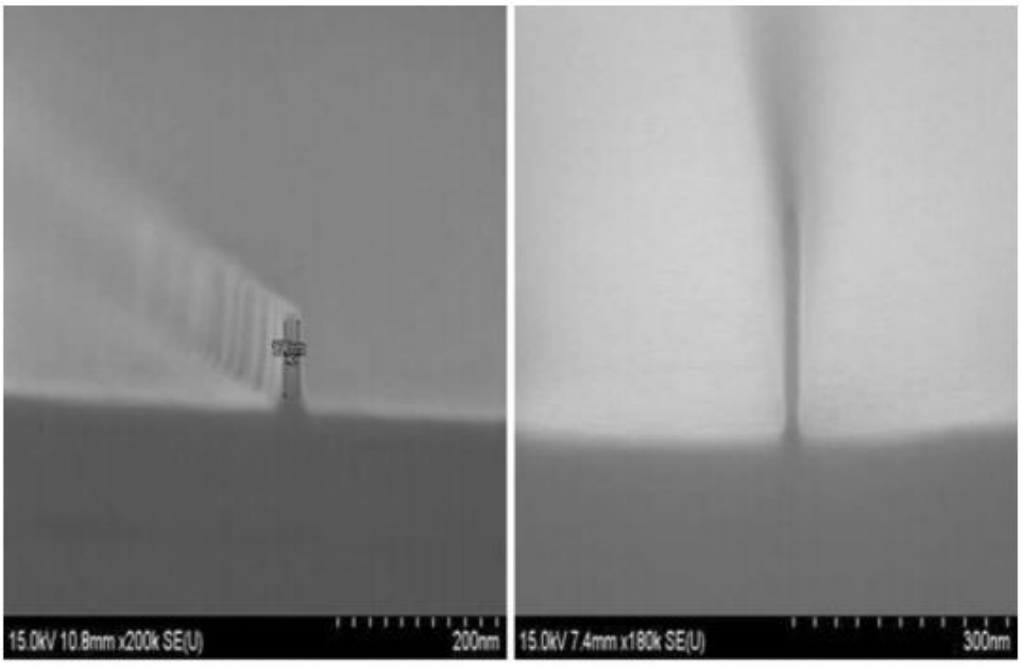

Figure 4.7: Cross-sectional SEM images of e-beam lithography test wafer for (a) active region (silicon) and (b) control gate (amorphous silicon). The width of the defined active is 17 nm and the length of the control gate is 20 nm.

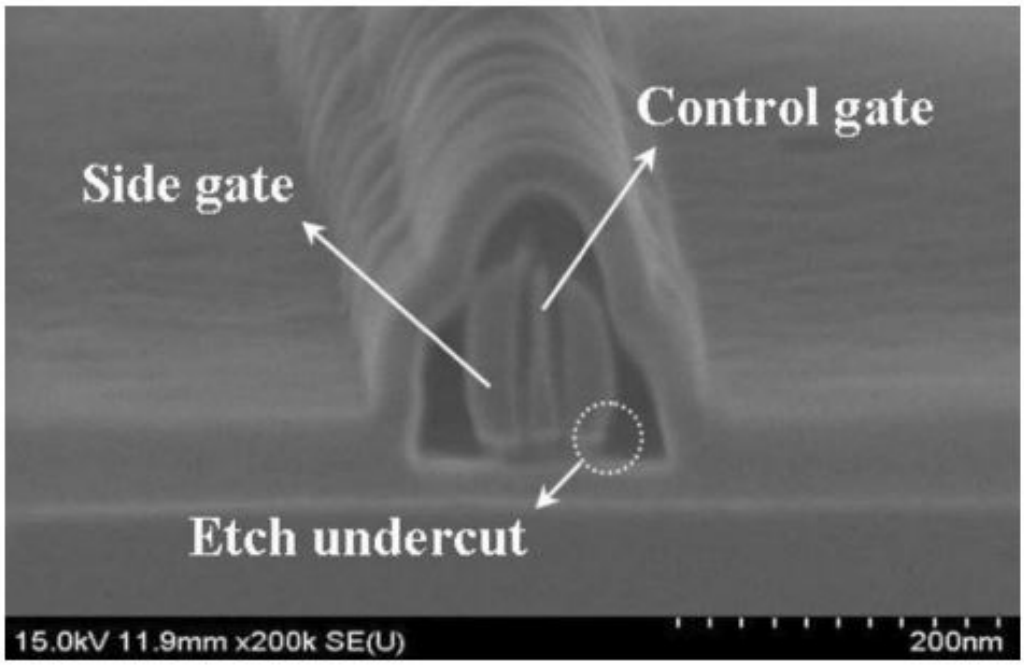

Figure 4.8: Cross-sectional SEM image of test wafer for side gate formation. Due to over-etch, etch undercut effect makes the length of the side gate bottom (25 nm) smaller than deposition thickness (30 nm). This result is advantageous for SET operation by reducing the tunneling barrier width and decreasing the capacitance between the side gate and the quantum dot

control gate, which reduces the control gate length to approximately 10 nm, and increases the gate oxide thickness to about 25 nm. Followed by the oxidation, 30 nm of amorphous silicon for the side gate is deposited. The side wall spacer that is formed by etching the deposited amorphous silicon becomes the side gate. In order to remove the residual amorphous silicon at the side of the silicon-on-insulator (SOI)active region, amorphous silicon for the side gate is over-etched, and etch undercut effect results in 5 nm decrease in the side gate length, as shown in Fig. 3. As+ ions are implanted at 11 keV after the tetraethoxysilane (TEOS) sidewall spacer formation. The dose is set to $1 \times 1015cm^{-2}$. Next, wafers are annealed at $1050°C$ for 7s in a rapid thermal anneal (RTA) tool to activate the dopants. Although RTA process results in dopant diffusion, the wide TEOS sidewall spacer results in an underlap structure. Afterwards, general backend process is conducted.

Chapter 5

Implementation of SET in Simple Digital Circuits

5.1 Introduction

Single Electron Transistors have the potential to be a very promising candidate for future computing architectures due to their low voltage operation and low power consumption. This chapter presents a family of digital logic cells based on DGSET.

5.2 SET Inverter

In digital logic, an inverter or NOT gate is a logic gate which implements negation. An inverter circuit outputs a voltage representing the opposite logic-level to its input. An inverter is the simplest digital circuit. Fig. 5.1 shows a CMOS inverter.

In this section the structure and operation of Complementary SET (CSET) inverter will be discussed using complementary logic. P-type an N-type DGSETs are used to build an inverter circuit.

5.3 Circuit Representation of SET Inverter

The DC characteristics of N-type and P-type DGSETs were shown in Fig. 3.5 and 3.7 respectively. If we use these two switches to replace the NMOS and PMOS

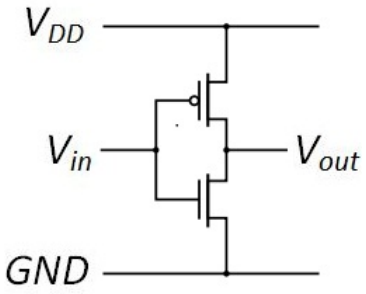

Figure 5.1: Schematic diagram of a CMOS inverter

of the CMOS inverter respectively in Fig. 5.1 the Complementary SET (CSET) inverter or simply SET inverter can be built.

5.4 SET Inverter Operation

Fig. 5.2 illustrates a CSET inverter. The combination of P-type and N-type DGSET results the operation of CSET inverter, which is illustrated in Fig. 5.3. The transfer characteristic shown in Fig. 5.3 is essentially ideal, and similar to its well-matched CMOS counterparts. The only notable difference is the presence of the shaded regions, where both n and p switches are off. Although not encountered under quasistatic operating conditions, it is interesting to note that even when the system enters these regions the errors tend to be self-correcting. Suppose, as an example, that for $V_{in} = V_{DD}$, on one inverter the output takes on its maximum error, $V_{out} = 0.1875V_{DD}$. When this becomes the input to a subsequent inverter gate, the maximum possible deviation on its output will be halved to $V_{out} = 0.90625V_{DD}$, and so on at each subsequent stage. This occurs because the slope of the threshold curves for junction 1 is $C_G/(C_\Sigma - C_1) = 1/2$ in this example.

5.5 Simple Digital Circuits using SET

The simple digital circuits which can be built with CMOS can also be built with DGSET. This implementation of SET has made the use of complementary SET possible. In this section simple digital circuits i.e. 2-input NAND gate and 2-input NOR gate circuit representation using DGSET is discussed. In these circuits the

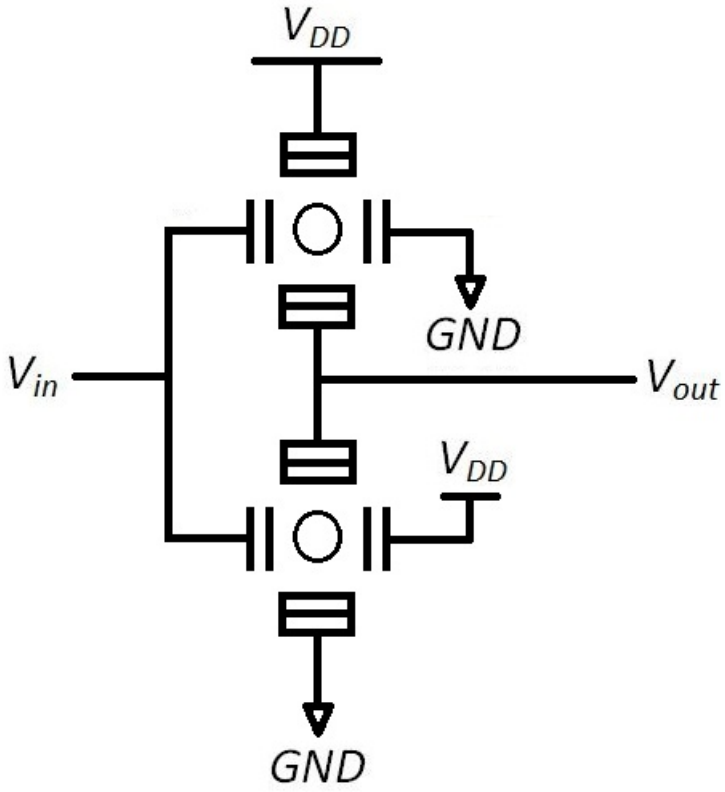

Figure 5.2: Schematic diagram of CSET inverter

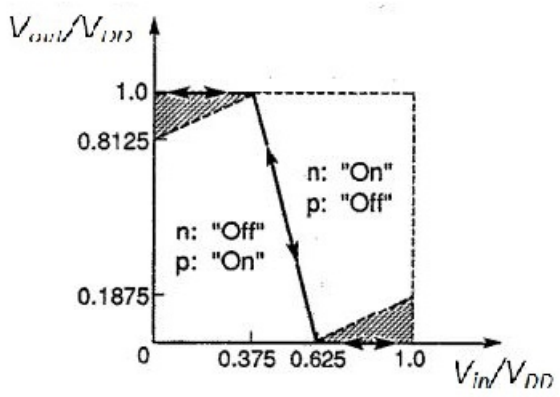

Figure 5.3: Transfer characteristic of the inverter circuit in Fig. 5.2, calculated for the example parameters given in Eq. 3.1

background charge, Q_0 is neglected.

5.5.1 2-input NAND Gate Using SET

Fig. 5.4 shows a 2-input CMOS NAND gate. It uses 2 PMOSes and 2 NMOSes or in short 2 CMOS. The PMOSes can be replaced by P-type SETs and the NMOSes can be replaced by N-type SETs. Thus the 2-input NAND gate can be built using SETs.

5.5.2 2-input NOR Gate Using SET

Fig. 5.6 shows a 2-input CMOS NOR gate. It uses 2 PMOSes and 2 NMOSes or in short 2 CMOS. The PMOSes can be replaced by P-type SETs and the NMOSes can be replaced by N-type SETs. Thus the 2-input NAND gate can be built using SETs.

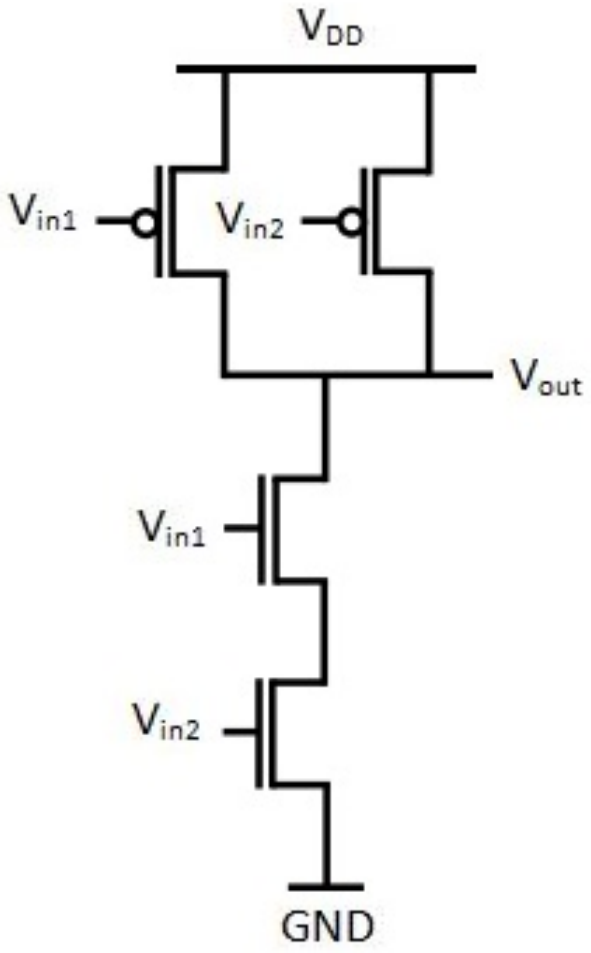

Figure 5.4: 2-input CMOS NAND gate

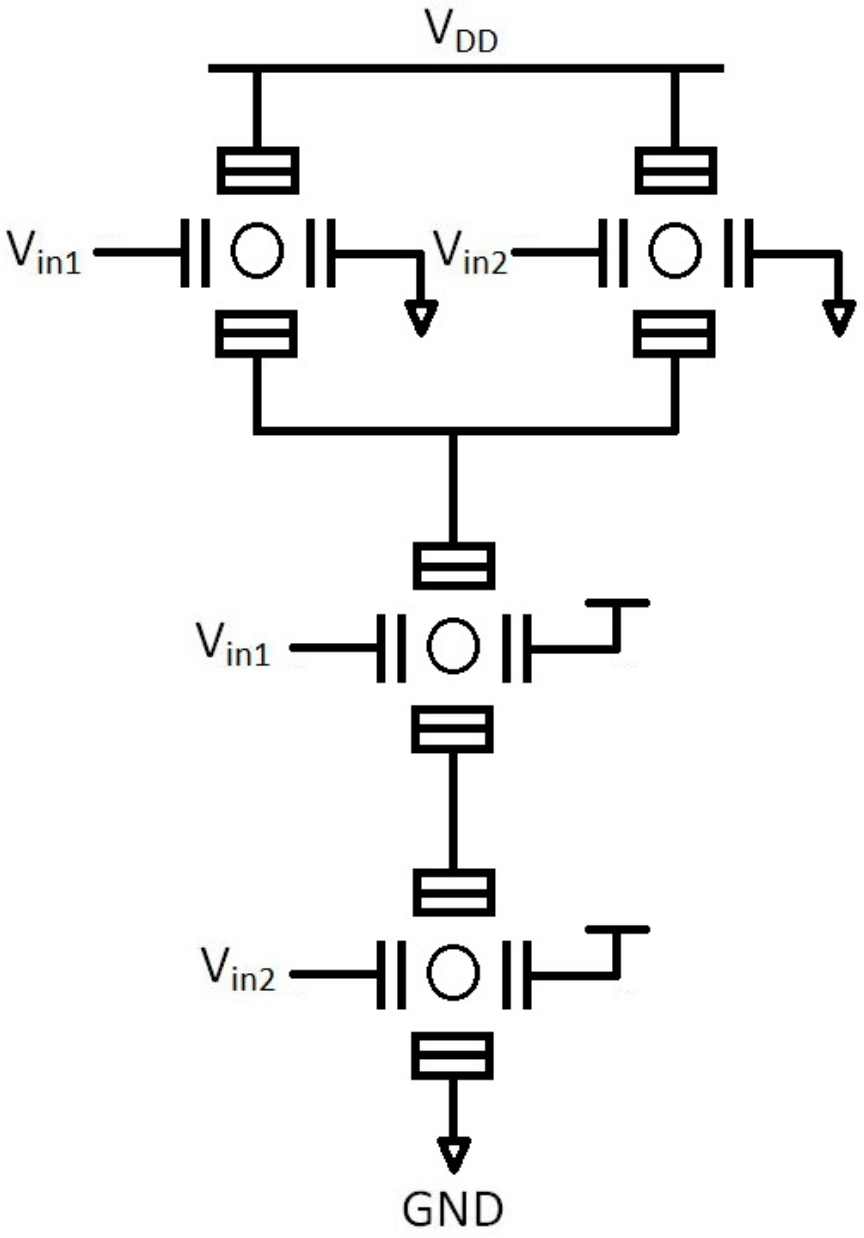

Figure 5.5: 2-input CSET NAND gate

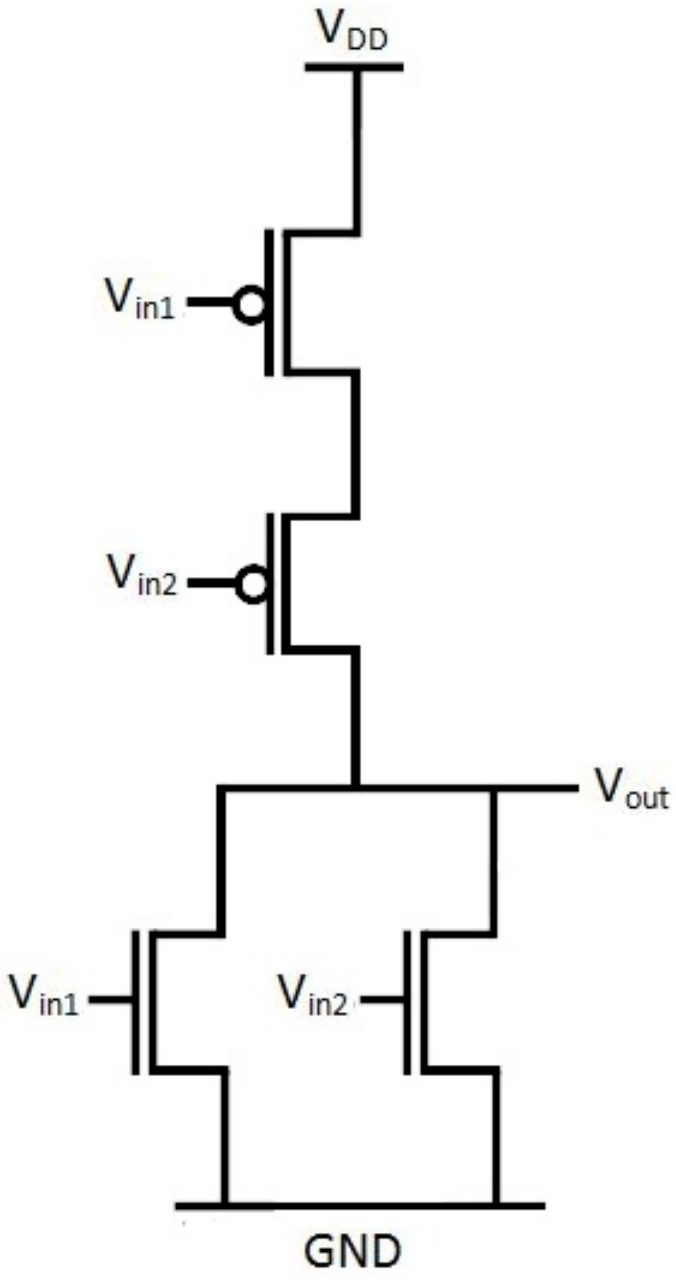

Figure 5.6: 2-input CMOS NOR gate

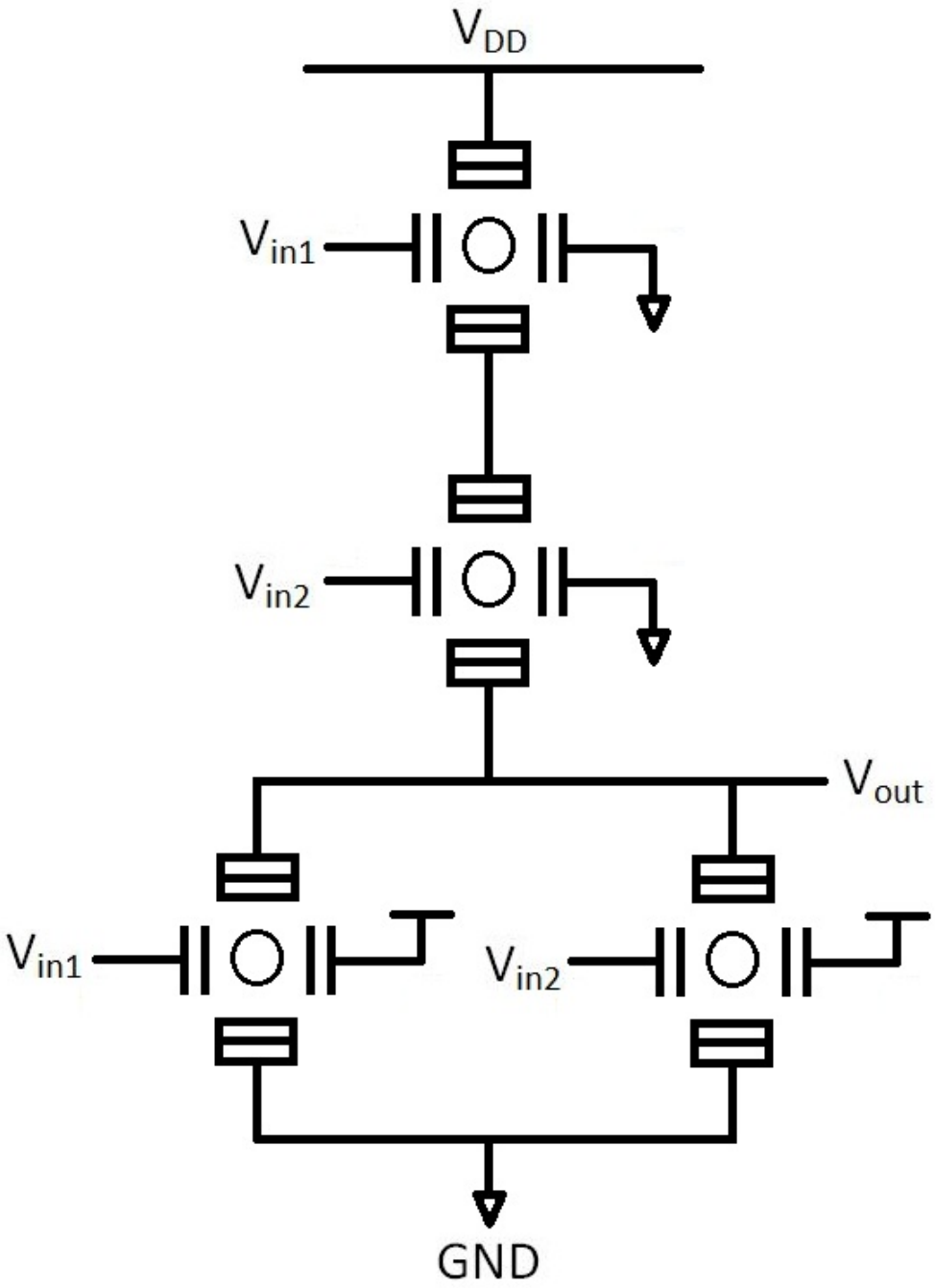

Figure 5.7: 2-input CSET NOR gate

Chapter 6

The model of SET

6.1 Introduction

An exact model for a single-electron transistor was developed within the circuit simulation package SPICE. This model uses the orthodox theory of single electron tunneling and determines the average current through the transistor as a function of the bias voltage, the gate voltage, and the temperature. Circuits including single-electron transistors, field-effect transistors (FETs), and operational amplifiers were then simulated. In these circuits, the single-electron transistors provide the charge sensitivity while the FETs tune the background charges, provide gain, and provide low output impedance.

Single-electron transistors (SETs) are used to perform sensitive charge measurements and are widely discussed as possible components of dense integrated circuits. These devices are attractive for applications in integrated circuits because they can be very small and they dissipate little power. However, SETs have low gain, high output impedances, and are sensitive to random background charges. This makes it unlikely that single-electron transistors would ever replace field-effect transistors (FETs) in applications where large voltage gain or low output impedance is necessary. The most promising applications for SETs are charge sensing applications such as the readout of few electron memories, the readout of charge-coupled devices, and precision charge measurements in metrology. In these applications, field effect transistors are used to buffer the high output impedance of SET transistors and to automatically tune the background charges. Here a SPICE model is presented for a single-electron transistor that can be used to perform simulations of circuits where single-electron transistors are combined with other circuit elements.

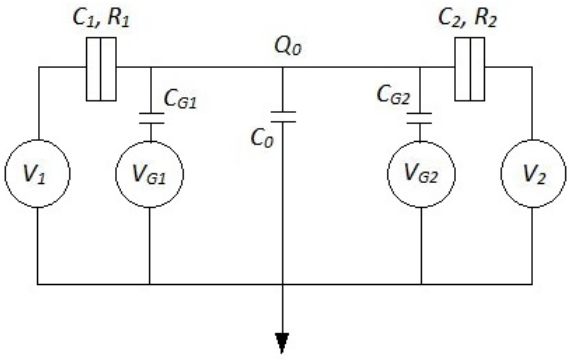

Figure 6.1: A schematic diagram of a single-electron transistor showing the two tunnel junctions, two gates, the stray capacitance C_0, and the background charge Q_0

6.2 The Model

Figure 6.1 shows a schematic of a SET indicating the two tunnel junctions. In the model described here, two gates are coupled to the island. This is because many circuit applications require SETs with two gates. A voltage source is attached to each electrode (the source, the drain, and the two gates). In addition to the two gates, a stray capacitance C_0 to ground and a background charge Q_0 are included in the model. To determine the average current that flows through the transistor, first the voltages of the island for the relevant charge states must be calculated. Simple electrostatics will show that the voltage of the island when a charge of ne is present on the island is,

$$V(n) = \frac{(ne + Q_0 + C_1V_1 + C_2V_2 + C_{G1}V_{G1} + C_{G2}V_{G2})}{C_\Sigma} \tag{6.1}$$

Here e is the positive elementary charge, n is an integer that specifies the number of elementary charges that have been added to the island, $C = C_1 + C_2 + C_{G1} + C_{G2} + C_0$ is the total capacitance of the island of the transistor, and the other quantities are defined in Fig. 6.1. The energy it takes to move an infinitesimally small charge dq from ground at a potential $V = 0$ to the island is $V dq$. As soon

as charge is added to the island, the voltage of the island changes. By integrating VdQ from 0 to e one can show that the electrostatic energy needed to add a charge e to the island is,

$$eV(n) + \frac{e^2}{2C_\Sigma} \tag{6.2}$$

The change in energy when a charge e tunnels from a lead at voltage V_i to the island is thus,

$$\Delta E_i = -eV_i + eV(n) + \frac{e^2}{2C_\Sigma} \tag{6.3}$$

When a charge of e tunnels from the island to a lead, the signs of the first two terms in Eq. 2.3 are reversed. The change in energy can be used to calculate the tunnel rate, which is given by the expression,

$$\Gamma_i = \frac{\Delta E_i}{e^2 R_i[\exp(\frac{\Delta E_i}{kT}) - 1]} \tag{6.4}$$

where R_i is the tunnel resistance, T is the temperature and k is Boltzmanns constant. There are four possible single-electron tunneling events for a SET. A charge e can tunnel left through tunnel junction 1 (Γ_{1L}), one can tunnel right through tunnel junction 1 (Γ_{1R}), one can tunnel left through tunnel junction 2 (Γ_{2L}), or one can tunnel right through tunnel junction 2 (Γ_{2R}). Higher order tunnel events where two or more electrons tunnel simultaneously are not considered in this model.

Once the rates for all the relevant charge states have been determined, the probabilities that the charge states are occupied can be determined from the recursion relation,

$$P(n) = P(n-1)\left(\frac{\Gamma_{2L}(n-1) + \Gamma_{1R}(n-1)}{\Gamma_{2R}(n) + \Gamma_{1L}(n)}\right) \tag{6.5}$$

The average current flowing through the transistor in the direction from tunnel junction 1 to tunnel junction 2 is,//

$$I = \sum_n eP(n)\left(\Gamma_{1R}(n) - \Gamma_{1L}(n)\right) \tag{6.6}$$

and the average voltage of the island is,//

$$V = \sum_n P(n)V(n) \tag{6.7}$$

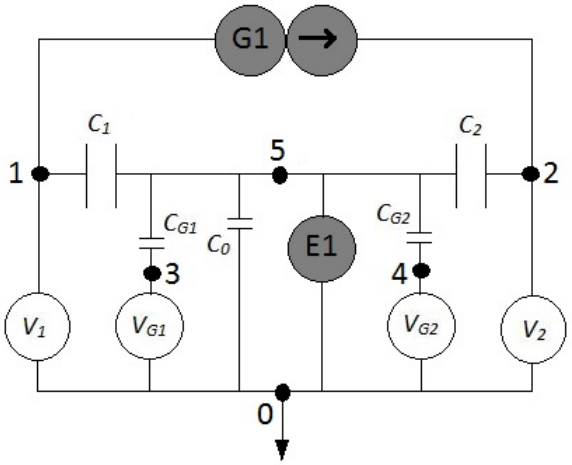

Figure 6.2: The model of a SET in SPICE. The white voltage sources are external to the SET model and the gray sources are internal to the model. E1 is a voltage source that fixes the voltage of the island of the SET (node 5) using eq. (6.7) and G1 is a current source that specifies the source - drain current using eq. (6.6).

To efficiently calculate the current and voltage, first the charge state n that has the highest probability to be occupied should be determined. This charge state can be estimated using Eq. 6.5. The most probable charge state is,//

$$n_{opt} = -\frac{(Q_0 + C_1V_1 + C_2V_2 + C_{G1}V_{G1} + C_{G2}V_{G2})}{e} + \frac{C_\Sigma}{e}\frac{V_1R_2 + V_2R_1}{R_1 + R_2} \qquad (6.8)$$

Eq.s 6.1 6.8 were implemented in SPICE to calculate the values for the voltage source E_1 and the current source G_1 in the SPICE-SET model depicted in Fig. 6.2. The exact SPICE of the SET Model is uploaded in this website http://lamp.tu-graz.ac.at/ hadley/set/spice/. The model can handle arbitrarily large gate voltages. Depending on the number of charge states implemented in the model, it can also handle arbitrarily high bias voltages and temperatures. The simulation time is linearly dependent on this number of charge states. The simulations described here were performed with a SPICE-SET model that includes eleven charge states around the most probable charge state. This is sufficient to perform room temperature simulations of transistors with a total capacitance of a few atto Farads. It is straightforward to extend this model to include more charge states as outlined in

the source code on the Internet. By comparing the charging energy with the electron energies that are provided by the temperature and the expected maximum voltage difference V_{max} between source and drain, the number of charge states necessary can be estimated by,

$$n \approx \frac{2C_{\Sigma}}{e^2} \left(e\Delta V_{\max} + 7kT \right) \tag{6.9}$$

Here we have chosen to consider only electrons with a thermal energy of less than $7kT$ which leaves us with an accuracy of about e^{-7} for the tunnel rates, ie. the accuracy is in the 0.1 percent range.

Chapter 7

Digital Circuits Using SET and Simulation Results

7.1 Introduction

In this chapter circuit diagrams and simulation results are attached. The results show pretty good results. All the simulations were done in the temperature $27k$. Initially the background charge Q_0 was not considered. Later the background charge was considered. The model was built by *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley.* Using this model we built inverter, NAND gate, NOR gate, half adder and full adder circuits and run their simulations. All the circuits used complementary SET (CSET).

7.2 SET Inverter

We have built four different circuits. At first we did not consider background charge Q_0. We built two circuits and analyzed their results. Next we built two more circuits considering background charge Q_0 and analyzed their simulation results. Among these circuits we chose the best bias for SETs and use this biasing in the next circuits.

7.2.1 SET Inverter Siulation Not Considering Background Charge

We have built two circuits of SET inverter considering background charge, Q_0. For N-type DGSET $Q_0 = 0.15e$ and for P-type DGSET $Q_0 = -0.15e$ was considered. We considered the temperature $27k$ and the supply voltage $V_{DD} = 35mV$.

In first circuit we used the biasing used by Professor Tucker and in the second circuit we used the biasing used by *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley.*

Biasing used by Professor Tucker Not Considering Q_0

Professor Tucker used the side gate bias voltages as $0mV$ (for P-type DGSETs) and $35mV$ (for N-type DGSETs).He used the following equations for biasing,

$$C_1 = 2C_2,\ C_{G2} = 7C_2,\ C_{G1} = 8C_2, C_{\Sigma} = 18C_2 \text{ and } V_{DD} = 1.5e/2C_{\Sigma} \tag{7.1}$$

We used these data in the SET SPICE model and analyzed the DC and transient characteristics of the SET inverter circuit. We used $V_{DD} = 35mV$. Thus we get the following capacitive values,

$C_1 = 3.809524\times10^{-19}Coulomb$, $C_2 = 1.904762\times10^{-19}Coulomb$, $C_{G1} = 1.5238095\times 10^{-19}Coulomb$ and $C_{G2} = 1.3333333 \times 10^{-19}Coulomb$.

The following resistive values were used in this simulation,

$R_1 = 10^5\Omega$ and $R_2 = 10^5\Omega$.

Fig. 7.1 depicts the circuit diagram of SET inverter using the bias values of *Professor Tucker.*

Fig. 7.2 and Fig. 7.3 show the DC analysis and transient analysis respectively for this biasing. We have generated the numerical values of input and output voltages

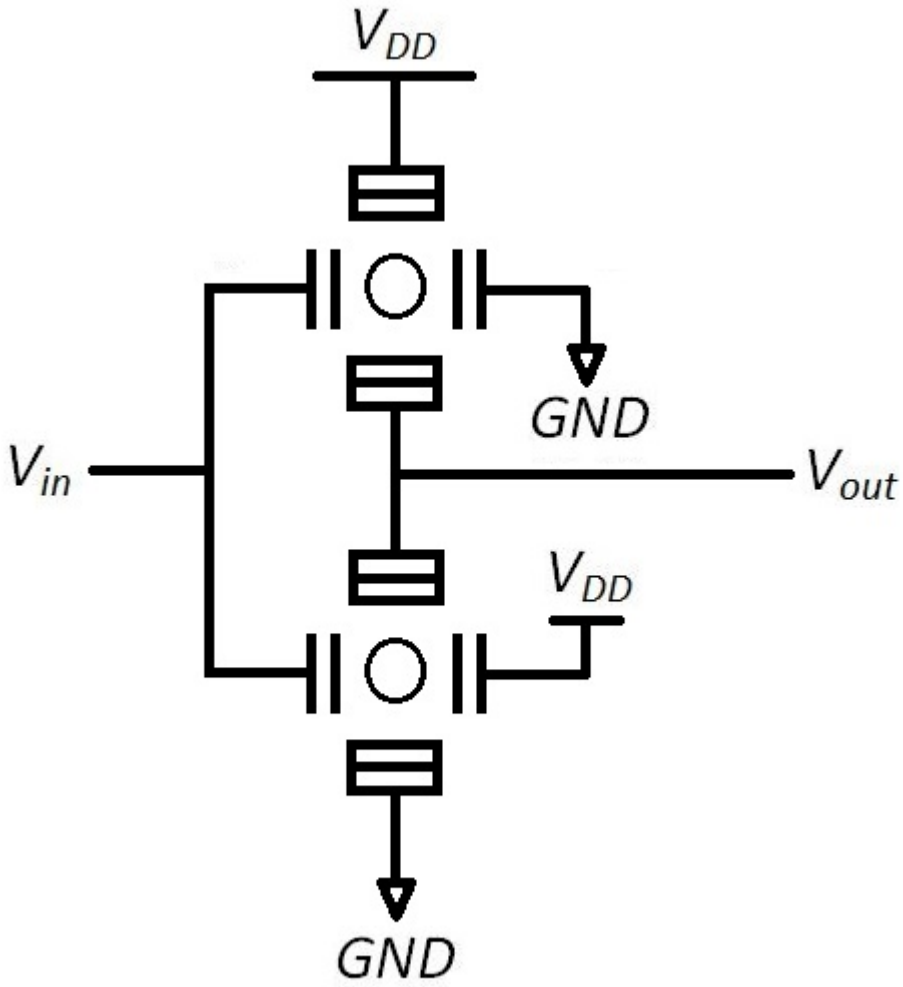

Figure 7.1: SET Inverter using the bias value of *Professor Tucker* considering $Q_0 = 0$

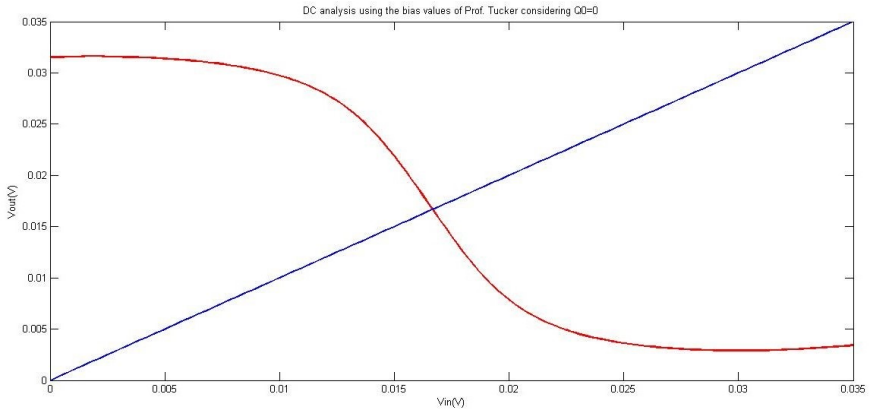

Figure 7.2: DC analysis using the bias values of *Professor Tucker* considering $Q_0 = 0$

and plotted them in MATLAB.

Results of DC Analysis:

Inversion Voltage:
$V_{inv} = 16.540mV$.

Results of Transient Analysis:

Steady State Output Low Voltage $= 9.881mV$
Steady State Output High Voltage $= 31.517mV$
10% of Voltage Range $= 6.22655mV$
90% of Voltage Range $= 28.70695mV$

Rise Time:
Time at $V_{out} = 6.2428mV$, $t_1 = 22.365ns$
Time at $V_{out} = 28.671mV$, $t_2 = 22.928ns$
Rise Time, $t_r = t_2 - t_1 = (22.928 - 22.365)ns = 0.563ns$.

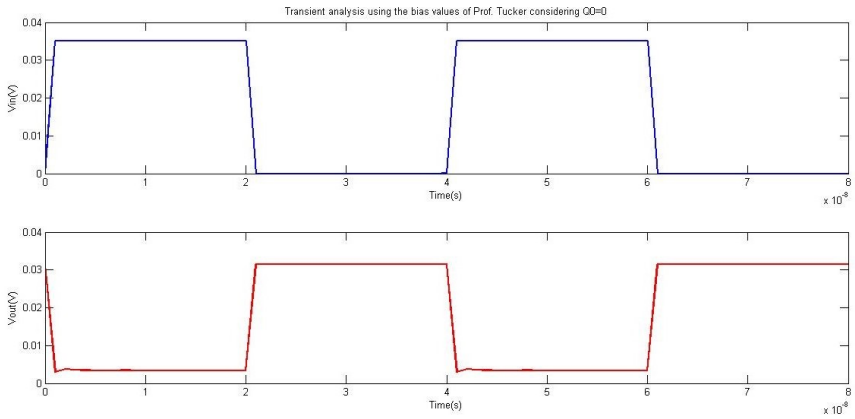

Figure 7.3: Transient analysis using the bias values of *Professor Tucker* considering $Q_0 = 0$

Fall Time:
Time at $V_{out} = 28.671mV$, $t_1 = 41.329ns$
Time at $V_{out} = 6.2428mV$, $t_2 = 41.929ns$
Fall Time, $t_f = t_2 - t_1 = (41.92941.329)ns = 0.600ns$.

Biasing used by Professor Lientschnig Not Considering Q_0

Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley used the side gate bias voltages as $0mV$ (for both N-type and P-type DGSETs). They the following capacitive values for biasing,

$C_1 = 10^{-18}Coulomb$, $C_2 = 10^{-18}Coulomb$, $C_{G1} = 2 \times 10^{-18}Coulomb$ and $C_{G2} = 0Coulomb$.

The following resistive values were used in this simulation,

$R_1 = 10^5\Omega$ and $R_2 = 10^5\Omega$.

Fig. 7.4 depicts the circuit diagram of SET inverter using the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley.*

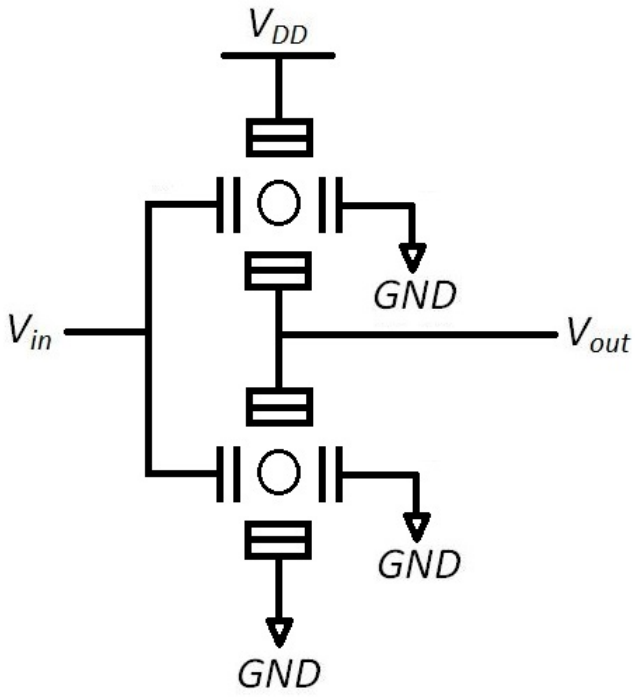

Figure 7.4: SET Inverter using the bias value of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = 0$

Fig. 7.5 and Fig. 7.6 show the DC analysis and transient analysis respectively for this biasing. We have generated the numerical values of input and output voltages and plotted them in MATLAB.

Results of DC Analysis:

Inversion Voltage:
$V_{inv} = 17.500mV$.

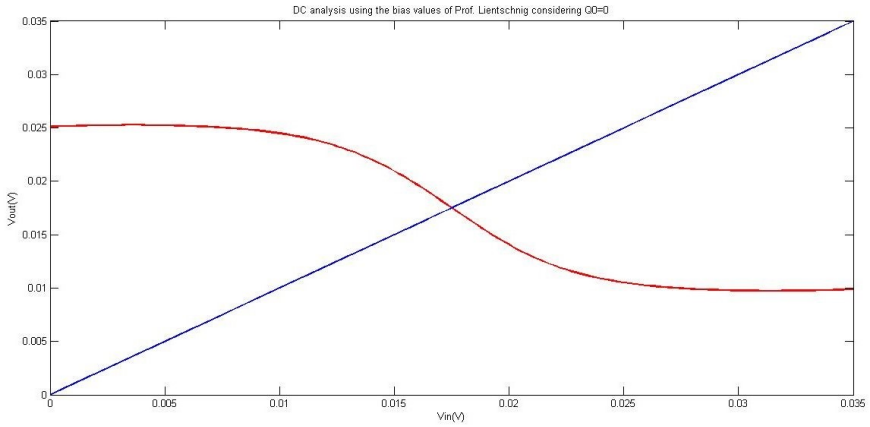

Figure 7.5: DC analysis using the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = 0$

Results of Transient Analysis:

Steady State Output Low Voltage $= 3.4165mV$
Steady State Output High Voltage $= 25.119mV$
10% of Voltage Range $= 11.4048mV$
90% of Voltage Range $= 23.59525mV$

Rise Time:
Time at $V_{out} = 11.445mV$, $t_1 = 22.364ns$
Time at $V_{out} = 22.584mV$, $t_2 = 22.962ns$
Rise Time, $t_r = t_2 - t_1 = (22.962 - 22.364)ns = 0.598ns$.

Fall Time:
Time at $V_{out} = 23.584mV$, $t_1 = 41.362ns$
Time at $V_{out} = 11.445mV$, $t_2 = 41.960ns$
Fall Time, $t_f = t_2 - t_1 = (41.96041.362)ns = 0.598ns$.

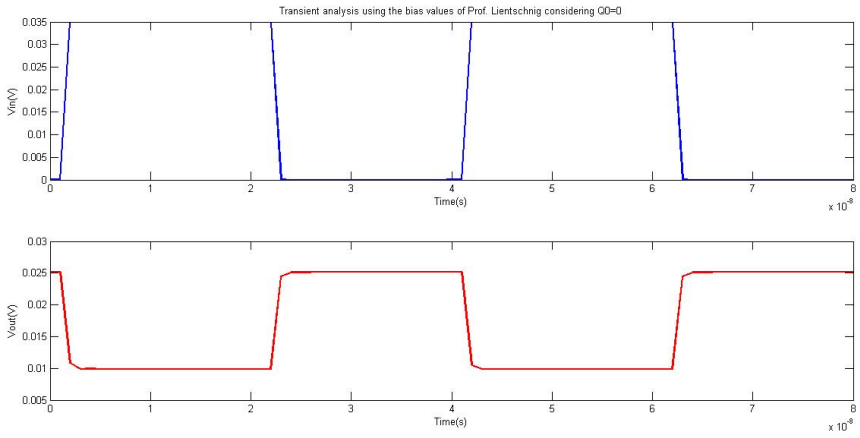

Figure 7.6: Transient analysis using the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = 0$

7.2.2 SET Inverter Simulation Considering Background Charge

We have built two circuits of SET inverter considering background charge, Q_0. For N-type DGSET $Q_0 = 0.15e$ and for P-type DGSET $Q_0 = -0.15e$ was considered. We considered the temperature $27k$ and the supply voltage $V_{DD} = 35mV$.

In first circuit we used the biasing used by Professor Tucker and in the second circuit we used the biasing used by *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley.*

Biasing used by Professor Tucker Considering Q_0

Professor Tucker used the side gate bias voltages as $0mV$ (for P-type DGSETs) and $35mV$ (for N-type DGSETs).He used the following equations for biasing,

$C_1 = 2C_2$, $C_{G2} = 7C_2$, $C_{G1} = 8C_2$,$C_\Sigma = 18C_2$ and $V_{DD} = 1.5e/2C_\Sigma$ (7.2)

We used these data in the SET SPICE model and analyzed the DC and transient characteristics of the SET inverter circuit. We used $V_{DD} = 35mV$. Thus we get the following capacitive values,

$C_1 = 3.809524 \times 10^{-19} Coulomb$, $C_2 = 1.904762 \times 10^{-19} Coulomb$, $C_{G1} = 1.5238095 \times 10^{-19} Coulomb$ and $C_{G2} = 1.3333333 \times 10^{-19} Coulomb$.

The following resistive values were used in this simulation,

$R_1 = 10^5 \Omega$ and $R_2 = 10^5 \Omega$.

Fig. 7.7 depicts the circuit diagram of SET inverter using the bias values of *Professor Tucker*. Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.2 and Fig. 7.3 show the DC analysis and transient analysis respectively for this biasing. We have generated the numerical values of input and output voltages and plotted them in MATLAB.

Results of DC Analysis:

Inversion Voltage:
$V_{inv} = 17.143mV$.

Results of Transient Analysis:

Steady State Output Low Voltage = $13.185mV$
Steady State Output High Voltage = $21.323mV$
10% of Voltage Range = $13.9988mV$
90% of Voltage Range = $20.5092mV$

Rise Time:
Time at $V_{out} = 13.988mV$, $t_1 = 22.288ns$
Time at $V_{out} = 20.462mV$, $t_2 = 22.874ns$
Rise Time, $t_r = t_2 - t_1 = (22.874 - 22.288)ns = 0.586ns$.

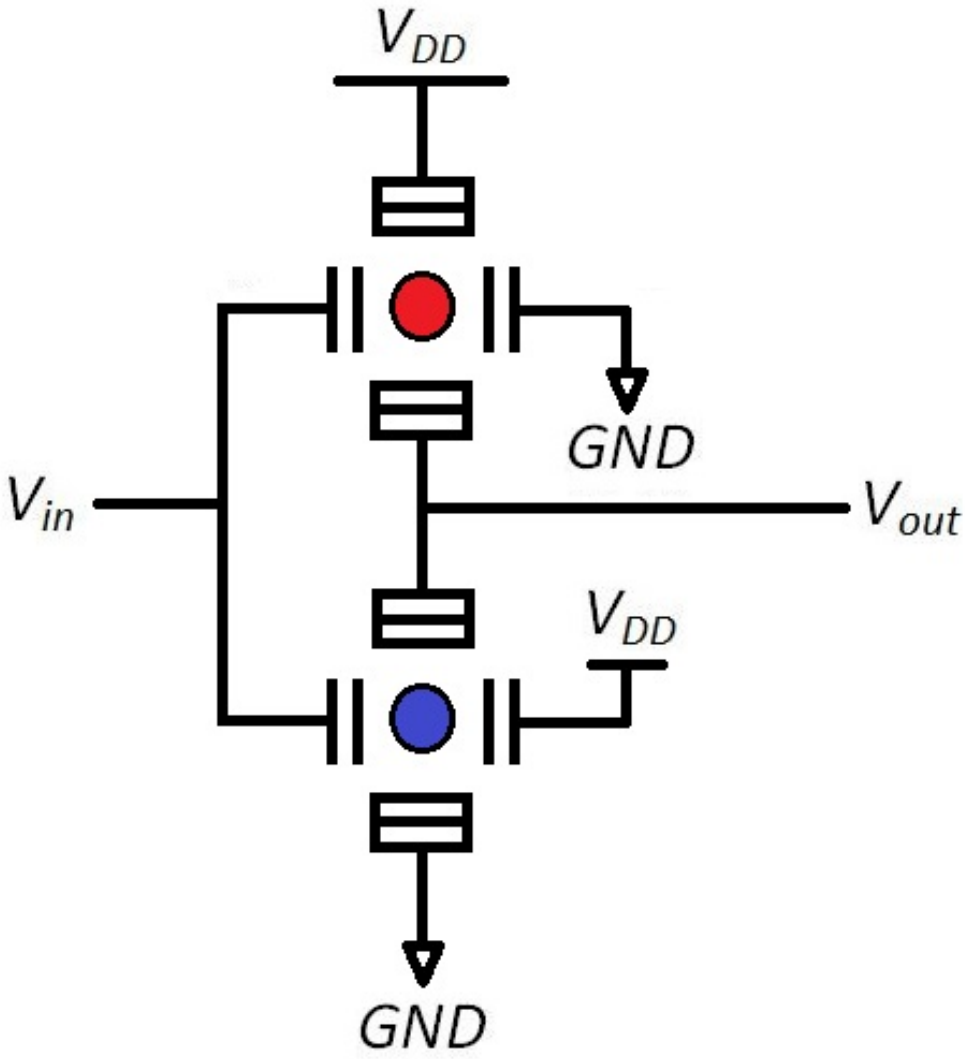

Figure 7.7: SET Inverter using the bias value of *Professor Tucker* considering $Q_0 = |1.5e|$

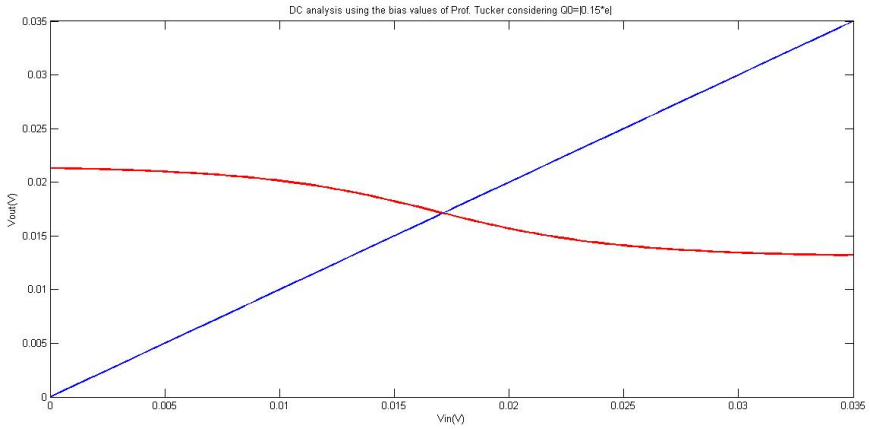

Figure 7.8: DC analysis using the bias values of *Professor Tucker* considering $Q_0 = |1.5e|$

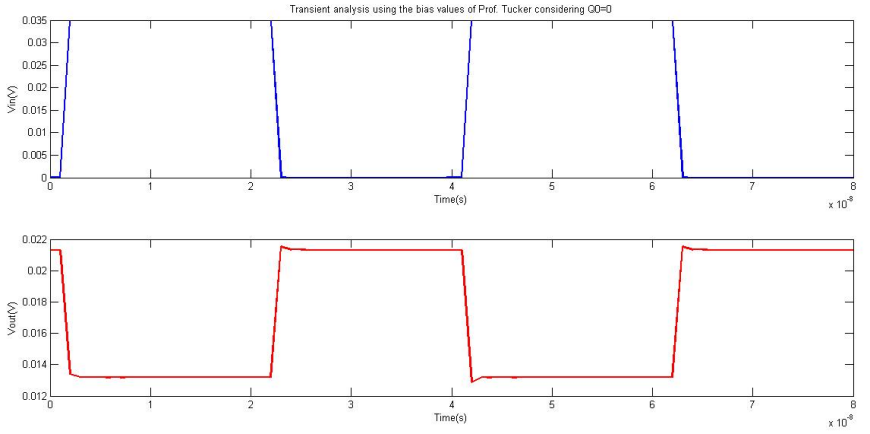

Figure 7.9: Transient analysis using the bias values of *Professor Tucker* considering $Q_0 = |1.5e|$

Fall Time:
Time at $V_{out} = 20.462mV$, $t_1 = 41.250ns$
Time at $V_{out} = 13.988mV$, $t_2 = 41.857ns$
Fall Time, $t_f = t_2 - t_1 = (41.85741.250)ns = 0.607ns$.

Biasing used by Professor Lientschnig Considering Q_0

Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley used the side gate bias voltages as $0mV$ (for both N-type and P-type DGSETs). They the following capacitive values for biasing,

$C_1 = 10^{-18}Coulomb$, $C_2 = 10^{-18}Coulomb$, $C_{G1} = 2 \times 10^{-18}Coulomb$ and $C_{G2} = 0Coulomb$.

The following resistive values were used in this simulation,
$R_1 = 10^5\Omega$ and $R_2 = 10^5\Omega$.

Fig. 7.10 depicts the circuit diagram of SET inverter using the bias values of Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley. Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.11 and Fig. 7.12 show the DC analysis and transient analysis respectively for this biasing. We have generated the numerical values of input and output voltages and plotted them in MATLAB.

Results of DC Analysis:
Inversion Voltage:
$V_{inv} = 17.500mV$.

Results of Transient Analysis:
Steady State Output Low Voltage = $5.1931mV$
Steady State Output High Voltage = $29.807mV$
10% of Voltage Range = $7.65449mV$
90% of Voltage Range = $27.34561mV$

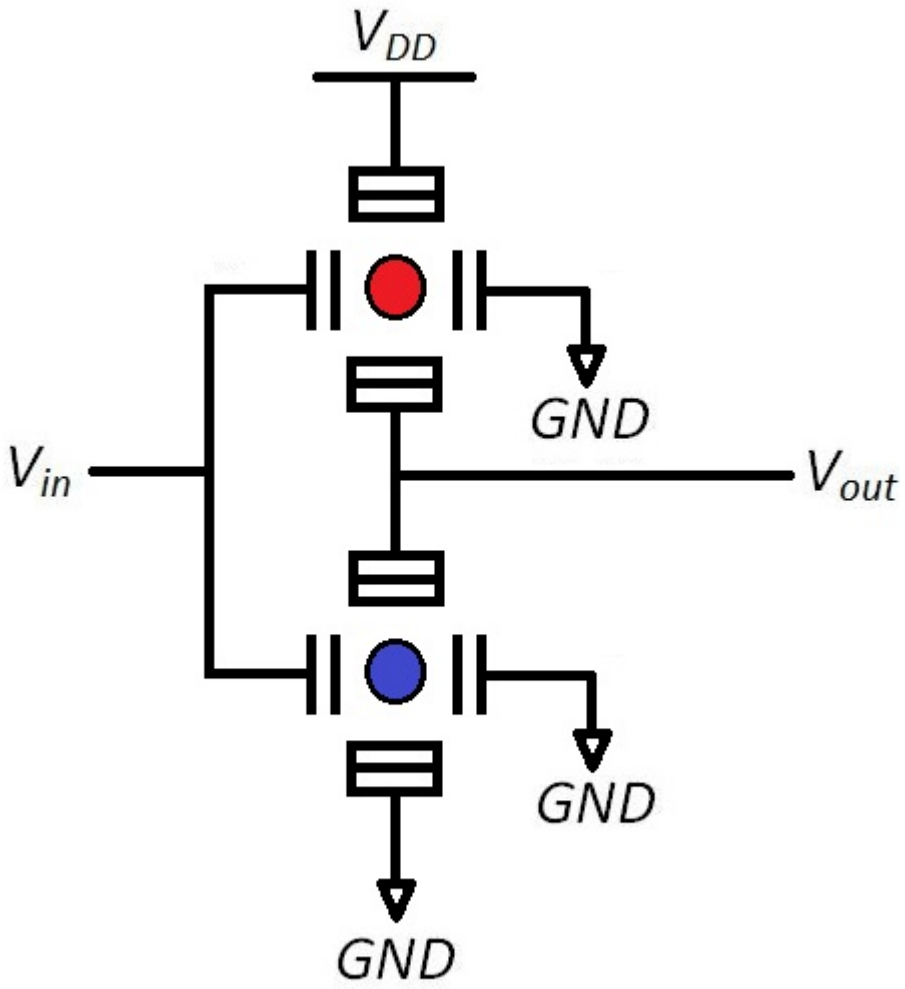

Figure 7.10: SET Inverter using the bias value of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = |1.5e|$

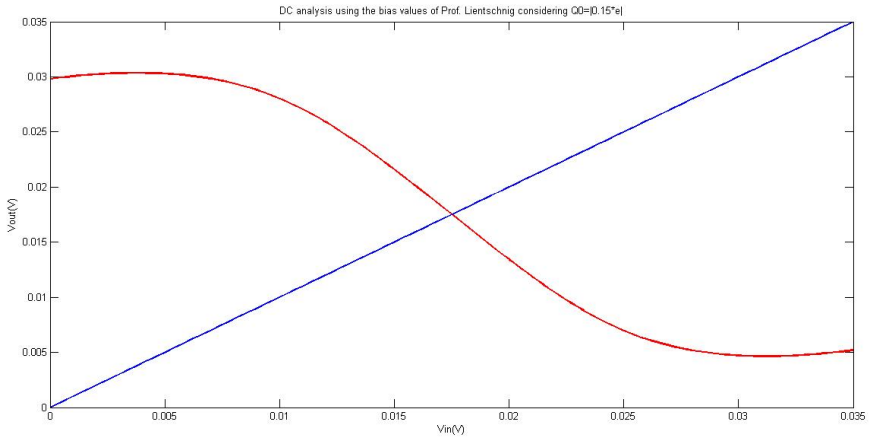

Figure 7.11: DC analysis using the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = |1.5e|$

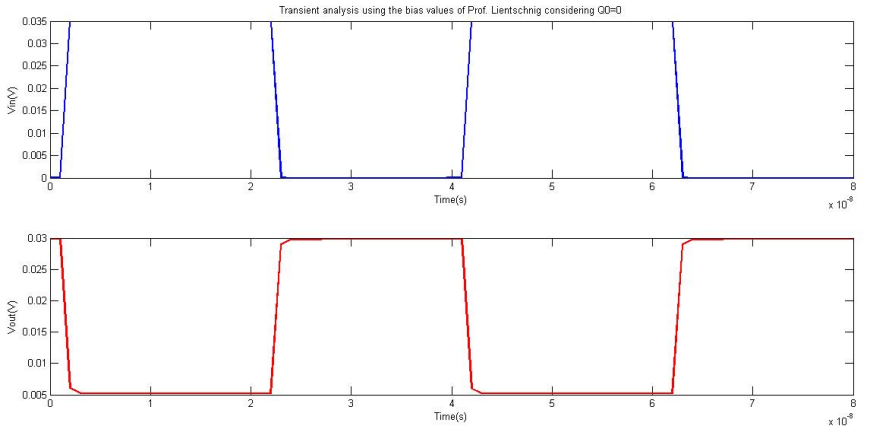

Figure 7.12: Transient analysis using the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering $Q_0 = |1.5e|$

Rise Time:
Time at $V_{out} = 7.6301mV$, $t_1 = 22.324ns$
Time at $V_{out} = 27.399mV$, $t_2 = 22.932ns$
Rise Time, $t_r = t_2 - t_1 = (22.932 - 22.324)ns = 0.608ns$.

Fall Time:
Time at $V_{out} = 27.399mV$, $t_1 = 41.323ns$
Time at $V_{out} = 7.6301mV$, $t_2 = 41.931ns$
Fall Time, $t_f = t_2 - t_1 = (41.93141.323)ns = 0.608ns$.

7.2.3 Best Biasing for SET Inverter

In Table 7.1, the comparison of different biasing for SET inverter circuit has been shown,

Table 7.1: Inversion voltage (V_{inv}), Rise time (t_r), Fall time (t_f) of SET Inverter for different biasing values

Serial	Bias Values	$V_{inv}(mV)$	$t_r(ns)$	$t_f(ns)$
1	Biasing by *Tucker* Not Considering Q_0	16.540	0.563	0.600
2	Biasing by *Lientschnig* Not Considering Q_0	17.500	0.598	0.598
3	Biasing by *Tucker* Considering Q_0	17.143	0.586	0.607
4	Biasing by *Lientschnig* Considering Q_0	17.500	0.608	0.608

Analyzing all the simulations of the inverter we can see that, the bias values of serial no. 4 i.e., the bias values of *Professor Gnther Lientschnig, Professor Irek Weymann and Professor Peter Hadley* considering the background charge, Q_0 is the best. So following bias values were used for the next circuits,

$C_1 = 10^{-18}Coulomb$
$C_2 = 10^{-18}Coulomb$
$C_{G1} = 2 \times 10^{-18}Coulomb$
$C_{G2} = 0Coulomb$
$V_{G2} = 0mV$ for P-type DGSET

$V_{G2} = 0mV$ for N-type DGSET
$R_1 = 10^5\Omega$
$R_2 = 10^5\Omega$
$Q_0 = -1.5e$ for P-type DGSET (Red colored island)
$Q_0 = +1.5e$ for N-type DGSET (Blue colored island)

7.3 Some Digital Circuits Using SET

We have simulated the following circuits using the preferred bias values mentioned in section 2.2.3,

- 2-input NAND gate
- 2-input NOR gate
- Half adder
- Full adder
  - Circuit 1
  - Circuit 2

All the circuits were built using CSET.

7.3.1 2-input NAND Gate

The truth table of 2-input NAND gate is shown in Table 7.2,

Table 7.2: Truth table of 2-input NAND gate

V_{in1}	V_{in2}	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

The circuit diagram of 2-input NAND gate using the preferred bias values is shown in Fig. 7.13. Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.14 shows the transient analysis of 2-input NAND gate using SET. The output curve is almost similar to the ideal output curve.

7.3.2 2-input NOR Gate

The truth table of 2-input NOR gate is shown in Table 7.3,

Table 7.3: Truth table of 2-input NOR gate

V_{in1}	V_{in2}	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

The circuit diagram of 2-input NOR gate using the preferred bias values is shown in Fig. 7.15. Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.16 shows the transient analysis of 2-input NOR gate using SET. The output curve is almost similar to the ideal output curve.

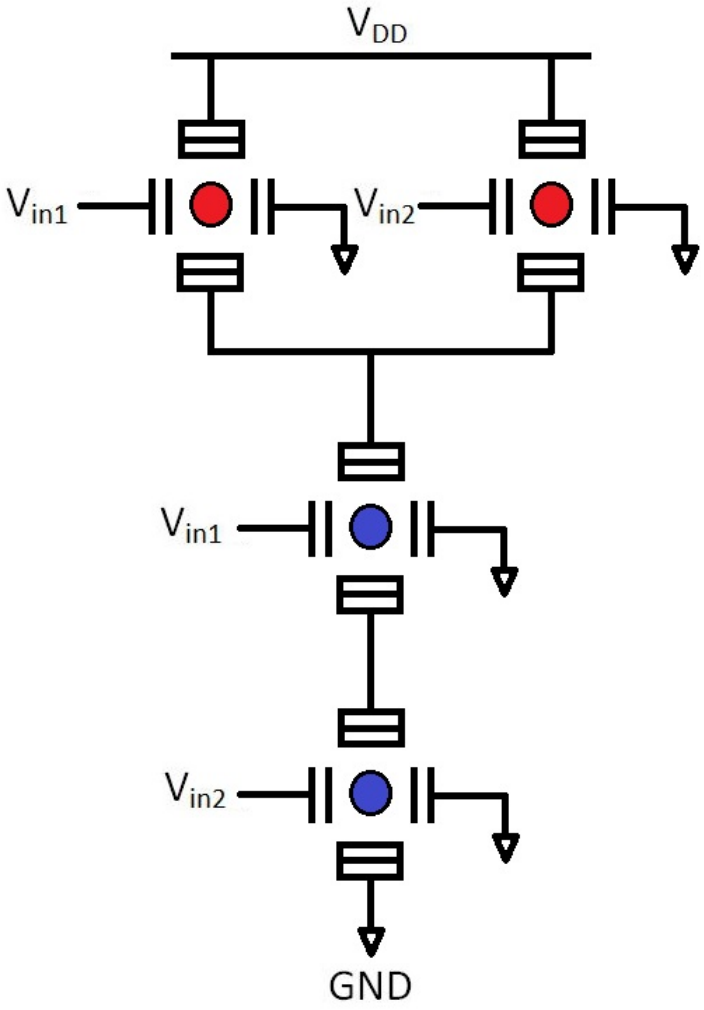

Figure 7.13: 2-input NAND gate using SET with preferred bias values

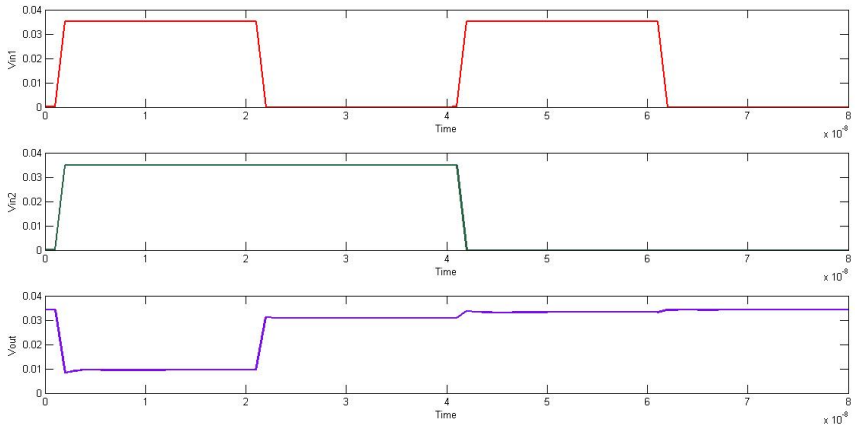

Figure 7.14: Transient Analysis of 2-input NAND gate using the preferred bias values

7.3.3 Half Adder

The truth table of Half adder is shown in Table 7.4,

Table 7.4: Truth table of Half adder

V_{in1}	V_{in2}	C_{out}	S_{out}
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The circuit diagram of half adder using the preferred bias values is shown in Fig. 7.17 (S_{out} part) and in Fig. 7.18 (C_{out} part). Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.19 shows the transient analysis of half adder circuit using SET. The output curve is almost similar to the ideal output curve.

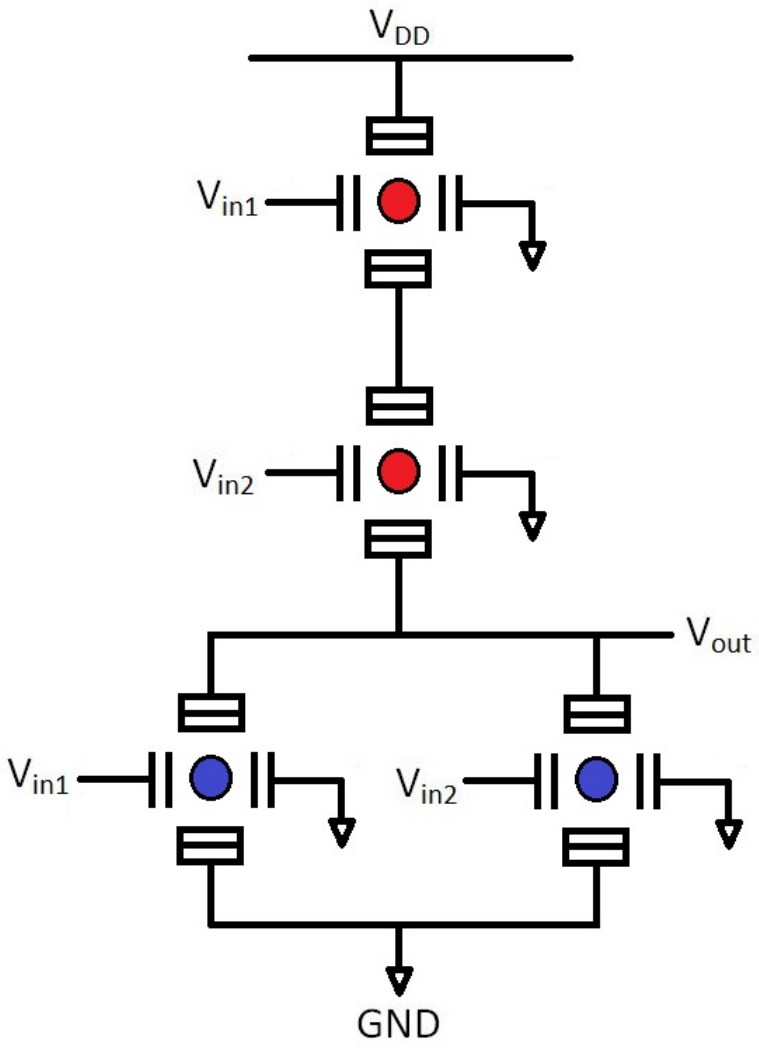

Figure 7.15: 2-input NOR gate using SET with preferred bias values

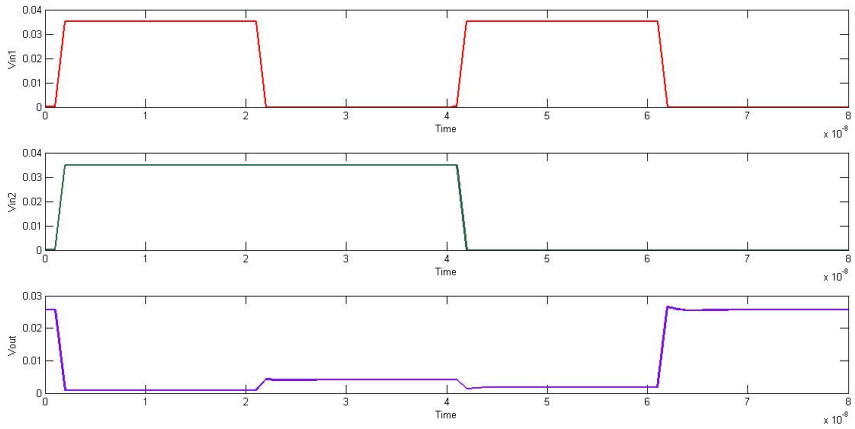

Figure 7.16: Transient Analysis of 2-input NOR gate using the preferred bias values

7.3.4 Full Adder

We have simulated two different circuits of full adder using SET using preferred bias values. After that we will choose the better circuit.

The truth table of Full adder is shown in Table 7.5,

Table 7.5: Truth table of Full adder

V_{in1}	V_{in2}	C_{out}	S_{out}	
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

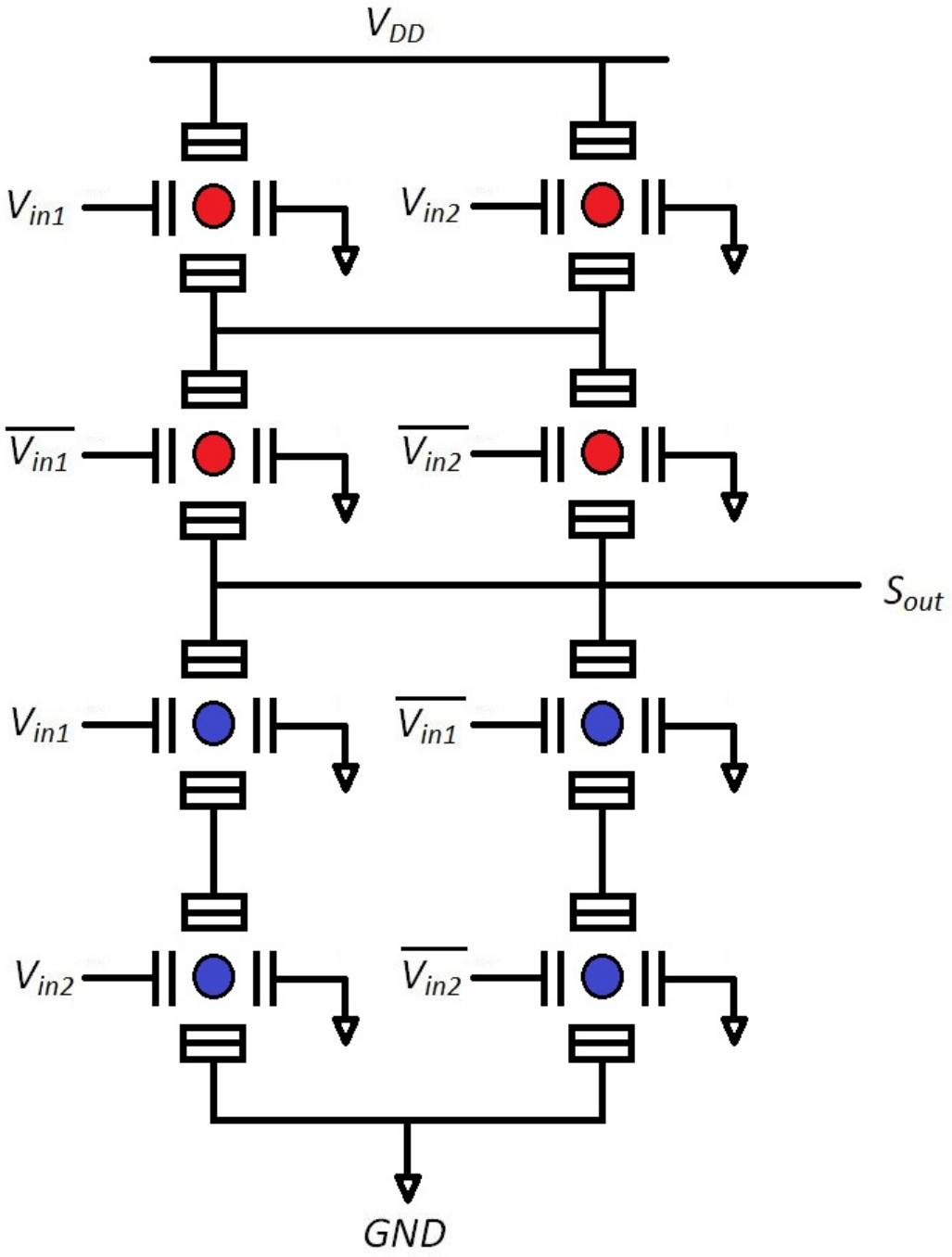

Figure 7.17: Half adder circuit (S_{out} part)

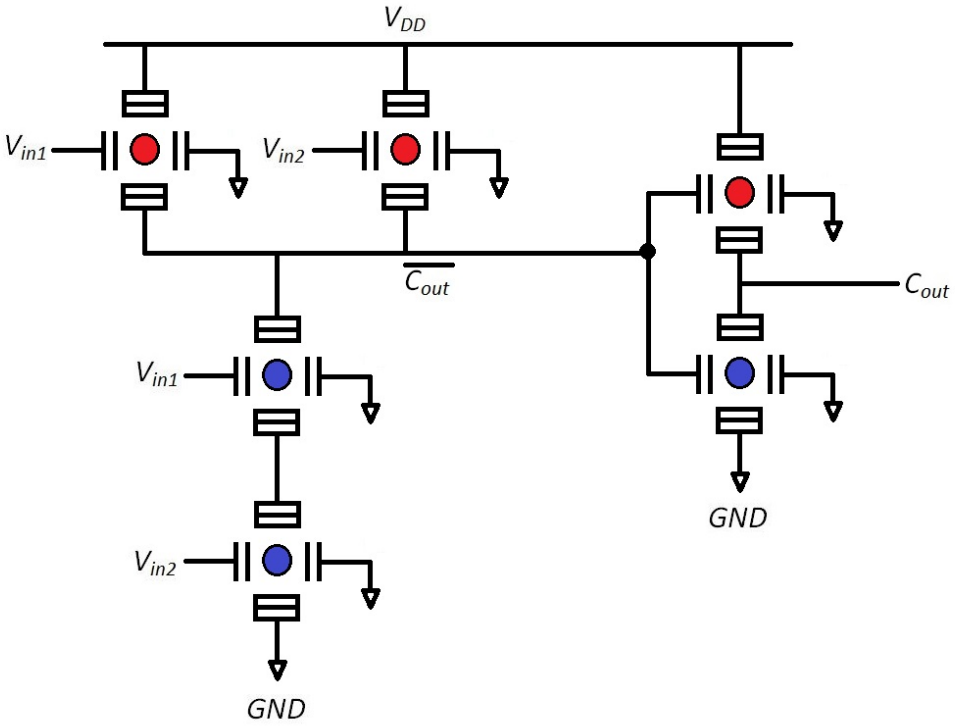

Figure 7.18: Half adder circuit (C_{out} part)

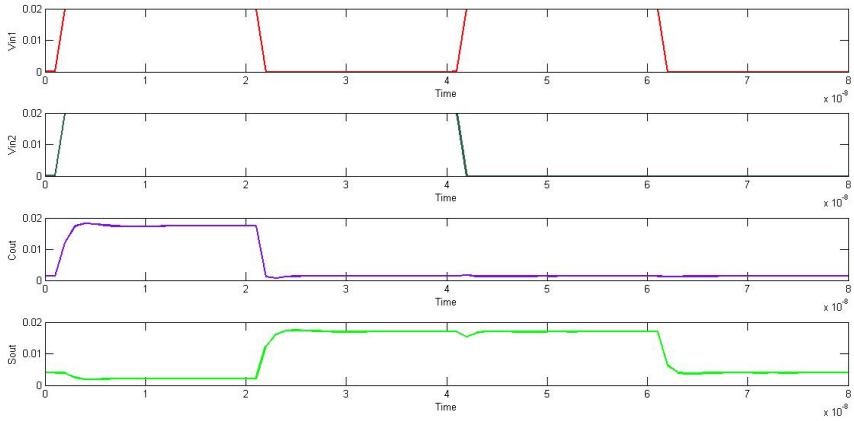

Figure 7.19: Transient Analysis of half adder circuit using the preferred bias values

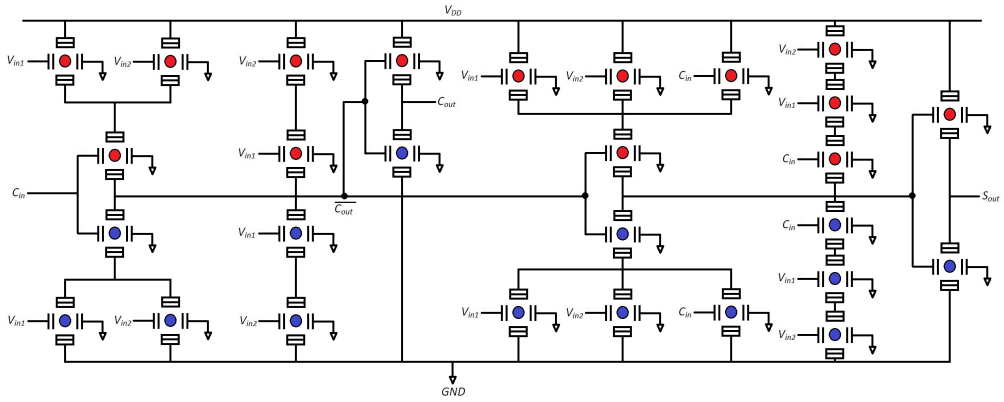

Figure 7.20: Full adder circuit-1

Full Adder - Circuit-1

The circuit diagram of full adder (circuit-1) using the preferred bias values is shown in Fig. 7.20. Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.21 shows the transient analysis of full adder circuit-1 using SET. The output curve is almost similar to the ideal output curve.

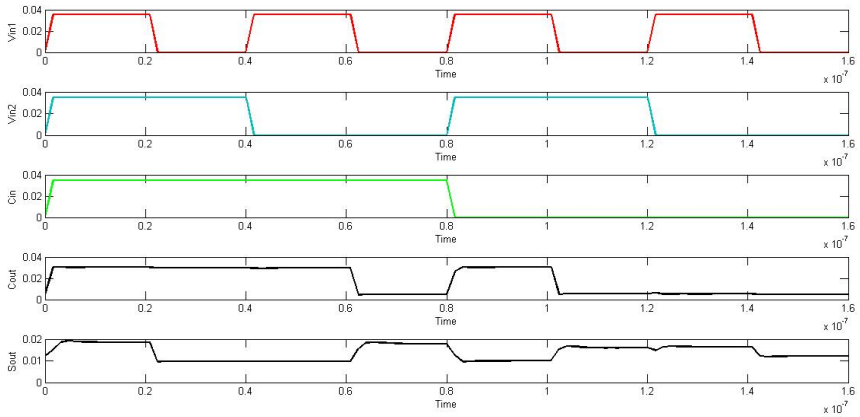

Figure 7.21: Transient Analysis of full adder circuit-1 using the preferred bias values

Full Adder - Circuit-2

The circuit diagram of full adder using the preferred bias values is shown in Fig. 7.22 (C_{out} part) and in Fig. 7.23 (S_{out} part). Red color of island indicates that, it has $Q_0 = -1.5e$ (P-type DGSET) and blue color of island indicates that, it has $Q_0 = +1.5e$ (N-type DGSET).

Fig. 7.24 shows the transient analysis of full adder circuit-2 using SET. The output curve is almost similar to the ideal output curve.

Better Full Adder Circuit

Circuit-1 needed 28 DGSETs. But circuit-2 needed 42 DGSETs. So circuit-1 is better from the view of space and power consumption. But the difference between Low level output voltage and high level output voltage is very less for circuit-1. In this case circuit-2 showed very good performance. So considering all limitations circuit-2 is chosen as full adder circuit.

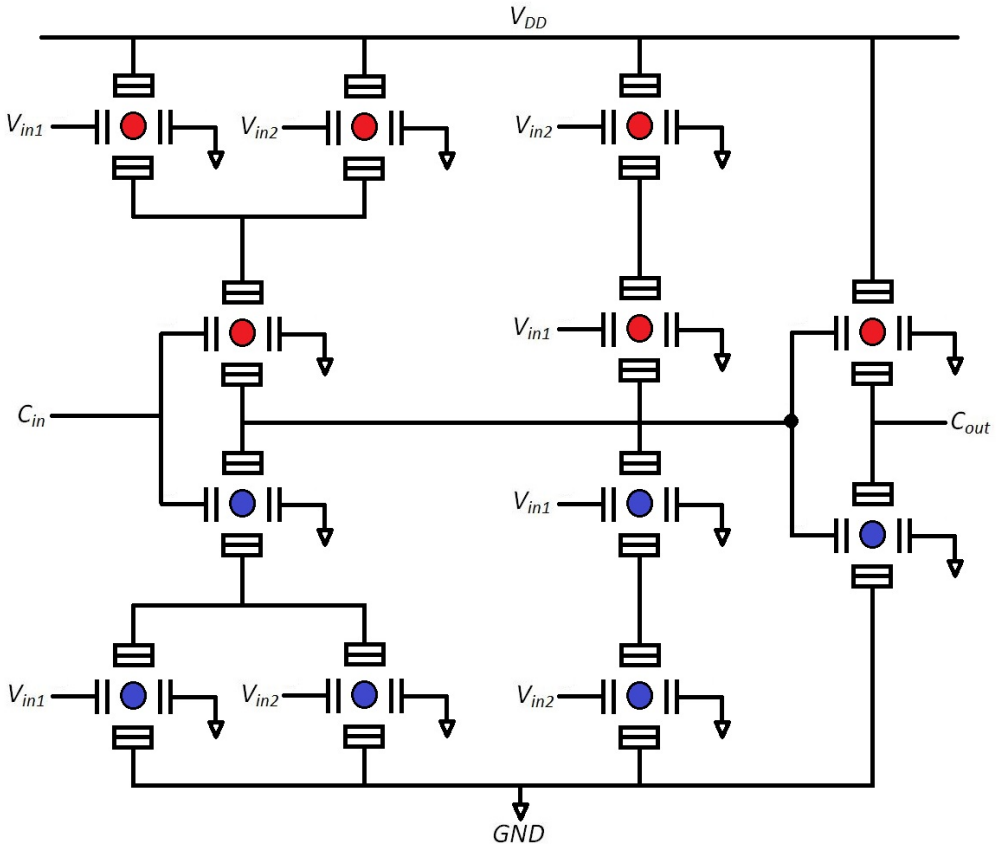

Figure 7.22: Full adder circuit-2 (C_{out} part)

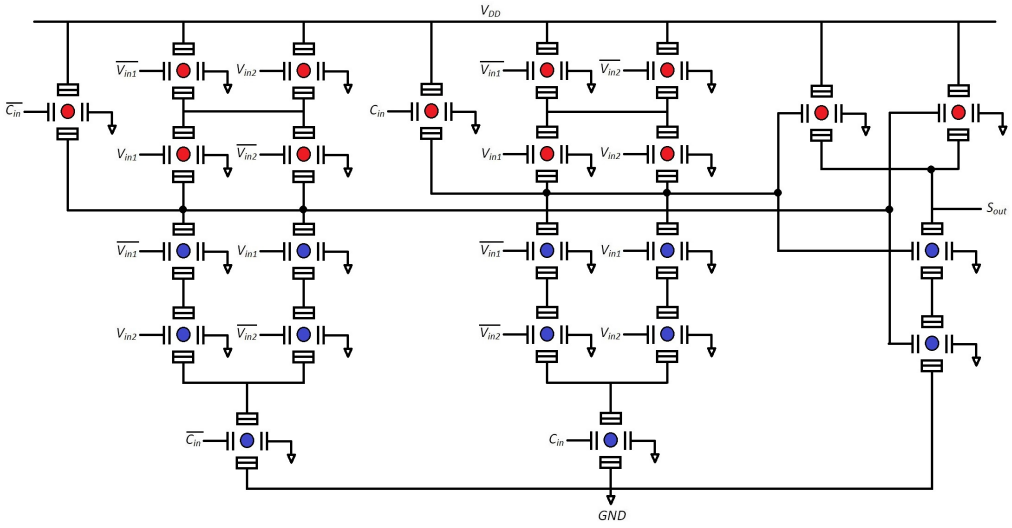

Figure 7.23: Full adder circuit-2 (S_{out} part)

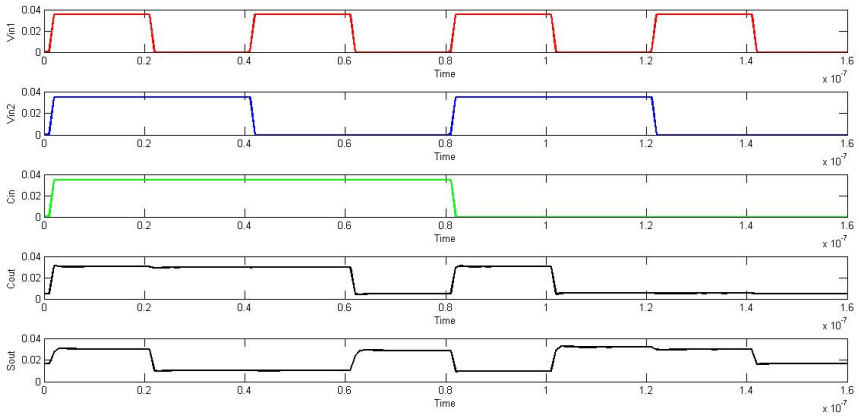

Figure 7.24: Transient Analysis of full adder circuit-1 using the preferred bias values

Chapter 8

Conclusion And Future Works

8.1 Summary And Conclusion

In this thesis a very promising nano-device Single Electron Transistor has been focused. The main contribution of this thesis work is to justify the importance of SET and to make SET an efficient competitor of MOSFET. The thesis can be summarized as follows:

- We discussed about basic structures of SET.
- We discussed about theory of operation, stability plot and regions of operations of SET.
- We studied about SET with two gates which is called Dual Gate Single Electron Transistor (DGSET).
- We emphasized on P-type Dual Gate SET and N-type Dual Gate SET and their operations.
- Preliminary simulations of following Complementary SET (CSET) logic circuits were performed and good results were obtained.
  - Inverter
  - 2-input NAND gate
  - 2-input NOR gate
  - Half adder
  - Full adder

8.2 Future Works

With the current progress of our work, we have several future goals that we want to achieve.

- To study Complex Logic circuit implementation using SET.
- To probe analog implementations of SET.
- Literature shows SET-MOS Hybrid circuits have better performance. We intend to learn about these hybrid circuits.

Bibliography

[1] KK Likharev, "Single-electron devices and their applications ", Proc.IEEE, vol. 87, pp. 606-632, Apr. 1999.

[2] Khondker Zakir Ahmed, "Application of a single electron transistor in a Rate Controlled Oscillato", Thesis submitted to the Department of Electrical and Electronic Engineering of Bangladesh University of Engineering and Technology in partial fulfillment of the requirement for the degree of Master of Science in Electrical And Electronic Engineering, 2008.

[3] J. R. Tucker, "Complementary digital logic based on the Coulomb blockade", J. Appl. Phys. 72, 4399, 1992.

[4] Mohamed Amine Bounouar, Arnaud Beaumont, Francis Calmon and Dominique Drouin, "On the Use of Nanoelectronic Logic Cells Based on Metallic Single Electron Transistors", Proc. IEEE Conf. Ultimate Integration on Silicon (ULIS), pp. 157-160, Mar. 2012.

[5] Ken Uchida, KazuyaMatsuzawa, Junji Koga, Ryuji Ohba, Shin-ichi Takagi and AkiraToriumi, "Analytical Single-Electron Transistor (SET) model for design and analysis ofrealistic circuits", Jpn. J. Appl. Phys., 39 (2000) pp. 2321-2324, 2000.

[6] M. Hasani, K. Abbasian, GH. Karimian and M.J. Asadi, "Design of a Half-Adder Using Silicon Quantum Dot-Based Single-Electron Transistor Operating at Room Temperature", Journal of Electron Devices, vol. 18 (2013), pp. 1505-1509, 2013.

[7] Mohamed Amine Bounouar, Arnaud Beaumont, Francis Calmon and Dominique Drouin, "Room Temperature Double Gate Single Electron Transistor Based Standard Cell Library", Proc. IEEE Conf. Nanoscale Architectures, pp. 146-151, Jul. 2012.

[8] Gnther Lientschnig, Irek Weymann and Peter Hadley, "Simulating Hybrid Circuits of Single-Electron Transistors and Field-Effect Transistors", Jpn. J. Appl. Phys. vol. 42 (2003) pp. 64676472 2009.

[9] Gnther Lientschnig, "Single-Electron and Molecular Devices", A doctoral degree at the Technical University of Delft, 2003.

[10] Sangwoo Kang, Dae-Hwan KIM, Il-Han Park, Jin-Ho Kim, Joung-Eob Lee, Jong Duk Lee and Byung-Gook Park, "Self-Aligned Dual-Gate Single-Electron Transistors", Jpn. J. Appl. Phys., 47 (2008) pp. 3118-3122, 2008.

[11] Dong Seup Lee, Sangwoo Kang, Kwon-Chil Kang, Joung-Eob Lee, Jung Hoon Lee, Kwan-Jae Song, Dong Myong Kim, Jong Duk Lee and Byung-Gook Park, "Fabrication and Characteristics of Self-Aligned Dual-Gate Single-Electron Transistors", IEEE Trans. Nanotech., vol. 8, pp. 492-497, Jul. 2009.

[12] Yasuo Takahashi, Akira Fujiwara, Yukinori Ono, Katsumi Murase, Morinosato Wakamiya and Atsugi-shi, "Silicon Single-Electron Devices and Their Applications", Proc. IEEE Conf. Multiple-Valued Logic, pp. 411-420, May 2000.