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RESEARCH TREND AND POTENTIAL APPLICATION OF SPIN BASED DEVICE

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A Dissertation on,

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Abstract

This thesis is focused on the new technology evolved in the electronics field based on the spin property of electron that is Spintronics, at the interface between magnetism and electronics, which is a new field of research in considerable expansion. The basic concept of Spintronics is the manipulation of spin currents, in contrast to mainstream electronics in which the spin of the electron is ignored. Adding the spin degree of freedom provides new effects, new capabilities and new functionalities.

The article describes the development of Spintronics from the first studies of spin dependent transport in ferromagnetic materials to the discovery of the giant magnetoresistance and to the most recent advances. Everybody has already a spintronic device on their desktop, since the read heads of the hard disc drives of today use the giant magnetoresistance (GMR) phenomenon to read the magnetic information on the disc.

The GMR was the first step on the road of the utilization of the spin degree of freedom in magnetic nanostructures and triggered the development of an active field of research which has been called Spintronics. Today this field is extending considerably, with very promising new axes like the phenomena of spin transfer, Spintronics with semiconductors, molecular Spintronics or single-electron Spintronics etc.

In this review article we have tried to give an overall idea about the fundamentals of Spintronics, emergence of Spintronics in the field of data storage, Spintronics in the field of semiconductor and various Spintronic devices, their applications and future of Spintronics.

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Chapter 1

Introduction

Back in 1965 Intel co-founder Gordon E Moore predicted (which famously known as Moore's Law) that "The number of transistors on a chip will double in every two years." That means more number of transistors are integrated on a smaller chip as days pass. But Moore's Law will run out of momentum very soon as the size of transistors approaches the dimension of atoms—this has been called the end of the silicon road map. Researchers are now seeking new concepts of electronics that sustain the growth of computing power. One promising solution is called "Spintronics", which is based on the "spin" property of electrons as they are being transmitted. It also enhance the multi functionality of devices i.e. carrying out processing and data storage on the same chip. The spin orientation of conduction electrons survives for a relatively long time (nanosecond). This property of spin based system makes Spintronics devices particularly attractive for memory storage, magnetic sensor applications, and potentially for quantum computing, where electron spin would present as a bit of information.

There have been many other reviews written on Spintronics, most focusing on a particular aspect of the field.

We divide them here, for an easier orientation, the spin based field into two main categories-namely

1. Spin based memory devices.
2. Spin based semiconductor.

We found enormous development in first category. And only theoretical success in second category. Let us first define the term Spintronics and logic behind spin based devices.

1.1 Spintronics Definition

The word "Spintronics" refers to the devices that take advantage of electrons' quantum property called "spin". It is a new branch of electronics in which electron spin, in addition to charge, is

manipulated to yield a desired outcome.It is an emerging field that exploits the fact that current flowing through transistors, that are made of certain materials, can store data not only as charge but as magnetic moment.

1.2 Fundamentals of Spin

1) In addition to their mass and electric charge, electrons have an intrinsic quantity of angular momentum called spin, almost as if they were tiny spinning balls.
2) Associated with the spin is a magnetic field like that of a tiny bar magnet lined up with the spin axis.
3) Scientists represent the spin with a vector. For a sphere spinning "west to east" the vector points "north" or "up". It points "down" for the opposite spin.
4) In a magnetic field, electrons with "spin up" and "spin down" have different energies.
5) In an ordinary electric circuit the spins are oriented at random and have no effect on current flow.
6) Spintronic devices create spin-polarized currents and use the spin to control current flow

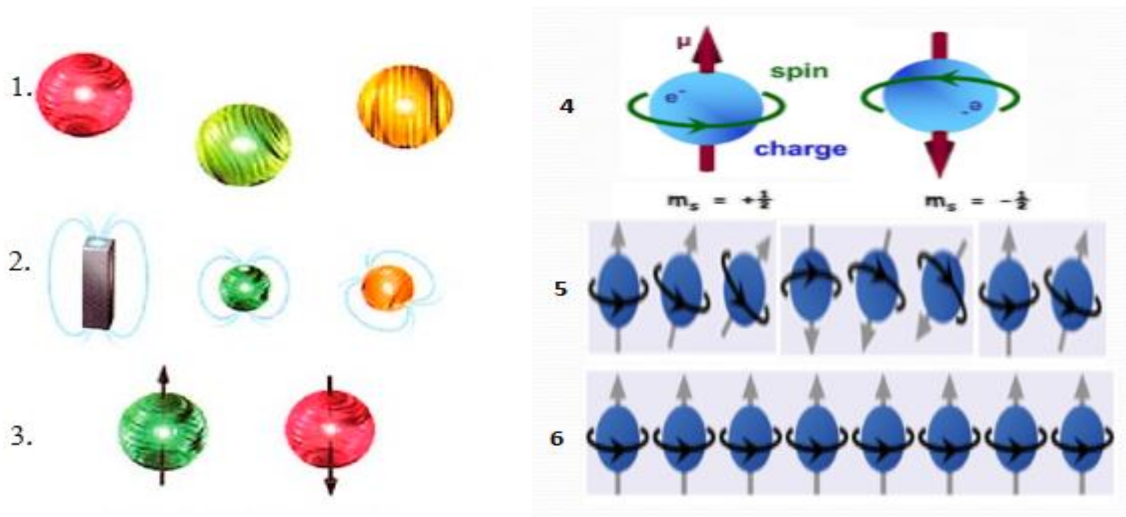


Figure 1.1 Fundamentals of Spin [1].

1.3 Basic Scheme

A spintronic device has a basic scheme-

- First, information is stored into spins as an orientation (i.e. up or down).
- Then, the spins that are attached to mobile electrons carry information along a path or wire.
- The information is then read at a terminal point.

1.4 Electronics vs. Spintronics

The movement of spin, like the flow of charge, can also carry information among devices.

So, what is the advantage of spin property of electrons?

One advantage of spin over charge is that spin can be easily manipulated by externally applied magnetic fields, a property already in use in magnetic storage technology (GMR).

Another more subtle (but potentially significant) property of spin is its relaxation time—once created it tends to stay that way for a long time, unlike charge states, which are easily destroyed by scattering or collision with defects, impurities or other charges.

These characteristics open the possibility of developing devices that could be much smaller, consume less electricity and be more powerful for certain types of computations than is possible with electron-charge-based systems (Electronics).

1.5 Brief History

Spintronics emerged from discoveries in the 1980s concerning spin-dependent electron transport phenomena in solid-state devices. These includes-

1985: The observation of spin-polarized electron injection from a ferromagnetic metal to a normal metal by Johnson and Silsbee.

1988: Discovery of Giant Magneto Resistance (GMR) independently by Albert Fert and Peter Grünberg opened the way to efficient control of charge transport through magnetization. And for

their work they had been awarded Nobel Prize in Physics in 2007 and also the field of spintronics was recognized. The recent expansion of hard-disk recording owes much to this development. Mainly scientists began developing new spin-based electronics, beginning with this discovery.

1990: The theoretical proposal of a spin field-effect-transistor by Datta and Das. The idea of semiconductor spintronics came from this proposal.

2012: In the study published in *Nature*, IBM Research and the Solid State Physics Laboratory at ETH Zurich announced they had found a way to synchronize electrons, which could extend their spin lifetime by 30 times to 1.1 nanoseconds, the time it takes for a 1 GHz processor to cycle [2].

Chapter 2

Emergence of Spintronics in the field of Data Storage

(Spin Based Memory Devices)

In the information era, a new promising science (Spintronics) has been strongly addressed which has produced a breakthrough and diffusion in technological products (mainly in memory) based on the spin property of electron. We are only habituated with the charge property of electrons, but electrons have both charge and spin, which were considered separately until very recently. In classical electronics, charges are moved by electric fields to transmit information and are stored in a capacitor to save it. For more than thirty years physicists and engineers devoted their researches and efforts mostly to charge-transfer devices, developing the actual semiconductor industry and granting to it a tremendous growth rate, witnessed by the well-known Moore law: the doubling of computation speed (proportional to the transistor number per chip1) every 18 months [27]. However scientist faced a lot of problem in scaling of such devices. Spintronic devices come as a revolution to face those problems. Now a days the principal application of spintronic devices is in the field of magnetic data storage which can have information density growth rate faster than the corresponding Moore law. The discovery of Giant magnetoresistance (GMR) causes a revolutionary change in the field of data storage, which opened the way to efficient control of charge transport through magnetization. The recent expansion of hard-disk recording owes much to this development. We are starting to see a new paradigm where magnetization dynamics and charge currents act on each other in nanostructured artificial materials. In the following articles we have tried to give some idea about the spintronic devices in the field of data storage.

2.1 Anisotropic magnetoresistance (AMR)

The interdependence between magnetization and charge transport is not a new story. For instance, anisotropic magnetoresistance (AMR), which links the value of the resistance to the respective orientation of magnetization and current, was first observed in 1856 by William Thomson, but its amplitude was weak (up to a few per cent variation in resistance on changing the relative orientation of magnetization and current). Nevertheless, the introduction by IBM in 1991 of a magnetoresistive read head based on AMR was a major technological step forward [28].

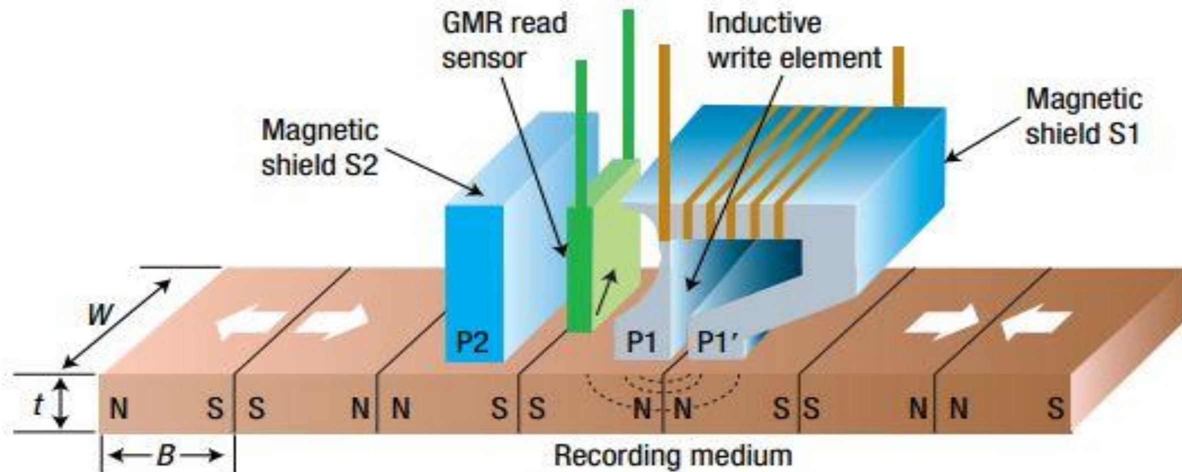


Fig 2.1: Schematic structure of the magnetoresistive head for hard-disk recording introduced by IBM for its hard disk drives in 1991. A magnetic sensor based on anisotropic magnetoresistance (left) is added to the inductive 'ring-type' head (right) still used for writing. The distances p1–p1´ and p1–p2 between the pole pieces of the magnetic shields s1 and s2 define respectively the 'write' and 'read' gaps, on which depends the minimum length 'B' of the magnetic domains. 'W' is the track width and 't' is the thickness of the recording medium. Note that in today's hard disk recording, 'W' and 'B' are of the order of 100 nm and 30 nm respectively, but with a different arrangement of head and domains in 'perpendicular recording'.

IBM developed AMR technology, based on the principle that certain metals undergo changes in electrical resistance in the presence of a magnetic field. AMR heads allowed IBM to store 1 gigabit on one square inch of magnetic recording media, and areal densities have increased to over 3 gigabits per square inch.

In hard disk drives (HDD), the head flies at constant height above the magnetic domains that define the 'bits' in the recording medium, and senses the spatial variations of the stray magnetic field of these domains. Error rate, the number of data bits correctly decoded by the recording head and fly height, the distance between the read/write elements of the head and the magnetic layer of the media are key design parameters in the quest for higher areal density. Designers strive to keep error rate and fly height as large as possible. Error rate for performance reasons and fly height for reliability. For a given head technology, however, these are mutually exclusive goals. To achieve higher areal densities with thin film inductive (TFI) heads, fly heights had to decrease in order to maintain acceptable error rates. Increasing the ability of the head to detect magnetic signals (i.e. head sensitivity) and slow the rate at which fly height decreased was possible for a time. Eventually, new technologies were needed. Hence the development and introduction of Magneto-Resistive (MR), both anisotropic and giant magnetoresistive, technology.

Anisotropic Magnetoresistive (AMR) head technology is currently the primary read/write head technology used in hard drives, replacing TFI heads. AMR heads were introduced first in mobile drives around 1994 and in desktop drives around 1995. Today, all of Western Digital's current desktop and enterprise class (workstations, servers, RAID systems) of hard drives incorporate AMR heads to meet ever increasing capacity requirements. Unlike TFI heads, where the read and write elements are the same, read and write elements in the AMR head are separate in order to optimize read and write capabilities. The write element is a conventional TFI head, while the read element in an AMR head is composed of a thin stripe of magnetic material. The stripe's resistance changes in the presence of a magnetic field, producing a strong signal with low noise amplification and permitting significant increases in areal densities. As the disk passes by the read element, the disk drive circuitry senses and decodes changes in electrical resistance caused by the reversing magnetic polarities. The AMR read element's greater sensitivity provides a higher signal output per unit of recording track width on the disk surface. Not only does magnetoresistive technology permit more data to be placed on disks, but it also uses fewer components than other head technologies to achieve a given capacity point. The AMR read element is smaller than the TFI write element. In fact, the AMR read element can be made smaller than the data track so that if the head were slightly off-track or misaligned, it would still remain over the track and able to read the written data on the track. Its small element size also precludes the AMR read element from picking up interference from outside the data track, which accounts for the AMR head's desirable high signal-to-noise ratio. The AMR head had a relative 'magnetoresistance' (hereafter referred to as $\Delta R/R = (R_{max} - R_{min})/R_{min}$) of the order of only 1%, but this was enough to increase the growth rate of HDD storage areal density from 25% per year, its value since nearly the introduction of HDD in 1957, up to 60% per year.

AMR heads offer a higher signal-to-noise ratio than TFI heads, resulting in superior error rates in drives using them. However, the most important advantage of AMR heads is that they can read from areal densities about four times denser than TFI heads at higher flying heights. The result is markedly improved hard drive performance.

2.1.1 AMR Head Challenges

Manufacturing AMR heads can present difficulties. AMR thin film elements are extremely sensitive to electrostatic discharge, which means special care and precautions must be taken when handling these heads. The AMR thin film stripe is also sensitive to contamination and, because of the materials used in its design, subject to corrosion.

AMR heads also introduced a new challenge not present with TFI heads: thermal asperities—i.e., the instantaneous temperature rise that causes the data signal to spike and momentarily disrupt the recovery of data from the drive. Thermal asperities are transient electrical events, usually associated with a particle, and normally do not result in mechanical damage to the head. Although they can lead to misreading data in a large portion of a sector, new design features can detect these events. A thermal asperity detector determines when the read input signal exceeds a predetermined threshold, discounts that data value and signals the controller to re-read the sector.

2.2 GMR Technology

The founding step of spin electronics has been triggered by the discovery of the giant magnetoresistance (GMR) was actually to build magnetic multilayers with individual thicknesses comparable to the mean free paths, so that evidence could be seen for spin-dependent electron transport. In 1988, a group led by Peter Grünberg and Albert Fert independently reported magneto resistive effects in anti-Ferro magnetically coupled multilayers of Fe/Cr up to 50% at low temperature in "giant" multilayer structures. This effect was named the Giant Magneto resistance (GMR).

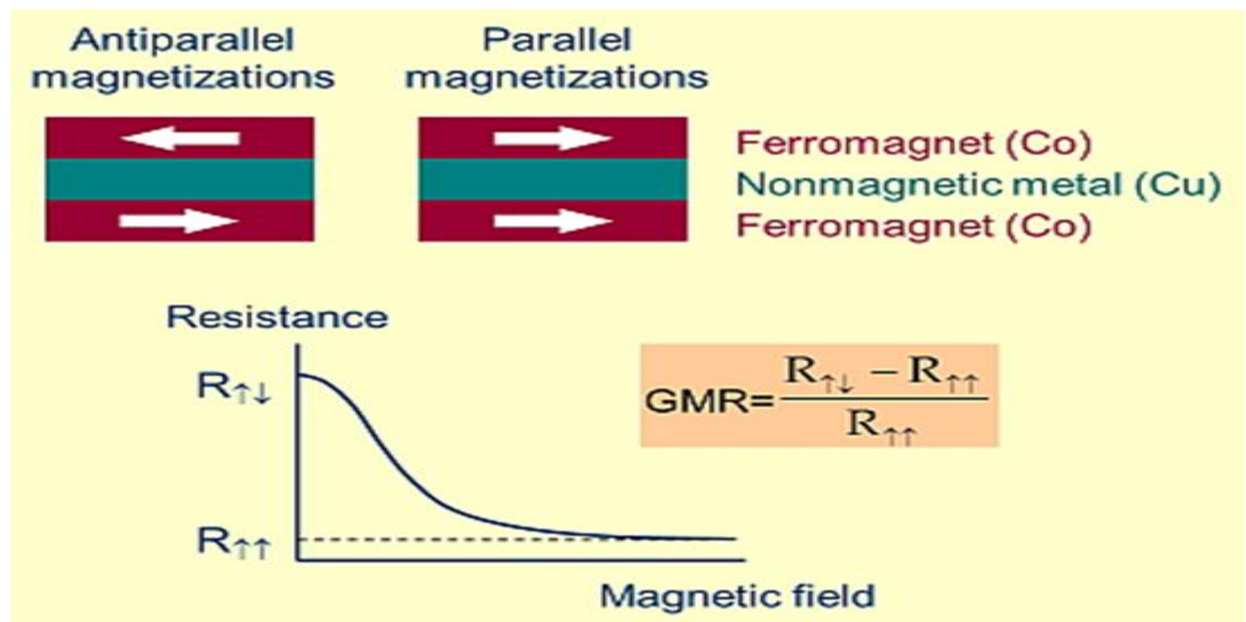


Fig 2.2: Schematic of Giant Magnetoresistance (GMR), showing parallel and anti-parallel effect of magnetization in Ferromagnets.

GMR is composed of two ferromagnetic material separated by a nonmagnetic metal layer. Parallel magnetization in the ferromagnets allow very low resistance while anti-parallel magnetization in the ferromagnets give very high resistance, which provide a great magnetoresistance (MR) value even at room temperature, as the magnetoresistance can be found by the following equation,

$$\mathbf{MR} = (R_{anti\text{-}parallel} - R_{parallel})/R_{parallel}$$

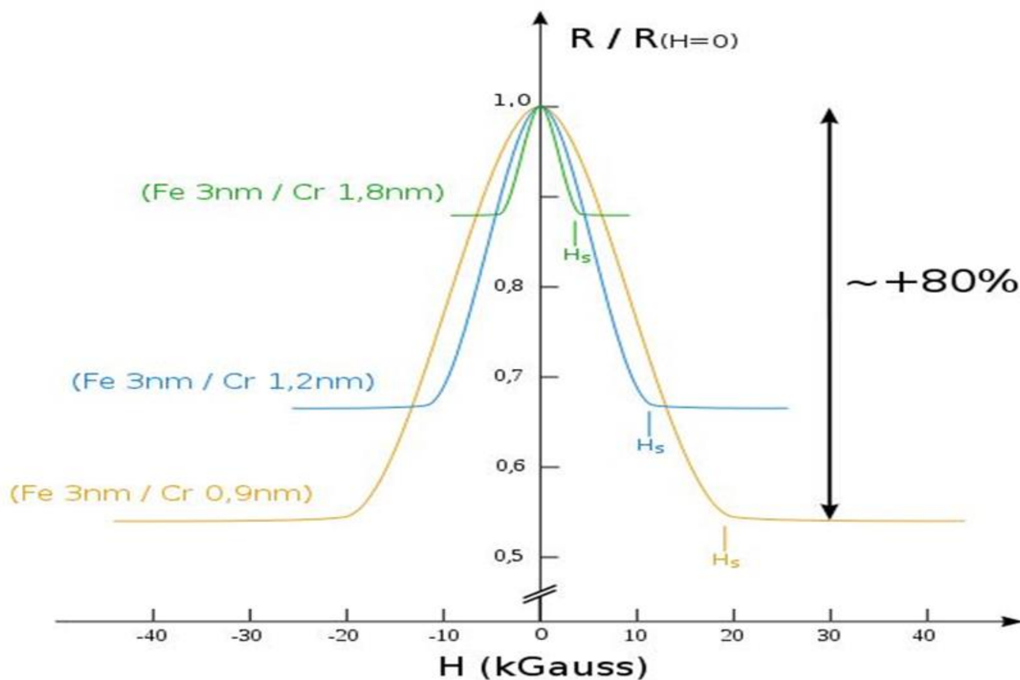


Fig 2.3: The founding results of Albert Fert and Peter Grünberg (1988): change in the resistance of Fe/Cr super lattices at 4.2 K in external magnetic field H. The current and magnetic field were parallel to the axis. The arrow to the right shows maximum resistance change. Hs is saturation field [29].

GMR technology has brought a major technological advance over AMR technology. GMR are the most sensitive sensors yet developed for reading computer data on hard drives. Based on the "giant magnetoresistive effect," a discovery in magnetism made almost 15 years ago in Europe, IBM's further research transformed the effect into a practical reality. IBM's commercial production of

GMR heads is well underway. In 1998 Western Digital entered into an agreement with IBM to purchase advanced GMR heads for its EIDE desktop hard drives. Read-Rite Corp., TDK/SAE Corp. and others continue to supply Western Digital with AMR and GMR heads for its enterprise class as well as some of the EIDE desktop hard drives.

Like AMR heads, GMR heads incorporate separate MR read and TFI write elements. However, the GMR read elements are formed from more complex structures with a higher sensitivity to the changing magnetization on the disk. While in AMR sensors, a single film changes resistance in response to a change in magnetic field on the disk, in GMR sensors, two films, separated by a very thin electrically conductive layer, perform this function. The result is that GMR heads achieve even higher areal densities and performance levels than AMR heads.

AMR heads can read areal densities over 3 gigabits per square inch, on the other hand the newer GMR heads can be scaled to very small dimensions to read areal densities in excess of 10 gigabits per square inch while still maintaining good signal amplitude. Looked at another way, GMR heads can read data on hard drives that can pack over three times more data into the same space.

2.2.1 How GMR Sensors Work

GMR sensors work by exploiting the quantum nature of electrons. Electrons have two spin directions: up and down. Electrons with spin direction parallel to a film's magnetic orientation move freely, thereby producing low electrical resistance. When electrons move in the opposite spin direction, they are hampered by more frequent collisions with atoms in the film, thereby producing higher resistance.

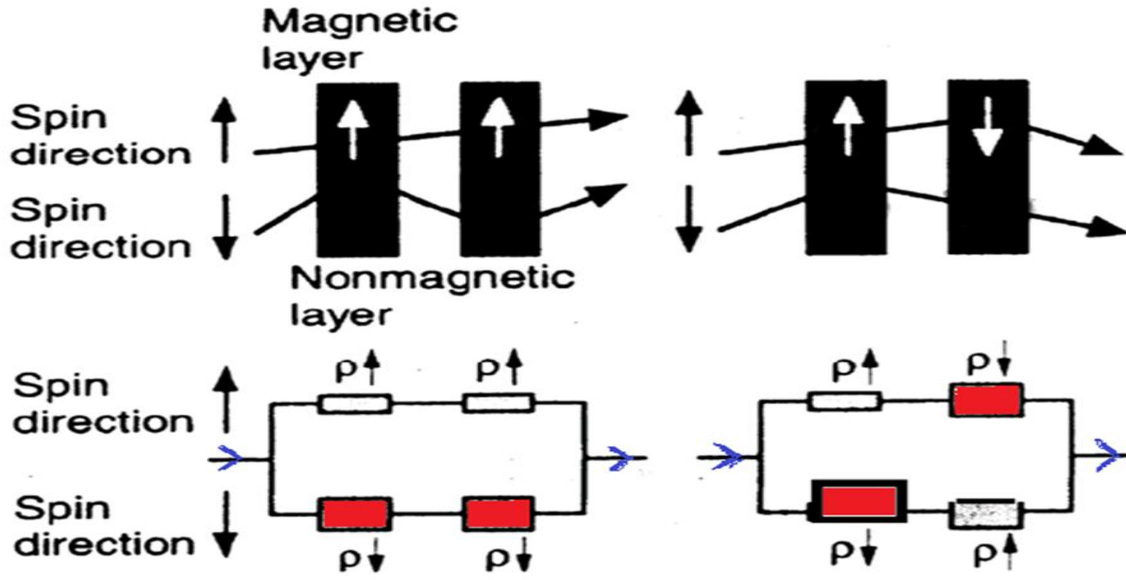


Fig 2.4: Representation of the flow of spin up and down electron through the multilayer structure of GMR.

When the magnetization in both the layers are parallel, then one spin polarization experiences $\rho\uparrow$ through both layers, the other spin polarization $\rho\downarrow$ in both layers. Let us consider,

$\rho\uparrow = \rho(1-B)$ and $\rho\downarrow = \rho(1+B)$, where ρ is the resistivity and B is a constant of coefficient. Then the effective resistivity is,

$$\rho\uparrow\uparrow = \rho\downarrow\downarrow = (2\rho\uparrow\rho\downarrow)/(\rho\uparrow + \rho\downarrow) = \rho(1-B^2)$$

In anti-parallel magnetization in the ferromagnetic layers, each spin channel experiences $\rho\uparrow$ and $\rho\downarrow$ in series. The effective resistivity is,

$$\rho\uparrow\downarrow = (\rho\uparrow + \rho\uparrow)/2 = \rho$$

So, parallel magnetization in the ferromagnets gives much lower resistivity than in the case of anti-parallel magnetization.

$$\rho(\text{parallel}) = \rho(1-B^2) < \rho = \rho(\text{anti-parallel})$$

Changes in the magnetic field originating from the disk cause a rotation of the sensor film's magnetic orientation, which in turn, increases or decreases the resistance of the entire structure. Low resistance occurs when the sensor and pinned films are magnetically oriented in the same

direction, since electrons with parallel spin direction move freely in both films. Higher resistance occurs when the magnetic orientations of the sensor and pinned films oppose each other, since the movement of electrons of either spin direction is restrained by one or the other of these magnetic films.

Where the resistance changes in AMR heads are approximately 2 percent, in GMR heads, they are typically 7 to 8 percent. Because their percent change in resistance is as much as four times greater than in AMR sensors, GMR sensors can operate at significantly higher areal densities as they are more sensitive to magnetic fields from the disk.

GMR heads' greater sensitivity makes it possible to detect smaller recorded bits and read them at higher data rates. Larger signals from GMR heads also help to overcome electronic noise.

Beyond GMR, the next step in hard drive technology will be "Synthetic Spin Valve" GMR or Colossal MR (CMR). This development is underway utilizing materials and layers yet being proven in research labs.

2.3 Spin Valve

The GMR is an outstanding example of how structuring materials at the nanoscale can bring to light fundamental effects that provide new functionalities. And indeed the amplitude of the GMR immediately triggered intense research, soon achieving the definition of the spin-valve sensor [29-31].

The spin valve is just a tri layer film in which one layer (for example, F2) has its magnetization pinned along one orientation. The rotation of the free F1 layer magnetization then 'opens' (in P configuration) or 'closes' (in AP configuration) the flow of electrons, acting as a sort of valve.

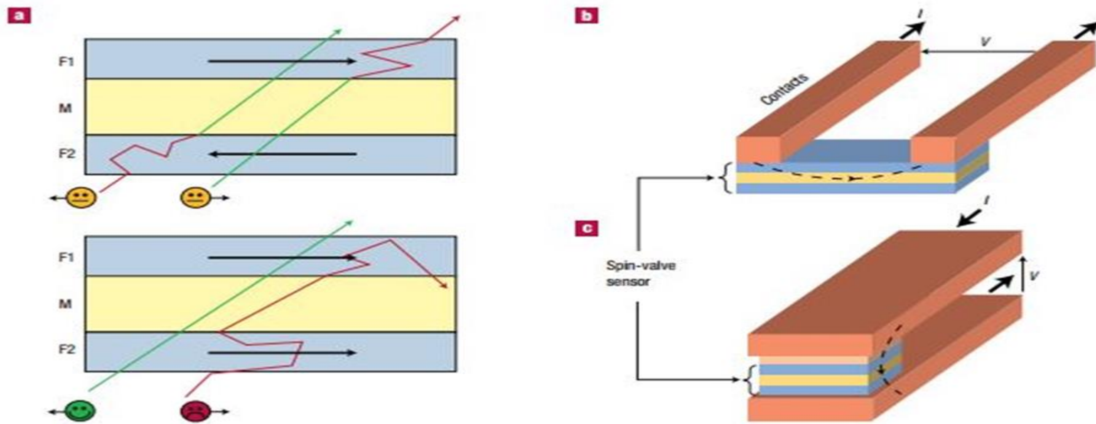


Fig 2.5: The spin valve. a. Schematic representation of the spin-valve effect in a tri layer film of two identical ferromagnetic layers F1 and F2 sandwiching a non-magnetic metal spacer layer m, the current circulating in plane. b. Schematic arrangement of the 'current in plane' spin-valve sensor in a read head. c. schematic arrangement of the 'current perpendicular to plane' spin-valve sensor in a read head. In both configurations, the recording medium travels parallel to the front face of the sensor.

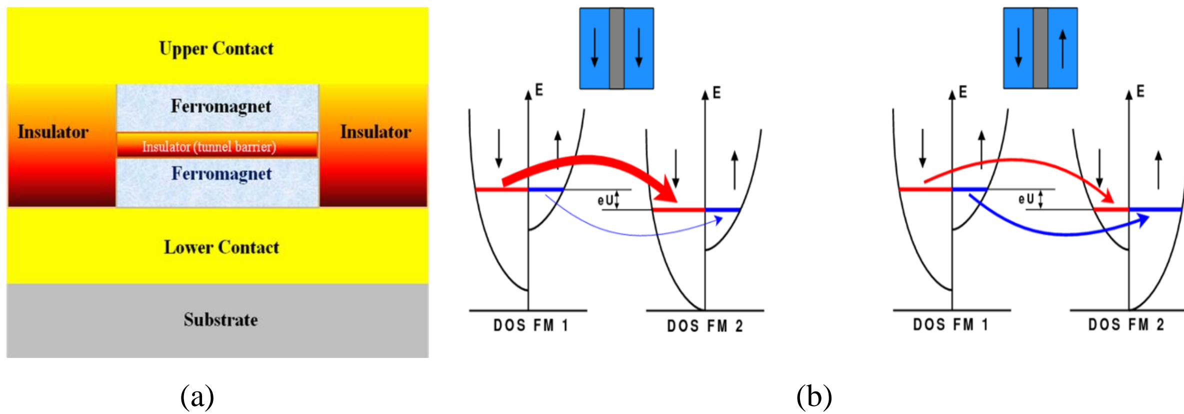
When the two magnetic layers are magnetized parallel (lower scheme in Fig), the spin-up electrons (spin antiparallel to the magnetization) can travel through the sandwich nearly un-scattered, providing a conductivity shortcut and a low resistance. In contrast, in the antiparallel case (top scheme) both spin-up and spin-down electrons undergo collisions in either F1 or F2, giving rise to a higher overall resistance.

The introduction of the spin-valve sensor by IBM in 1997 to replace the AMR sensor in magnetoresistive HDD read heads, has increased the growth rate for storage areal density immediately up to 100% per year. Together, the sequential introduction of the magnetoresistance and spin-valve head, by providing a sensitive and scalable read technique, contributed to increase the raw HDD areal recording density by three orders of magnitude (from ~0.1 to ~100 Gbit in–2) between 1991 and 2003. This jump forward opened the way both to smaller HDD form factors (down to 0.85-inch disk diameter) for mobile appliances such as ultra-light laptops or portable multimedia players, and to unprecedented drive capacities (up to a remarkable 1 terabyte) for video recording or backup. HDDs are now replacing tape in at least the first tiers of data archival strategies, for which they provide faster random access and higher data rates.

However, the areal density growth rate started to slow down after 2003, when other problems joined the now limiting spin-valve head.

2.4 Magnetic Tunnel Junction (MTJ)

A big revolutionary change came from replacing the non-magnetic metallic spacer layer M of the spin valve by a thin (~1–2 nm) non-magnetic insulating layer, thus creating a magnetic tunnel junction (MTJ). In that configuration the electrons travel from one ferromagnetic layer to the other by a tunnel effect, which conserves the spin. Again, this is not a new story, as it was proposed by Jullière24 in 1975, but its practical realization with a high magnetoresistance (up to 30% at 4.2 K) had to wait until 1995 once considerable progress had been made in deposition and Nano patterning techniques [33,34]. The first MTJs used an amorphous of Al_2O_3 insulating layer between ferromagnetic metal layers. The tunnel magnetoresistance (TMR) of such stacks reached a limit around 70% at room temperature. Much higher effects were later obtained with a single-crystal MgO barrier [35,36].



(a) (b)

Fig 2.6: a. Schematic of a Magnetic tunnel junction. b. Schematic representation of the tunnel magneto resistance in the case of two identical ferromagnetic metal layers separated by a non-magnetic amorphous insulating barrier such as Al_2O_3, the tunneling process conserves the spin. When electron states on each side of the barrier are spin-polarized, then electrons will more easily find free states to tunnel to when the magnetizations are parallel than when they are anti-parallel .

The magnetic tunnel junction is clearly a CPP (Current perpendicular to the plane) 'vertical' device, with a magnetic behavior similar to a spin valve but magnetoresistance values up to two orders of magnitude higher. It is stable up to reasonable breakdown voltages (above 1 V), and the equipment suppliers rapidly developed reliable techniques to scale down its dimensions to well below 100 nm. So its development had an immediate impact on storage applications.

MTJs have an intrinsic high resistance (with resistance–area products above 1 Ω cm^2), and with further downscaling it will become difficult to maintain a high signal-to-noise ratio with an increasing sensor resistance. Then CPP spin valves or degenerate MTJs could become more favourable.

2.5 Magnetoresistive Random-Access Memory (MRAM)

Magnetoresistive random-access memory (MRAM) technology combines a magnetic tunnel junction (MTJ) device with standard silicon-based microelectronics to obtain a combination of qualities not found in any other memory technology. MRAM is a high-speed, nonvolatile memory with unlimited read and write endurance. Because the data is stored in the magnetic state of the bit and is read out by sensing the resistance of the bit, MRAM is fundamentally different from commonly available commercial memories, such as dynamic RAM and flash memory, those are based on stored charge. Table 2.1 shows a qualitative comparison of MRAM and four other commercial memories.

Table 2.1: Comparison of Memory Technologies.

Property	SRAM	DRAM	Flash	FeRAM	MRAM
Read	Fast	Moderate	Fast	Moderate	Moderate-Fast
Write	Fast	Moderate	Slow	Moderate	Moderate-Fast
Nonvolatile	No	No	Yes	Partially	Yes
Endurance	Unlimited	Unlimited	Limited	Limited	Unlimited
Refresh	No	Yes	No	No	No
Cell Size	Large	Small	Small	Medium	Small
Low voltage	Yes	Limited	No	Limited	Yes

Since only MRAM combines non-volatility, read/write endurance, speed, and density, it has the potential to displace other memory technologies, particularly in applications that would otherwise require multiple memory types. An analysis of expected density and reduced system complexity shows that MRAM will also be cost-competitive, overall system costs are reduced by eliminating the need for integrating multiple types of memory. MTJ-based MRAM makes use of quantum mechanical tunneling of spin-polarized electrons through a very thin (15 Å) di-electric. The relative orientation of the magnetization in the two ferromagnetic layers determines the resistance of the MTJ structure. MRAM devices are designed to have two stable magnetic states that correspond to high- and low-resistance states. Low resistance occurs when the two layers have the same magnetization orientation; high resistance occurs when the orientations are opposed to each other.

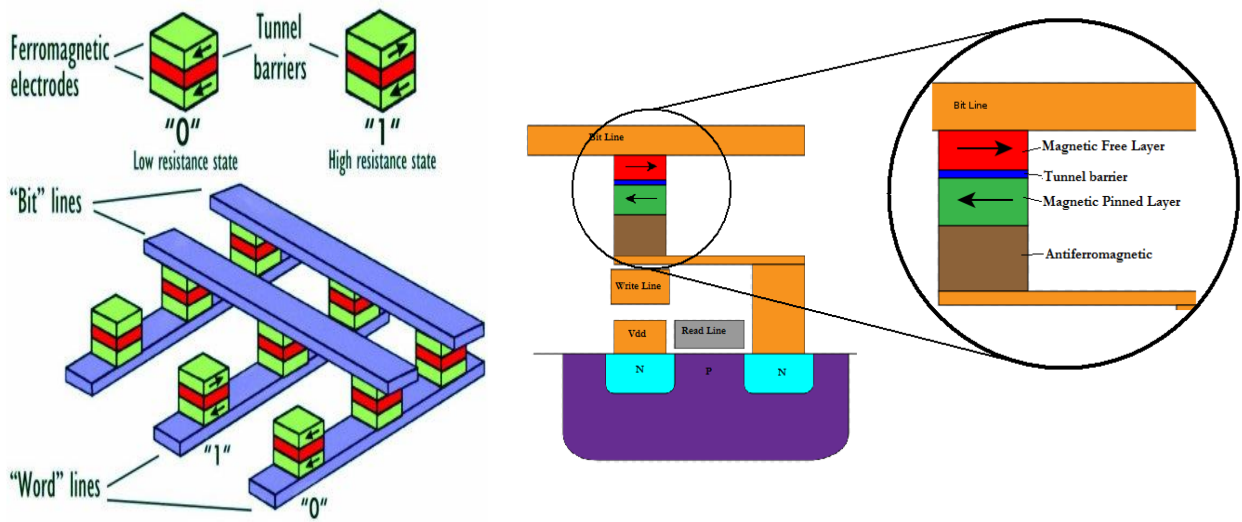


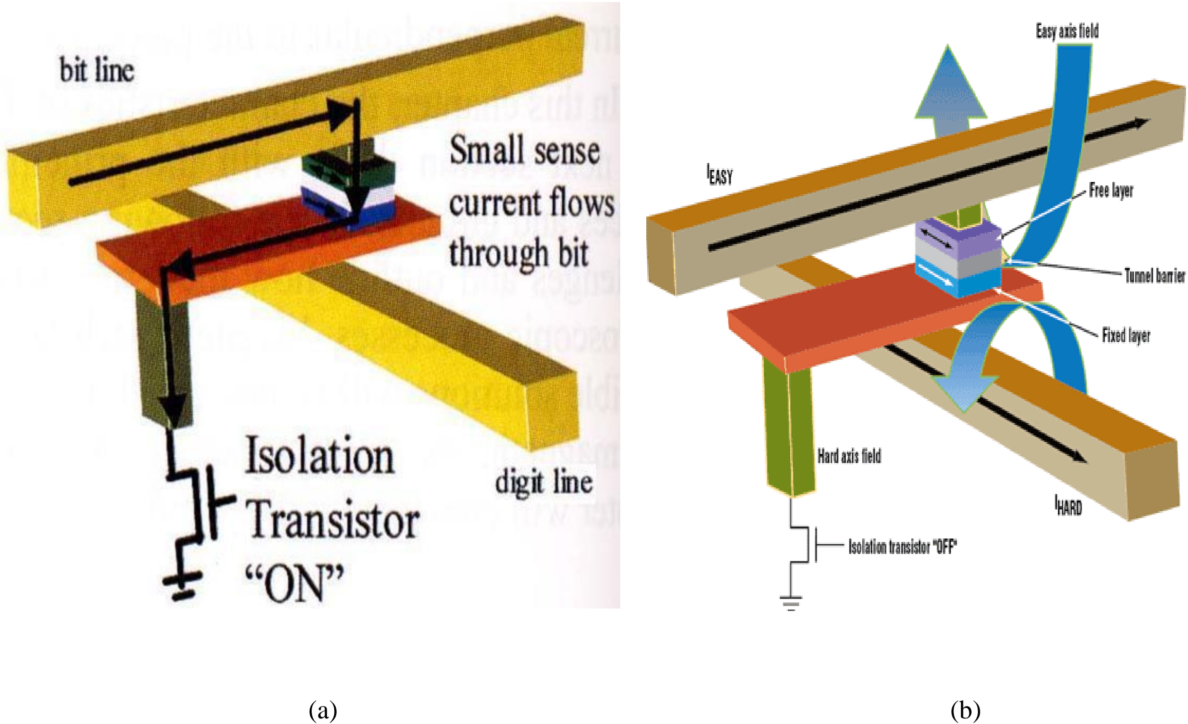
Fig 2.7: Magnetoresistive random-access memory (MRAM) technology combining a magnetic tunnel junction (MTJ) device with standard silicon-based microelectronics.

Unlike most other semiconductor memory technologies, the data is stored as a magnetic state rather than a charge, and sensed by measuring the resistance without disturbing the magnetic state. Using a magnetic state for storage has two main benefits.

First, the magnetic polarization does not leak away over time like charge does, so the information is stored even when the power is turned off. Second, switching the magnetic polarization between the two states does not involve actual movement of electrons or atoms, and thus no known wear-out mechanism exists.

2.5.1 MRAM: Reading and Writing process

From the cross point architecture we can see that MRAM has two bit lines and in between them there is MTJs which are coupled with silicon based microelectronics. To sense, or read, the bit, the isolation transistor is turned on and a current (I_{sense}) is passed through the magnetic



(a) (b)

Fig 2.8: Cross point architecture of a MRAM showing Read and Write process in MARAM showing reading (a) and writing process (b).

tunnel junction (MTJ). Measuring the electrical resistance of a small sense current from a supply line through the cell to the ground and comparing it with the reference value give the required read states. If the measured resistance is found to be higher than the reference value, then the read logic level will be high (1) and on the other hand if the resistance measured is found to be lower than the reference value then the read logic level will be low (0).

Writing, or programming, the bit involves applying currents (I) to each of the write lines so that field is generated at the bit from both lines simultaneously. When current is passed through the write lines, an induced magnetic field is created at the junction, which alters the polarity of the free layer. In order to change the polarity of the free layer, both fields are necessary. Only the bit in which current is applied in both hard and easy axis will be written. The other bits will remain half-select.

For conventional MRAM bits, a write operation consists of sending pulses of current down each of the two programming lines (write lines 1 and 2), so that they simultaneously apply both easy and hard axis magnetic fields to the bit. The system is engineered so that the field from a single pulse on either programming line is not sufficient to switch the bit, but the field generated by the combination of both programming lines is enough for switching to occur.

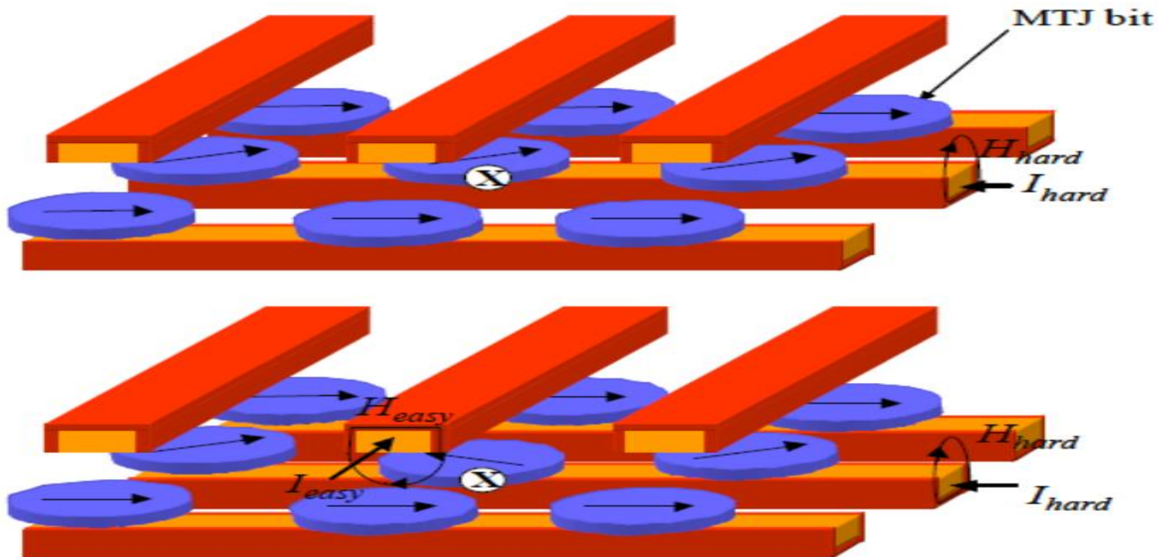


Fig 2.9: Writing process in a MRAM showing Easy and Hard axis.

2.5.2 Application of MTJ Based MRAM

MRAM devices are ideal replacement for battery-backed SRAM (BBSRAM). MRAM is a fast, non-volatile memory with unlimited endurance—a combination of characteristics not available in any other individual semiconductor memory product. MRAM is much faster—35 ns compared to BBSRAM at 70 ns read/write speed. It is a more reliable replacement of BBSRAM because it is a single-chip solution, compared to BBSRAM's complex multi-component system (including SRAM, battery and control chip). MRAM is directly swappable with BBSRAM since it has a standard JEDEC SRAM pin out and the ability to be written in a byte-wise configuration similar to BBSRAM.

Additionally, MRAM is priced competitively with BBSRAM. In addition to BBSRAM replacement, MRAM offers other significant performance advantages over existing memory technologies. For instance, nonvolatile memories, such as hard disk and flash, store instructions

and data from operating systems and individual programs, and transfer them to the processor when needed. This transfer can become a bottleneck and hinder processor performance. MRAM stores this same information, but with the capability to deliver it directly to the microprocessor without creating a bottleneck. These characteristics make MRAM a perfect nonvolatile memory for RAID servers, data streaming, system configuration and black-box applications.

MRAM is a revolutionary memory product that provides the highest density, the best price/performance and highest reliability of all non-volatile RAM product alternatives. MRAM technology is well positioned to supply high density, low-cost embedded memory capable of replacing Flash, SRAM and EEPROM with a single unified memory in many future microcontroller and system-on-chip products.

2.5.3 Problems Associated with MRAM

The use of a magnetic field to write the information still remained a considerable limitation. This can easily be understood. Let us assume that information is stored in the form of the magnetization orientation of a nanoparticle of volume V. The energy barrier fighting the thermal excitations is given by KV, where K is the anisotropy constant per unit volume. Non-volatility — usually defined by a maximum error rate, for example 10–9, over a 10-year period — is obtained when KV > 50–60k_BT, where k_B is the Boltzmann constant and T is the temperature. So reducing V requires a corresponding increase in K, but then the writing field increases proportionally with K, whereas the power available to create it decreases as the dimensions are downscaled. So conventional MRAM has two main drawbacks: i) Poor scalability and ii) High write current. To solve these problems a new technology has evolved ad it is Spin-Torque Transfer Magnetic RAM (STT MRAM).

2.6 Spin-Torque Transfer Magnetic RAM (STT MRAM)

Spin-torque transfer magnetic RAM (STT MRAM) is a promising candidate for future embedded applications. It combines the desirable attributes of current memory technologies such as SRAM, DRAM, and flash memories (fast access time, low cost, high density, and non-volatility). It also solves the critical drawbacks of conventional MRAM technology: poor scalability and high write current. The demand for on-chip embedded memories has grown significantly over the last few decades. On-chip memories can be accessed fast (contrary to large miss penalty associated with off-chip memories) and hence, increases the bandwidth of high performance processors. Several

memory technologies have been explored by researchers in the past. Static-RAM (SRAM) provides excellent read and write proper-ties but the cell size is relatively large (6-T structure) [T-transistor] and limits the amount of memory that can be integrated within the die. On-chip DRAMs have been explored as a possible alternative to SRAMs due to its small cell size (1-T or 3-T structures). However, leakage of information is severe in such memories and periodic refresh rates make them undesirable for portable electronics with limited battery life. In contrast to SRAMs and DRAMs, flash memories do not require external power to store data due to their nonvolatile nature. However, high-voltage and slow-write operations with limited read/write endurance overshadow the inherent advantages such as high integration density and simple architecture.

Spin-torque transfer magnetic random access memory (STT MRAM), derived from the cutting edge of research on Spintronics, is orthogonal to all previous memory technologies [37]. It combines all desirable memory attributes, e.g., nonvolatility, unlimited endurance, low power, high speed, and high memory density. Therefore, STT MRAM has gained lots of attention in today's memory community. Fig.{} shows the structure of a typical STT MRAM bit-cell. It consists of a transistor, a spintronic device (magnetic tunneling junction), word line (WL), bit line (BL) and source line (SL).

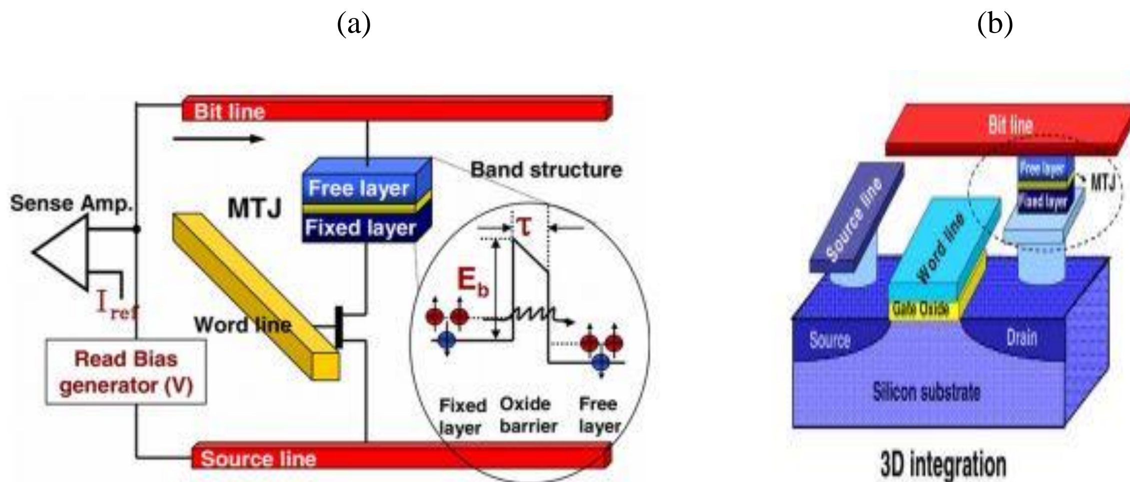


Fig 2.10: STT MRAM bit cell in 1-transistor-1-MTJ (1T1M) configuration includes: 1) Spintronic device: MTJ; 2) bit line; 3) source line; 4) word line; 5) nMOS; and 6) read driver. b. Cross section of an STT MRAM bit cell. MTJ is integrated with nMOS (dominating cell area) using 3-D technology

The basic building block of STT MRAM cell is the magnetic tunneling junction (MTJ). The MTJ is integrated with CMOS circuitry using 3-D technology [37]. When a sufficient current density passes through the MTJ, the spin polarized current will exert a spin transfer torque to switch the magnetization of free layer. This is the fundamental mechanism of STT MRAM. It allows STT-RAM to have a smaller cell size and write current than MRAM.

2.6.1 Operating Principle of STT MRAM

The equivalent circuit for an STT MRAM bit cell in read and write operations is shown in Fig (2.11).

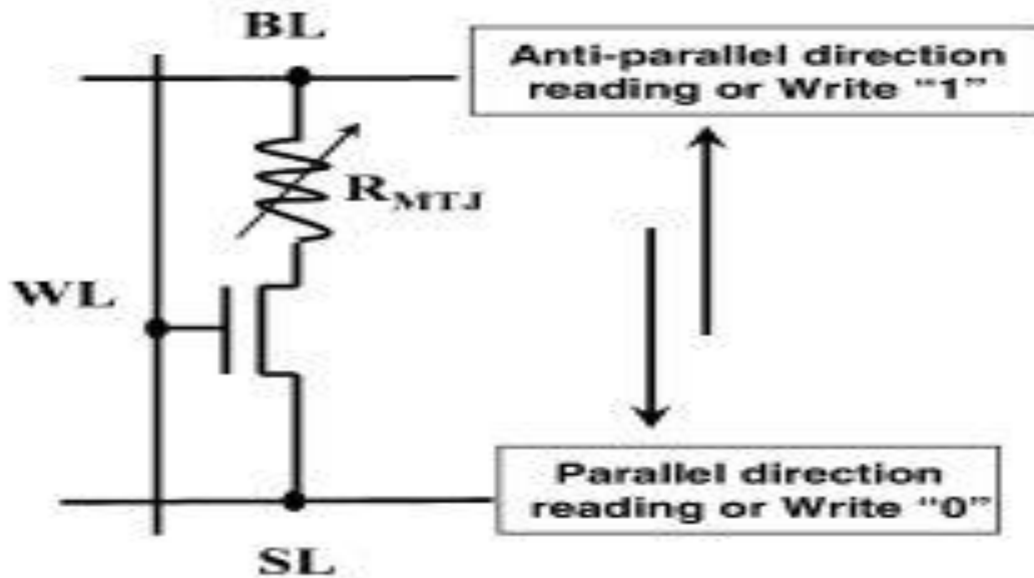


Fig 2.11: Equivalent circuit diagram of an STT MRAM bit cell in read and write operation.

There are two ways of reading a cell, namely parallel direction reading and anti-parallel direction reading. In parallel direction reading, we apply a small bias to BL and SL is grounded. After activating WL, cur-rent flows from BL to SL. In anti-parallel direction reading, the voltage polarity applied to BL and SL is switched and current flows in the reverse direction (from SL to BL).

In contrast to read operation, writing data to a cell requires much higher current. Due to the hysteresis nature of MTJ bi-directional current flow is required. For example, when writing a "0" to a cell storing "1", BL is precharged to V_{DD} and SL is grounded. If the cell current is above the switching threshold current of MTJ, the magnetization direction of the free layer begins to rotate from anti-parallel (high resistance state) to parallel direction (low resistance state).

2.6.2 STT-MRAM to Reduce Issues Associated with Conventional MRAM

Two major issues associated with conventional MRAM are: 1) high write current and 2) poor scalability [37], [38]. Conventional MRAM uses external current induced magnetic field to switch the magnetization direction of free layer from one direction to the other during write operation [28]. As MRAM scales, the magnetic field strength required for switching magnetization increases, resulting in dramatically increased write current and high power dissipation. In contrast to conventional MRAM, STT MRAM uses the direct injection of spin polarized current by spintronic device (MTJ) itself to switch the magnetization of the free layer and hence requires much less write current. More importantly, in STT MRAM, switching threshold current reduces with MTJ scaling, making it low power and highly scalable.

Chapter 3

Spin Transistor

(Spin Based Semiconductor)

Dramatic progress in the present integrated electronics has been powered by the miniaturization of transistors and the high degree of device integration, since the size reduction and large-scale integration of transistors provide improvements in integrated circuit performance including reliability and production cost. Metal–oxide–semiconductor field-effect transistors (MOSFETs) and complementary MOS (CMOS) devices (hereafter, both are referred to as MOS devices) based on sophisticated Si technology are a fundamental building block for mainstream integrated circuits, and they play an essential role as Btechnology drivers[in the current electronics. This is, of course, due to the excellent scalability and integration ability of MOS devices. The rapid and continual progress in the scaled down technology of MOS devices (that is, the so-called scaling) is known as Moore's law [43]–[45]. However, the scaling of preproduction MOS devices has already reached a physical limit of several nanometers, indicating the end of scaling in the near future. In such extremely scaled-down devices, leakage currents induced by quantum mechanical phenomena, various parasitic elements, and variability in device characteristics give raise to serious performance degradation problems. In addition, the production cost including facility investment becomes huge. These mean that the effect of scaling weakens for nanometer-scale MOS devices. Therefore, scaling in dependent technologies for improving device/circuit performance has attracted considerable attention.

In highly interconnected integrated circuits, the high current drivability of the transistors is very important for the circuit performance, since the circuit speed is dominated by charging/discharging of the load capacitance.

Therefore, the operating speed and operating principle of the individual transistors hardly affect the circuit speed, as long as they exhibit high current drivability. In addition, the high current drivability is also indispensable for other performance indices of the integrated circuits, such as low (dynamic) power dissipation. From these viewpoints, a great deal of effort has been made to achieve much higher current drivability for MOS devices so far. Therefore, it has been explored that new channel structures, such as fin, nanowire, and other three-dimensional structures, and new channel materials with high carrier mobility, such as strained Si, Ge, III-V compound semiconductors, and grapheme, are introduced into MOS devices. An effect equivalent to scaling

can be substantially achieved by introducing new channel structures/materials without scaling, which is sometimes called the Bmore Moore [approach or the Bextended CMOS] concept [46]. It should be noted that the operating principle of extended CMOS devices is the same as that of ordinary MOS devices, although the channel structure and material of extended CMOS devices are replacing conventional ones. Introduction of new functionality, such as quantum effects and spin-related phenomena, into integrated circuits is also expected to be an alternative approach instead of the scaling. By introducing new functionality, the transistor performance itself would not become superior to conventional MOS devices. However, there exists a possibility for improving the circuit performance by employing new circuit architectures based on newly added functionality. In order to achieve such new architectures, a new MOS device with the desired functionalities must be realized. One approach is a combination of a MOS device with a so-called functional device at the circuit level. In many cases, functional devices have no characteristics (in particular, high current drivability) suitable to integrated circuits, except for new functionalities. Therefore, they should be used in combination with MOS devices. For example, this approach was examined in quantum effect devices. A quantum effect transistor consisting of an ordinary field-effect transistor (FET) and a resonant tunnel device was demonstrated. Another approach is the device-level integration of a MOS device and a functional device with a hybrid structure. Several functional MOS devices that contain the structure of two-terminal functional devices in their device structure have been proposed so far, such as a Josephson junction [47], [48], a Esaki diode [49], a resonant tunnel device and a magnetic tunnel junction. The important features of functional MOS devices, except for newly added functionalities, could be high current drivability and exponentially steep on/off switching of MOS devices, which would be inaccessible to any other functional device. The paradigm shift from device scaling to the introduction of new functionalities to MOS devices could become an important route to future integrated electronics technology. Note that an electronic device based on new physical phenomena and/or new state variables is called a beyond-CMOS device, and new devices uniting a beyond-CMOS element with an ordinary MOS device are referred to as the Bnonconventional extended CMOS [46].

The aim of recently emerging spintronics (spin electronics) research is to manipulate spin degrees of freedom in solid state devices and provide new concepts for future electronics and photonics employing spin degrees of freedom. One of the most attractive research directions is to control charge and spin transport phenomena in active electronic devices, i.e., spin transistors. Spin transistors are a new type of concept device that unites an ordinary transistor with the useful functions of a spin (magneto resistive) device. The interesting features of spin transistors are nonvolatile information storage and reconfigurable output characteristics, which are very useful and suitable functionalities for future high performance integrated circuit architectures such as

nonvolatile logic (e.g., nonvolatile power-gating systems) and reconfigurable logic (e.g., nonvolatile field programmable gate arrays). Following the first proposal of the spin transistor concept by Datta and Das and Johnson, a wide variety of spin transistors based on various operating principles have been proposed so far.

In this article, we present the current status and outlook of spin transistors. After a brief review of the fundamental and key phenomena/technologies for spin transistors in Section II, the device structure, operating principle, and features of various spin transistors are described in Sections III, IV, and V, in which we focus on potential-effect spin transistors in the Section III and field effect spin transistors in Sections IV and V. Finally, integrated circuit applications of spin transistors, including nonvolatile logic and reconfigurable logic systems that are the most suitable applications of spin transistors, are presented in Section VI.

3.1 Requirements for Spin Transistor [3]

Spin transistors, which generally have two ferromagnetic layers as a spin injector and a spin detector, can be active three-terminal devices. Ideally, spin transistors exhibit ordinary transistor actions with variable output characteristics which can be controlled by the relative magnetization configuration of the two ferromagnetic layers. In many cases, the trans-conductance, gm (the output-current drive capability for the input voltage) of spin transistors can be switched by the relative magnetization configuration. This feature is often referred to as magnetization configuration-dependent output characteristics. To express qualitatively magnetization configuration dependent output characteristics, the magneto-current ratio defined by

$\gamma MC = (IC_P - IC_{AP}) / IC_{AP}$

where P and AP refer to the parallel and antiparallel magnetic state of the base spin valve, respectively. Furthermore, the magnetization configuration can be also used as nonvolatile binary data. Owing to these useful features, spin transistors are potentially applicable to integrated circuits for ultrahigh-density nonvolatile memory whose memory cell is made up of a single spin transistor and for nonvolatile reconfigurable logic based on multifunctional spin transistor gates. Although magnetization-configuration dependent output characteristics are needed to realize such “spin-electronic” integrated circuits, device performance as a “transistor” is still important. In order to be used in integrated circuits as active devices, spin transistors must satisfy the following requirements-

1) Large magnetocurrent ratio (γMC) for nonvolatile memory and logic functions.

2) High transconductance (gm) for high-speed operation.

3) High amplification capability (voltage, current, and/or power gains) to restore propagating signals between transistors and to be applied for analog circuits.

4) Small power-delay product and small OFF-current for low-power dissipation.

5) Excellent scalability and simple device structure for high degree of integration and high process yield.

Thus, it is important to explore spin transistors that simultaneously satisfy all the requirements noted above [items 1)–5)].

3.2 Fundamental of Spin Transistor

3.2.1 Two-Terminal Magnetoresistive Devices

Two-terminal magneto resistive devices are a basic building block of spin transistors. After the discovery of the giant magneto resistance (GMR) effect in ferromagnetic/ nonmagnetic metal multilayers, magneto resistive devices have received considerable attention. Here, we briefly review two-terminal magneto resistive devices from the viewpoint of their application to spin transistors. Their magneto resistive memory (MRAM) applications were reviewed in. Fig. 3.1 schematically shows the structures and typical current–voltage ðI_VÞ characteristics of two-terminal magneto resistive devices. Spin valve (SV) devices consist of at least two ferromagnetic metal (FM) layers separated by an ultrathin nonmagnetic metal (NM) spacer layer, as shown in Fig. 3.1(a). They are classified into current-in-plane (CIP) and current-perpendicular-to-plane (CPP) geometries, and CPP-SVs have been applied to spin transistors. Ferromagnetic transition metals and their related alloys, including full-Heusler alloys, have been applied to the ferromagnetic layers and nonmagnetic transition metals and other nonmagnetic metals have been used for the spacer layer. Magnetic tunnel junctions (MTJs) have a device structure

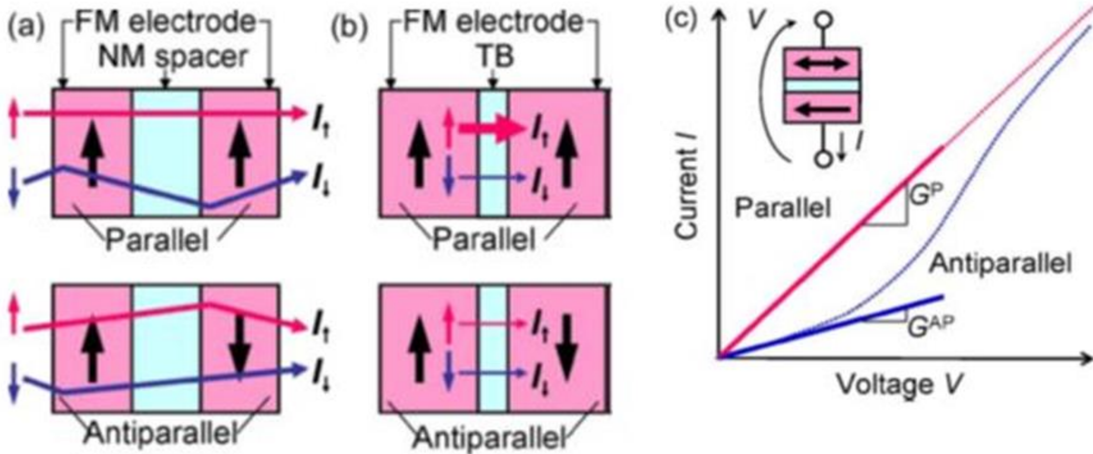


Fig 3.1: Schematic representations of (a) CPP-SV and (b) MTJ devices. (c) current–voltage characteristics of these devices. FM, NM, and TB represent ferromagnetic metal, nonmagnetic metal, and tunnel barrier, respectively.

similar to SVs, however the metallic spacer in the SVs is replaced by an insulating tunnel barrier (TB) layer, as shown in Fig. 3.1(b). The MTJ technology was initially developed by the invention of the AlO_x tunnel barrier, and its subsequent dramatic progress has been due to the development of MgO tunnel barriers.

Furthermore, half-metallic ferromagnet electrodes using full-Heusler alloys have also had a great impact on the MTJ technology [50]. SVs and MTJs are designed to establish two relative magnetization configurations of parallel and antiparallel alignments. The electrical conductance of both the devices depends on the magnetization configuration. SVs and MTJs exhibit qualitatively the same features in spite of different mechanisms, i.e., a high conductance is achieved in parallel magnetization and it becomes low in antiparallel magnetization, as schematically shown by solid lines in Fig. 3.1(c). This phenomenon can be attributed to spin dependent scattering for SVs and to spin-dependent tunneling for MTJs, which is sometimes called the spin valve effect for SVs and the tunneling magnetoresistance (TMR) effect for MTJs. The magnetoresistance ratio is defined by _MR ¼ ðGP _ GAPÞ=GAP that is a measure of magnetoresistive devices, where GP and GAP represent the electrical conductance in the parallel and antiparallel magnetization configurations, respectively. Note that the I_V characteristics of the magnetoresistive devices well reflect the feature of their device structures, and the _MR value often depends on a bias voltage. In the case of MTJs, it is known that the I_V characteristics show a nonlinear behavior and _MR decreases with increasing bias voltage, as schematically shown by the dashed curves in Fig. 1(c). The _MR of MTJs is much higher than that of SVs. In contrast, the resistivity of SVs is much lower than that of MTJs, which is caused by a difference in the resistivity between the metallic spacer layer and the insulating tunnel barrier. The spin-filter effect that

enables the selective propagation of carriers depending on their spin orientation is also useful for magnetoresistive devices. Fig. 3.2 shows the basic structure of two-terminal spin-filter devices. Ferromagnetic tunnel barriers [Fig. 3.2(a)], using a ferromagnetic insulator (FI), and ferromagnetic pn junctions [Fig. 3.2(b)], using a ferromagnetic semiconductor (FS), can act as spin filters based on the spin-dependent tunnel barrier and the spin-dependent built-in potential, respectively. By installing a ferromagnetic electrode as a spin injector or a spin detector to these spin-filter devices, magnetization configuration- dependent I_V characteristics can be obtained, i.e., they act as a magnetoresistive device.

In order to establish the parallel and antiparallel magnetization configurations of magnetoresistive devices, exchange bias induced by anti-Ferro magnets is commonly used. When an anti-ferromagnetic/ferromagnetic layered structure is cooled with a magnetic field from a temperature above the Neel temperature of the anti-Ferro magnet layer (that is lower than the Curie temperature of the ferromagnetic layer), a magnetic anisotropy, the so called exchange bias, is induced in the structure. The resulting hysteresis loop of the anti-ferromagnetic/ferromagnetic system is shifted along the field axis (generally in the opposite direction to the applied field during the cooling) by the anisotropy, which is referred to as the spinning [of the Ferro magnet layer. When one of two ferromagnetic layers in a magnetoresistive device is sufficiently pinned (which is called the pinned layer), the parallel and antiparallel configurations can be easily formed by magnetization switching of the other ferromagnetic layer (which is called the free layer), since the magnetization of the pinned layer

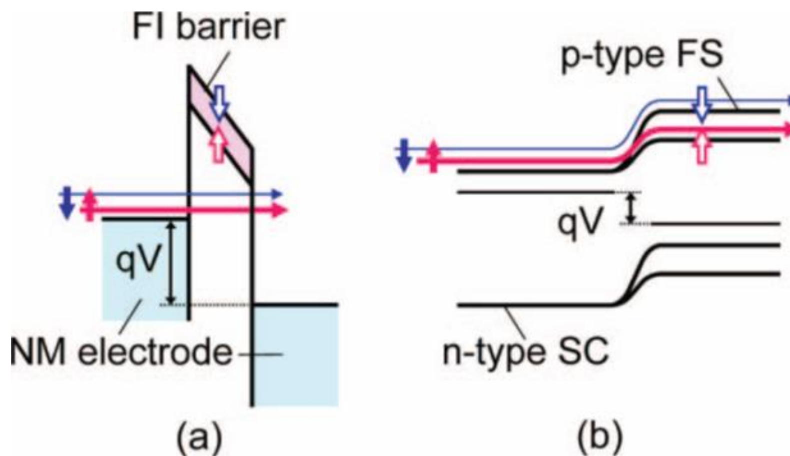


Fig. 3.2: Schematic representations of the spin-filter effect in (a) ferromagnetic tunnel barrier and (b) ferromagnetic pn junction. FI, FS, and SC represent ferromagnetic insulator, ferromagnetic semiconductor, and semiconductor, respectively.

cannot be switched by the magnetic field for the magnetization reversal of the free layer. Note that a shape magnetic anisotropy of ferromagnetic films is often used in laboratory experiments for

generating different cervicitis in ferromagnetic electrodes in magnetoresistive devices, which is also useful for achieving the formation of the parallel and antiparallel configurations.

Attractive functionalities of two-terminal magnetoresistive devices for integrated circuit applications are nonvolatile information storage based on the magnetization configuration and reconfigurable output characteristics depending on it. Therefore, these devices are promising not only for nonvolatile memory but also for new logic circuits using the nonvolatile and reconfigurable features. However, the two-terminal magnetoresistive devices would not be suitable for logic circuits when they used as logic elements, since they are a passive device. Of course, logic circuits can be configured by using two terminal passive devices. Nevertheless, these devices have no following functions that are strongly required for logic circuits: high current drivability for high-speed and low power operations and for sufficient fan-out, amplification capability for the restoration of attenuating signal, sufficient cutoff behavior for low standby power, and sufficient isolation behavior between input and output. (Note that the isolation behavior is required for logic devices, since the unidirectional propagation of a logic signal from input and output is crucial for logic circuits.) Therefore, three terminal transistor-type magnetoresistive devices, that is, spin transistors, are attractive. Spin transistors are a new concept device that unites an ordinary transistor with the useful functions of a two-terminal magnetoresistive device, which is realized by the device-level integration of these devices with a hybrid structure. Several ordinary potential effect transistors (PETs) and FETs are applied to spin transistors as their basic device structure, as described in this paper. It is worth noting that ordinary transistors (such as MOSFETs) used in present integrated electronics completely satisfy the above-described requirements.

Another way to use two-terminal passive magnetoresistive devices in logic circuits is in a circuit-level combination of magnetoresistive devices with CMOS circuits. Although this method is not necessarily ideal, there is the advantage that the present MRAM technology can be applied to spin transistors, as also discussed in this paper.

3.2.2 Spin Injection and the Conductivity Mismatch Problem

In the case of spin injection from an ordinary Ferro magnet (i.e., a ferromagnetic metal) to a semiconductor through the ohmic junction, a high efficiency spin injection can hardly be achieved, which is known as the conductivity (or impedance) mismatch problem [51]. This originates from the fact of the large difference in electrical conductivity between a ferromagnetic metal and a semiconductor, as shown below. Although the resistance of the spacer layer is not taken into account in CPP-SV devices as shown in Fig. 3.1(a), it becomes problematic when the spacer layer

belongs to a semiconductor. In general, the conductivity mismatch problem is treated by using electrochemical potential for spin-up and spin-down electrons. Here, we introduce a simple resistance network model for qualitative understanding. In the resistance network model, a ferromagnet can be expressed by a parallel circuit of two different resistances that represent the majority and minority spin channels of the ferromagnet. This circuit model can show the current spin-polarization of the ferromagnet. In a similar fashion, a semiconductor is expressible by a parallel circuit of two resistances of the same magnitude for spin-up and spin-down electrons. Fig. 3.3(a) shows the resistance network model of a ferromagnet (FM1)/semiconductor (SC)/ferromagnet (FM2) junction in the parallel magnetization configuration, where it is assumed that the FM1/SC and SC/FM2 junctions are ohmic, and that spin flip in the SC region can be eliminated. Rmaj FM and Rmin FM ð> Rmaj FMÞ represent the resistances for the majority and minority spin channels in FM1 and FM2, respectively, and RSC represent the resistance for the spin-up and spin-down channels in SC (both are equal). Here, the majority spin of FM1 is assumed to be the spin-up. The conductivity mismatch problem can be understood by treating the currents of the spin-up and spin-down channels in the parallel magnetization configuration. When the resistance of SC is comparable with that of FM1 and FM2, the combined resistances for the spin-up and spin-down channels are different. The resulting current for the spin-up channel is higher than that for the spin-down channel. Therefore, the total current that flows in this structure is spin-polarized.

When RSC is much higher than Rmaj FM and Rmin FM , which is an actual case, the situation is quite different. In this case, Rmaj FM and Rmin FM can be neglected, and the voltage drop is caused entirely in the SC region. Therefore, the spin dependent resistances (Rmaj FM and Rmin FM) of FM1 and FM2 have no effect on the currents in the spin-up and spin down channels, i.e., the currents are determined by spin independent RSC, and thus the total current cannot be spin-polarized. This phenomenon is referred to as the conductivity mismatch problem.

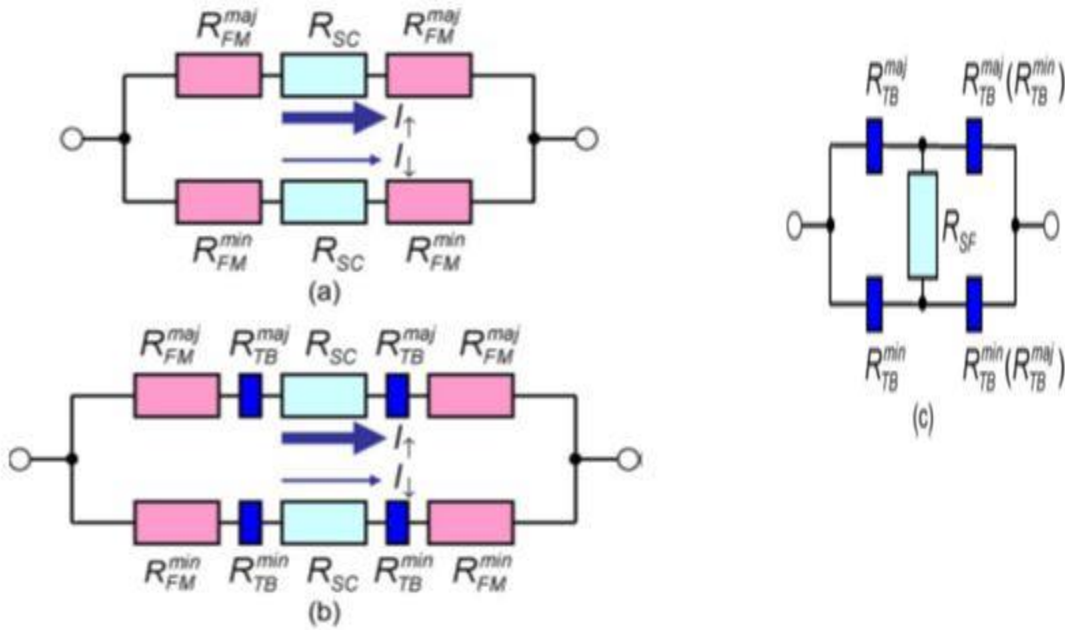


Fig. 3.3: Resistor network model for an FM/SC/FM junction. (a) Equivalent circuit for parallel magnetization. (b) Equivalent circuit with interface resistance for parallel magnetization. (c) Equivalent circuit for parallel magnetization in the case of high interface resistance. The parentheses represent the equivalent circuit for antiparallel magnetization.

In order to evade the conductivity mismatch problem, it was proposed to add tunnel barriers (TB1 and TB2) at the interfaces of the FM1/SC and SC/FM2 junctions instead of the ohmic contacts, as shown in Fig. 3.3(b). The tunnel barriers can be formed by placing an ultrathin insulator at the interfaces, and also by using a ferromagnetic metal/ semiconductor Schottky junction. The contact resistance (tunnel resistance) of such a tunnel barrier would be spin dependent, owing to the effect of the ferromagnetic electrode. Fig. 3(b) shows the equivalent circuit of a FM1/TB1/ SC/TB2/FM2 junction including the effect of the spin dependent tunnel resistance, where Rmaj TB ½Rmin TB ð> Rmaj TB Þ_ represents the tunnel resistance of TB1 and TB2 for the majority [minority] spin channel. When Rmaj TB and Rmin TB are comparable with RSC or, more preferably, higher than RSC, the combined resistances for the spin-up and spin-down channels become sufficiently different. Therefore, the total current passing through this structure is spin-polarized by introducing the tunnel barriers at the interfaces. It is also predicted that the conductivity mismatch problem can be excluded by the use of a half-metallic ferromagnet (HMF) [8] with a spin polarization of 100% as a ferromagnetic electrode, in which the addition of a tunnel barrier is not required. However, in practice, this could be challenging, since there is a difficulty in the material formation/processing of completely spin-polarized HMFs. There is also a possibility that the spin polarization of HMF electrodes deteriorates at the interface with a semiconductor. Eventually, a tunnel barrier (formed by an ultrathin insulating film or a Schottky junction) would be required

even for an HMF electrode. Nevertheless, HMFs are the most promising material to achieve spin injection with high efficiency, since they can exhibit a very high spin polarization that is inaccessible to ordinary Ferro magnets (even if the spin polarization is not exactly 100%). Note that the conductivity of ferromagnetic semiconductors is in the same range of that of semiconductors. Therefore, the ohmic contact between a ferromagnetic semiconductor and a semiconductor is applicable to spin injection without the conductivity mismatch problem. We next consider the problem that arises when the tunnel resistance of TB1 and TB2 is enlarged. In this case, it is necessary to include the effect of the spin-flip phenomenon in the SC region, since a high contact resistance of TB2 can restrict the amount of electrons passing from SC through TB2 to FM2. This situation can be expressed by a bridge circuit shown in Fig. 3(c), where the resistance ðRSFÞ between the spin-up and spin-down channels expresses the effect of the spin flip and the resistances of FM1, SC, and FM2 are neglected. Furthermore, RSF! 0 (i.e., a short circuit) can be assumed when the tunnel resistance of TB1 and TB2 is very high. The circuit shown in Fig. 3(c) represents the case of parallel magnetization, and the case of antiparallel magnetization is indicated in parentheses. The short circuit has no effect on the current spin-polarization in parallel magnetization, owing to the equilibrium condition of the bridge circuit.

However, the short circuit acts on the spin polarization of the current in antiparallel magnetization and thus the magnetoresistance ratio. The combined resistances in the parallel and antiparallel magnetization configurations become equal, and the resulting magnetoresistance ratio is zero. Therefore, when the tunnel resistances of TB1 andTB2 are too high, a sufficient magnetoresistance ratio cannot be obtained by the effect of the spin flip in the SC region. The precise description of the appropriate range of the tunnel resistance was given by.

Spin injection into semiconductors have been revealed by optical and electrical methods. Spin light emitting diodes (spin-LEDs) are often used to verify spin injection phenomena. In spin-LEDs, spin polarized electrons are electrically injected from a ferromagnetic electrode to a semiconductor through a Schottky barrier or a tunneling barrier. The spin polarization of the injected electrons (i.e., the spin injection efficiency) can be obtained by analyzing the circular polarized light emitting from the quantum well fabricated in the semiconductor region. The spin injection efficiency from several percent to several tens percent was observed for spin-LEDs using III-V semiconductors. Spin-LEDs were also applied to the verification of spin injection into Si, using a Si n-i-p LED structure. Nonlocal multi-terminal devices are commonly used for studying the spin injection/transport phenomena in semiconductors. Spin-polarized electrons are injected from one ferromagnetic electrode placed in the Blocal[part of the device and pure spin currents generated by the spin injection are detected by another ferromagnetic electrode placed in the Bnonlocal[part.

The nonlocal measurement effectively eliminates any spurious phenomena induced by a stray field from the ferromagnetic electrodes. However, measurements of the Hanle effect (that is, spin precession and dephasing of conduction electrons in a perpendicular magnetic field) would be essential for the verification of spin-current detection. Spin injection and coherent spin transport including the Hanle effect in Si and GaAs were clearly observed by using nonlocal multi-terminal devices. A recently reported measurement technique of the Hanle effect using a hot electron transistor is described in Section III-A.

3.2.3 Spin Relaxation in Semiconductors

When spin-dependent transport phenomena are applied to transistors, i.e., spin transistors, the spin relaxation of conduction electrons in semiconductors can play an important role in spin-transistor operations. Spin relaxation in semiconductors can be classified by its mechanism, i.e., Elliott–Yafet (EY) [52], [53], D'yakonov–Perel' (DP) [54], Bir–Aronov–Pikus (BAP) [55], and hyperfine interaction mechanisms. From the viewpoint of spin-transistor applications, the EY mechanism in elemental semiconductors such as Si and the DP mechanism in III-V compound semiconductors such as GaAs, as shown in Fig. 3.4 (a) and (b), respectively, are especially important.

The EY mechanism is a spin relaxation process caused by scattering via phonons, impurities, boundaries and so on. In the electronic band structures of semiconductors, the spin up and spin-down states are mixed by the spin-orbit interaction of the constituent elements of the host material. As a result, the spin-up state contains a small component of the spin-down state and vice versa. (The amplitude of the mixed component depends on the strength of the spin-orbit interaction.) Therefore, spin polarized electrons in a semiconductor will get a chance for a spin flip after many scattering events, although the probability of the spin flip might not be so high. Therefore, the rate of the spin relaxation (that is given by the reciprocal of the spin relaxation time) caused by the EY mechanism is proportional to the rate of the momentum relaxation. A similar spin relaxation is also caused by the spin-orbit interaction induced by the potentials of impurities in highly impurity-doped samples. The EY mechanism appears in elemental semiconductors, such as Si, with a center of inversion symmetry (which is caused in the diamond structure of elemental semiconductors) and in compound semiconductors, such as GaAs, without a center of inversion symmetry (which is caused in the zinc blend structure of compound semiconductors). The EY mechanism can appear in narrow-gap compound semiconductors having a strong spin-orbit interaction, although the DP mechanism described below dominates in middle-gap compound semiconductors, such as GaAs and InGaAs, that have a moderate spin-orbit interaction. The EY mechanism is also a predominant process of spin relaxation in elemental semiconductors (owing to the lack of the DP mechanism in

this material system). In phosphorus-doped Si with a dopant concentration lower than _1018 cm_3, the spin relaxation time has no dependence on the dopant concentration above 200 K (i.e., the spin relaxation is restricted by phonon scattering), and a fairly long spin relaxation time of about 10 nsec was observed at room temperature, which is, of course, due to the very weak spin-orbit interaction in Si. In heavily impurity-doped Si samples, the spin relaxation time decreases with the doping concentration. However, a long spin lifetime greater than 140 ps was observed even in heavily doped n-type silicon at 300 K.

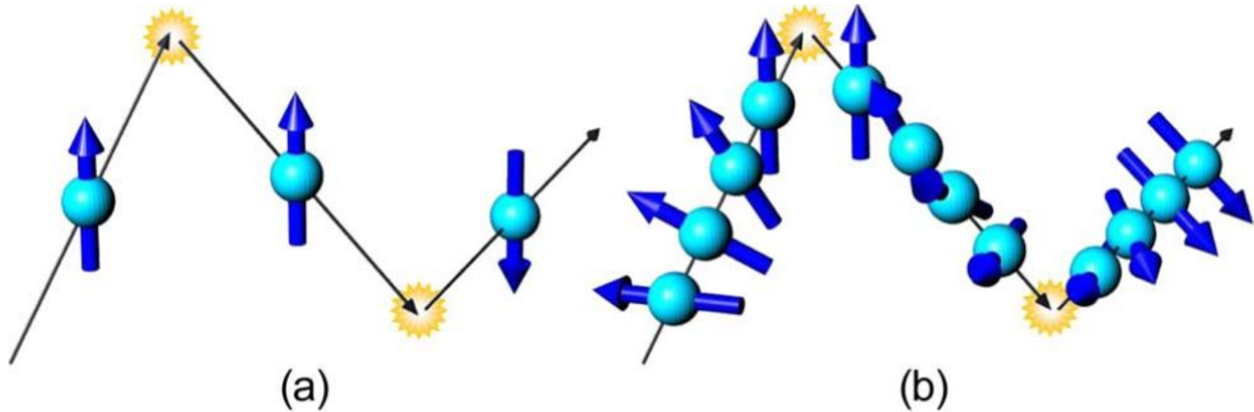


Fig. 3.4: Important spin relaxation mechanisms in semiconductors. (a) Elliott–Yafet mechanism, and (b) D'yakonov–Perel' mechanism.

The DP mechanism is an important spin-flip process of conducting electrons in compound semiconductors without\ a center of inversion symmetry. The spin degeneracy in their band structure is lifted by the spin-orbit interaction.

Therefore, spin-up and spin-down electrons, even in the same momentum state, experience different energies that depend on the momentum state. This situation is equivalent to causing an internal effective magnetic field depending on the momentum state. The spin moment of moving electrons precesses due to the effective magnetic field until scattering, and then the precession starts again after the scattering. However, the direction and the frequency of the precession change at random, since the effective magnetic field changes with the momentum scattering.

Therefore, the spin polarization diffuses with these precession processes. The remarkable feature of the DP mechanism is that the spin relaxation rate is proportional to the momentum relaxation time. The shorter the momentum relaxation time is, the lower the spin relaxation rate is (i.e., the spin relaxation time is longer). In middle-gap III-V semiconductors with a low or moderate

impurity concentration, the DP mechanism can dominate in a wide range of temperatures including high temperatures. In quantum well or hetero junction structures, the effective (Bychkov– Rashba) spin-orbit interaction is induced by structural inversion asymmetry, which also causes spin relaxation due to the DP mechanism. This spin relaxation mechanism plays an important role for III-V hetero structure systems. The DP mechanism was also found to be dominated in Si quantum well structures at low temperatures. The BAP mechanism is caused in p-type semiconductors. Electrons in p-type semiconductors are coupled with holes by the exchange interaction between them. The total spin is preserved by this coupling interaction. Since the effect of the spin-orbit interaction is very strong in the valence band, the spin relaxation of holes (that would be caused by the EY mechanism) is very fast in comparison with electrons. Because of the coupling interaction, the spin relaxation of electrons is quickly accompanied by that of holes. The BAP mechanism coexists with the EY and DP mechanisms, and stands out at lower temperatures or in heavily doped p-type samples. The hyperfine interaction between spin moments of an electron and nuclei causes a spin relaxation for a localized electron such as an electron confined in quantum dots or bound on donors. The wave function of a localized electron is spread over many lattice sites. Therefore, the magnetic moments of many nuclei affect the localized electron through an effective magnetic field induced by the hyperfine interaction, resulting in the spin relaxation of the localized electron. Since the hyperfine interaction is very weak, this spin relaxation mechanism is ineffectual to itinerant electrons. In GaAs the hyperfine interaction is caused by nuclear spins of the lattice nuclei, while in Si it frequently comes from donor 31P due to no nuclear spin of the most abundant isotope 28Si. Therefore, the hyperfine interaction in Si is much smaller than in GaAs. Nevertheless, in phosphorus-doped Si, the spin relaxation of electrons due to the hyperfine interaction was observed at low temperatures below 50 K, where the electrons are bound on the donor levels.

3.3 Spin Valve Transistor

3.3.1. Basic Device Structure and Properties

The SVT was introduced in 1995 and is the first working hybrid device in which ferromagnets and semiconductors have been closely integrated and both materials are essential in controlling the electrical transport through the device. The three-terminal device has the typical emitter/base/collector structure of a (bipolar) transistor, but is different in that the base region is metallic and contains at least two magnetic layers separated by a normal metal spacer (see figure 3.5). The two magnetic layers act as polarizer and analyser of electron spins, such that the relative orientation of the magnetization of the two layers determines the transmission of the base.

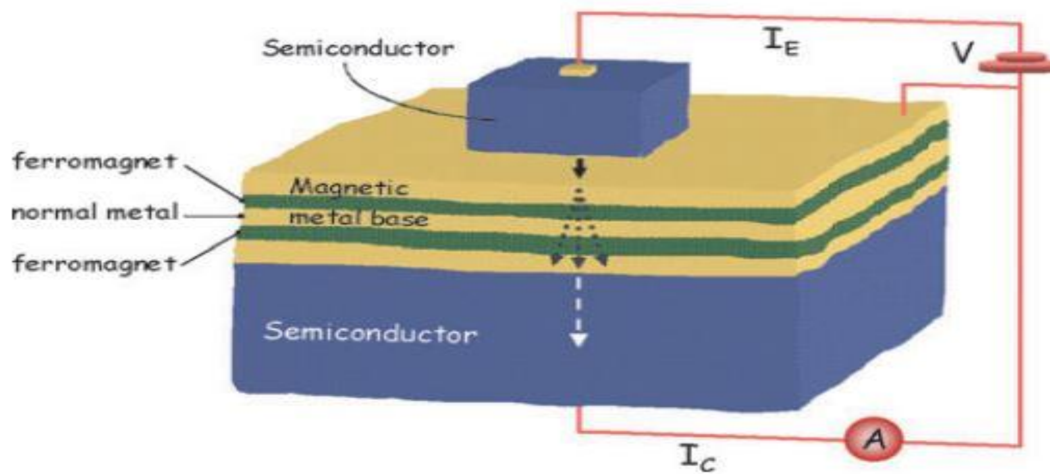


Figure 3.5: Basic layout of the SVT, showing the three terminal arrangement with semiconductor emitter (top), semiconductor collector (bottom), and the metallic base comprising two ferromagnetic thin layers separated by normal metals (middle).

The resulting salient feature of the SVT is that the collector current depends on the magnetic state of the base. This was first demonstrated by Monsma *et al* [4] in a SVT showing a huge change of 390% of the collector current in an applied magnetic field at low temperature. In 1998, the first device operating at room temperature was achieved, having a 15% effect in fields of a few kOe [5]. More recently, Anil *et al* [6, 7] succeeded in the reproducible fabrication of SVTs that exhibit magnetocurrent effects up to 400% at room temperature, and in small magnetic fields of only a few Oe.

Unlike other spintronic devices, the SVT is based on the spin-dependent transport of non-equilibrium, so-called hot electrons, rather than Fermi electrons. In order to illustrate this and explain the principle of operation, let us consider the specific structure that was used in [6]. That particular SVT uses silicon as the semiconductor for the emitter and collector, and has a metallic base that contains a Ni80Fe20/Au/Co spin valve (see figure 3.6). At the interfaces between the metal base and the semiconductors, energy barriers (Schottky barriers) are formed [8]. These energy barriers prevent electrons with the Fermi energy from travelling through the structure. To obtain the desired high quality Schottky barrier with good rectifying behaviour and thermionic emission dominating, low doped Si (1–10 Ω cm) is used, and thin layers of, e.g. Pt and Au are incorporated at the emitter and collector side, respectively. These also serve to separate the magnetic layers from direct contact with Si.

3.3.2 The Operation of the SVT

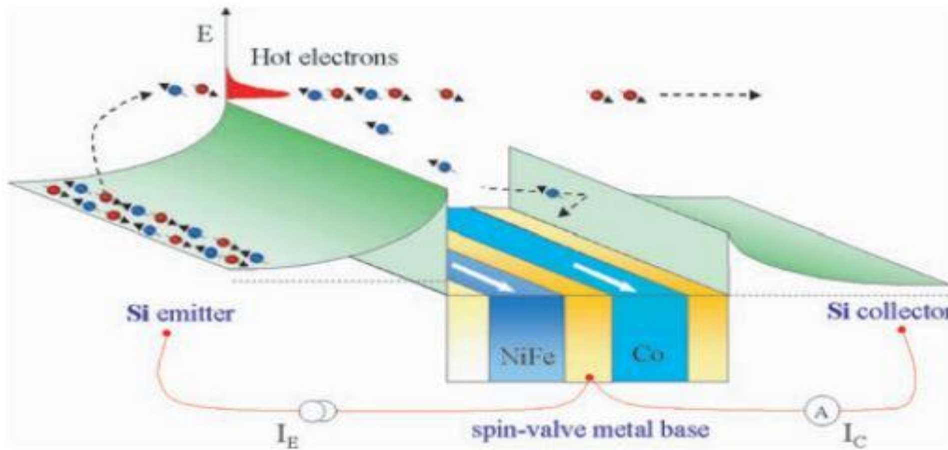


Figure 3.6: Schematic layout and energy band diagram of a SVT, showing the semiconductor emitter (left) and collector (right), and the metallic base comprising a spin valve (middle). Also depicted is the stream of electrons that is injected into the spin valve base above the Fermi energy.

A current is established between the emitter and the base (the emitter current IE), such that electrons are injected into the base, perpendicular to the layers of the spin valve. Since the injected electrons have to go over the Si/Pt Schottky barrier, they enter the base as non-equilibrium, hot electrons. The hot electron energy is determined by the emitter Schottky barrier height, which is typically between 0.5 and 1 eV, depending on the metal/semiconductor combination [8]. As the hot electrons traverse the base, they are subjected to inelastic and elastic scattering, which changes their energy as well as their momentum distribution. Electrons are only able to enter the collector if they have retained sufficient energy to overcome the energy barrier at the collector side, which is chosen to be somewhat lower than the emitter barrier. Equally important, a hot electron can only enter the collector if its momentum matches with that of one of the available states in the collector semiconductor. The fraction of electrons that is collected, and thus the collector current IC, depends sensitively on the scattering in the base, which is spin dependent when the base contains magnetic materials. The total scattering rate is controlled with an external applied magnetic field, which changes the relative magnetic alignment of the ferromagnetic $Ni_{80}Fe_{20}$ and Co layers in the base. At large applied fields, the two magnetic layers have their magnetization directions aligned parallel. This gives the largest collector current. When the magnetic field is reversed, the difference in switching fields of Co (22 Oe) and NiFe (5 Oe) creates a field region where the NiFe and Co magnetizations are antiparallel. In this state, the collector current is drastically reduced. The magnetic response of the SVT, called the magnetocurrent (MC) found is huge indeed.

It should be noted here that huge or even colossal magnetic response has been observed in other materials and devices. The uniqueness of the SVT is that the huge relative magnetic effect is obtained at room temperature, and that only small magnetic fields of a few Oe are required. The combination of these features is what makes it attractive. Furthermore, the results are reproducible and the properties of the device can be manipulated to a certain extent by controlling the thickness of layers, the type of materials, etc.

SVT should be viewed as a device with a magnetic field dependent electrical output, which is the basic functionality one needs for a magnetic field sensor or a magnetic memory element. Although current gain is thus not required for most applications, a small absolute current is a disadvantage.

Chapter 4

Spin MOSFET

(Spin Based Semiconductor)

4.1 Device Structures and Material Candidates

Fig. 4.1(a)–(d) schematically shows the structures of various types of spin MOSFETs, which can be classified by the materials of the source/drain and channel. These are field effect transistors with a MOS gate (that is, MOSFETs), and at least two of three constituents (source, drain, and channel) are ferromagnets. The simplest way to obtain a spin MOSFET structure is to replace the source/drain material of a ordinary MOSFET with a FS which forms a ferromagnetic p-n junction with the Si channel, as shown in Fig. 4.1(a).

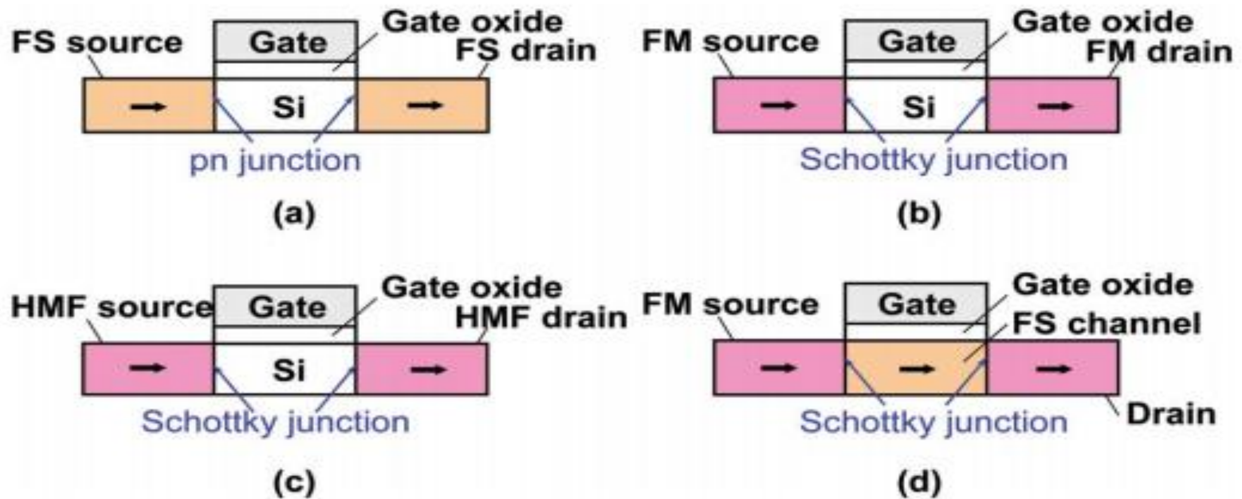


Figure 4.1: Schematic device structures of spin MOSFETs with (a) a ferromagnetic semiconductor (FS), (b) a ferromagnetic metal (FM), and (c) a halfmetallic ferromagnet (HMF) for the source/drain. A spin MOSFET with a FS channel and FM (or HMF) source/drain is also shown in Fig. 4.1(d).

Possible candidates for the source/drain materials are group-IV-based FSs, that is Si, Ge, and SiGe doped with magnetic ions [9]. Recently reported iron-silicide-based FSs, FexCo1−xSi and FexMn1−xSi [10], may also be candidates for the source/drain material. Since only a small spin-valve like magnetoresistive effect is expected in the carrier transport from the source to drain if the spin polarization of FS is moderate, an FS with an extremely large spin polarization must be used to obtain large magnetocurrent.

Fig. 4.1 (b) schematically shows a spin MOSFET using ferromagnetic Schottky contacts for the source/drain. The structure of the spin MOSFET is similar to that of Schottky MOSFETs [11], [12] except for the Schottky contact material of a FM. This type of spin MOSFET can be operated as not only n-channel and p-channel devices but also as accumulation and inversion type channel devices. Possible materials for the source/drain are FMs with large spin polarization. CoFe and CoFeB are commonly used in magnetic tunnel junctions (MTJs) as the ferromagnetic electrodes, which exhibit large TMR, indicating large spin polarization [13], [14]. Fe_3Si is also an attractive candidate [15]. Recently, high spin injection efficiency from Fe3Si into a semiconductor was reported using a Fe3Si/GaAs Schottky junction [16]. Note that one of the important challenges is to realize low Schottky barrier (SB) height (typically less than 0.2 eV) for high transconductance of the spin MOSFET [17]. When the tunneling emission through the SB is used for the injection of carriers from the source to the channel, relatively large magnetocurret ratios can be expected, owing to the spin-dependent transport similar to the TMR effect in MTJs. However, it is predicted that the magnetocurrent ratio in the spin MOSFET will exhibit unwanted bias-dependence, i.e., it decreases with increasing bias voltages. Fig. 4.1(c) schematically shows the device structure of the spin MOSFET using HMF contacts for the source/drain. HMFs have metallic and insulating spin bands, and thus the spin polarization of 100% at the Fermi energy. The metallic spin band of the HMF contact forms a Schottky junction with the Si channel (as described later). This type of spin MOSFET can also be applied to not only n-channel and p-channel devices but also accumulation- and inversion-type channel devices. Possible candidates for the HMF materials are Heusler alloys, CrO_2, Fe_2O_3, half metallic compounds (CrAs, MnAs, and CrSb) with zinc-blende (ZB)-type crystal structures.In particular, half-metallic ZB-type compounds and FSs using a wide gap semiconductor as a host material are promising, since their predicted high Curie temperature and large band gap of the insulating spin band [18] are useful for the HMF source/drain in the spin MOSFET [19].

Fig. 4.1(d) schematically shows another type of spin MOSFET. The device has a MOS capacitor structure with an FS channel and a ferromagnetic FM (or HMF) source/drain. The interfaces between the source/drain and the FS channel are Schottky junctions. Although the structure is similar to Schottky MOSFETs [11], [12], this type of spin MOSFET should be operated in the accumulation-channel mode. Note that it is not necessary to make both of the source and drain

contacts FM (or HMF)/FS Schottky junctions. A nonmagnetic-metal/FS Schottky junction can be used for one of the source and drain contacts. Possible candidates for the channel materials are group-IV (Si, Ge, and SiGe)-based FSs [20]. Recently, it is well recognized that SiGe and Ge, as well as Si and strained Si, are important as channel materials for advanced MOSFETs with high performance [21], [22].This type of spin MOSFET exhibits large magnetocurrent, which is insensitive to the bias conditions [23]. The electrical manipulation of magnetization reversal (EMMR) of the FS channel is also useful for nonvolatile memory applications [23].

4.2 Operation Principle of the Spin MOSFET with HMF Contacts for the Source/Drain

In this section, we describe the operating principle of the n-channel accumulation-type spin MOSFET using HMF contacts for the source/drain [Fig. 4.1(c)]. Fig. 4.2(a) schematically shows the band diagram of the spin MOSFET under a common source bias condition with and without a gate-source bias V_{GS}, where the relative magnetization configuration of the HMF source/drain is parallel. Owing to the metallic and insulating spin bands of the HMF source/drain material, spin dependent barrier structures appear as shown in the figure, i.e., a SB with a lower barrier height φSB for up-spin electrons and a rectangular energy barrier with a higher barrier height φHM for down-spin electrons.

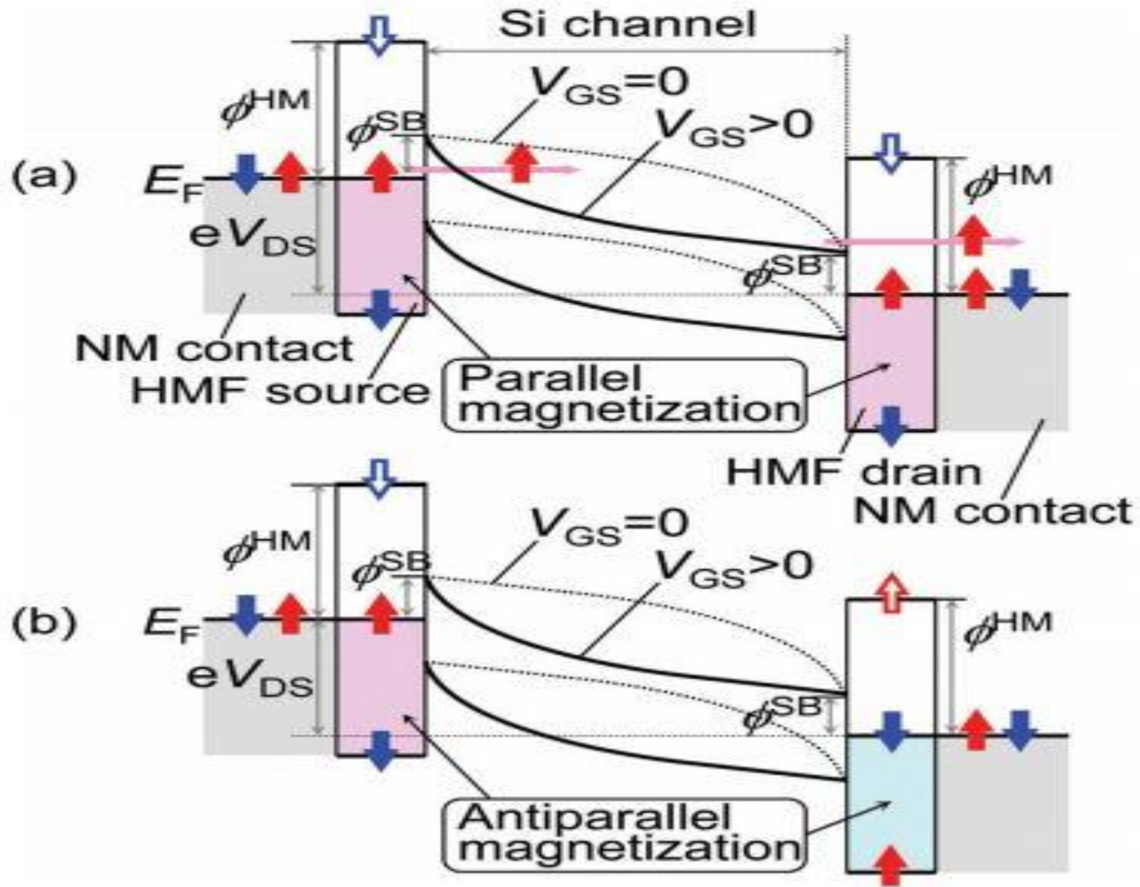


Fig. 4.2: Schematic band diagrams of the spin MOSFET in (a) parallel and (b) antiparallel magnetization configurations. Solid arrows in the HMF source/drain show up-spin and down-spin electrons at the Fermi energy of the metallic spin band and at the valence band edge of the insulating spin band. Open arrows represent the conduction band edge of the insulating spin band of the HMF source/drain.

When a drain-source bias V_{DS}(>0)is applied at V_{GS}=0, neither up-spin nor down-spin electrons are injected from the source to the channel due to the reverse-biased source-SB for up-spin electrons [as shown by the upper dotted curve in Fig. 4.2(a)] and the high rectangular barrier for down-spin electrons. By applying V_{GS} (>0), the width of the source-SB is reduced [as shown by the upper solid curve in Fig. 4.2(a)] and thus up-spin electrons in the metallic spin band of the HMF source can tunnel through the thinned source-SB into the channel. On the other hand, the injection of down-spin electrons is blocked even under the nonzero biases of V_{DS} and V_{GS} owing to the high rectangular barrier at the source. Thus, the HMF source acts not only as a contact for blocking the OFF-current but also as a spin-injector of up-spin electrons from the HMF source to the channel. In the parallel magnetization configuration, the up spin electrons injected in the channel can be transported to the nonmagnetic drain contact through the metallic up-spin band of the HMF drain,

resulting in a drain–current. By flipping the magnetization of the HMF drain, the antiparallel magnetization configuration is realized and the HMF barrier height for up-spin electrons becomes higher at the drain, as shown in Fig. 4.2(b). Thus, the up-spin electrons can hardly pass through the HMF drain to the nonmagnetic drain contact. Namely, the HMF drain works as a spin-detector, that is, the HMF drain selectively extracts up-spin electrons from the channel when the magnetization of the HMF source and drain is parallel. By combing these spin-filter effects of the HMF source/drain, an extremely large magnetocurrent ratio can be expected due to the high spins electivity of the HMF source/drain.

4.3 Operation Principle of the Spin MOSFET with an FS Channel

Next, we show the operation principle of the spin MOSFET of Fig. 4.1(d). Here, an n-channel accumulation-type spin MOSFET with a channel of non-degenerate FS is presented to explain its operating principle. Non degenerate FSs are commonly used in the analysis of FS-based devices such as ferromagnetic Schottky junction, ferromagnetic p-n junction, and magnetic bipolar transistor [17], [18]. Hereafter, it is assumed that the FS channel is a free layer and the FM source/drain is a pinned layer, and that the magnetization direction of the FM drain is always the same as that of the FM source.

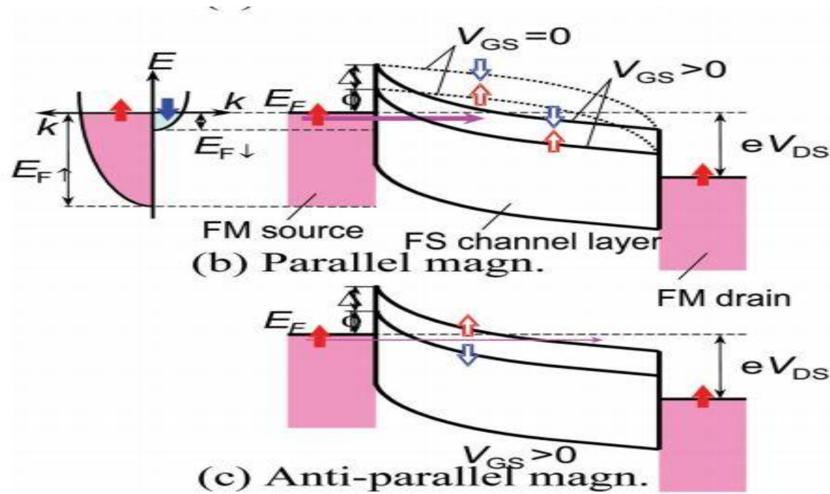


Fig. 4.3: Schematic (a) device structure and band diagrams of the spin MOSFET with an FS channel and FM source/drain in (b) parallel and (c) antiparallel magnetization configurations.

Fig. 4.3 schematically shows the (a) structure and (b) (c) band diagram of the spin MOSFET under a common source bias condition with and without a gate-source bias V_{GS}, where the relative

magnetization configuration of the FS channel and FM source/drain is parallel in (b) and antiparallel in (c). Assuming that the nonmagnetic-metal/FS Schottky junction model given by Lebedeva and Kuivalainen [24] can be extended to the FM/FS Schottky junction. we used qualitative approximation that a spin-dependent SB appears at the source/drain junction due to the energy splitting Δ of the up- and down-spin bands of the FS channel, i.e., a lower SB height φ for up-spin electrons and a higher SB height $\varphi+\Delta$for down-spin electrons, as shown in Fig. 4.3(b). When a drain-source bias V_{DS} (>0) is applied with $V_{GS}=0$, neither up-spin nor down-spin electrons are injected from the source to the channel due to the reverse biased SB of the source [as shown by the upper two dotted curves in Fig. 4.3(b)]. By applying V_{GS} (>0), the SB width is reduced [as shown by the upper two solid curves in Fig. 4.3(b)] and thus up- and down-spin electrons in the FM source can tunnel through the thinned SB into the channel. When the magnetization configuration of the FS channel and FM source is parallel, the SB height is low for the majority spin (up-spin) electrons in the FM source. Thus, a large output (drain) current can flow. When the magnetization configuration becomes antiparallel by flipping the magnetization of the FS channel, the SB height for the majority spin electrons in the FM source is higher, as shown in Fig. 4.3(c). Thus, a current by majority spin electrons is drastically reduced, since the tunnel current exponentially decreases with increasing the barrier height. Although the SB height is lower for the minority spin (down-spin) electrons in the FM source, tunneling current through the SB is small due to the narrow bandwidth $EF\downarrow$ of the minority spin band. Therefore, the output current depends on the relative magnetization of the FS channel and FM source/drain. Note that when a degenerate FS is used for the cannel, the structure of the source/drain should be slightly modified in order to avoid the tunnel contact formation between the channel and source/drain even at $V_{GS}=0$. A nonmagnetic semiconductor spacer or a tunnel barrier is applicable to the source/drain junctions for this case.

4.4 Reconfigurable Logic Gates Using Spin MOSFET

A simple device model was applied to the spin MOSFET for performing logic simulations. Since gm ($=\partial ID/\partial VGS$) of the spin MOSFET shows an approximately linear increase with increasing gate bias V_{GS} when V_{GS} is higher than the threshold voltage Vt, the output characteristics (the drain–current ID) of the spin MOSFET can be approximated as as $ID = \beta(VGS - Vt)^2$, where β is the gain coefficient.. This means that the ordinary device models for conventional MOSFETs are useful for the spin MOSFET. Thus, the absolute drain–current values of the spin MOSFETs and conventional MOSFETs are not needed in the static operation analysis of the presented logic gates.

Instead, the gain coefficient ratios of the load and driver transistors are used in the following simulations. To reproduce the magnetization-configuration-dependent output characteristics of the spin MOSFET, large and small gain coefficients are introduced into the device model of a single spin MOSFET, that is, the spin MOSFET in parallel (antiparallel) magnetization is represented by a MOSFET with a large (small) gain coefficient β_P (β_{AP}). Since the gain coefficient of MOSFETs is proportional to the device dimension ratio W/L (where W is the channel width and L is the channel length), βP And βAP for a single spin MOSFET are separately realized by the appropriate choice of W/L values for parallel and antiparallel magnetizations. Note that although the gate capacitance of this spin MOSFET model is changed according to the W/L values for parallel and antiparallel magnetizations, this variation of the gate capacitance can be neglected when using a νMOS input stage.

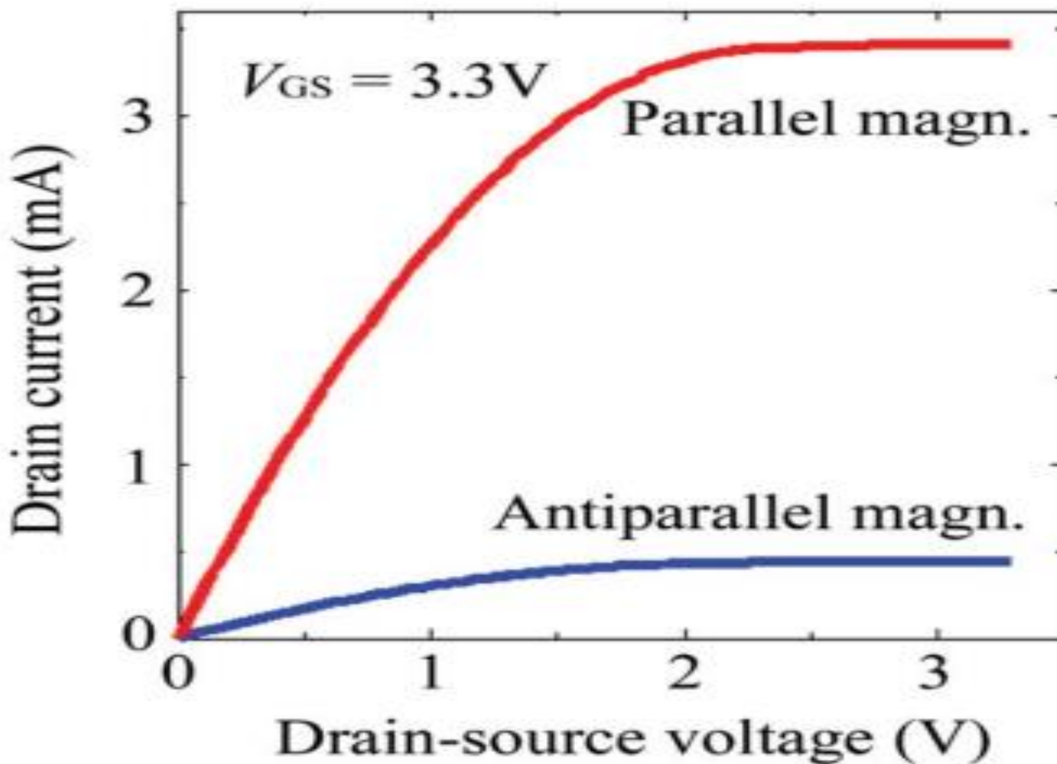


Figure 4.4: Output characteristics of a spin MOSFET in parallel magnetization (red) and antiparallel magnetization (blue).

Red and blue curves in Fig. 4.4 show the output characteristics of this spin MOSFET model in parallel and antiparallel magnetizations respectively. The gain coefficient ratio β_P / β_{AP} of the spin MOSFET is a suitable parameter for controlling the device performance, since β_P / β_{AP} directly

determines the magnetization-configuration-dependent output characteristics of the spin MOSFET as well as the operational margin of the reconfigurable logic gates presented in this thesis.

Although the operational margin depends on the ratio β_P / β_{AP}, the appropriate range of β_P / β_{AP} seems to be extremely wide, 3–1000, as estimated from our simulated results. Note that the operating speed and power dissipation of the proposed reconfigurable logic gates also depends on the gain coefficient ratio β_P / β_{AP}, e.g., a large β_P / β_{AP} ratio results in small power dissipation at the expense of the operating speed.

4.4.1 Reconfigurable AND / OR Gate

Fig. 4.5(a) shows a reconfigurable NAND/NOR gate for the output VO1, which acts as an AND/OR gate for the outputVO2. The NAND/NOR gate can be realized by using a p-channel MOSFET as the active load (Q1) and an n-channel spin MOSFET as the driver (Q2) of a CMOS inverter with a νMOS input stage having two binary inputs (A and B). Here, the gain coefficients ofQ1 and Q2 in parallel and antiparallel magnetizations are expressed by β1, βP2 and βAP2, respectively.

The νMOS input stage consists of a floating gate coupled capacitively with two input gates. The floating-gate voltage VFG of the νMOS is given by [25], [26]

$$VFG= (C_A A+C_B B)/ (C0+CA+CB) \approx (A+B)/2$$

Where C0 denotes a capacitance between the substrate and the floating gate, CA and CB represent a coupling capacitance for inputs A and B, and we assume CA=CB and CA, CB>> C0. The binary input voltages of 0 and VDD for A and B can be simply expressed by "0" and"1" which are measured in the units of VDD (hereafter, quotation marks are used to denote values measured in the units of VDD). When the input combinations are A=B="0" and A=B="1", V_{FG} is "0"and "1," respectively. When one of the two inputs is "1" (i.e., A="0", B="1", or A="1", B="0"), V_{FG} is "1/2."

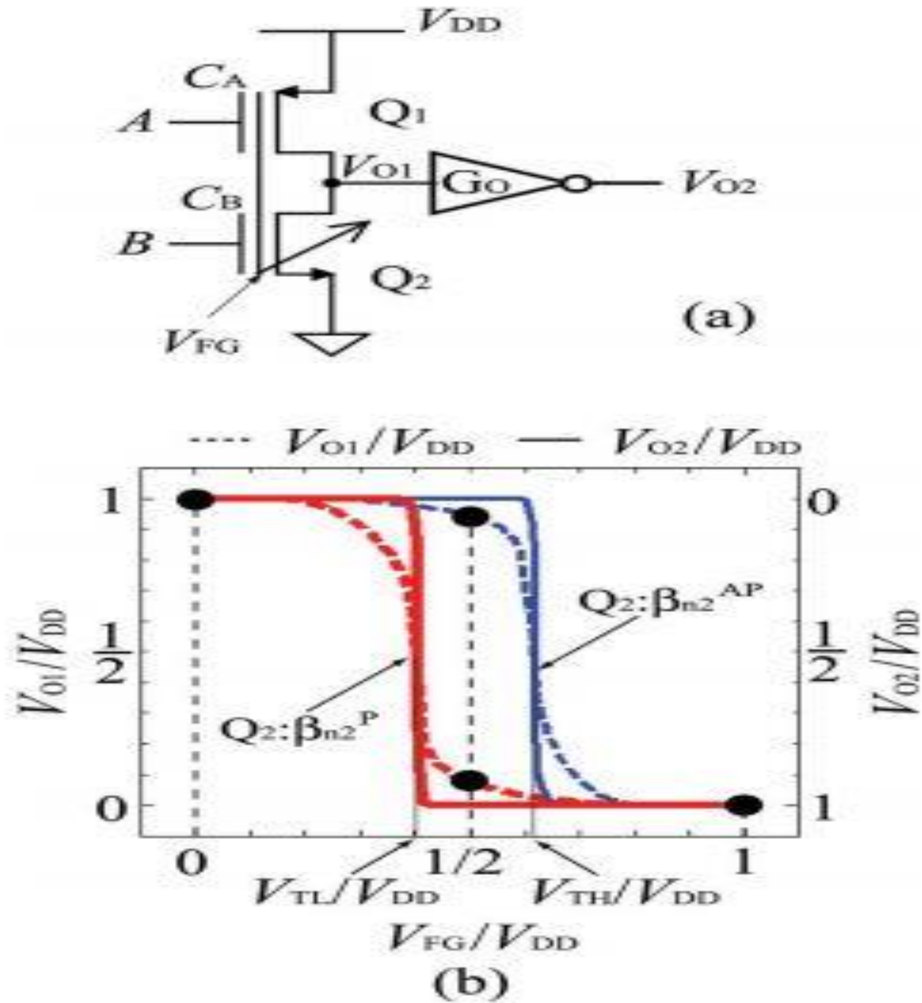


Figure 4.5: (a) Circuit configuration of a reconfigurable NAND/NOR gate for the output VO1 and a reconfigurable AND/OR gate for the output VO2. (b) Calculated transfer characteristics with Q2in the parallel magnetization state (red curve) and in the antiparallel magnetization state (blue curve), where dotted and solid curves are the transfer characteristics for outputsVO1 and VO2, respectively The function of a CMOS inverter GO(whose logic threshold voltage is set at 1/2VDD) in the output stage. Note that this logic gate can also be configured with a p-channel spin MOSFET asQ1and an n-channel MOSFET as Q2, and with p- and n-channel spin MOSFETs as Q1 and Q2, respectively.

Red and blue dotted curves in Fig. 4.5(b) show the transfer characteristics (VO1/VDD versus VFG/VDD) of the reconfigurable logic gate in parallel and antiparallel magnetizations for the spin MOSFET Q2, respectively, where βP 2/β1=2.7 and AP 2 /β1=0.4. When the magnetization of the source and drain of Q2is parallel, the logic threshold voltage VT is VTL, which is lower than "1/2." By flipping the magnetization of Q2 from the parallel to antiparallel configuration, the logic threshold voltage VT is changed to VTH, which is higher than "1/2" [see Fig. 4.5(b)]. This can be explained by assuming that the conventional MOSFET.

4.4.2 Logic Operations of the Reconfigurable AND/OR Gate

The logic operations of the reconfigurable NAND/NOR gate can be obtained using the transfer characteristics shown in Fig. 4.5(b). When the spin MOSFET Q2 is in the parallel magnetization state, the logic threshold voltage V_{TL} is lower than “1/2” as shown by the red dotted curve in the figure. For the input combinations of A=B=“0”, {A=“0”, B=“1”, or A=“1”, B=“0”}, and A=B=“1”, V_{FG} takes “0,” “1/2,” and “1,” respectively, as described above.

These V_{FG} values are transformed toVO1=“1”, “0” and “0,” respectively, via the transfer characteristics. Thus, the reconfigurable logic gate shows a NOR function when Q2 is in the parallel magnetization state. Note that when V_{FG}=“1/2” {A=“0”, B=“1”, or A=“1”, B=“0”}, VO1 is slightly higher than “0.” However, this deviation can be included in a logic margin, i.e., using the logic margin ΔV, the “0” level for VO1 is given by “0”≤VO1≤“0”+ΔV. This deviation disappears after the inverse amplification from VO1 to VO2 by the output inverter GO, as shown by the solid red curve in Fig. 4.5 (b), while the logic function is inverted from NOR for the output VO1 to OR for VO2.

When the spin MOSFET Q2 is in antiparallel magnetization, the logic threshold voltage V_{TH} is higher than VFG=“1/2”, as shown by the dotted blue curve in Fig. 4.5(b). Due to this transfer characteristics, the input combinations of A=B=“0”, {A=“0”, B=“1”, or A=“1”, B=“0”} and A= B=“1” (corresponding to VFG=“0”, “1/2” and “1,” respectively) are transformed to VO1=“1”, “1” and “0.” Thus, the reconfigurable logic gate shows a NAND function when Q2 is in the antiparallel magnetization state. Note that when V_{FG}=“1/2” {A=“0”, B=“1”, or A=“1”, B=“0”}, VO1 is slightly lower than “1.” Since this deviation can be included in the logic margin for the “1” level (“1”−ΔV≤VO1≤“1”), it is also eliminated by the output inverter GO, as shown by the solid blue curve in Fig. 4.5(b). The logic function for the output VO2 is inverted from NAND to AND.

Chapter 5

Spintronic Devices

5.1 Spin Transfer Nano-Oscillators

The use of spin transfer nano-oscillators (STNOs) to generate microwave signal in nanoscale devices have aroused tremendous and continuous research interest in recent years. Their key features are frequency tuning ability, nanoscale size, broad working temperature, and easy integration with standard silicon technology. In 1996, John Slonczewski [39] and Luc Berger [40] predicted a different way to modify a magnetic configuration of nano magnets based on the spin-transfer-torque (STT) effect from a spin-polarized current. The current-induced switching (reversal) offers promising applications in future magnetic random access memory (STT-MRAM). The current-induced magnetization precession enables magnetic nanostructures to be new type of high-frequency tunable nanoscale oscillators, namely spin-transfer nano-oscillators (STNOs) or spin-torque nano-oscillators.

The STNOs can be roughly classified as the unpatterned point contact devices and patterned nanopillars according to the patterning geometry. There are different parameters describing the STNO performances, such as oscillator frequency, output power, linewidth, Q factor, power dissipation, phase noise, and robustness among them. Each parameter may be relevant in spite of the different device geometries. This review does not intend to exhaustively revise the "state of the art" on the optimization of all possible device performance characteristics. We rather focus on giving some idea about all types of STTNOs.

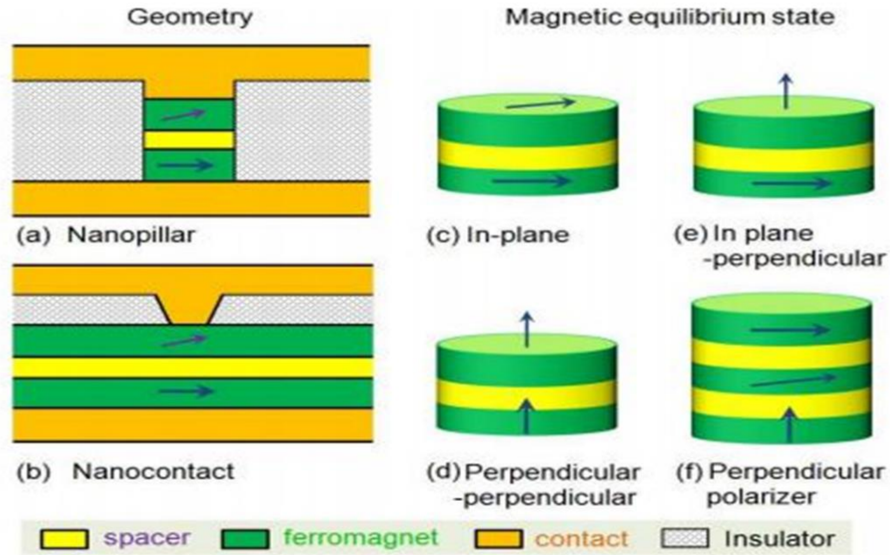


Fig 5.1: Different configurations of STNOs based on the type of the patterned geometry and the magnetic state.

5.1.1 Operating Principle

The simple configuration of a STNO consists of a relatively thick "fixed" magnetic layer, which serves as a polarizer, a nonmagnetic spacer, and a relatively thin magnetic "free" layer.

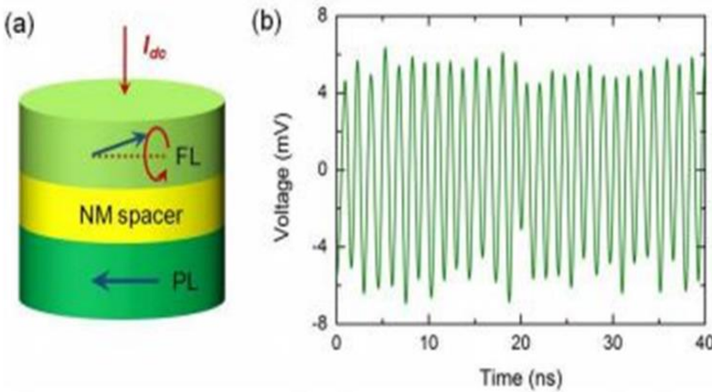


Fig 5.2: (a) A STNO device consists of a "fixed" layer that serves as polarizer (PL) and a "free" layer (FL) whose magnetization is excited into steady state oscillations, NM spacer denotes non-magnetic layer i.e. insulator or non-magnetic metal. (b) Voltage oscillations produced by steady-state precession of the magnetic free layer in a nanopillar sample.

A dc current, spin-polarized from the polarizer, when large enough to transfer a sufficient STT to cancel out the intrinsic damping losses of the free layer, leads to a steady-state magnetization dynamics. The magnetoresistive (MR) effect converts the magnetization oscillation to a microwave voltage Fig 5.2(b). The nonmagnetic spacer can be used, either a nonmagnetic metal (e.g. copper) or a thin dielectric (e.g. MgO), the corresponding structure is usually called a giant magnetoresistance (GMR) spin valve or a magnetic tunnel junction (MTJ). It is important to note that in order that the STT becomes significant, high current

densities are required (on the order of 10 7Acm-2) achievable experimentally with applied currents of few milliamperes. For a spin valve device, it is trouble-free to apply large current to produce oscillations, but the output power is relatively low being the magnetoresistance signal small. On the other hand, for a MTJ an opposite scenario exists. A large output power can be delivered being the resistance change up to several hundred Ohms, but the maximum bias current is limited by the barrier breakdown voltage (~1.0 V). As consequence, the MTJ must have together to high tunneling-MR (TMR) high transparency (low resistance-area product).

5.1.2 Output Power and Linewidth

The output power and linewidth are the two most important parameters for a STNO. Although large numbers of experiments have been made to push the technology beyond the mere proof of concept, the important bottlenecks in STNO technology lies in the enhancement of its output power and simultaneously the improvement of the linewidth. The difficulty of attaining high power and narrow linewidth STNO arises not only in device fabrication, but also in the choice of the material and the design.

5.1.2.1 Output Power

We would like to first look at the key factors to determine the output power of a single STNO. It is well known that the dc current (I) flowing perpendicular to the layers of a STNO excites magnetization oscillations in the free layer, which give rise to a temporal variation in the resistance due to MR effect, $R(t) = \Delta R + R/2 \times \cos(\omega t)$, where R is approximately equal to the dc resistance and ΔR is the oscillation amplitude of the resistance induced by I. The temporal variation of the resistance generates a microwave voltage $V(t) = I \times R(t)$. Thus the output power delivered from the STNO to a load with impedance R_L is approximately given by,

$$P_{out} = V_{out}^2/2R_L$$

$$= I^2 \Delta R^2 R_L / 8(R+R_L)^2$$

From this equation it is evident that maximizing the output power requires one to maximize the ΔR value and to optimize the impedance matching ratio R/R_L. It is worthwhile to note that $\Delta R = Am \times MR$ (Am is related to the amplitude of magnetization oscillation, $MR = (R_{AP}-R_P)/R_P$, RAP and RP are the resistances when the magnetizations between the fixed and free layer are aligned anti-parallel and parallel respectively). Thus the output power is approximately proportional to the MR effect, the oscillation amplitude of magnetization and the impedance match ratio R/R_L.

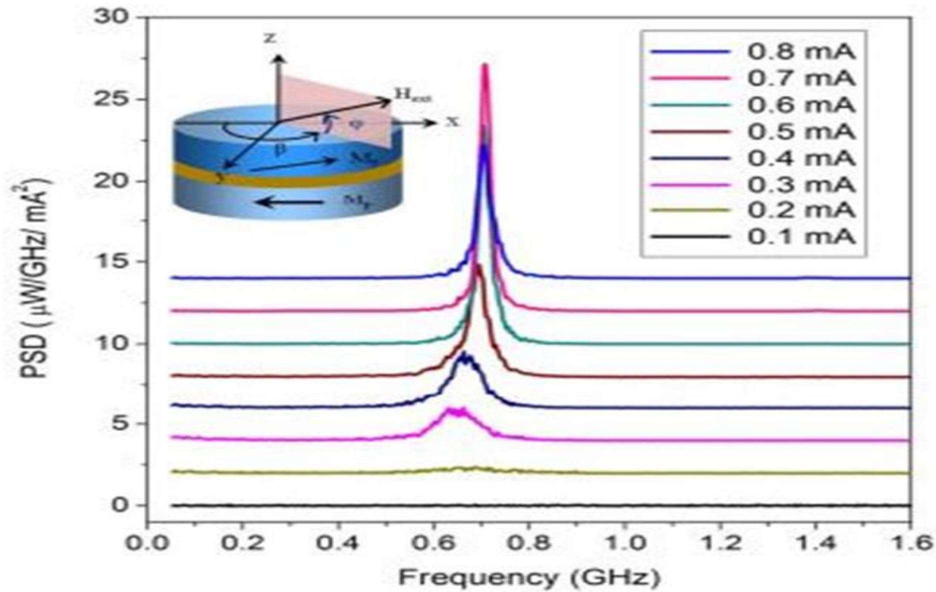


Fig 5.3: Microwave emission spectra measured at positive currents between 0.1 mA and 0.8 mA with 0.1 mA steps. The power spectral densities (PSD) normalized by I^2 have been offset by 2 μW/GHz/mA^{2}for clarity. The external magnetic field is applied at out-of-plane direction (i.e. β=120° & φ= 40.4°) with an amplitude of 264 Oe. Inset: Definition of the coordinate system. Here β is the angle between the external magnetic field Hext and the reference layer in the x-y plane, and φ is the angle with respect to the x-y plane.

Recent experiments demonstrated that MgO-based STNOs with large TMR ratio are able to deliver this large power, due to the excitation of a uniform mode where the magnetization oscillates around the equilibrium configuration of the magnetization as also indicated by micro-magnetic simulations. Even so, there is still room to boost the output power for MTJ STNO through the achievement of the large-amplitude oscillations.

5.1.2..2 Linewidth

For any oscillators, the linewidth (full width at half maximum of the power spectra, Δf) is a measure of the phase noise, which is one of the most important figures of merit.

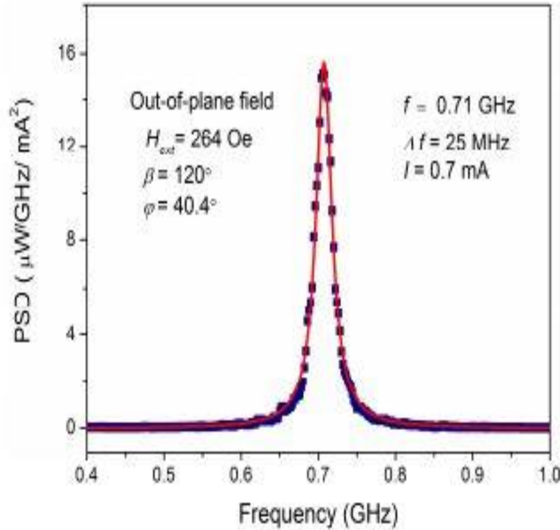


Fig 5.4: An example of MTJ-based nanopillar STNO spectra showing a narrow linewidth at room temperature.

Fig 5.4 shows a power spectra of a STNO with f= 0.71 GHz, and Δf = 25 MHz. Differently from linear or quasi-linear oscillators where the phase noise is decoupled from the power noise, in STNOs exists an intrinsic coupling between oscillation amplitude and phase due to the dependence of the effective field on the magnetization. This coupling gives rise to an additional contribution to the phase noise coming from a renormalization of the power noise via the non-linear frequency shift (N).In general, the linewidth of STNOs strongly depends on both device geometry and materials and the operation conditions. The linewidth for a single nano-contact device can vary from a few MHz to 100 MHz as the current and applied magnetic fields are varied, while line widths for nano-pillars can vary from several tens MHz to the GHz level.

One of remaining challenges in the STNO design is the achievement of a narrow linewidth and a large output power at the same time in order to utilize them for practical applications.

5.1.3 Advantages of STNOs over Standard VCO

The STNOs have many intriguing advantages over a standard LC-tank voltage-controlled oscillator (VCO). Firstly, they are highly tunable by bias current and magnetic field. While the frequency variation in VCO is only 20% compared to the carrier frequency, the oscillation frequency of the STNOs can be tuned by current over a range of several GHz and by magnetic field up to 40 GHz for particular configurations [41].Secondly, STNOs are among the smallest microwave oscillators developed, over 50 times smaller than a standard VCO in complementary metal-oxide-semiconductor (CMOS) technology. Thirdly, STNOs work over a broad range of temperatures and can be biased at low voltages (< 1.0 V). Finally, their simple structure is a key

ingredient for on-chip realization. All those advantages make the STNOs promising for on chip-to-chip micro-wireless communications, small array transmitters, microwave sources for nano sensors, local on chip clocks for VLSI applications, and very high-density massively-parallel microwave signal processors [42].

5.2 DMS-based Sensors

There is a growing market for magnetoresitive DNA chips. These involve the use of MR sensors to detect bimolecular recognition processes between an immobilized probe and a magnetically labeled target [56]. The integration of DNA and other biomolecules array and detection methods based on a portable, inexpensive and fully electronic approach is being actively pursued. Magnetic labels are often used to provide a means for cell separation, drug delivery or contrast enhancement in magnetic resonance (MR) imaging. Integrated MR sensors detect the fringe field of the label that binds to the hybridized target. For MR biochip applications, a small magnetizing field is applied to magnetize the nonpermanent particles. The magnetic field can be created by either on-chip current lines or an external electromagnet. If an AC field is used, lock-in amplifiers are used for optimal signal-to-noise during particle detection.

One concept based on DMS thin films is illustrated in Fig. 5.5. The transition metal-doped DMS would serve as the source S to inject spin-polarized electrons into a Nano scale wire in which the spin polarization would be maintained, Fig. 5.5(a). The electrons would then be collected at the drain D. This device is not a conventional field-effect transistor as there is no gate. A specific receptor R, either for chemical or biological sensing, would be attached to the nanowire, Fig. 5b. Many chemical or biological agents possess magnetic ions. Binding of such an agent A with the receptor, Fig. 5c would lead to changes in the local magnetic field of the nanowire and would alter the polarized current. A single device could be replicated thousands of times with an assortment of receptors to form a microarray. The aligned receptor array could consist of genetically manipulable and combinatorial selective molecular recognition units that would be responsive to an agent-receptor binding event involving a specific reaction of each Sub element. This would confer absolute specificity for each individual reaction based on the particular spin-coupled properties of that sub element resulting in a unique pattern for all sub element responses taken together. The DMS based array could also be integrated with Si microelectronics for real-time processing of the signals. DMS materials offer rich choices of organic and biomolecules for functionalization which form strong bonds on oxide surfaces. Using photo or electron-beam

lithography, multiple electrodes can be patterned on a single Nano belt, which forms a Nano scale FET on a Si/SiO2 substrate. Owing to the single-crystal quality of the Nano belts, the FETs with *B*0.05mm channel length should be in the ballistic regime and high FET performance is

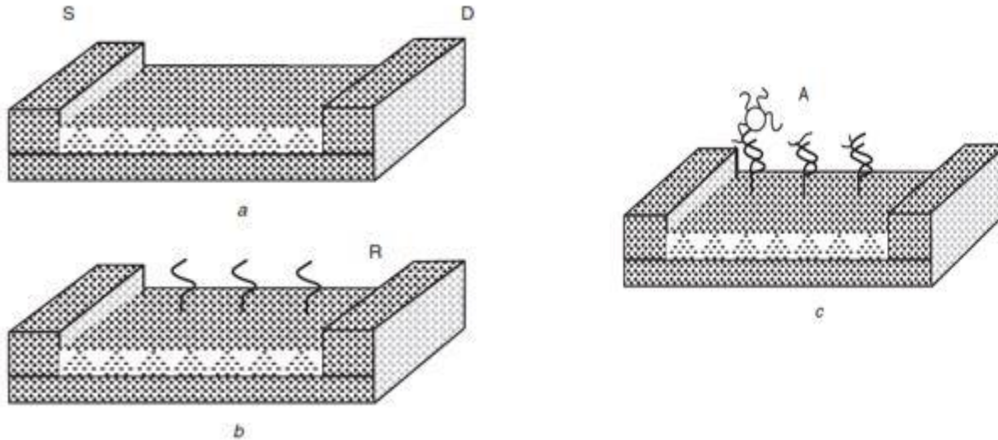
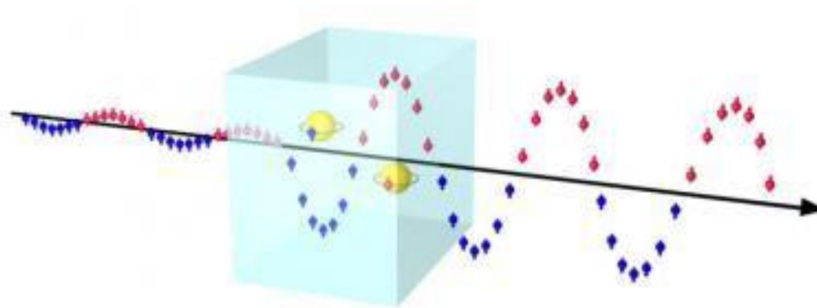


Fig. 5.5: Schematic representation of detection of biological molecules using a nanowire spin filter (S. von Molnar and J.M. Zavada, private communication) a Spin-polarized electrons passing in Nano scale wire from source region S to detector region D b Bio receptors R attached to Nano scale wire c Bonding of a single receptor Ri with a bio agent A

expected. Coupled with the large surface-to-volume ratio of the Nano belt geometry, these devices are expected to be chemical and biological sensors with extraordinary sensitivity. Nano scale FETs based on Si nanowires have shown promise as effective biosensors, but oxide Nano belt FETs may have several advantages over those devices including demonstrated bulk electrical sensitivity to molecular binding, rich surface functionalization choices and structural flexibility in assembling device arrays [57]. ZnO is particularly well-suited to this purpose, because of the ease with which long (several mm) nanowires and Nano belts can be formed, and due to its biocompatibility [58]. We have recently shown the ability to reproducibly contact individual Nano rods for fabrication of MOSFETs and chemical sensors.

5.3 Spin Amplifier



A schematic picture of the defect-engineered spin amplifier demonstrated in this work. The wave pattern symbolizes the time variation of the spin signal, namely the difference between the numbers of spin-up and spin-down electrons. The red and blue arrows represent the period with more spin-up and spin-down electrons, respectively. The amplitude of the wave reflects the strength of the spin signal, which is weak before entering the spin amplifier but becomes stronger when exiting. The defects that have enabled the spin-amplification functionality of a non-magnetic semiconductor are indicated by the yellow balls, each with a spin-polarized localized electron (indicated by the red and blue arrows). The spin direction of this localized electron rapidly follows the sign of the input spin signal, which serves to only attract and remove the incoming electrons with an undesired spin orientation. This leads to a significant enhancement in the spin polarization of the electrons passing the spin amplifier, giving rise to a strongly amplified output spin signal that has truthfully cloned the exactly same time-varying function and thus the spin-encoded information of the input spin signal.

Chapter 6

Future of Spintronics

6.1 Fast Magnetic Switching

A feature of spin-electronic device performance which we have not discussed in detail is device bandwidth. There are two aspects to this, namely device response to electrical and magnetic signals, respectively. The former is determined by the same considerations as govern the speed of conventional electronics—diffusion rate, charge storage, parasitic capacitance and its spin analogue. Magnetic switching time of the spin polarizing nano-elements is, however, another matter which is new to spin electronics, though some analogies may be drawn with the high-frequency response of recording media. Analysis of high-speed magnetic switching of nano-elements is widely researched and found to be highly dependent on sample shape and coupling of the switching mode to the spin-wave spectrum. MRAM nano-element access/write times of the order of nanoseconds are routinely achievable which is highly competitive with other memory technology. However in the future, higher magnetic switching speeds are desirable.

6.2 Optically Pumped Magnetic Switching

One potential option for making a fast write-time magnetic memory is to use a spin-electronic device in which one of the magnetic nano-elements is a FM spin-split insulator. The memory function is contained in the orientation of this magnetic insulator relative to a metallic FM electrode. However, because the insulator is optically transparent, its moment might be reversed very rapidly by connecting the Zeeman energy reservoir to a suitable optical transition energy reservoir by off-resonance optical irradiation. This would function as a high-frequency analogue of dynamic nuclear polarization. An alternative scheme might involve optical-microwave double resonance whereby the device is continuously bathed in microwave radiation and the switching is achieved by exposure to a short pulse of optical radiation.

The principle in both cases is to induce energy transfer between two different energy baths—magnetic and electronic with who's Hamiltonians the operators representing the irradiation do not commute.

6.3 Spin Electronic Automotive Position and Motion Sensor

Magnetic field detection has widespread application in commercial fields as diverse as information storage and retrieval, programmable gate arrays, aviation electronics, fuel injection, electronic engine management and automotive active safety systems. For example, the world market for automotive sensors alone currently stands at 3 billion Euro and, growing at over 10% per year, is projected to be worth 8.5 billion Euros. The key drivers behind this growth include: the need for improved internal combustion engine management to reduce automotive emissions, braking and anti-skid systems and safety devices, drive by wire control systems, etc. As these various technologies develop, the sensitivity, stability, noise rejection and reliability specifications of the magnetic sensor elements employed become ever more demanding and there is increased pressure on the basic technology to respond to these requirements.

6.4 The Spin Diode

An idea for a two-terminal spin device, which was originally mooted by Mattheis, consists of a five-layer magnetic system in which three FM metal layers are mutually spaced by thin PM metal layers. From left to right the FM layer magnetizations point respectively along the y-, z and x-directions, y-polarized spins leaving the first layer precess 90° about the z-oriented magnetization in the second layer (whose thickness is thus determined by the precession frequency of the spin) and transfer to the x-oriented third layer to whose magnetization they are now parallel. However, if spins transfer in the opposite direction from the right-hand x-oriented layer, these also precess 90° in the centre layer and end up antiparallel to the y-orientation of the left-hand layer to which they are unable to transfer due to absence of density of states of the right polarization. Thus, the entire system functions as a spin diode which is capable of fulfilling the memory and blocking function of a two-terminal MRAM element in a single hit. Tunnel versions of this device should also be realizable which, because their function is wholly determined by density of states asymmetry, should offer higher on/off ratios.

6.5 Spin-split Insulator as a Polarizing Injector—Application to Semiconductor Injection

The transport properties have been studied of spin split Europium-based insulators at low temperatures and the empirical data presented would seem to suggest that these—or room temperature analogues thereof—might act as convincing spin polarizers. However to date, little practical use has been made of these materials. The physics relies on the fact that, because the insulator band gap is spin split, a tunneling quasi-particle with its energy in the band gap sees a different tunnel barrier height depending on its spin. Accordingly, its evanescent wave function has a spin-dependent decay constant. For unpolarized electrons incident on a sufficiently thick

barrier, this implies a high spin asymmetry for the tunnel current and hence suggests itself as an ideal way to spin inject into materials such as semiconductors. Since no metal is involved, no problems of Schottky barrier interface states and differential material resistivity are called into play and the insulator/semiconductor combination affords a high degree of flexibility in choosing the point on the semiconductor band structure where spin injection occurs.

6.6 Novel Fast Switching MRAM Storage Element

The above ideas could be combined to produce a new type of tunnel MRAM storage element consisting of a FM film, a spin-split magnetic insulator and a normal metal. The memory function would then comprise the magnetic configurations of the magnetic metal and the magnetic insulator: the former would be magnetically pinned and the latter would be rapidly switchable by optical double resonance techniques.

6.7 Quantum–coherent Spin Electronics

Perhaps the most far-reaching development in spin electronics will be the establishment of quantum coherent spin devices. By this is meant devices whose construction is on a sufficiently short length scale that the quantum coherence of the electronic wave function is preserved across the device, thereby coupling input and output electrical signals. Earlier in this chapter we have considered the importance of the various mesomagnetic length scales in generating the novel characteristics and properties of spin-electronic devices. In fact, the spin diffusion length, which is the determining size threshold for spin electronics, is the least exacting length scale to reach, being typically thousands of angstroms for pure metals. At the other end of the scale of difficulty is the quantum coherence length which is of the order of mean free path, i.e. comparable with the length scale on which momentum scattering events occur, i.e. typically tens of angstroms upwards. On a slightly longer length scale are inelastic scattering events which change not only the momentum but also the energy of the carriers. Nanofabrication technology is such that devices may now be constructed with relative ease on the 10Å scale. Atypical example is the double barrier resonant tunnel diode— three metal layers sandwiching two insulating layers—which relies for its performance on quantum mechanical interference between opposite faces of the central potential well. Since insulating barriers may now be prepared to angstrom precision it is but a short step to a three-terminal spin transistor whose emitter, base and collector are phase coherent. A foreshadow of this concept is to be found in the patent of Ounadjela and Hehn. A recent theoretical analysis is offered by Wilczynski and Barnas.

6.8 The Tunnel-grid Spin Triode

The device which is essentially the double barrier resonant tunnel diode with FM collector and emitter and an added electrical contact to the non-magnetic base layer. In operation, the base and collector are biased progressively positive relative to the emitter. In line with the above discussion, the base layer is thin compared with the mean free path—and here we mean hot electron mean free path—so little carrier scattering occurs in the base and the phase coherence of the electrons launched by the emitter is preserved into the collector. However, although the base layer does not appreciably scatter the transiting carriers and so does not demand significant base current, it nonetheless is substantial enough to define the electrostatic potential across the successive barriers and hence to modulate the current tunneling from emitter to collector. In this respect the base is not unlike the grid electrode in a vacuum triode. Thus we have a device in which the emitter-collector conductance may be controlled by applying potential to a high impedance base, thereby affording power gain. Moreover, due to the FM nature of the electrodes, the device characteristics are also switchable by applying an external magnetic field. Other permutations of this basic configuration are imaginable, e.g. making all three layers—or indeed any pair of them—FM or, using a spin-split insulator as the spin-polarizing injector stage.

Summary and Outlook

The review paper describes a new era of devices based on Spintronics. Spintronics devices exploit the electron's spin or magnetic moment to perform their functions. Unlike conventional charge based semiconductor electronic devices, which works on charge injection, transport, and controlled manipulation, Spintronics device specifically exploits spin properties. These properties are exploited by adding the spin degree of freedom to conventional charge based electronic devices or using spin alone to yield potential advantage of non-volatility, increased data processing speed, decreased power consumption, and increased integration densities.

In less than twenty years, Spintronics have increased the capacity of our hard discs considerably and getting ready to enter the RAM of our computers or the microwave emitters of our cell phones. Spintronics with semiconductors or molecules is very promising too. It can also be mentioned that another perspective, out of the scope of this lecture, might be the exploitation of the truly quantum mechanical nature of spin and the long spin coherence time in confined geometry for quantum computing in an even more revolutionary application. Spintronics should take an important place in the technology of our century.

We are starting to see a new paradigm where magnetization dynamics and charge currents act on each other in nanostructured artificial materials. Ultimately, 'spin currents' could even replace charge currents for the transfer and treatment of information, allowing faster, low-energy operations: spin electronics is on its way.

In this review article we have tried give an overall idea about the fundamental of Spintronics, Spin injection, Spin relaxation, Spintronics in the field of data storage, Spintronic devices-> their fundamentals, operation and applications. This is mainly a review paper and we have tried to give an overall idea about the recent research trend of Spintronic devices and their potential applications.

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